

## X-SP3T SWITCH GaAs MMIC

### ■ GENERAL DESCRIPTION

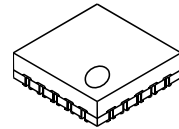
The NJG1655SCC is a GaAs X (Cross)-SP3T switch MMIC which is designed for switching of balanced triple-band filters.

This switch features very low phase error between on state paths, low insertion loss and low control voltage.

This switch integrates a logic decoder function and high ESD protection circuits.

The small PCSP20-CC package is adopted.

### ■ PACKAGE OUTLINE



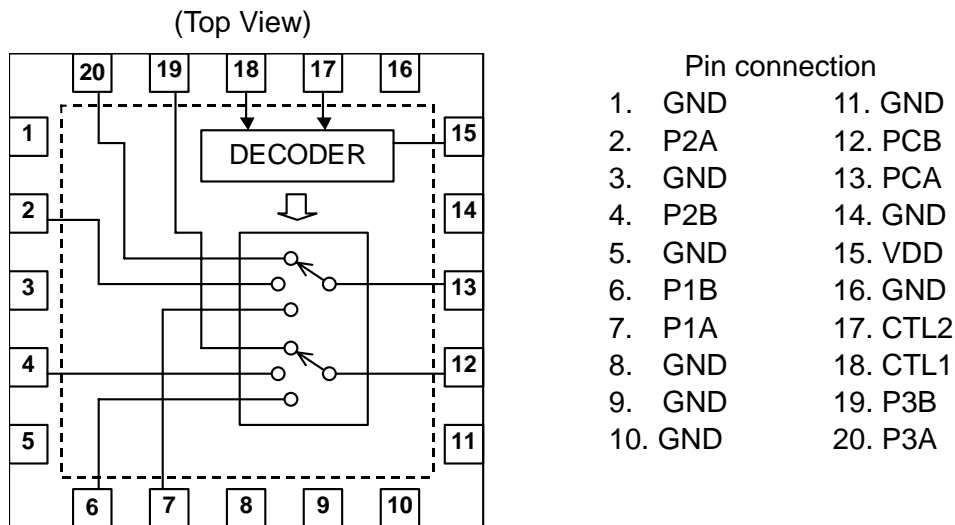
NJG1655SCC

### ■ FEATURES

- Low voltage operation
- Low voltage Logic control
- Low insertion loss
  
- Operating current consumption
- Control current consumption
- Small package

$V_{DD}=+1.5\sim+4.5V$   
 $V_{CTL(H)}=+1.3V$  min,  
 0.4dB typ. @f=1.0GHz,  $P_{IN}=0dBm$ ,  $V_{DD}=2.7V$   
 0.5dB typ. @f=2.0GHz,  $P_{IN}=0dBm$ ,  $V_{DD}=2.7V$   
 20 $\mu$ A typ. @  $V_{DD}=2.7V$   
 5 $\mu$ A typ. @  $V_{CTL(H)}=1.8V$   
 PCSP20-CC (Package size: 2.7x2.7x0.8mm)

### ■ PIN CONFIGURATION



### ■ TRUTH TABLE

"H"= $V_{CTL(H)}$ , "L"= $V_{CTL(L)}$

ON PATH	CTL1	CTL2
PCA-P1A PCB-P1B	H	L
PCA-P2A PCB-P2B	L	L
PCA-P3A PCB-P3B	L	H

X (Cross) -SP 3 T Switch : Switch that output port of two SP3T switches crosses internally.

NOTE: The information on this datasheet is subject to change without notice.

## ■ ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	$P_{IN}$	$V_{DD}=2.7\text{V}$ , $V_{CTL}=0\text{V}/1.8\text{V}$	28	dBm
Supply Voltage	$V_{DD}$	VDD terminal	5.0	V
Control Voltage	$V_{CTL}$	CTL terminal	5.0	V
Power Dissipation	$P_D$		500	mW
Operating Temp.	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage Temp.	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS

(General conditions:  $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ ,  $V_{DD}=2.7\text{V}$ ,  $V_{CTL(L)}=0\text{V}$ ,  $V_{CTL(H)}=1.8\text{V}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$		1.5	2.7	4.5	V
Operating Current	$I_{DD}$		-	20	40	$\mu\text{A}$
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control Voltage (HIGH)	$V_{CTL(H)}$		1.3	1.8	4.5	V
Control Current	$I_{CTL}$		-	5	10	$\mu\text{A}$
Insertion Loss 1	LOSS1	$f=1.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	0.4	0.55	dB
Insertion Loss 2	LOSS2	$f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$	-	0.5	0.7	dB
Isolation 1	ISL1	$f=1.0\text{GHz}$ , $P_{IN}=0\text{dBm}$ PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	24	26	-	dB
Isolation 2	ISL2	$f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$ PCA-P1A,P2A,P3A, PCB-P1B,P2B,P3B	18	20	-	dB
Isolation 3	ISL3	$f=2.0\text{GHz}$ , $P_{IN}=0\text{dBm}$ PCA-PCB	15	17	-	dB
Phase Error	PE	$f=2\text{GHz}$	-3	-	3	deg
Input Power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2\text{GHz}$	18	23	-	dBm
VSWR	VSWR	$f=2\text{GHz}$ , on state	-	1.1	1.3	
Switching Time	$T_{sw}$		-	2	5	$\mu\text{s}$

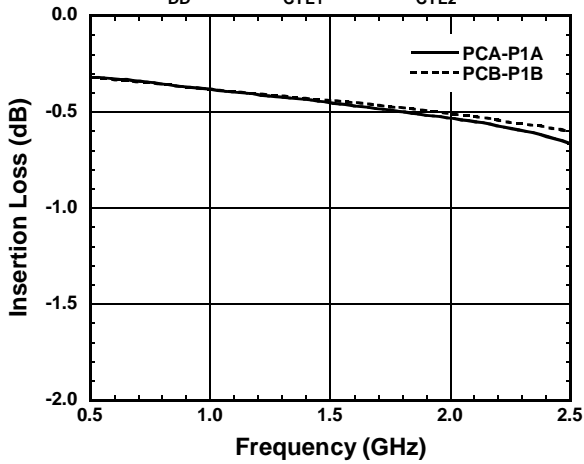
## ■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
2	P2A	The 2nd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P2B port at the same time. An external capacitor is required to block DC voltage.
4	P2B	The 2nd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P2A port at the same time. An external capacitor is required to block DC voltage.
6	P1B	The 1st RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P1A port at the same time. An external capacitor is required to block DC voltage.
7	P1A	The 1st RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P1B port at the same time. An external capacitor is required to block DC voltage.
12	PCB	Common RF port of the 2nd switch. This port is connected with either of P1B, P2B, and P3B port. An external capacitor is required to block DC voltage.
13	PCA	Common RF port of the 1st switch. This port is connected with either of P1A, P2A, and P3A port. An external capacitor is required to block DC voltage.
15	VDD	Positive voltage supply terminal. The positive voltage (+1.5~+4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
17	CTL2	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
18	CTL1	Control signal input terminal. This terminal is set to High-Level (+1.3V~4.5V) or Low-Level (0~+0.4V).
19	P3B	The 3rd RF port of the 2nd switch. This port is connected with PCB port. PCA port is connected with P3A port at the same time. An external capacitor is required to block DC voltage.
20	P3A	The 3rd RF port of the 1st switch. This port is connected with PCA port. PCB port is connected with P3B port at the same time. An external capacitor is required to block DC voltage.
1,3,5,8,9, 10,11,14, 16	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)

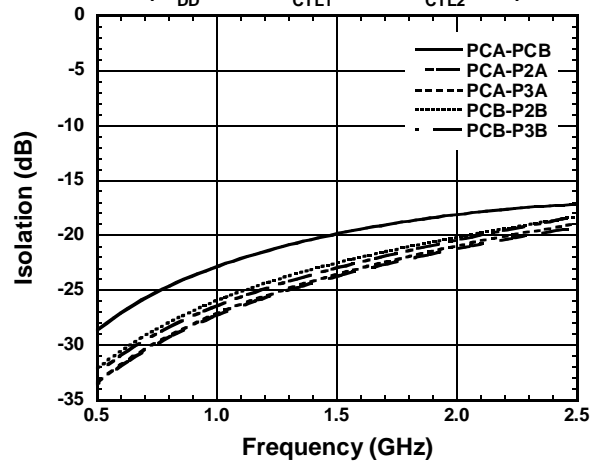
### Insertion Loss vs. Frequency

( $V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V$ )



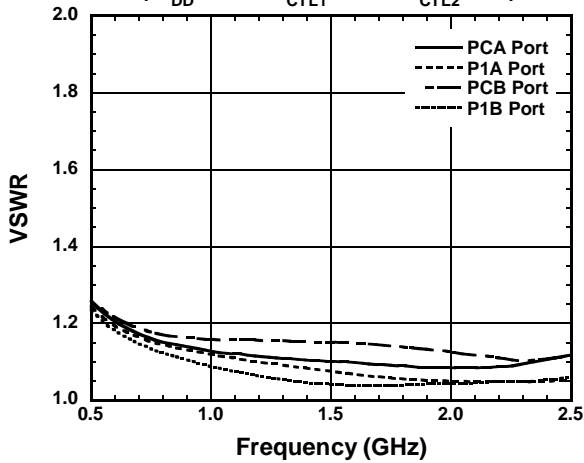
### Isolation vs. Frequency

( $V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V$ )



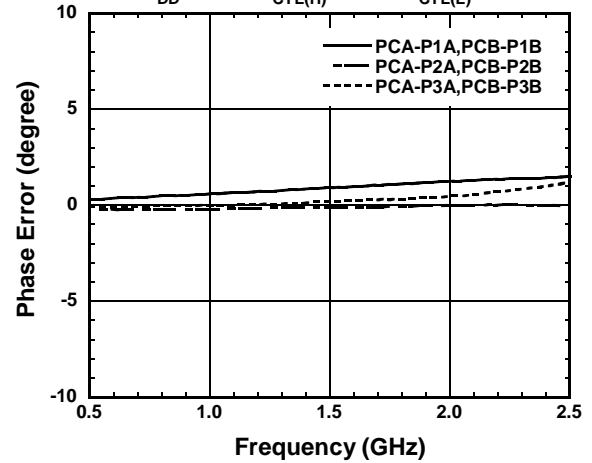
### VSWR vs. Frequency

( $V_{DD}=2.7V, V_{CTL1}=1.8V, V_{CTL2}=0V$ )



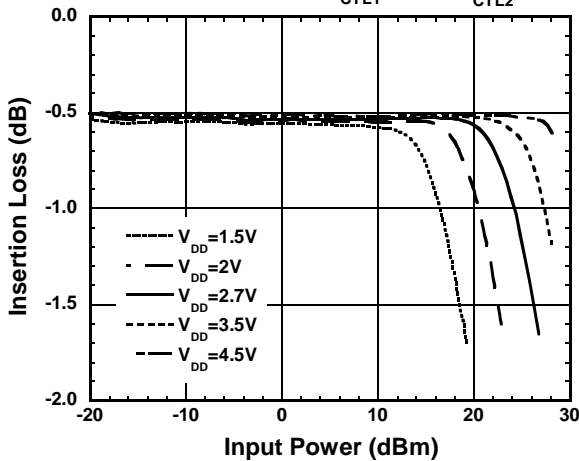
### Phase Error vs. Frequency

( $V_{DD}=2.7V, V_{CTL(H)}=1.8V, V_{CTL(L)}=0V$ )

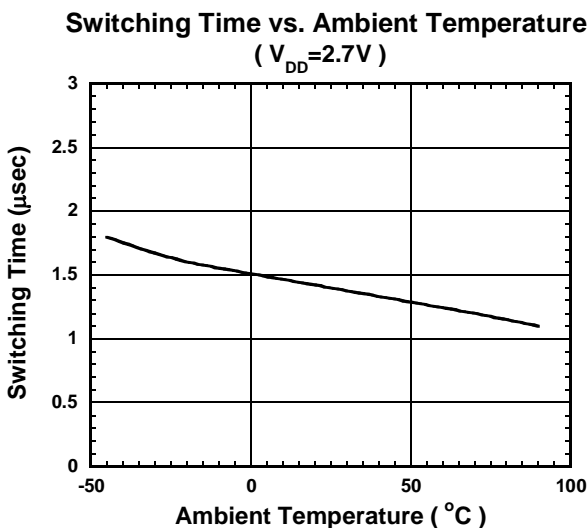
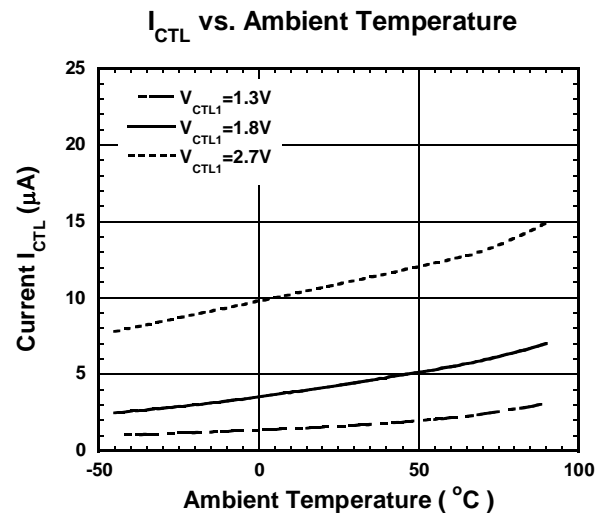
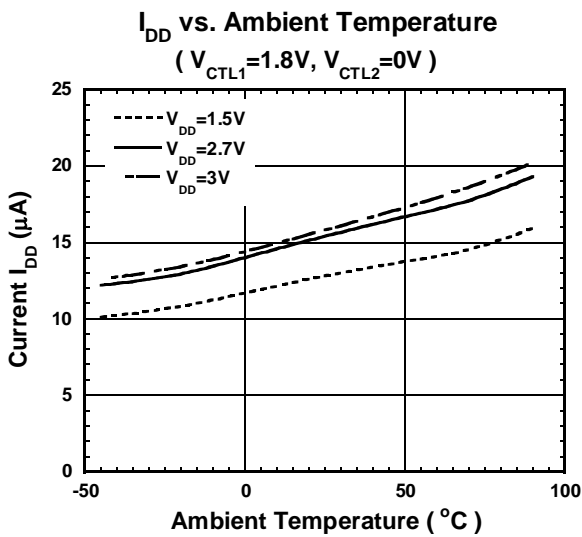
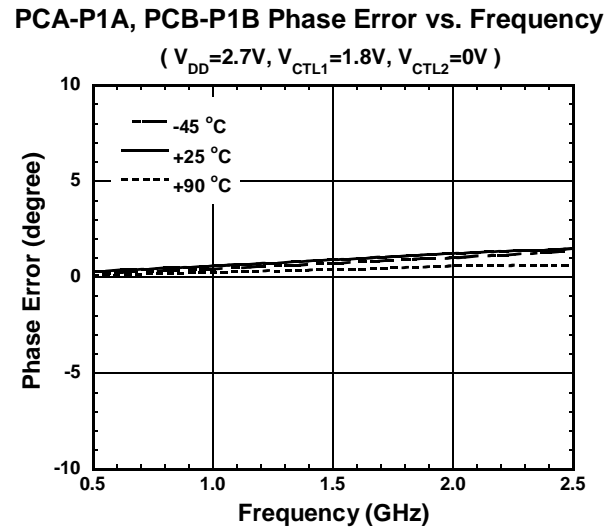
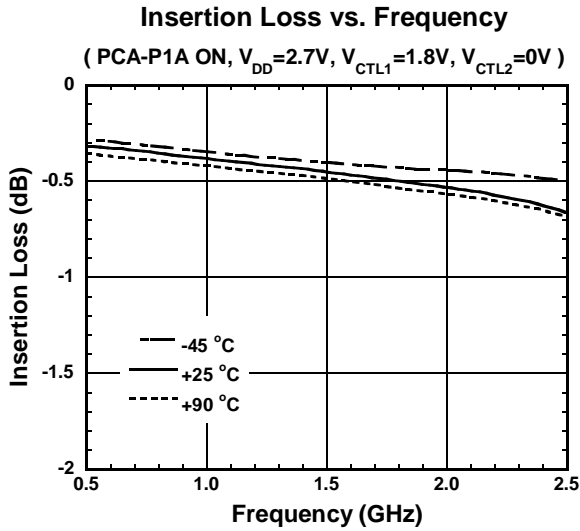


### Insertion Loss vs. Input Power

( $f=2GHz, PCA-P1A$  ON,  $V_{CTL1}=1.8V, V_{CTL2}=0V$ )

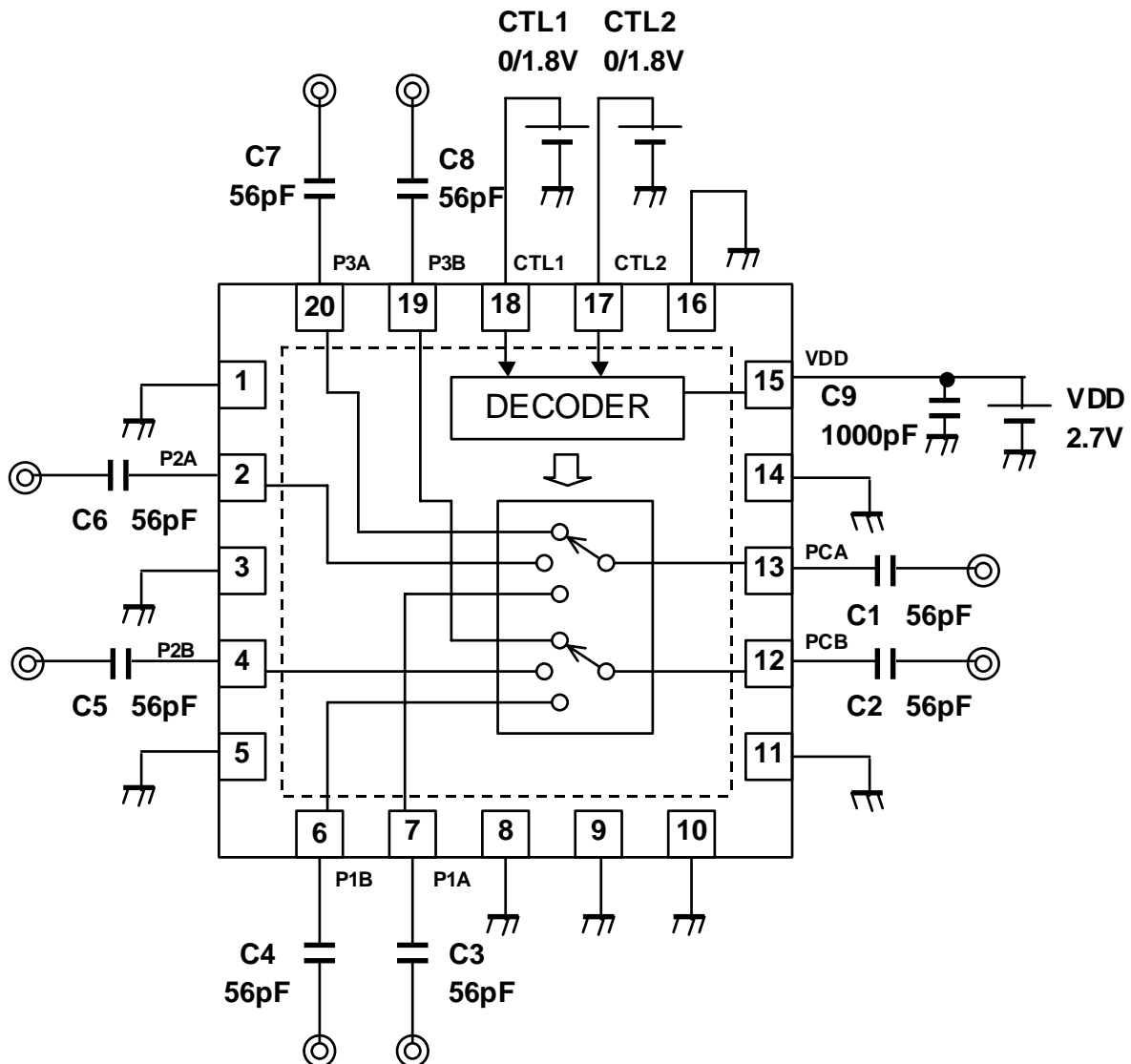


## ■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



# NJG1655SCC

## APPLICATION CIRCUIT

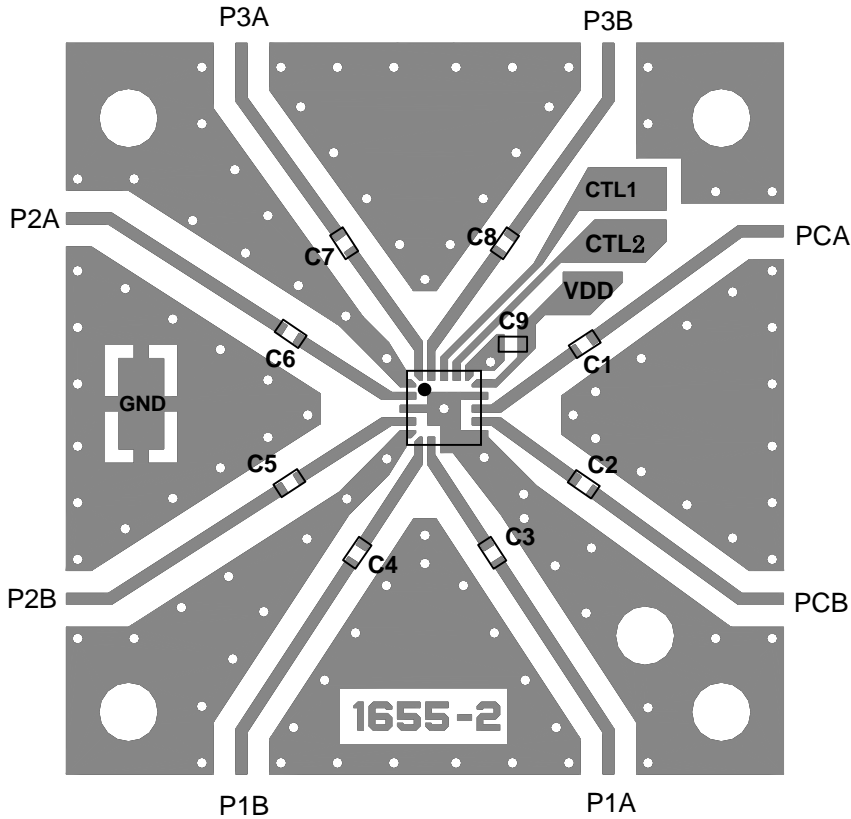


## PARTS LIST

PART ID	Value	Notes
C1~C8	56pF	MURATA (GRM15)
C9	1000pF	

## ■ TEST PCB LAYOUT

(TOP VIEW)



Losses of PCB, capacitors and connectors

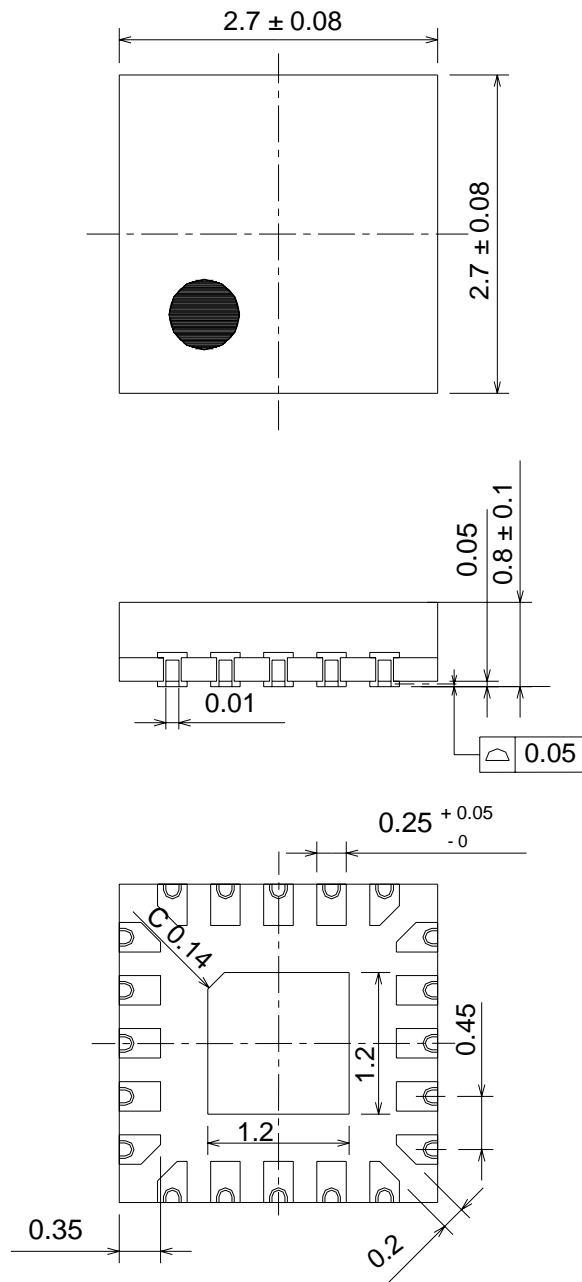
Frequency	Loss
1GHz	0.31dB
2GHz	0.53dB

PCB SIZE=26 x 26mm  
 PCB: FR-4, t=0.2mm  
 STRIPLINE WIDTH=0.4mm

### PRECAUTIONS

- [1] The DC blocking capacitors (C1~C8) must be placed at all RF terminals (PCA, PCB, P1A, P1B, P2A, P2B, P3A and P3B).
- [2] The bypass capacitor (C9) should be placed as close as VDD terminal.
- [3] Please layout ground pattern right under this IC to avoid degradation of isolation or high power characteristics..

## PACKAGE OUTLINE (PCSP20-CC)



Terminal Treat	:Au
Substrate	:FR4
Molding Material	:Epoxy resin
Weight	:14.5mg

Unit	:mm
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### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.