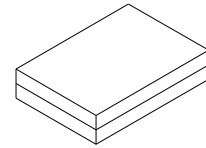


SP9T ANTENNA SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1673LG3 is a GaAs SP9T antenna switch IC designed for GSM/CDMA/UMTS multimode handsets. This switch features very small package size (3.2mmx2.5mmx0.85mm), high linearity, low insertion loss and high isolation. The NJG1673LG3 contains a switch die with on-chip logic circuits, ESD protection circuits and a LTCC substrate with built-in two LPFs on GSM transmit paths for suppression of transmitter harmonics. For saving current consumption, the NJG1673LG3 has a sleep mode.

■ PACKAGE OUTLINE

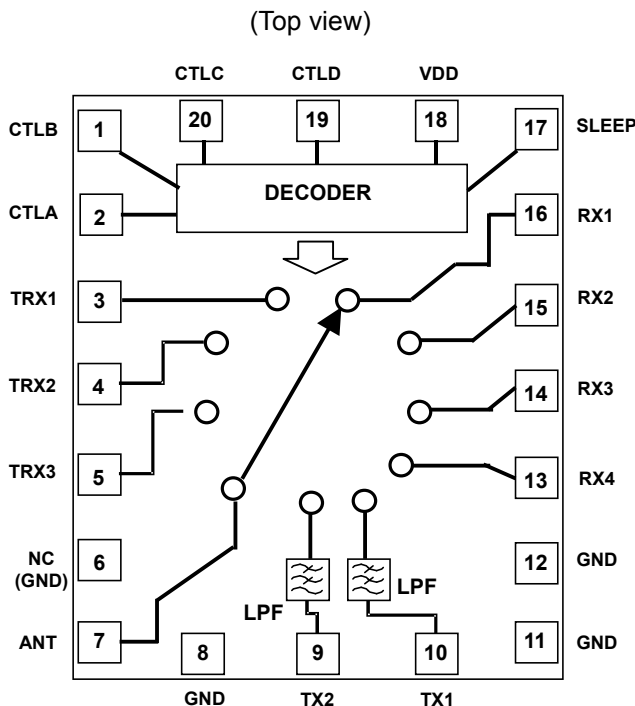


NJG1673LG3

■ FEATURES

- Small package LCSP20-G3 (Package size: 3.2mm x 2.5mm x 0.85mm typ.)
- Sleep mode
- High linearity
 - IMD3 -110dBm typ. @ UMTS Band 1/2/5, $P_{Tx}=20\text{dBm}$, $P_J=-15\text{dBm}$
 - IMD2 -110dBm typ. @ UMTS Band 1/2/5, $P_{Tx}=20\text{dBm}$, $P_J=-15\text{dBm}$
 - 2nd harmonics -75dBc typ. @ GSM850/900 Tx, $P_{in}=34\text{dBm}$
 - 3rd harmonics -75dBc typ. @ GSM1800/1900 Tx, $P_{in}=32\text{dBm}$
- Low insertion loss
 - 0.40dB typ. @ UMTS Band 5
 - 0.60dB typ. @ UMTS Band 2
 - 0.70dB typ. @ UMTS Band 1
 - 0.85dB typ. @ GSM850/900 Tx
 - 1.00dB typ. @ GSM1800/1900 Tx
- Built-in two LPFs
 - Attenuation 30dB typ. on GSM850/900 Tx @2fo / 3fo
 - Attenuation 30dB typ. on GSM1800/1900 Tx @2fo / 3fo
- Low operating voltage 2.5V~3.0V (2.7V typ)
- High ESD tolerance On-chip ESD protection circuit
- Lead-free and halogen-free

■ PIN CONFIGURATION



PIN CONNECTION

1. CTLB
2. CTLA
3. TRX1
4. TRX2
5. TRX3
6. NC (GND)
7. ANT
8. GND
9. TX2
10. TX1
11. GND
12. GND
13. RX4
14. RX3
15. RX2
16. RX1
17. SLEEP
18. VDD
19. CTLD
20. CTLC

NOTE: The information on this datasheet is subject to change without notice.

NJG1673LG3

■ TRUTH TABLE

"H"= $V_{CTL(H)}$, "L"= $V_{CTL(L)}$

On Path	CTLA	CTLB	CTLC	CTLD	SLEEP	VDD
TX1 - ANT	H	H	L	L	H	H
TX2 - ANT	H	L	L	L	H	H
ANT-RX1	L	L	L	L	H	H
ANT-RX2	L	L	H	L	H	H
ANT-RX3	L	H	H	L	H	H
ANT-RX4	L	H	L	L	H	H
ANT-TRX1	H	L	H	L	H	H
ANT-TRX2	H	H	H	L	H	H
ANT-TRX3	H	L	H	H	H	H
Sleep mode	X	X	X	X	L	X

* X: Do not care

■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$

PARAMETER	SYMBOL	CONDITIONS		Duty Cycle	RATINGS	UNITS
RF Input Power	Pin	GSM800 TX	824MHz~849MHz	4:8	36	dBm
		GSM900 TX	880MHz~915MHz	4:8	36	dBm
		GSM1800 TX	1710MHz~1785MHz	4:8	34	dBm
		GSM1900 TX	1850MHz~1910MHz	4:8	34	dBm
		UMTS(Band1)	1920MHz~1980MHz	CW	34	dBm
		UMTS(Band2)	1850MHz~1910MHz	CW	34	dBm
		UMTS(Band5)	824MHz~849MHz	CW	34	dBm
		All RX port	869MHz~2170MHz	CW	28	dBm
Supply Voltage	V_{DD}	V_{DD} terminal			3.2	V
Control Voltage	V_{CTL}	V_{CTL} terminal			4	V
Power dissipation	P_d	Four-layer FR4 PCB with through-hole (101mmx114mm), $T_j=150^{\circ}\text{C}$			2400	mW
Operating Temperature	T_{opr}				-40~+95	$^{\circ}\text{C}$
Storage Temperature	T_{stg}				-65~+150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS 1 (DC)

General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}	V_{DD} terminal	2.5	2.7	3.0	V
Operating current 1	IDD1	V_{DD} terminal, SLEEP =1.8V, TX1 ON 824MHz~915MHz, Pin=34dBm	-	600	1000	μA
Operating current 2	IDD2	V_{DD} terminal, Sleep mode, SLEEP =0V	-	4	10	μA
Control voltage (HIGH)	$V_{CTL(H)}$		1.35	1.8	3.0	V
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.4	V
Control current	ICTL	CTLA~D, SLEEP terminal	-	6	20	μA

NJG1673LG3

■ ELECTRICAL CHARACTERISTICS 2 (RF)

General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Insertion loss 1	LOSS1	TX1 - ANT, 824~849MHz, 880~915MHz, Pin=34dBm	-	0.85	1.10	dB
Insertion loss 2	LOSS2	TX2 - ANT, 1710MHz~1785MHz, 1850MHz~1910MHz, Pin=32dBm	-	1.00	1.30	dB
Insertion loss 3(1)	LOSS3(1)	ANT - RX1~3, 869MHz~894MHz, 925MHz~960MHz, Pin=10dBm	-	0.90	1.10	dB
Insertion loss 3(2)	LOSS3(2)	ANT - RX1~3, 1805MHz~1880MHz, 1930MHz~1990MHz, Pin=10dBm	-	1.10	1.30	dB
Insertion loss 4(1)	LOSS4(1)	TRX1~3 - ANT 824MHz~849MHz, 869MHz~894MHz, Pin=26dBm	-	0.40	0.55	dB
Insertion loss 4(2)	LOSS4(2)	TRX1~3 - ANT 880MHz~915MHz, 925MHz~960MHz, Pin=26dBm	-	0.45	0.60	dB
Insertion loss 4(3)	LOSS4(3)	TRX1~3 - ANT 1850MHz~1910MHz, 1930MHz~1990MHz, Pin=26dBm	-	0.60	0.75	dB
Insertion loss 4(4)	LOSS4(4)	TRX1~3 - ANT, 1920MHz~1980MHz, 2110MHz~2170MHz, Pin=26dBm	-	0.70	0.85	dB
VSWR 1	VSWR 1	TX1,2 ON, Input / output port	-	-	1.5	
VSWR 2	VSWR 2	RX1~4 ON, Input / output port	-	-	1.5	
VSWR 3	VSWR 3	TRX1~3 ON, Input / output On port	-	-	1.5	
Isolation 1	ISL1	TX1 ON, TX1 to RX1~4, 824~849MHz, 880~915MHz, Pin=34dBm	35	40	-	dB
Isolation 2	ISL2	TX2 ON, TX2 to RX1~4, 1710MHz~1785MHz, 1850MHz~1910MHz, Pin=32dBm	40	50	-	dB
Isolation 3(1)	ISL3(1)	RX1~4 ON, TX1 to ANT, 824~849MHz, 880~915MHz, Pin=10dBm	25	30	-	dB
Isolation 3(2)	ISL3(2)	RX1~4 ON, TX2 to ANT, 1710MHz~1785MHz, 1850MHz~1910MHz, Pin=10dBm	25	30	-	dB
Isolation 4	ISL4	TRX1~3 ON, TRX1~3 to RX1~4, 824MHz~849MHz, 880MHz~915MHz, 1850MHz~1910MHz, 1920MHz~1980MHz, Pin=26dBm	45	50	-	dB
Switching time	TSW	All paths $T_a=-20\text{deg}\sim+85\text{deg}$	-	3	8	μs

■ ELECTRICAL CHARACTERISTICS 2 (RF)

General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Units
2nd harmonics 1	2fo(1)	TX1 ON, fo= 824~849MHz, 880~915MHz, Pin=34dBm	-	-75	-70	dBc
2nd harmonics 2	2fo(2)	TX2 ON, fo= 1710MHz~1785MHz, 1850MHz~1910MHz, Pin=32dBm	-	-75	-70	dBc
2nd harmonics 3	2fo(3)	TRX1~3 ON, fo= 824MHz~849MHz, 1850MHz~1910MHz, 1920MHz~1980MHz, Pin=26dBm	-	-80	-70	dBc
3rd harmonics 1	3fo(1)	TX1 ON, fo= 824~849MHz, 880~915MHz, Pin=34dBm	-	-75	-70	dBc
3rd harmonics 2	3fo(2)	TX2 ON, fo=1710MHz~1785MHz, 1850MHz~1910MHz, Pin=32dBm	-	-75	-70	dBc
3rd harmonics 3	3fo(3)	TRX1~3 ON, fo= 824MHz~849MHz, 1850MHz~1910MHz, 1920MHz~1980MHz, Pin=26dBm	-	-80	-70	dBc
Attenuation 1	ATT(1)	TX1 ON, 1648MHz~1830MHz	25	30	-	dB
Attenuation 2	ATT(2)	TX1 ON, 2472MHz~2745MHz	25	30	-	dB
Attenuation 3	ATT(3)	TX1 ON, f=3296MHz~12750MHz	20	-	-	dB
Attenuation 4	ATT(4)	TX2 ON, 3420MHz~3820MHz	25	30	-	dB
Attenuation 5	ATT(5)	TX2 ON, 5130MHz~5730MHz	25	30	-	dB
Attenuation 6	ATT(6)	TX2 ON, f=6840MHz~12750MHz	13	-	-	dB

NJG1673LG3

■ ELECTRICAL CHARACTERISTICS 2 (RF)

General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Units
2nd order intermodulation distortion 1	IMD2(1)	TRX1~3 ON, Tone1: $f_{TX}=1950\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=190\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
2nd order intermodulation distortion 2	IMD2(2)	TRX1~3 ON, Tone1: $f_{TX}=1950\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=4090\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
2nd order intermodulation distortion 3	IMD2(3)	TRX1~3 ON, Tone1: $f_{TX}=1880\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=80\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
2nd order intermodulation distortion 4	IMD2(4)	TRX1~3 ON, Tone1: $f_{TX}=1880\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=3840\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
2nd order intermodulation distortion 5	IMD2(5)	TRX1~3 ON, Tone1: $f_{TX}=837\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=45\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
2nd order intermodulation distortion 6	IMD2(6)	TRX1~3 ON, Tone1: $f_{TX}=837\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=1719\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
3rd order intermodulation distortion 1	IMD3(1)	TRX1~3 ON, Tone1: $f_{TX}=1950\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=1760\text{MHz}$, $P_J=-15\text{dBm}$	-	-107	-100	dBm
3rd order intermodulation distortion 2	IMD3(2)	TRX1~3 ON, Tone1: $f_{TX}=1950\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=6040\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
3rd order intermodulation distortion 3	IMD3(3)	TRX1~3 ON, Tone1: $f_{TX}=1880\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=1800\text{MHz}$, $P_J=-15\text{dBm}$	-	-107	-101	dBm
3rd order intermodulation distortion 4	IMD3(4)	TRX1~3 ON, Tone1: $f_{TX}=1880\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=5720\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm
3rd order intermodulation distortion 5	IMD3(5)	TRX1~3 ON, Tone1: $f_{TX}=837\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=792\text{MHz}$, $P_J=-15\text{dBm}$	-	-107	-102	dBm
3rd order intermodulation distortion 6	IMD3(6)	TRX1~3 ON, Tone1: $f_{TX}=837\text{MHz}$, $P_{TX}=20\text{dBm}$, Tone2: $f_J=2556\text{MHz}$, $P_J=-15\text{dBm}$	-	-110	-102	dBm

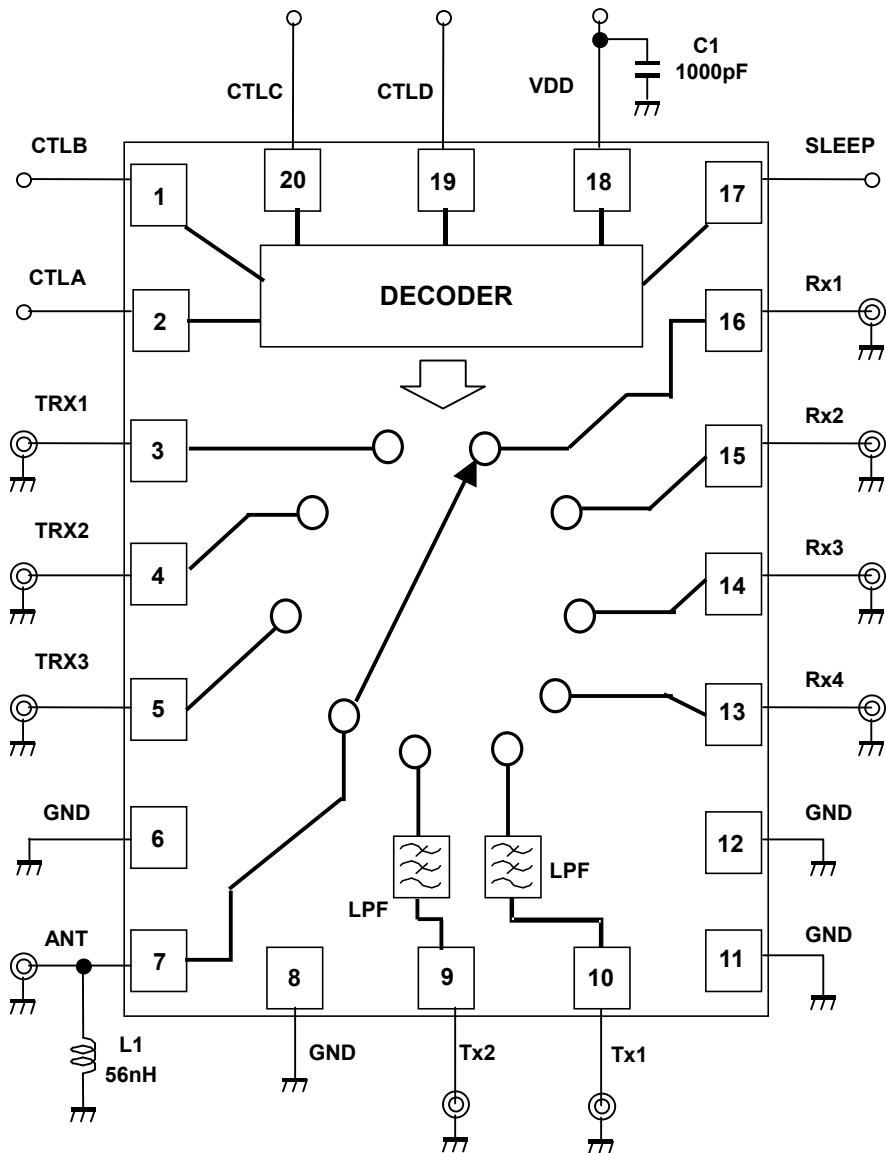
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	CTLB	Control signal input terminal. This terminal is set to High-Level (+1.35~+3.0V) or Low-Level (0~+0.4V).
2	CTLA	Control signal input terminal. This terminal is set to High-Level (+1.35~+3.0V) or Low-Level (0~+0.4V).
3	TRX1	RF transmitting/receiving port.
4	TRX2	RF transmitting/receiving port.
5	TRX3	RF transmitting/receiving port.
6	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Connect to the PCB ground plane.
7	ANT	RF transmitting/receiving port. Please connect an inductor with GND terminal for ESD protection.
8,11,12	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	TX2	RF transmitting port. This port is connected the LPF for GSM1800/1900 TX band into LTCC substrate.
10	TX1	RF transmitting port. This port is connected the LPF for GSM850/900 TX band into LTCC substrate.
13	RX4	RF receiving port.
14	RX3	RF receiving port.
15	RX2	RF receiving port.
16	RX1	RF receiving port.
17	SLEEP	Control terminal of switching between normal operation mode and sleep mode. This terminal is set to High-Level (+1.35~+3.0V) or Low-Level (0~+0.4V).
18	VDD	Positive voltage supply terminal. The positive voltage (+2.5~+3.0V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
19	CTLD	Control signal input terminal. This terminal is set to High-Level (+1.35~+3.0V) or Low-Level (0~+0.4V).
20	CTLC	Control signal input terminal. This terminal is set to High-Level (+1.35~+3.0V) or Low-Level (0~+0.4V).

NJG1673LG3

APPLICATION CIRCUIT

(TOP VIEW)



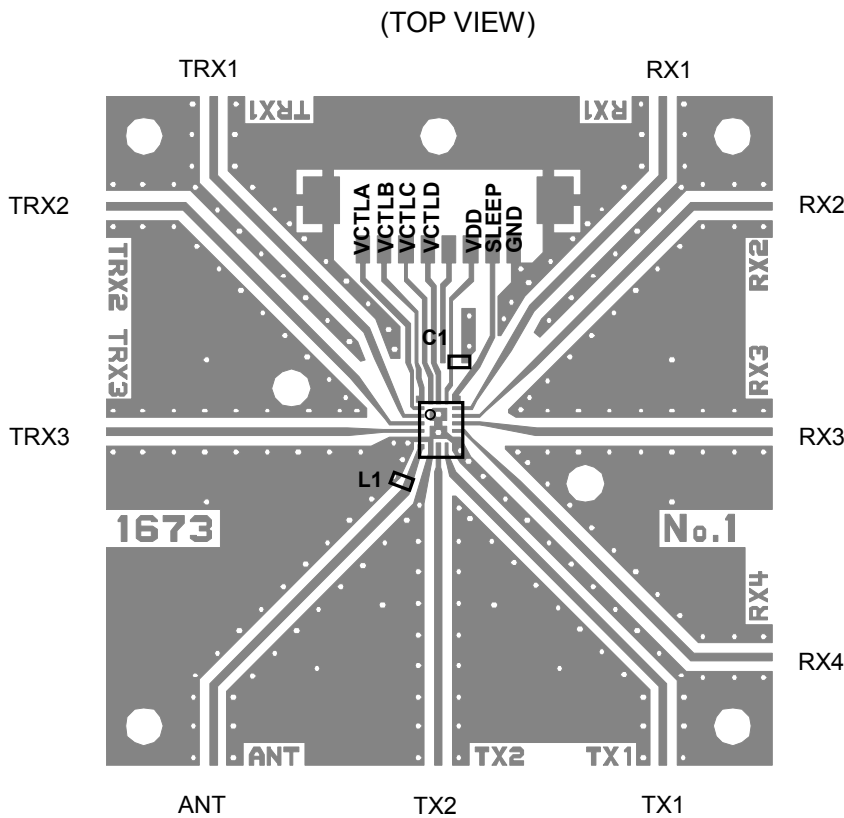
PARTS LIST^{*1}

Part Number	Parameters	Notes
C1	1000 pF	Bypass capacitor
L1	56 nH	*2

*1: No DC blocking capacitors are required on all RF ports. The DC levels of all RF ports are ground.

*2: The inductor of 56nH is required on ANT port in order to enhance ESD robustness.

■ TEST PCB LAYOUT



Board total losses (Connector and PCB)

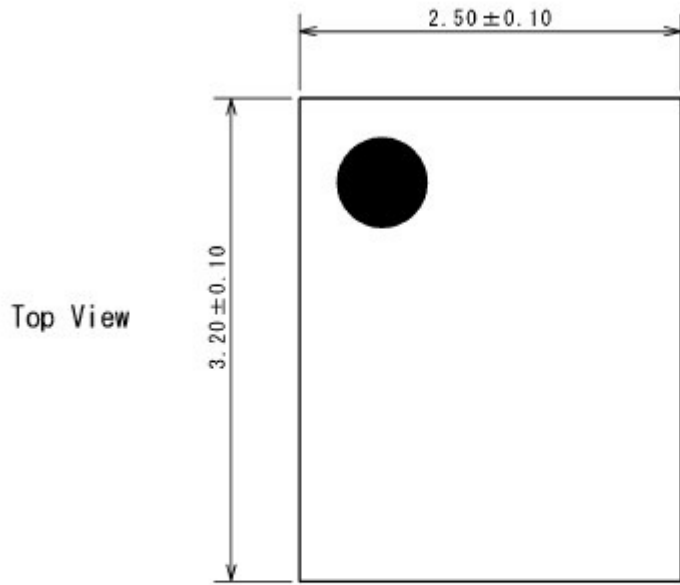
Mode	Frequency (MHz)	Loss (dB)
TX1	824	0.31
	849	0.32
	880	0.32
	915	0.34
TX2	1710	0.49
	1785	0.51
	1850	0.53
RX1	960	0.34
	1990	0.55
RX2	960	0.34
	1990	0.55
RX3	960	0.34
	1990	0.53
RX4	960	0.34
	1990	0.55
TRX1	894	0.33
	960	0.34
	1990	0.55
	2170	0.59
TRX2	894	0.33
	960	0.34
	1990	0.55
	2170	0.59
TRX3	894	0.33
	960	0.33
	1990	0.53
	2170	0.56

PRECAUTIONS

- [1] For good RF performance, the ground terminals should be directly connected to the ground patterns and the through-holes as close as possible by using relatively wide pattern.
- [2] Please connect exposed GND PADS (bottom side of IC) to PCB GND using through holes.

NJG1673LG3

PACKAGE OUTLINE (LCSP20-G3)



UNIT

mm

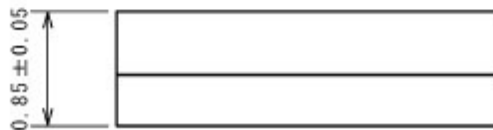
TERMINAL TREAT
SUBSTRATE
MOLDING MATERIAL

Ag/Ni/Pb/Au
Ceramic
Epoxy resin
(Halogen-Free)

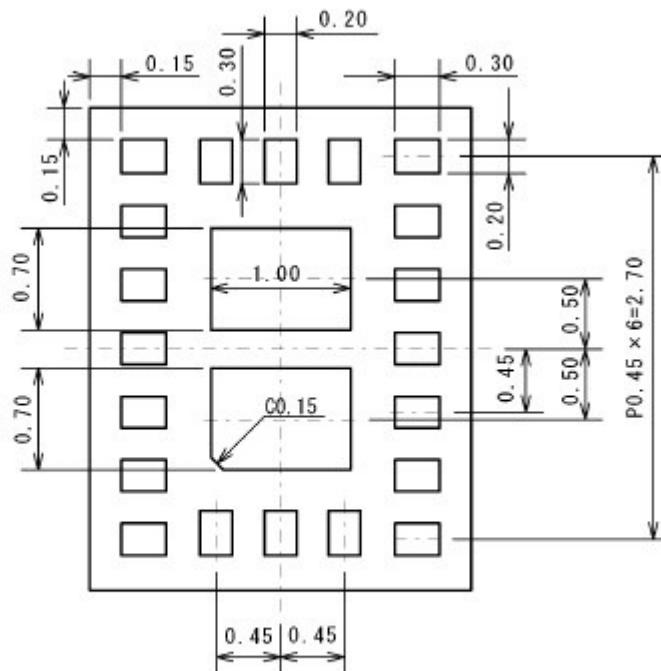
WEIGHT

20 mg

Side View



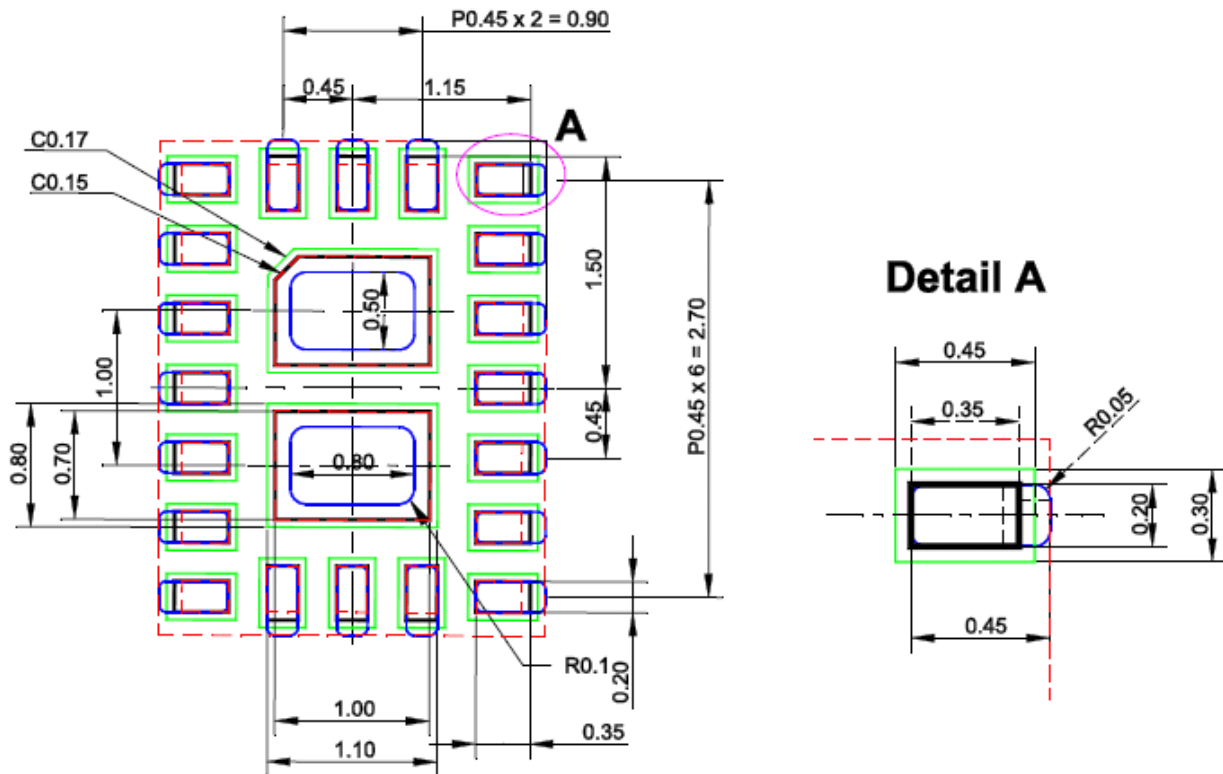
Bottom View



* In case of no designation is tolerance ±0.05mm

RECOMMENDED FOOTPRINT PATTERN

- - - - Red dot lines indicate the package outline and LGA pads (Top View).
- Black solid lines indicate the recommended "Land area" (Top View).
- Green solid lines indicate the recommended "Resist open area" (Top View).
- Blue solid lines indicate the recommended "Solder mask open area" (Top View).



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.