X-SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1692NB2 is a GaAs X (cross) – SPDT(DP4T) switch MMIC, which is designed for switching of balanced (differential) dual band filters.

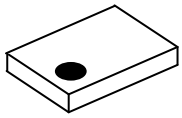
The NJG1692NB2 features very low insertion loss, low control voltage and wide frequency coverage.

The ESD protection circuits are integrated in the IC to achieve high ESD tolerance.

The NJG1692NB2 is assembled in a very small, lead-free, halogen-free, 1.55mm x 1.15mm, 10-pin EPCSP10-B2 package.

*) X-SPDT is a paired SPDT switch controlled synchronously. The X-SPDT includes two SPDT switches whose RF lines have a crossing inside the chip.

■ PACKAGE OUTLINE



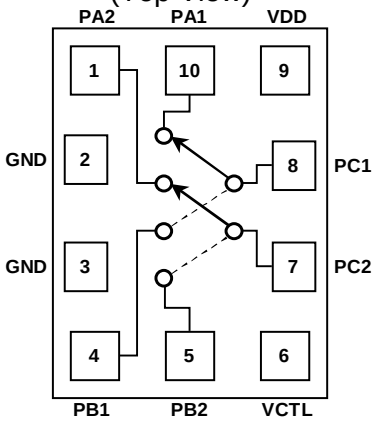
NJG1692NB2

■ FEATURES

- Low operation voltage V_{DD}=+1.5~+4.5V
- Low control voltage $V_{CTL(H)}$=1.8V typ.
- Low insertion loss 0.30dB typ. @f=1.0GHz, P_{IN}=0dBm
  0.35dB typ. @f=2.0GHz, P_{IN}=0dBm
  0.40dB typ. @f=2.7GHz, P_{IN}=0dBm
- High isolation 28dB typ. @f=1.0GHz, P_{IN}=0dBm
  22dB typ. @f=2.0GHz, P_{IN}=0dBm
  19dB typ. @f=2.7GHz, P_{IN}=0dBm
- Small and thin package EPCSP10-B2 (Package size: 1.55x1.15mm)
- RoHS compliant and Halogen Free
- MSL1

■ PIN CONFIGURATION

(Top View)



Pin connection
1. PA2
2. NC (GND)
3. GND
4. PB1
5. PB2
6. VCTL
7. PC2
8. PC1
9. VDD
10. PA1

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	VCTL
PC1-PA1,PC2-PA2	H
PC1-PB1,PC2-PB2	L

NOTE: The Information on this datasheet will be subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25℃, Z_s=Z_l=50Ω

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF input power	P_{IN}	V_{DD} =2.7V, VCTL=0V/1.8V	28	dBm
Supply voltage	V_{DD}	VDD terminal	5.0	V
Control voltage	V_{CTL}	VCTL terminal	5.0	V
Power dissipation	P_D	Four-layer FR4 PCB (101.5mmx114.5mm without through-hole), Tj=150℃	320	mW
Operating temp.	T_{opr}		-40~+90	℃
Storage temp.	T_{stg}		-55~+150	℃

■ ELECTRICAL CHARACTERISTICS

T_a=+25℃, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, with application circuit

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}			1.5	2.7	4.5	V
Operating current	I_{DD}			-	13	30	μA
Control voltage (LOW)	$V_{CTL(L)}$			0	-	0.45	V
Control voltage (HIGH)	$V_{CTL(H)}$			1.35	1.8	4.5	V
Control current	I_{CTL}			-	3	10	μA
Insertion loss 1-1	LOSS1-1	PC1-PA1, PC2-PB2	f=1.0GHz	-	0.30	0.45	dB
Insertion loss 1-2	LOSS1-2		f=2.0GHz	-	0.35	0.50	dB
Insertion loss 1-3	LOSS1-3		f=2.7GHz	-	0.40	0.55	dB
Insertion loss 2-1	LOSS2-1	PC1-PB1, PC2-PA2	f=1.0GHz	-	0.30	0.50	dB
Insertion loss 2-2	LOSS2-2		f=2.0GHz	-	0.40	0.55	dB
Insertion loss 2-3	LOSS2-3		f=2.7GHz	-	0.45	0.65	dB
Isolation 1-1	ISL1-1	PC1-PB1, PC2-PA2	f=1.0GHz	26	28	-	dB
Isolation 1-2	ISL1-2		f=2.0GHz	20	22	-	dB
Isolation 1-3	ISL1-3		f=2.7GHz	17	19	-	dB
Isolation 2-1	ISL2-1	PC1-PA1, PC2-PB2	f=1.0GHz	25	27	-	dB
Isolation 2-2	ISL2-2		f=2.0GHz	19	21	-	dB
Isolation 2-3	ISL2-3		f=2.7GHz	16	18	-	dB
Isolation 3-1	ISL3-1	PC1-PC2	f=1.0GHz	26	28	-	dB
Isolation 3-2	ISL3-2		f=2.0GHz	21	23	-	dB
Isolation 3-3	ISL3-3		f=2.7GHz	20	22	-	dB
Input power at 0.2dB compression point	$P_{-0.2dB}$	f=2.0GHz		20	24	-	dBm
VSWR	VSWR	f=2.0GHz, On port		-	1.2	1.4	
Switching time	T_{SW}	50% CTL to 10%/90% RF		-	1.5	5.0	μs

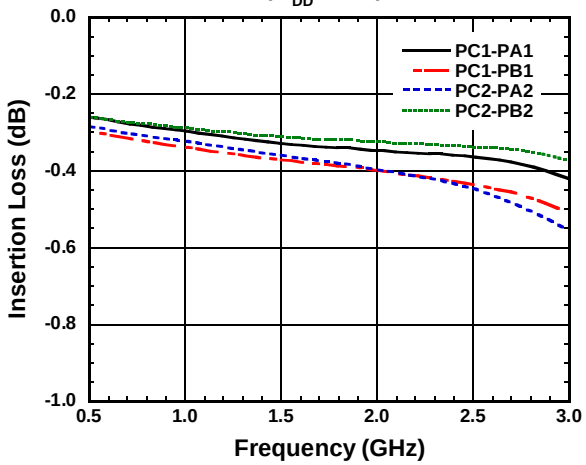
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	PA2	This port is connected to PC2 terminal by applying High-level (1.35~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
4	PB1	This port is connected to PC1 terminal by applying Low-level (0~0.45V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
5	PB2	This port is connected to PC2 terminal by applying Low-level (0~0.45V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
6	VCTL	Control signal input terminal. This terminal is set to high-level (1.35V~4.5V) or low-level (0~0.45V).
7	PC2	Common RF port. This port is connected with either of PA2 or PB2. An external capacitor is required to block DC voltage of internal circuit.
8	PC1	Common RF port. This port is connected with either of PA1 or PB1. An external capacitor is required to block DC voltage of internal circuit.
9	VDD	A supply voltage terminal (1.5~4.5V). Please place a bypass capacitor between this terminal and GND for avoiding RF noise from outside.
10	PA1	This port is connected to PC1 terminal by applying High-level (1.35~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.

■ **ELECTRICAL CHARACTERISTICS** (With application circuit, Loss of external circuit are excluded)

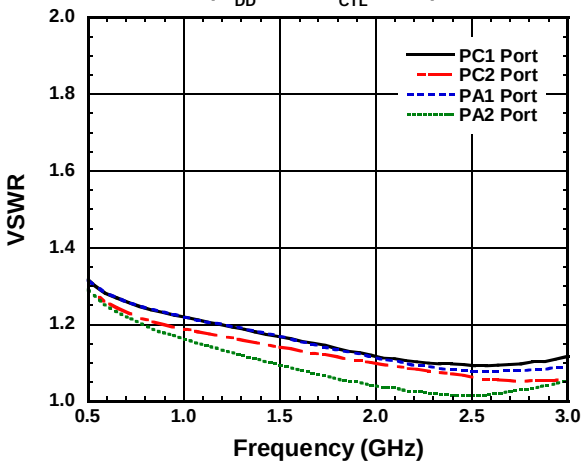
Insertion Loss vs. Frequency

(V_{DD}=2.7V)



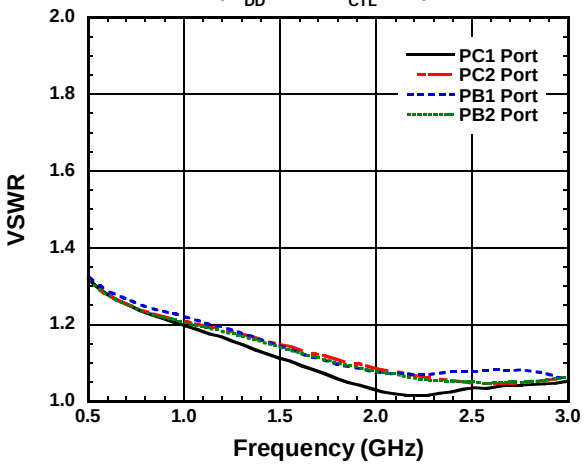
VSWR vs. Frequency

(V_{DD}=2.7V, V_{CTL}=1.8V)



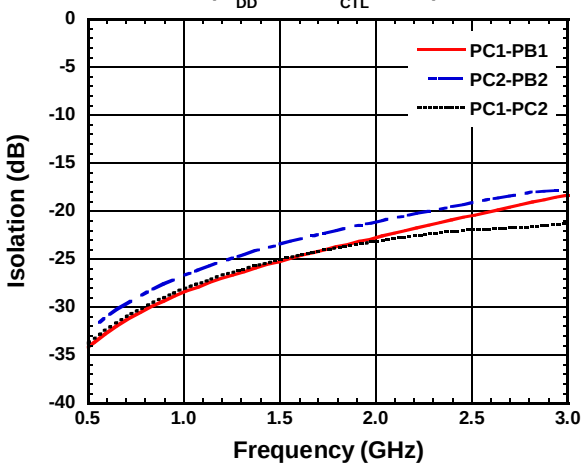
VSWR vs. Frequency

(V_{DD}=2.7V, V_{CTL}=0V)



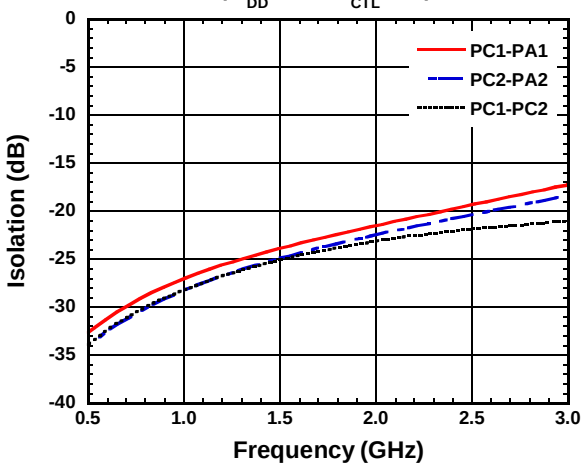
Isolation vs. Frequency

(V_{DD}=2.7V, V_{CTL}=1.8V)

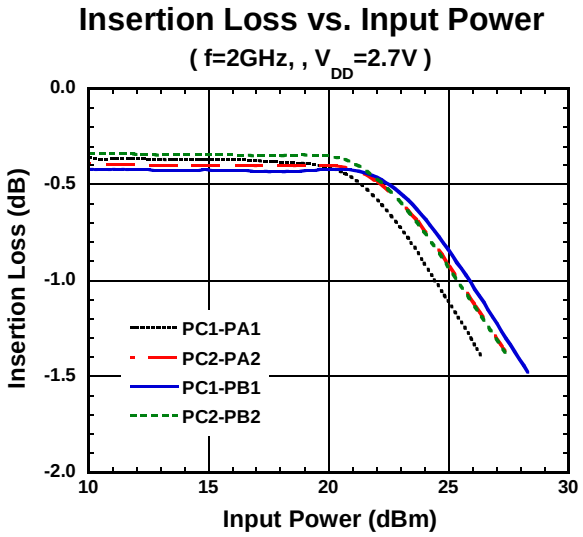


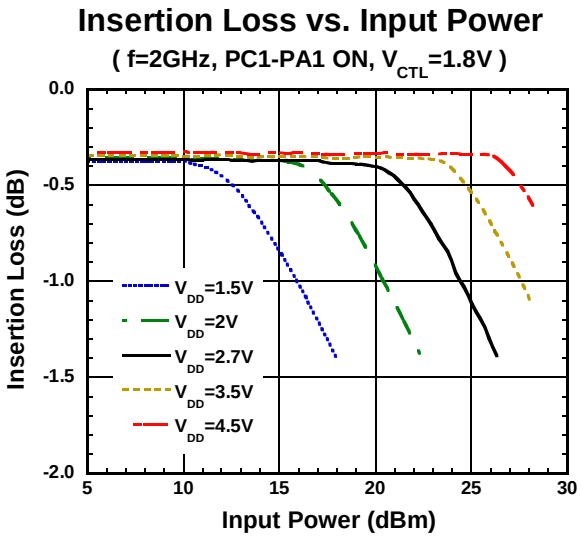
Isolation vs. Frequency

(V_{DD}=2.7V, V_{CTL}=0V)

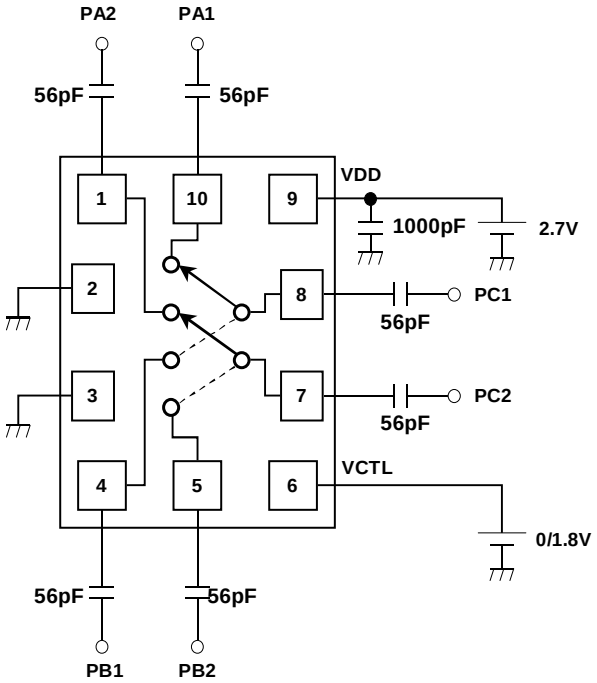


■ **ELECTRICAL CHARACTERISTICS (**With application circuit, Loss of external circuit are excluded)



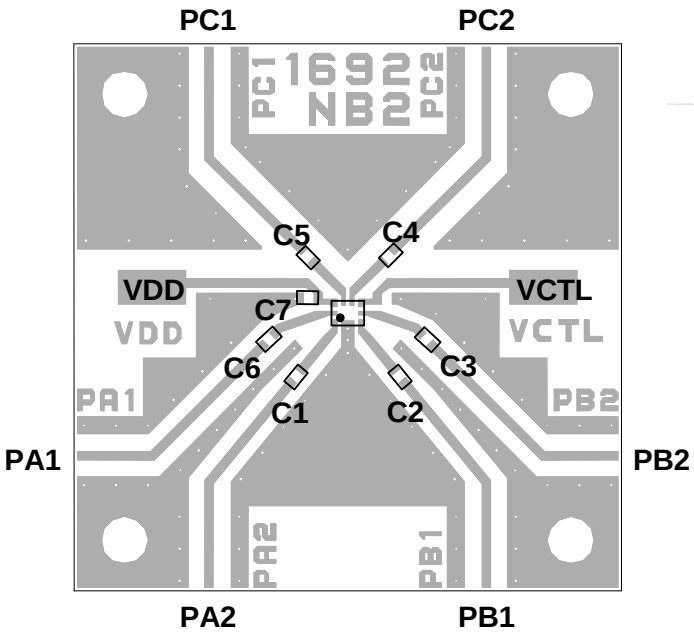


■ APPLICATION CIRCUIT



■ **PCB LAYOUT**

(TOP VIEW)



PCB: FR-4, t=0.2mm
Capacitor Size: 1005
Strip Line Width: 0.4mm
PCB Size: 26 x 26mm

Losses of PCB, capacitors and connectors

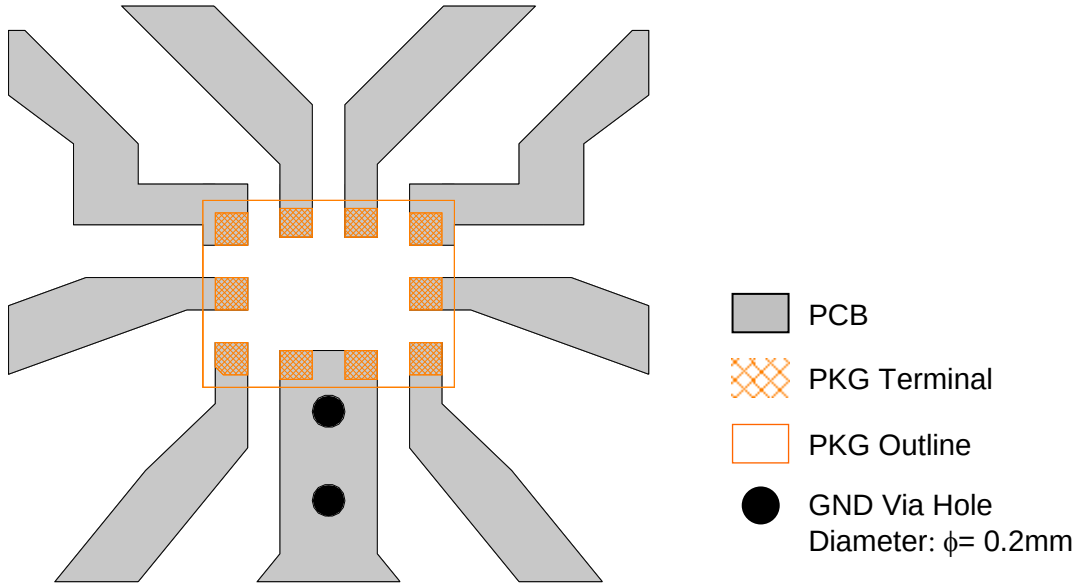
Frequency (GHz)	Loss (dB)
1.0	0.33
2.0	0.54
2.7	0.69

■ **PARTS LIST**

PART ID	Value	COMMENT
C1~C6	56pF	MURATA (GRM15)
C7	1000pF	MURATA (GRM15)

■ PCB LAYOUT (EPCSP10-B2)

(TOP VIEW)



■ PCB LAYOUT PRECAUTIONS

[1] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1~C6).(However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.)

[2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor (C7) close to VDD terminal.

[3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

■ RECOMMENDED FOOTPRINT PATTERN (EPCSP10-B2)

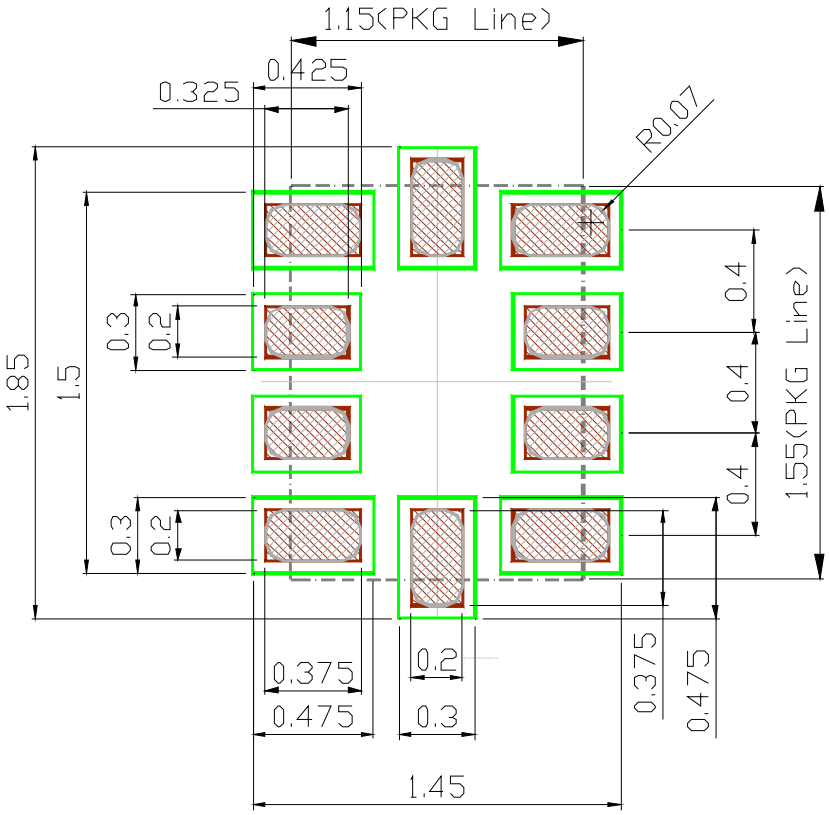
PKG : 1.15mm x 1.55mm

Pin pitch : 0.4mm

: Land

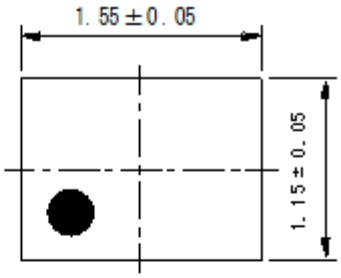
:Mask (Open area) *Metal mask thickness : 100um

:Resist(Open area)

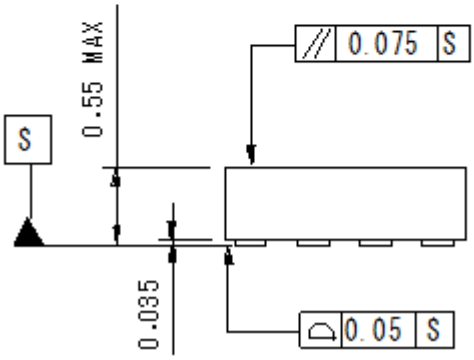


■ PACKAGE OUTLINE (EPCSP10-B2)

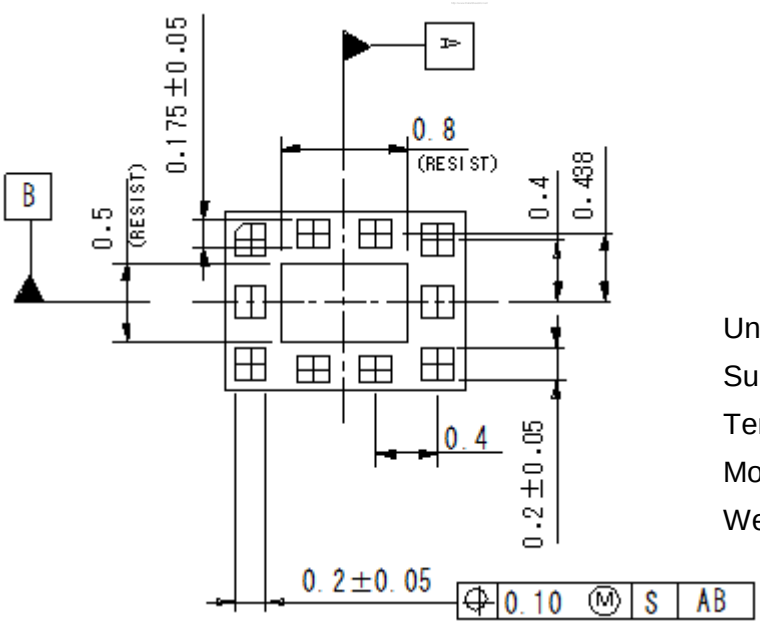
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Unit : mm
Substrate : FR-4
Terminal treat : Au
Molding material : Epoxy resin
Weight : 2.0mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.