High Isolation X-SPDT (DP4T) SWITCH

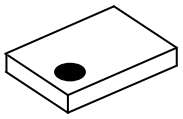
■ GENERAL DESCRIPTION

The NJG1800NB2 is a GaAs X (cross) – SPDT (DP4T) switch MMIC, which is designed for switching of balanced (differential) dual band filters. The switch IC features very low insertion loss and very high isolation for balanced signal input. It has integrated DC blocking capacitors at PC1 and PC2 ports. The ESD protection circuits are integrated in the IC to achieve high ESD tolerance.

The NJG1800NB2 is assembled in a very small, lead-free, halogen-free, 1.55mm x 1.15mm, 10-pin EPCSP10-B2 package.

*) X-SPDT is a paired SPDT switch controlled synchronously. The X-SPDT includes two SPDT switches whose RF lines have a crossing inside the chip.

■ PACKAGE OUTLINE



NJG1800NB2

■ APPLICATIONS

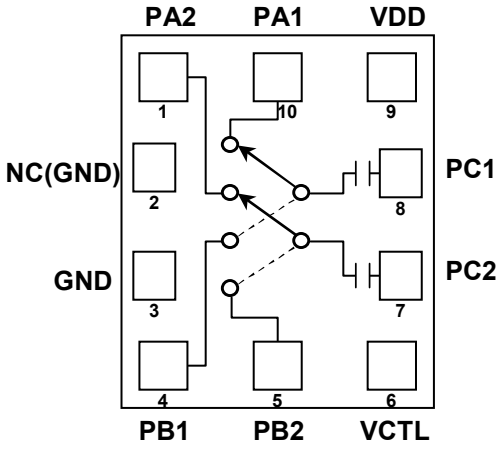
Balanced filter switching application
LTE, UMTS, CDMA and GSM Multi-mode or Multi-band applications
Mobile phone, Tablet PC, Data card, Router and others mobile device applications

■ FEATURES

- Low operation voltage V_{DD}=2.7V typ.
- Low control voltage $V_{CTL(H)}$=1.8V typ.
- High isolation 39dB typ. @f=2.0GHz, P_{IN}=0dBm
  (Balanced mode) 37dB typ. @f=2.7GHz, P_{IN}=0dBm
- Low insertion loss 0.38dB typ. @f=2.0GHz, P_{IN}=0dBm
  (Balanced mode) 0.36dB typ. @f=2.7GHz, P_{IN}=0dBm
- Small and thin package EPCSP10-B2 (Package size: 1.55x1.15x0.55mm)
- RoHS compliant and Halogen Free
- MSL1

■ PIN CONFIGURATION

(Top View)



Pin connection
1. PA2
2. NC (GND)
3. GND
4. PB1
5. PB2
6. VCTL
7. PC2
8. PC1
9. VDD
10. PA1

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

ON PATH	VCTL
PC1-PA1,PC2-PA2	H
PC1-PB1,PC2-PB2	L

NOTE: The Information on this datasheet will be subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25°C, Balanced mode Z_s=Z_l=100Ω, Singled mode Z_s=Z_l=50Ω

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF input power	P_{IN}	V_{DD} =2.7V, VCTL=0V/1.8V	28	dBm
Supply voltage	V_{DD}	VDD terminal	5.0	V
Control voltage	V_{CTL}	VCTL terminal	5.0	V
Power dissipation	P_D	Four-layer FR4 PCB (101.5mmx114.5mm without through-hole), Tj=150°C	320	mW
Operating temp.	T_{opr}		-40~+90	°C
Storage temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS

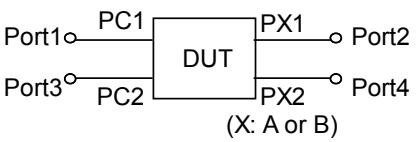
Balanced mode Z_s=Z_l=100Ω, Singled mode Z_s=Z_l=50Ω, T_a=+25°C, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		1.5	2.7	4.5	V
Operating current	I_{DD}	No RF input, V_{DD}=2.7V	-	13	30	μA
Control voltage (LOW)	$V_{CTL(L)}$		0	-	0.45	V
Control voltage (HIGH)	$V_{CTL(H)}$		1.35	1.8	4.5	V
Control current	I_{CTL}	$V_{CTL(H)}$=1.8V	-	3	10	μA
Balanced mode Insertion loss 1 (Note1)	B-LOSS1	f=0.5GHz, PC-PA,PB	-	0.45	0.65	dB
Balanced mode Insertion loss 2	B-LOSS2	f=1.0GHz, PC-PA,PB	-	0.40	0.60	dB
Balanced mode Insertion loss 3	B-LOSS3	f=2.0GHz, PC-PA,PB	-	0.38	0.58	dB
Balanced mode Insertion loss 4	B-LOSS4	f=2.7GHz, PC-PA,PB	-	0.36	0.56	dB
Balanced mode Isolation 1 (Note1)	B-ISL1	f=0.5 GHz, PC-PA,PB	45	50		dB
Balanced mode Isolation 2	B-ISL2	f=1.0GHz, PC-PA,PB	40	45		dB
Balanced mode Isolation 3	B-ISL3	f=2.0GHz, PC-PA,PB	34	39		dB
Balanced mode Isolation 4	B-ISL4	f=2.7GHz, PC-PA,PB	32	37	-	dB
Input power at 0.2dB compression point	$P_{-0.2dB}$	f=2.0GHz, PC1-PA1,PB1, PC2-PA2,PB2	18	22	-	dBm
VSWR	VSWR	f=2.0GHz, PC1-PA1,PB1, PC2-PA2,PB2	-	1.2	1.4	
Switching time	T_{SW}	50% CTL to 10%/90% RF	-	1.5	5.0	μs

Note1:

The conversion of singled mode S-parameter to balanced mode S-parameter uses the following formula.

$$\text{B - LOSS, B - ISL} = \frac{1}{2}\left(S_{21} - S_{23} - S_{41} + S_{43}\right)$$



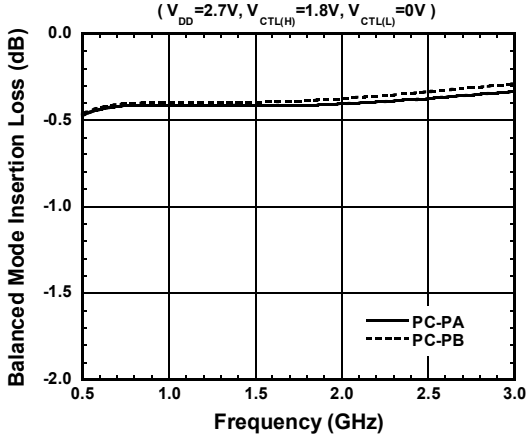
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	PA2	This port is connected to PC2 terminal by applying High-level (1.35~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
2	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground Plane.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for good RF performance.
4	PB1	This port is connected to PC1 terminal by applying Low-level (0~0.45V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
5	PB2	This port is connected to PC2 terminal by applying Low-level (0~0.45V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.
6	VCTL	Control signal input terminal. This terminal is set to high-level (1.35V~4.5V) or low-level (0~0.45V).
7	PC2	Common RF port. This port is connected with either of PA2 or PB2. No external capacitors are required.
8	PC1	Common RF port. This port is connected with either of PA1 or PB1. No external capacitors are required.
9	VDD	A supply voltage terminal (1.5~4.5V). Please place a bypass capacitor between this terminal and GND for avoiding RF noise from outside.
10	PA1	This port is connected to PC1 terminal by applying High-level (1.35~4.5V) at VCTL terminal. An external capacitor is required to block DC voltage of internal circuit.

■ **ELECTRICAL CHARACTERISTICS** (With application circuit, Loss of external circuit are excluded)

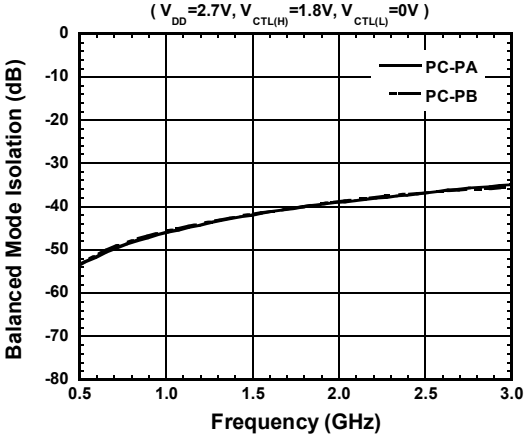
Balanced Mode Insertion Loss vs. Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



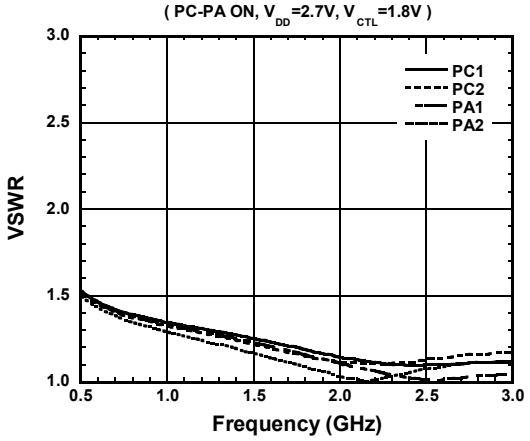
Balanced Mode Isolation vs. Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



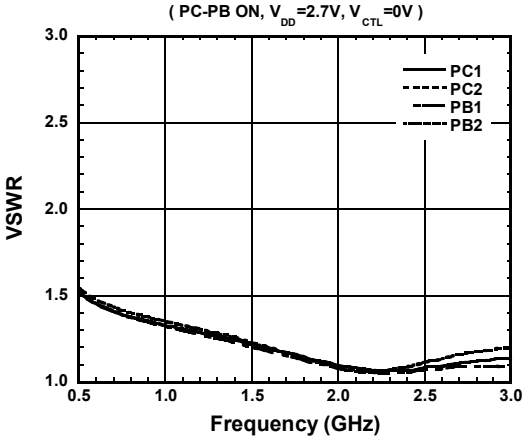
VSWR vs. Frequency

(PC-PA ON, V_{DD}=2.7V, V_{CTL}=1.8V)



VSWR vs. Frequency

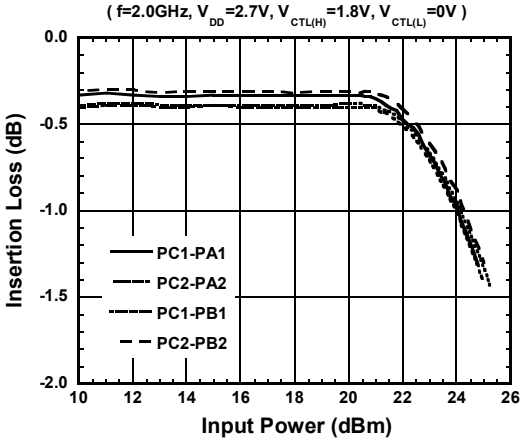
(PC-PB ON, V_{DD}=2.7V, V_{CTL}=0V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, Loss of external circuit are excluded)

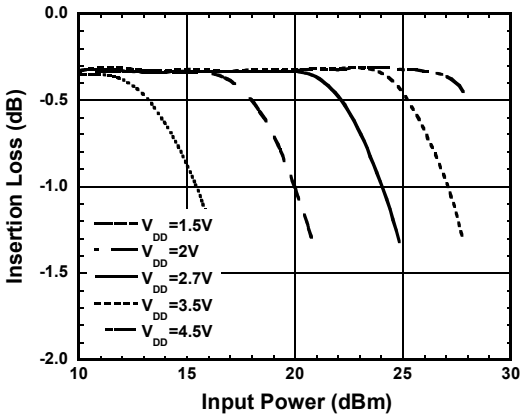
Insertion Loss vs. Input Power

(f=2.0GHz, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



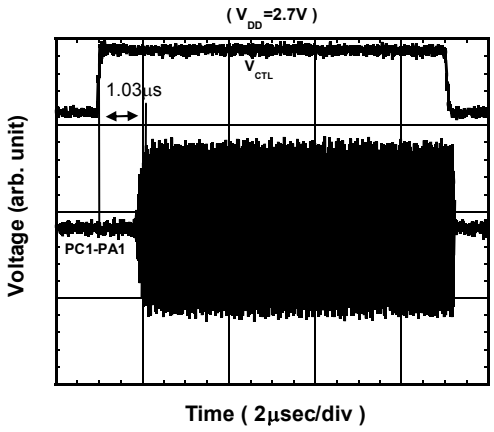
Insertion Loss vs. Input Power

(f=2.0GHz, PC1-PA1 ON, V_{CTL}=1.8V)



Switching Time

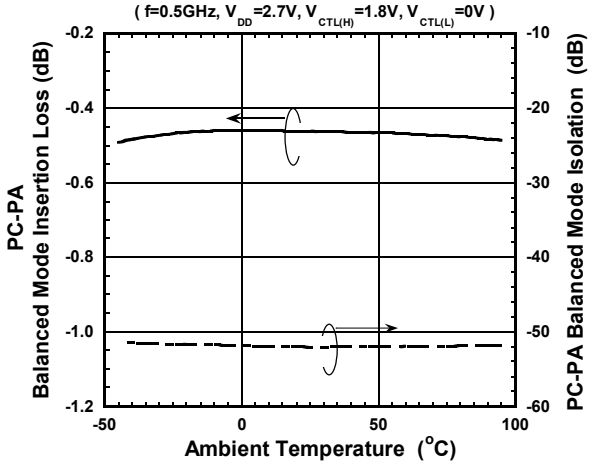
(V_{DD}=2.7V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, Loss of external circuit are excluded)

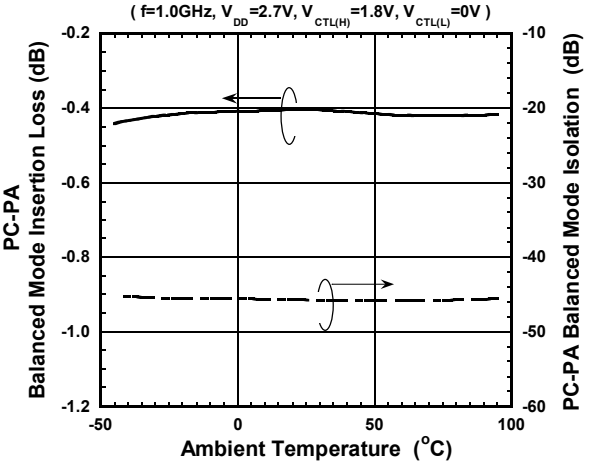
Balanced Mode Loss, ISL vs Ambient Temperature

(f=0.5GHz, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



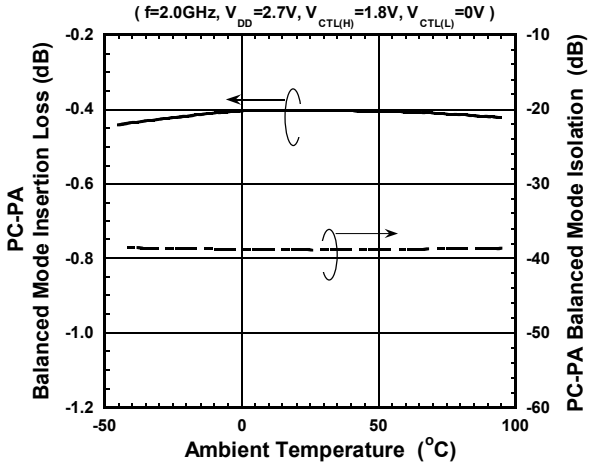
Balanced Mode Loss, ISL vs Ambient Temperature

(f=1.0GHz, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



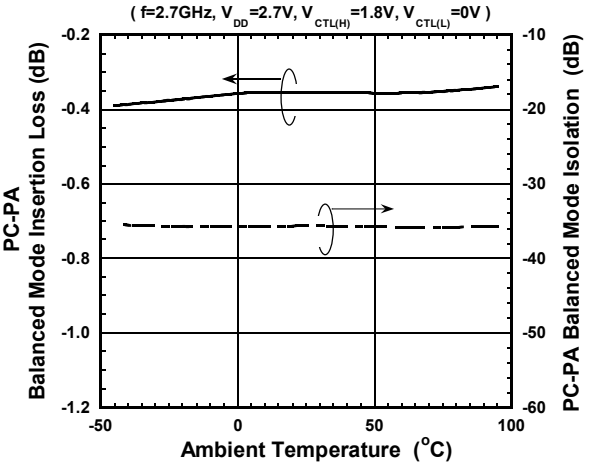
Balanced Mode Loss, ISL vs Ambient Temperature

(f=2.0GHz, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



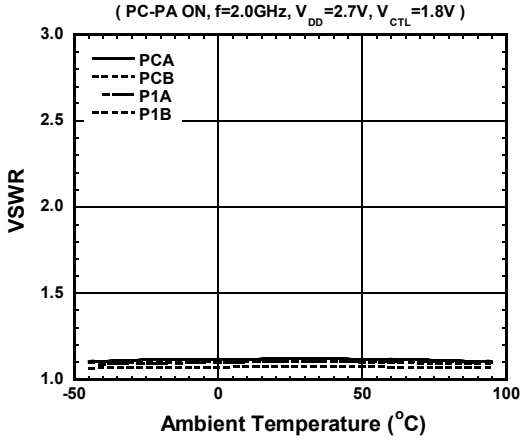
Balanced Mode Loss, ISL vs Ambient Temperature

(f=2.7GHz, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



VSWR vs. Ambient Temperature

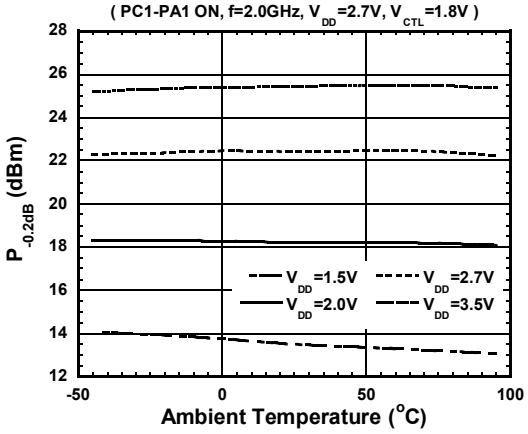
(PC-PA ON, f=2.0GHz, V_{DD}=2.7V, V_{CTL}=1.8V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, Loss of external circuit are excluded)

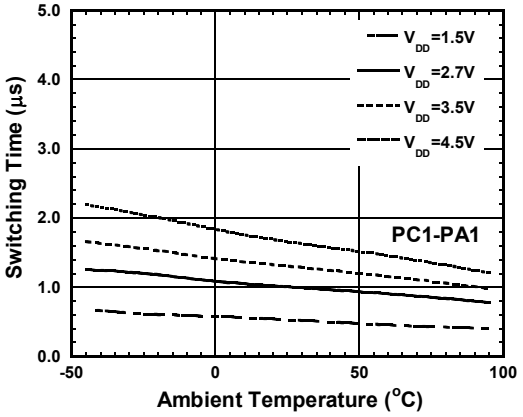
$P_{-0.2dB}$ vs. Ambient Temperature

(PC1-PA1 ON, f=2.0GHz, V_{DD}=2.7V, V_{CTL}=1.8V)



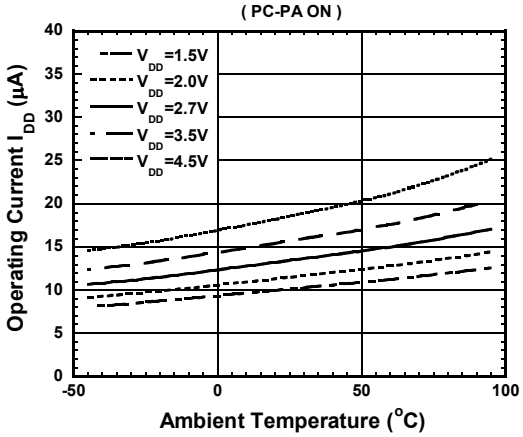
Switching Time vs. Ambient Temperature

(f=2.0GHz, PC-PA ON)

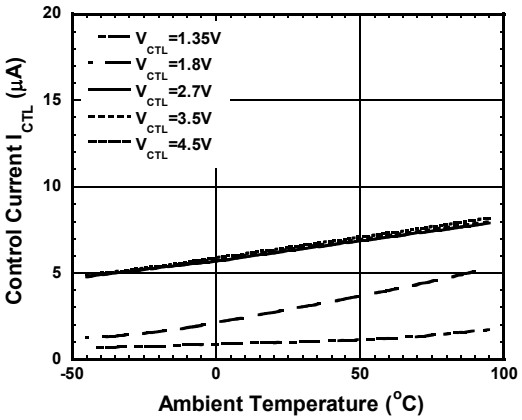


I_{DD} vs. Ambient Temperature

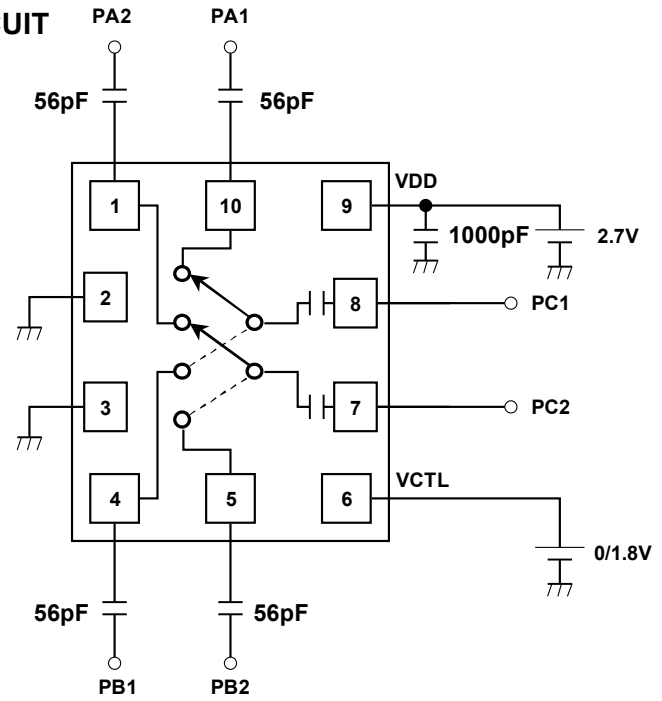
(PC-PA ON)



I_{CTL} vs. Ambient Temperature



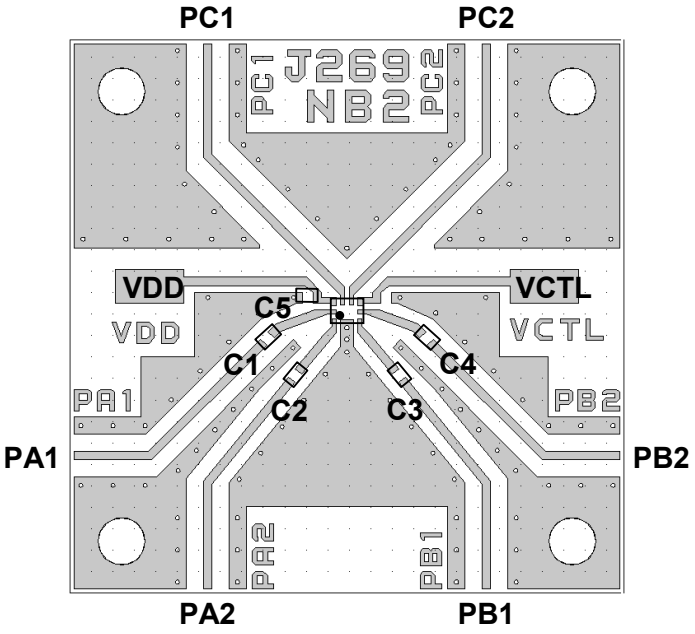
■ APPLICATION CIRCUIT



This IC has on-chip DC blocking capacitors at PC1 and PC2 ports, thereby requiring no external DC blocking capacitor for PC1 and PC2 ports. This is effective to reduce the DC blocking capacitors between the LNA port of the RFIC and corresponding X-SPDT (DP4T) switch.

■ PCB LAYOUT

(TOP VIEW)



PCB: FR-4, t=0.2mm
Capacitor Size: 1005
Strip Line Width: 0.4mm
PCB Size: 26 x 26mm

Losses of PCB, capacitors and connectors

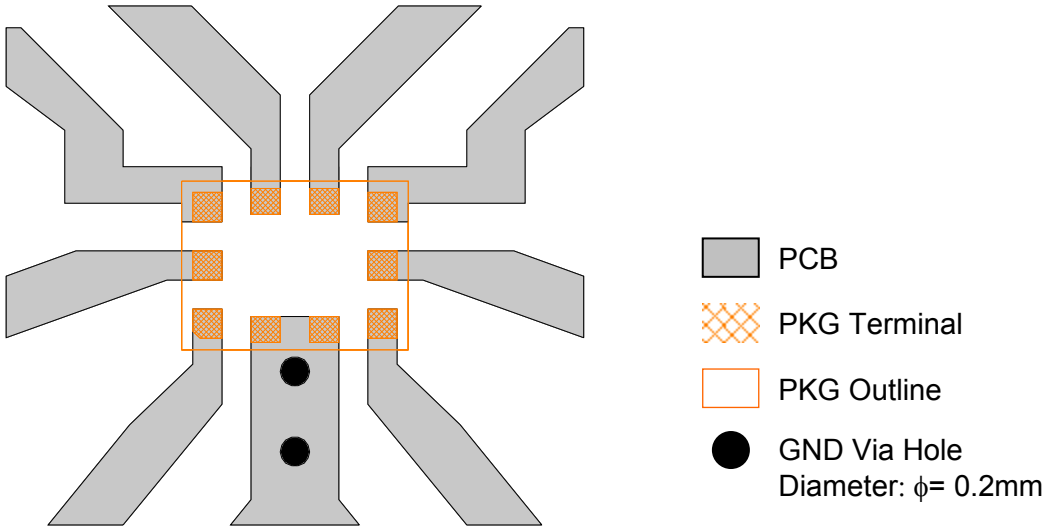
Frequency (GHz)	Loss (dB)
0.5	0.21
1.0	0.34
2.0	0.51
2.7	0.67

■ PARTS LIST

PART ID	Value	COMMENT
C1~C4	56pF	MURATA (GRM15)
C5	1000pF	

■ PCB LAYOUT (EPCSP10-B2)

(TOP VIEW)



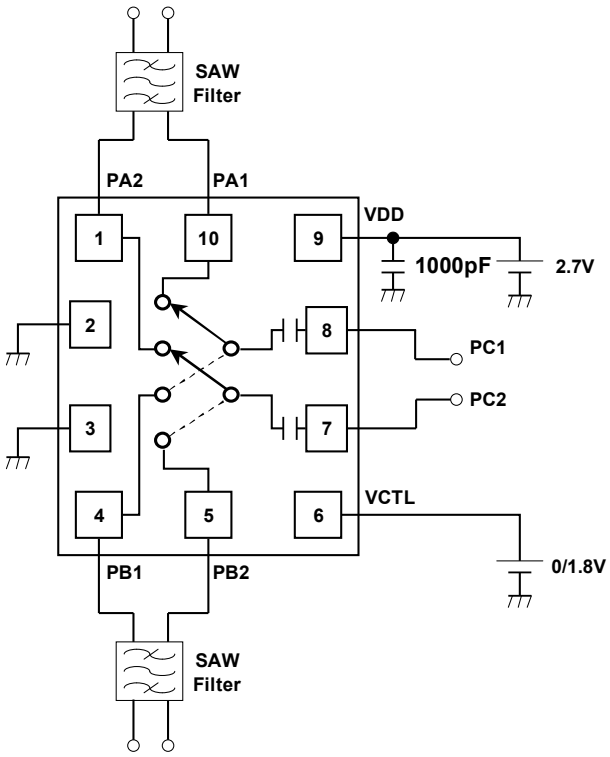
■ PCB LAYOUT PRECAUTIONS

[1] The DC current at PA1, PA2, PB1 and PB2 ports must be equal to zero, which can be achieved with DC blocking capacitors (C1~C4).(However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, e.g. the RF signals are fed by SAW filters that block DC current by nature, etc.)

[2] To reduce stripline influence on RF characteristics, please locate the bypass capacitor (C5) close to VDD terminal.

[3] For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

■ EXAMPLE OF TYPICAL USAGE



As shown in the example of typically used, no DC blocking capacitors are required at PA1, PA2, PB1 and PB2, where these ports are connected to SAW filters whose DC impedance to the ground is above 100Mohm or close to open circuited.

■ RECOMMENDED FOOTPRINT PATTERN (EPCSP10-B2)

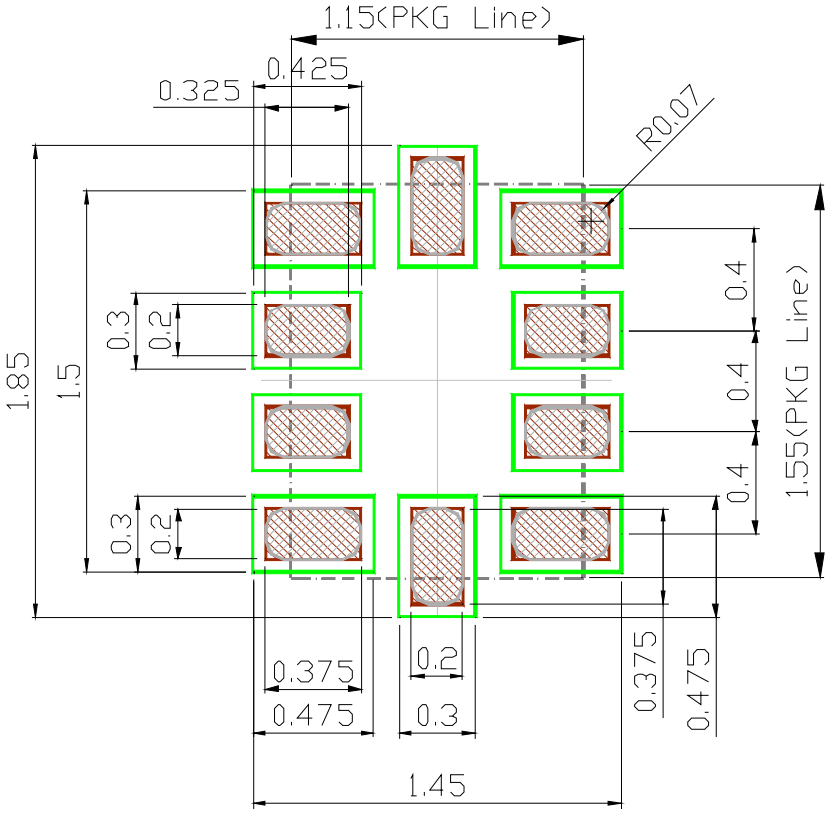
PKG : 1.15mm x 1.55mm

Pin pitch : 0.4mm

: Land

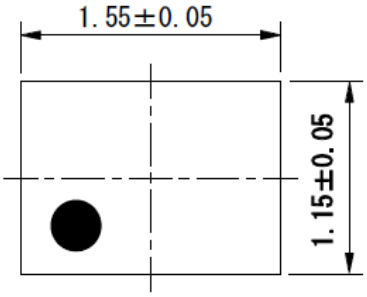
:Mask (Open area) *Metal mask thickness : 100um

:Resist(Open area)

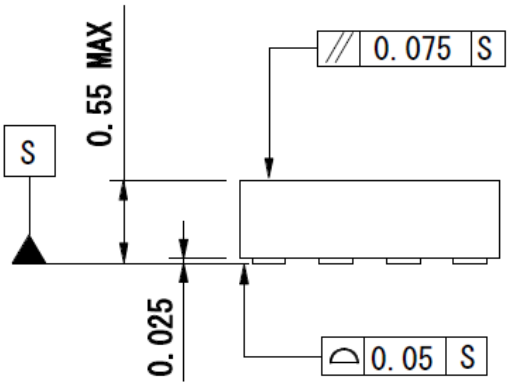


■ PACKAGE OUTLINE (EPCSP10-B2)

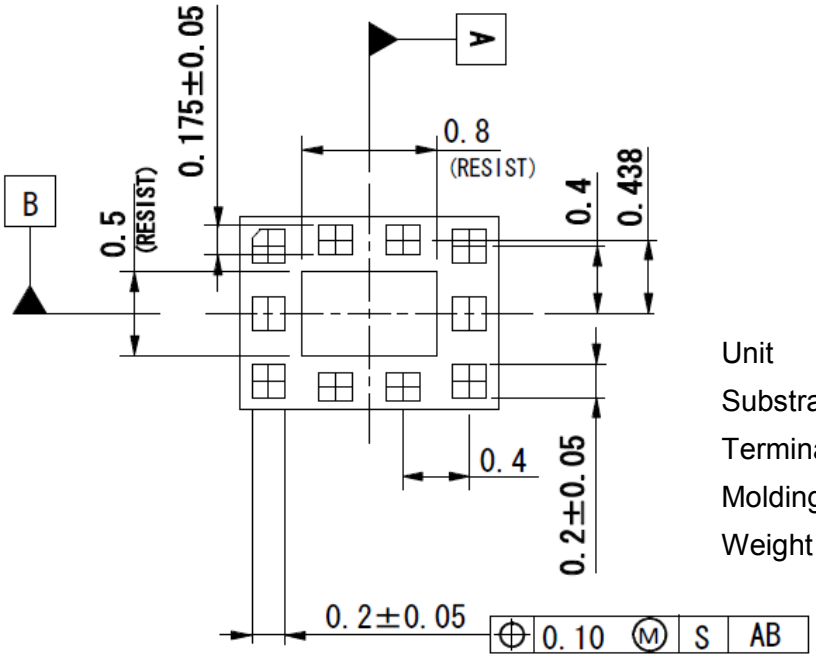
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Unit	: mm
Substrate	: FR-4
Terminal treat	: Au
Molding material	: Epoxy resin
Weight	: 2.0mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.