

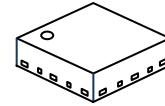
SP3T SWITCH GaAs MMIC

GENERAL DESCRIPTION

The NJG1808K94 is a low power SP3T switch controlled by two bits signals. The low loss performance and high Isolation makes the switch MMIC ideal choice for receiving application.

The NJG1808K94 SP3T switch is provided in a ultra small 9-pin QFN9-94 package with integrated DC blocking capacitor at PC port.

PACKAGE OUTLINE



NJG1808K94

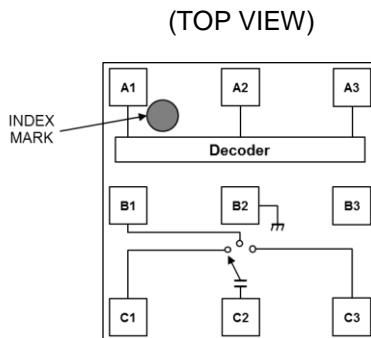
APPLICATIONS

- LTE,3G and 2G Multi-mode applications
- Pre PA switching, reception bands and LTE diversity antenna switching applications
- General purpose switching applications

FEATURES

- Low voltage logic control $V_{CTL(H)}=1.35V$ to 4.5V
- Low insertion loss 0.35dB typ. @f=1.0GHz, $P_{IN}=0dBm$
0.40dB typ. @f=2.0GHz, $P_{IN}=0dBm$
0.40dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- High isolation 29dB typ. @f=1.0GHz, $P_{IN}=0dBm$
26dB typ. @f=2.0GHz, $P_{IN}=0dBm$
24dB typ. @f=2.7GHz, $P_{IN}=0dBm$
- $P_{-0.2dB}$ 22dBm typ. @f=2.0GHz
- Ultra small & thin package QFN9-94 (Package size: 1.1 x 1.1 x 0.425mm typ.)
- RoHS compliant and Halogen Free, MSL1

PIN CONFIGURATION



- Pin connection
- A1. VCTL1
 - A2. VCTL2
 - A3. VDD
 - B1. P3
 - B2. NC(GND)
 - B3. GND
 - C1. P1
 - C2. PC
 - C3. P2

TRUTH TABLE

“H”= $V_{CTL(H)}$, “L”= $V_{CTL(L)}$

VCTL1	VCTL2	PATH
H	L	PC-P1
L	H	PC-P2
H	H	PC-P3

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	$V_{DD}=2.7\text{V}$	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1,VCTL2	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB (114.3x76.2mm, without through-hole) $T_j=150^{\circ}\text{C}$	310	mW
Operating Temperature	T_{opr}		-40 to +105	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

(General conditions: $T_a=+25^{\circ}\text{C}$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD terminal	1.5	2.7	4.5	V
Operating Current	I_{DD}		-	30	60	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1,VCTL2	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1,VCTL2	1.35	1.8	4.5	V
Control Current	I_{CTL}	$V_{CTL(H)}=1.8\text{V}$	-	5	10	μA

■ ELECTRICAL CHARACTERISTICS2 (RF CHARACTERISTICS)

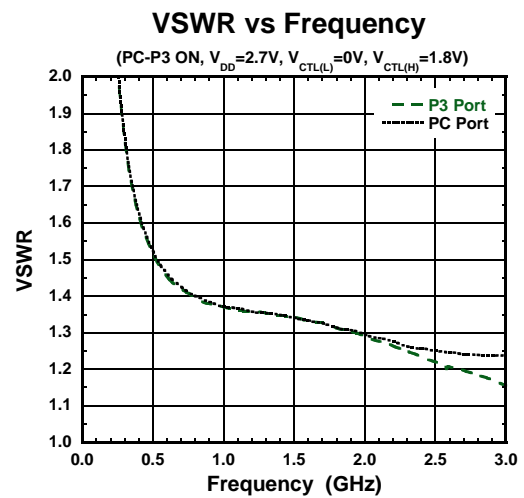
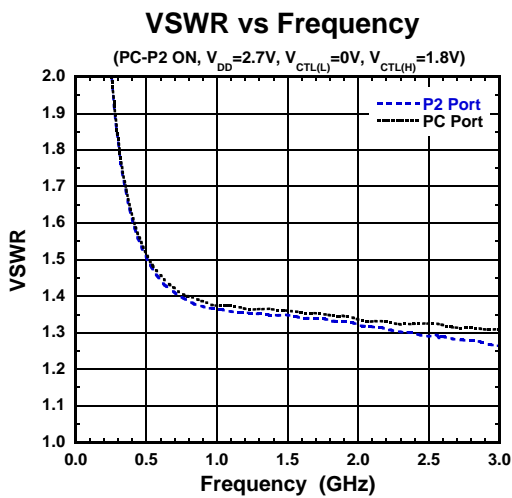
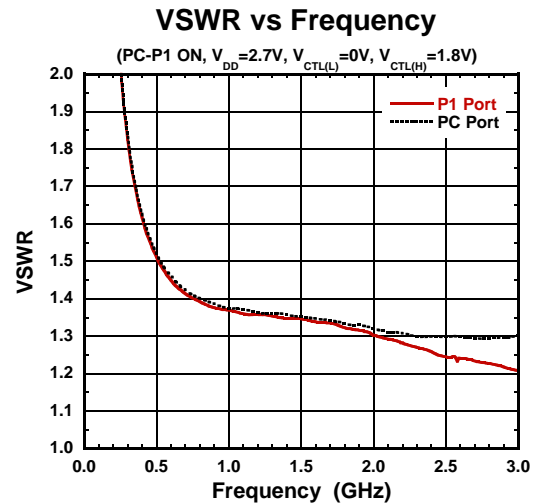
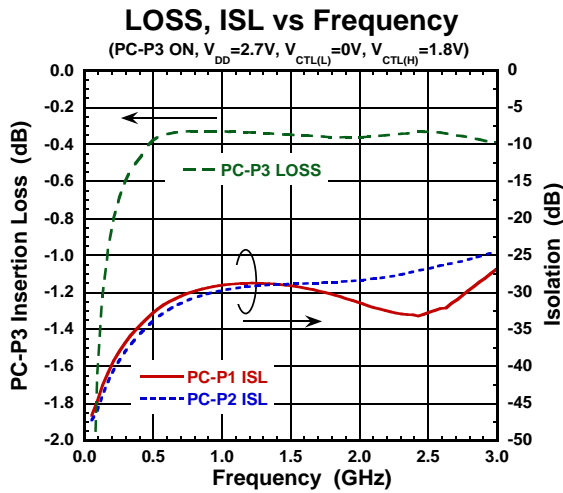
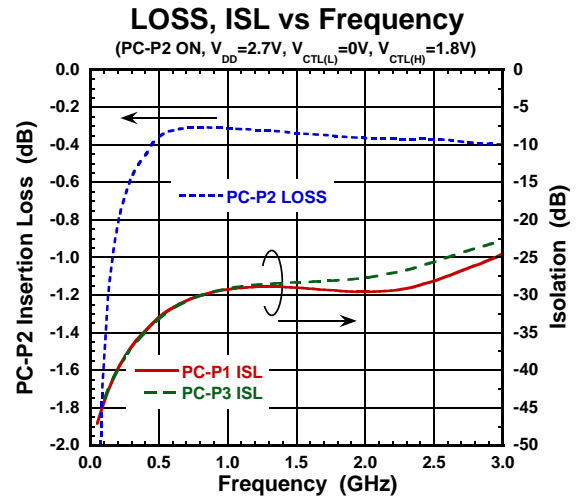
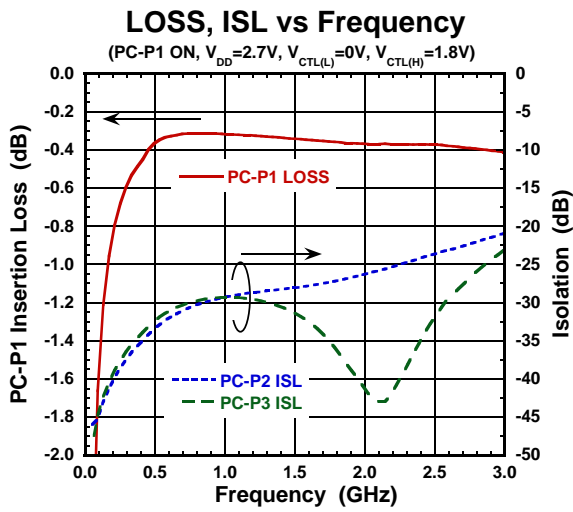
(General conditions: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$, $V_{DD}=2.7\text{V}$, $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=1.8\text{V}$, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	$f=0.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.35	0.55	dB
Insertion Loss 2	LOSS2	$f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.35	0.55	dB
Insertion Loss 3	LOSS3	$f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.40	0.60	dB
Insertion Loss 4	LOSS4	$f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	-	0.40	0.60	dB
Isolation 1	ISL1	PC-P1, P2, P3 $f=0.7\text{GHz}$, $P_{IN}=0\text{dBm}$	27	30	-	dB
Isolation 2	ISL2	PC-P1, P2, P3 $f=1.0\text{GHz}$, $P_{IN}=0\text{dBm}$	26	29	-	dB
Isolation 3	ISL3	PC-P1, P2, P3 $f=2.0\text{GHz}$, $P_{IN}=0\text{dBm}$	23	26	-	dB
Isolation 4	ISL4	PC-P1, P2, P3 $f=2.7\text{GHz}$, $P_{IN}=0\text{dBm}$	21	24	-	dB
Input power at 0.2dB Compression Point	$P_{-0.2\text{dB}}$	$f=2.0\text{GHz}$	18	22	-	dBm
VSWR	VSWR	$f=2.0\text{GHz}$, On port	-	1.3	1.5	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	2	5	μs

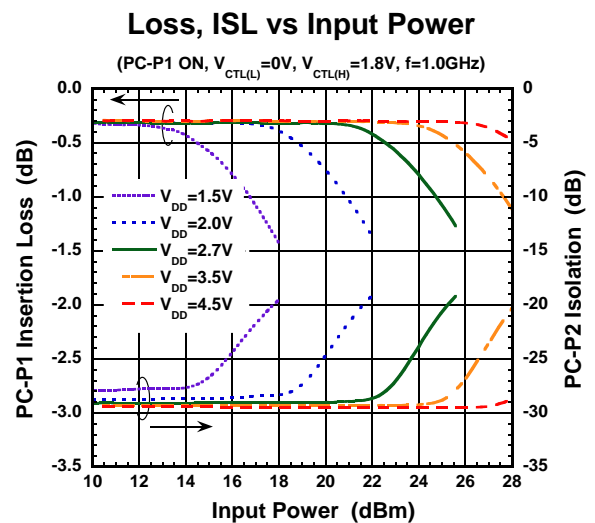
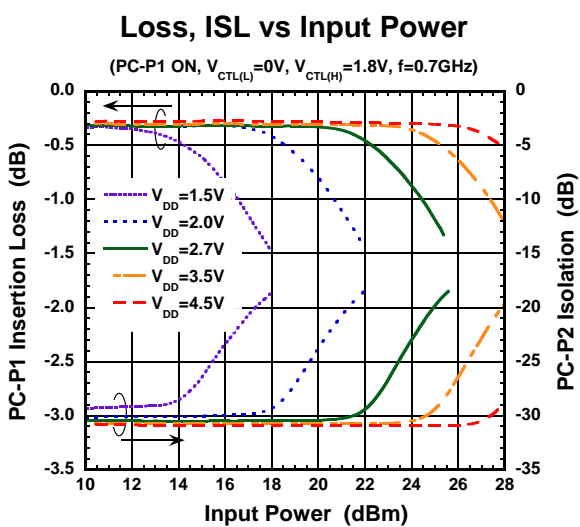
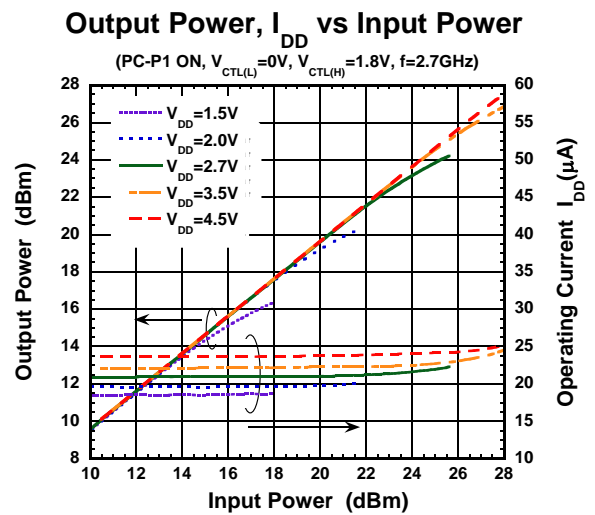
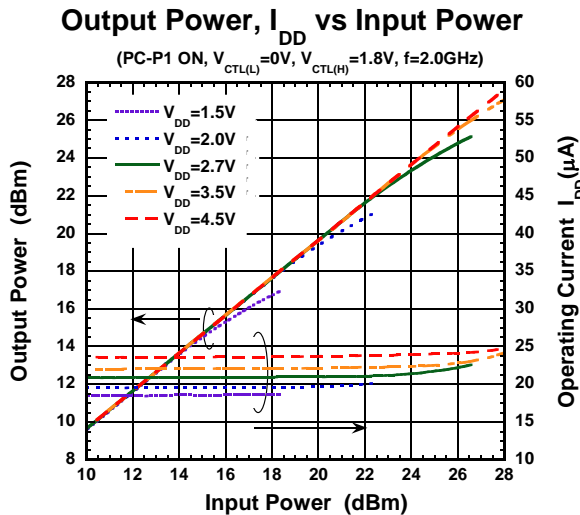
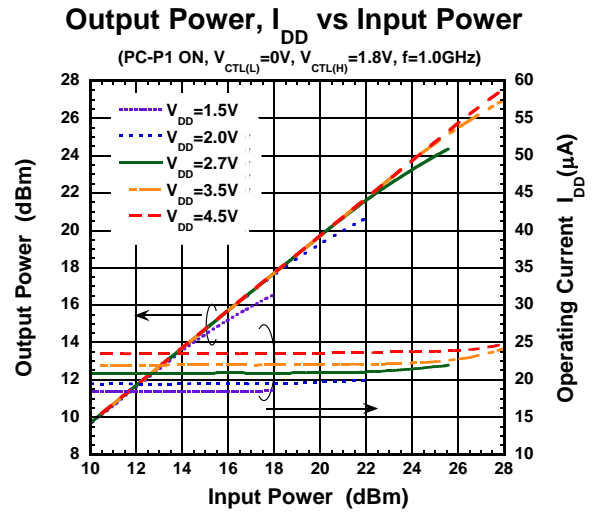
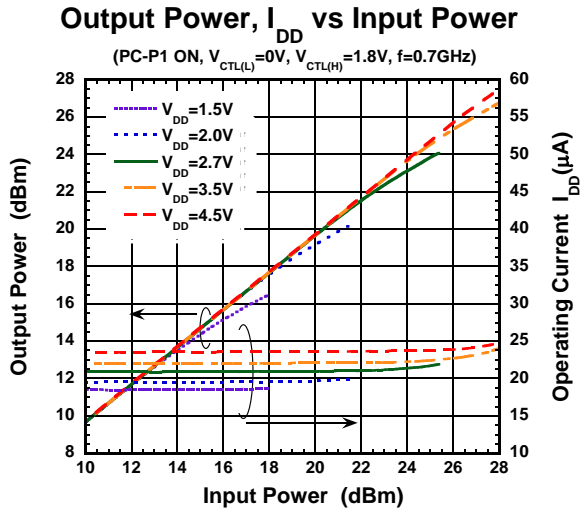
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
A1	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35 to +4.5V) or Low-Level (0 to +0.45V).
A2	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35 to +4.5V) or Low-Level (0 to +0.45V).
A3	VDD	Positive voltage supply terminal. The positive voltage (+1.5 to +4.5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
B1	P3	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
B2	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.
B3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
C1	P1	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.
C2	PC	RF input/output port. No DC blocking capacitor is required for this port because of internal capacitor.
C3	P2	RF input / output port. External capacitor is required to block the DC bias voltage of internal circuit.

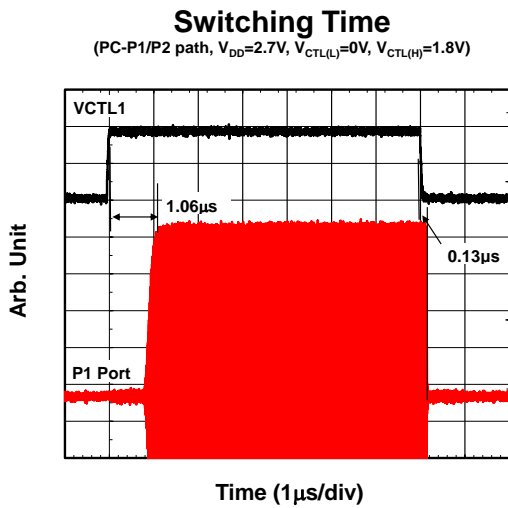
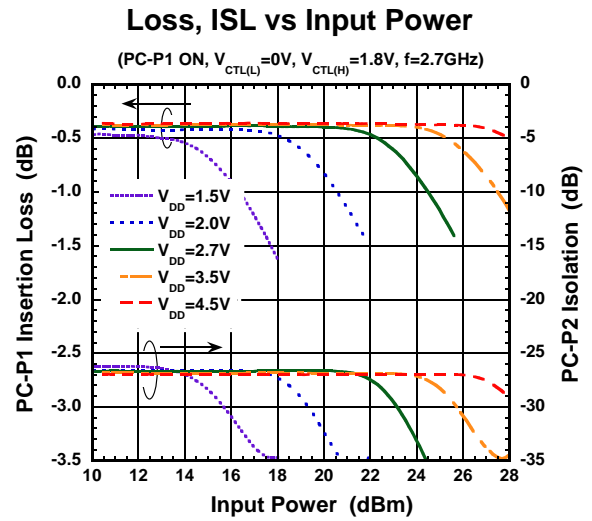
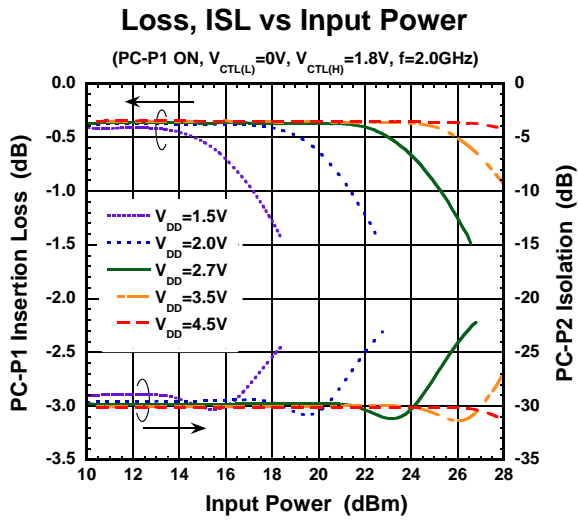
■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



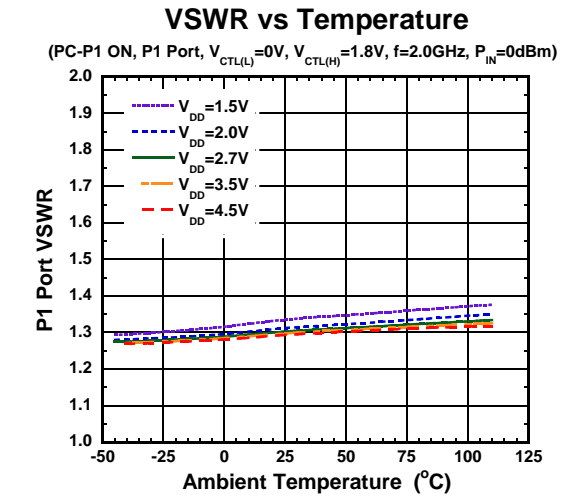
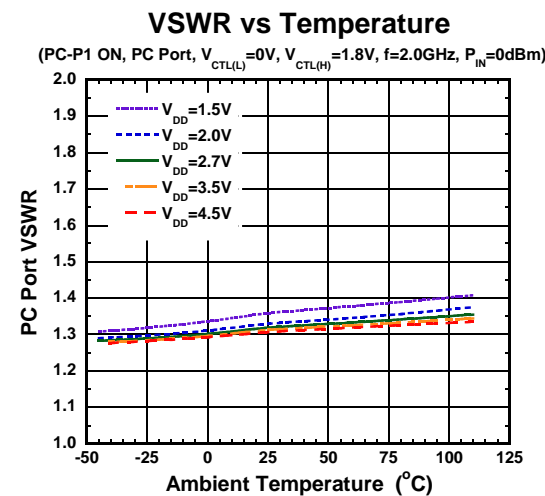
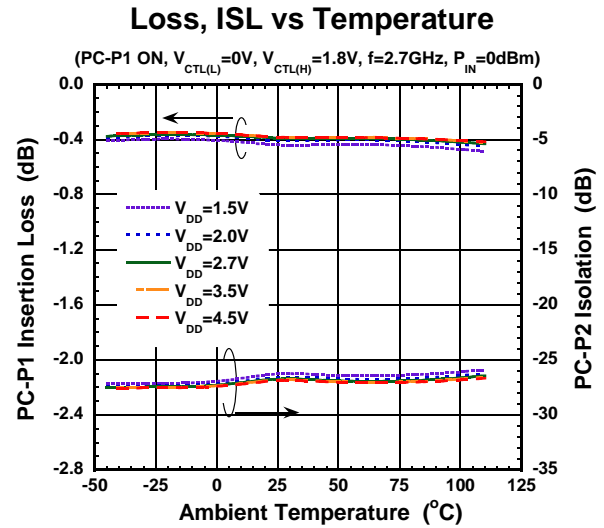
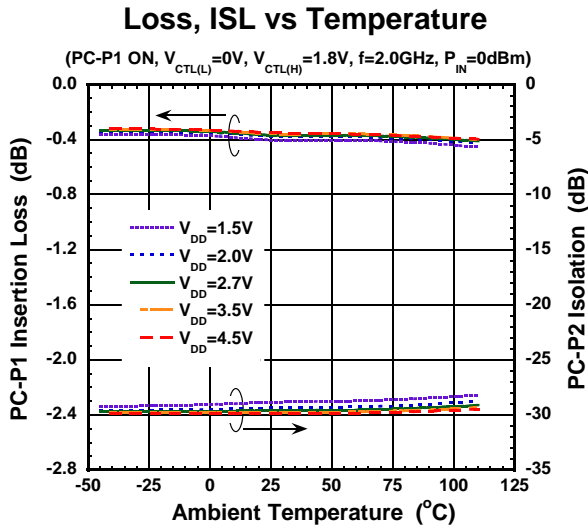
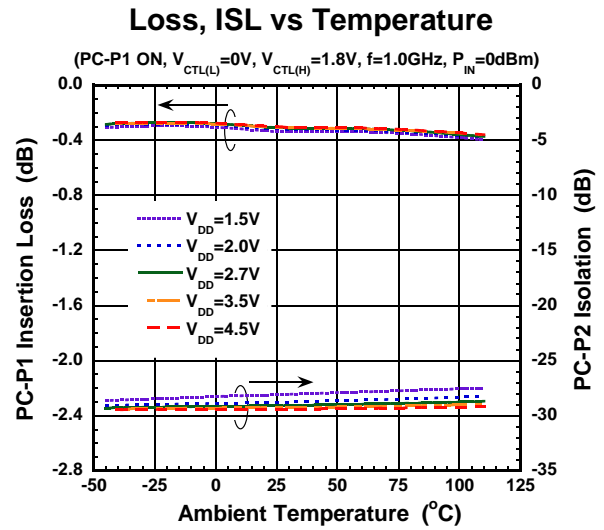
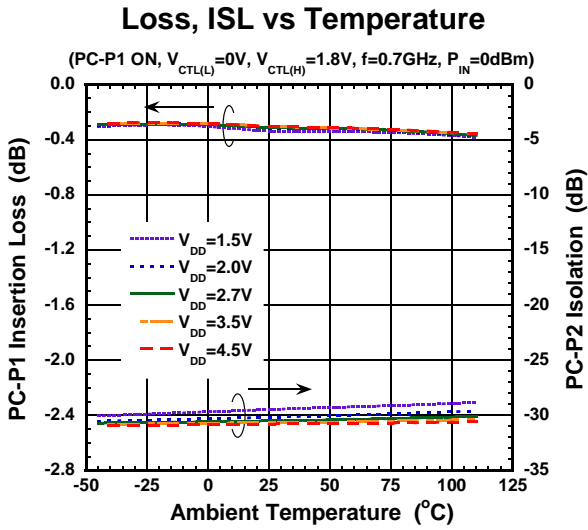
■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



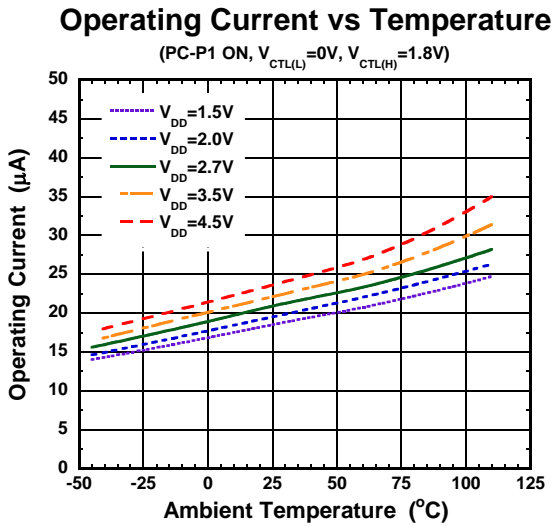
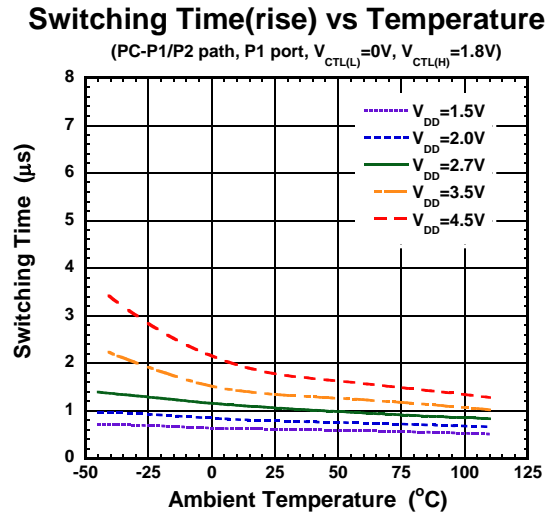
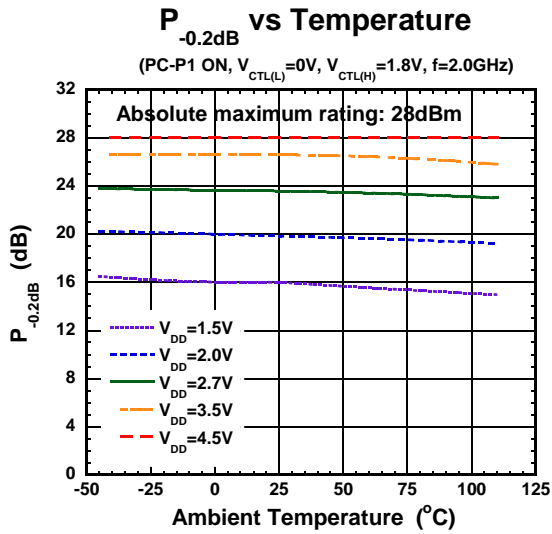
■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



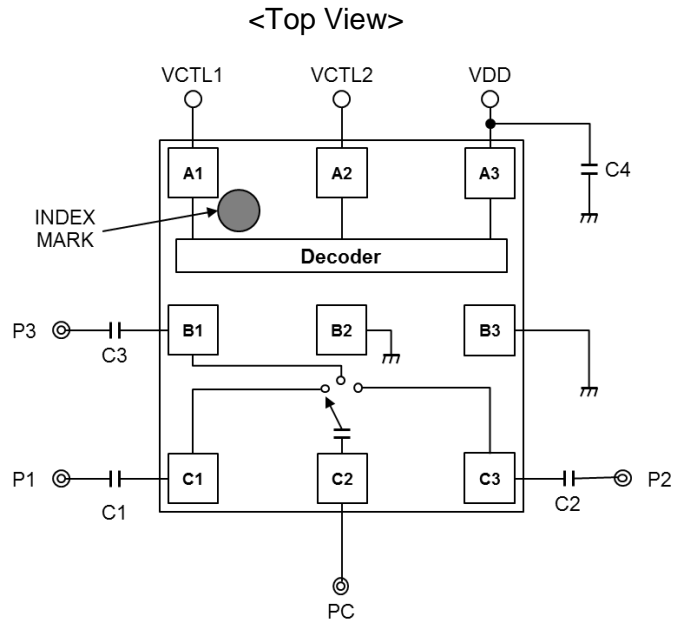
■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



■ ELECTRICAL CHARACTERISTICS (With Application circuit, Loss of external circuit are excluded)



APPLICATION CIRCUIT



NOTE:

[1] The DC blocking capacitor is not necessary at PC Port because of the integrated DC blocking capacitor.

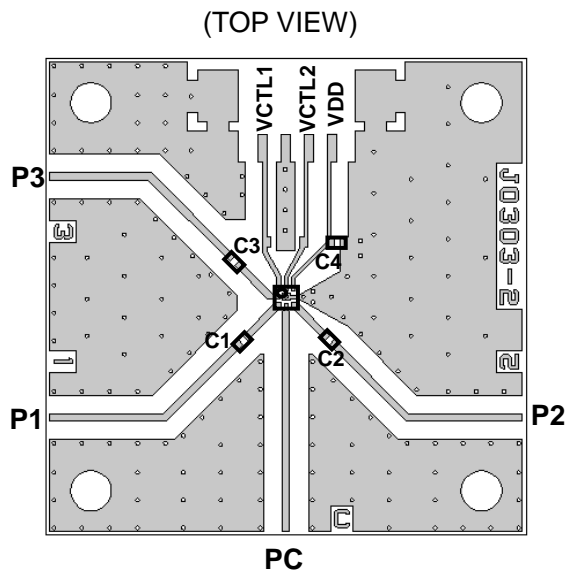
[2] The DC current at RF ports must be equal to zero, which can be achieved with DC blocking capacitors (C1, C2, and C3).

*However, in case there is no possibility that DC current flows, the DC blocking capacitors are unnecessary, i.e. the RF signals are fed by SAW filters that block DC current by nature, etc.

PARTS LIST

Part ID	Value	Notes
C1 to C3	56pF	MURATA (GRM15)
C4	1000pF	MURATA (GRM15)

RECOMMENDED PCB DESIGN

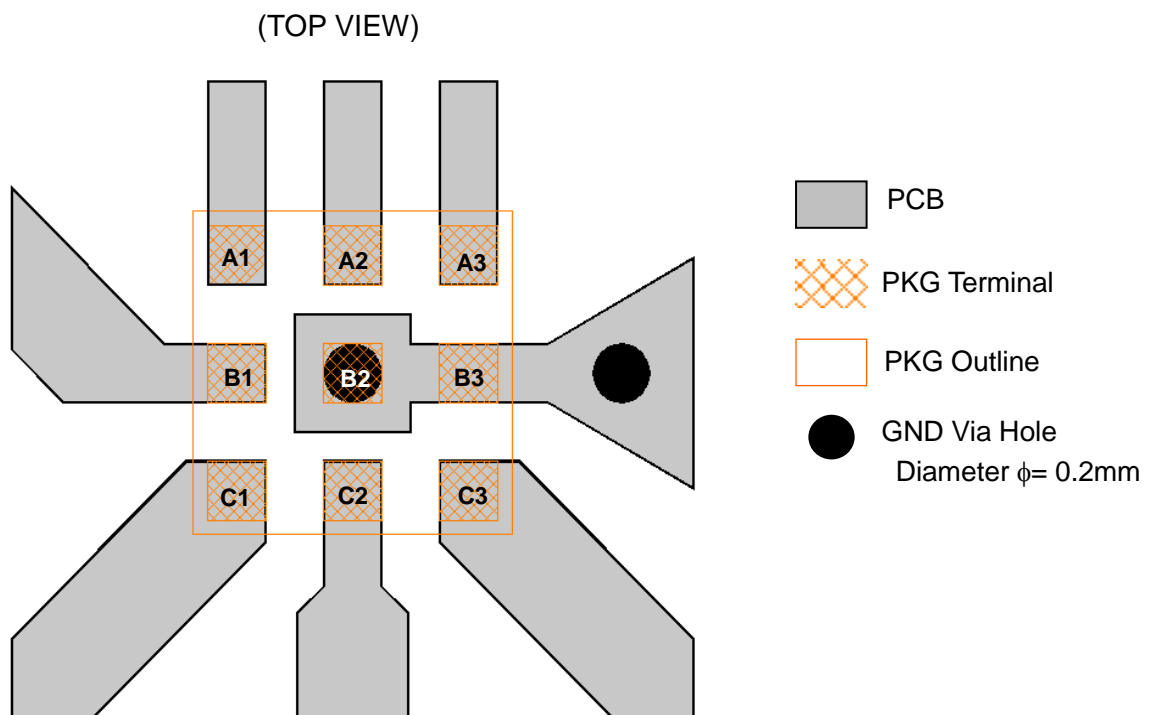


PCB: FR-4, t=0.2mm
 Capacitor Size: 1005(1.0x0.5mm)
 Strip Line Width: 0.38mm
 PCB Size: 25.8mmx25.8mm
 Through Hole Diameter: 0.2mm

Loss of PCB capacitors and connectors

Frequency(GHz)	Loss(dB)
0.7	0.24
1.0	0.29
2.0	0.45
2.7	0.59

PCB LAYOUT GUIDELINA (QFN9-94)






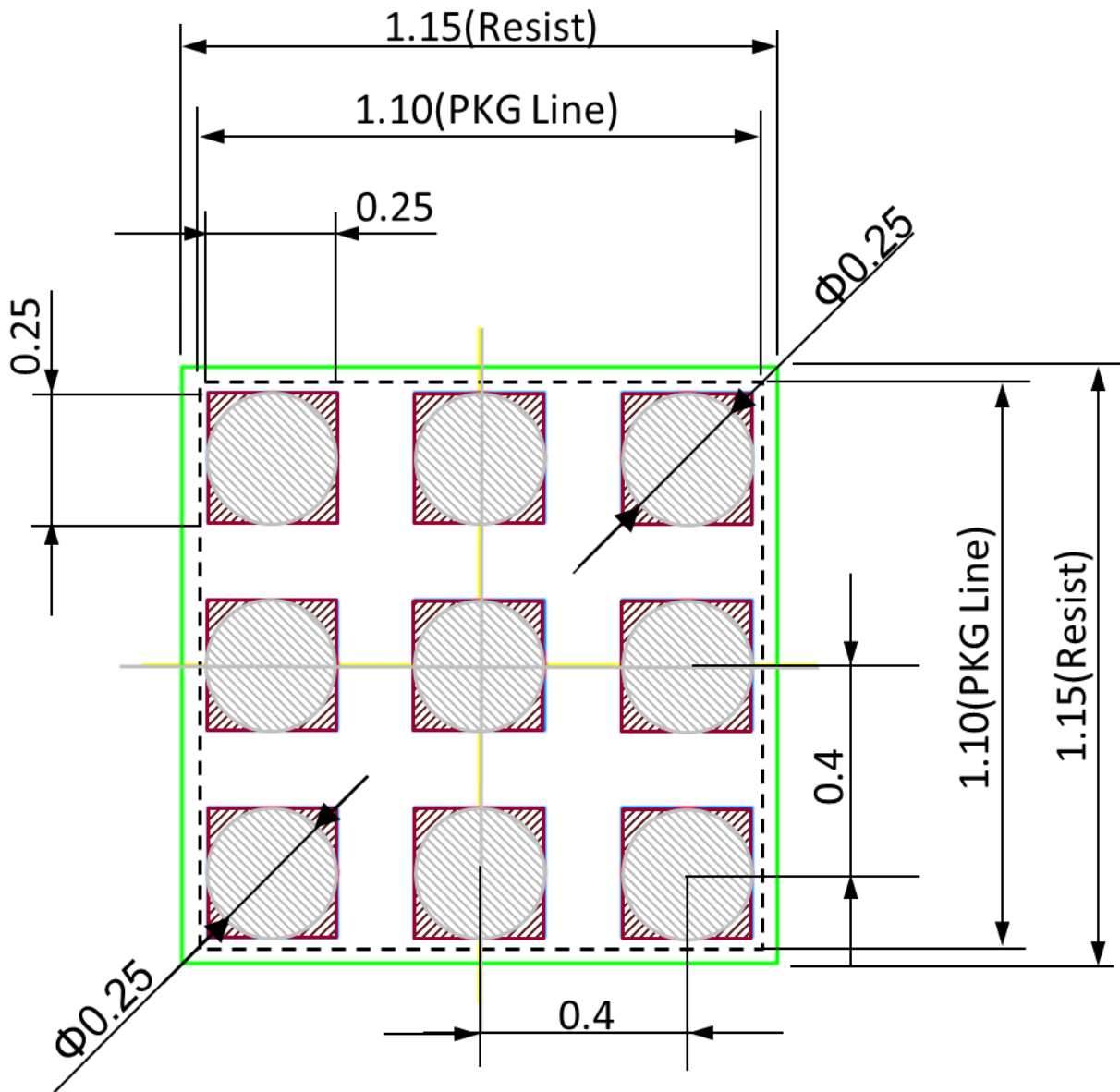
PRECAUTIONS

For good isolation, the GND terminals must be connected to the PCB ground plane of substrate, and the through-holes connecting the backside ground plane should be placed near by the pin connection.

RECOMMENDED FOOTPRINT PATTERN (QFN9-94 Package 1.1x1.1mm) <Reference>

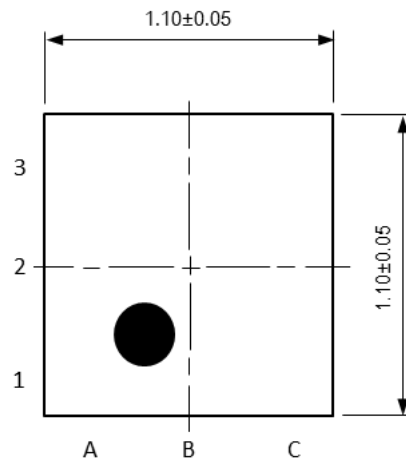
Package: 1.1mm x 1.1mm
 Pin pitch: 0.40mm

-  : Land
-  : Mask (Open area) *Metal mask thickness: 100μm
-  : Resist (Open area)

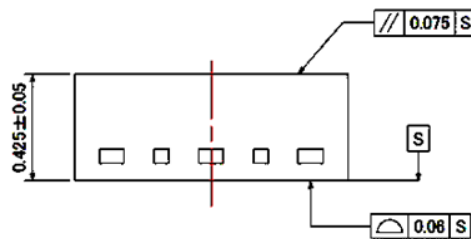


PACKAGE OUTLINE (QFN9-94)

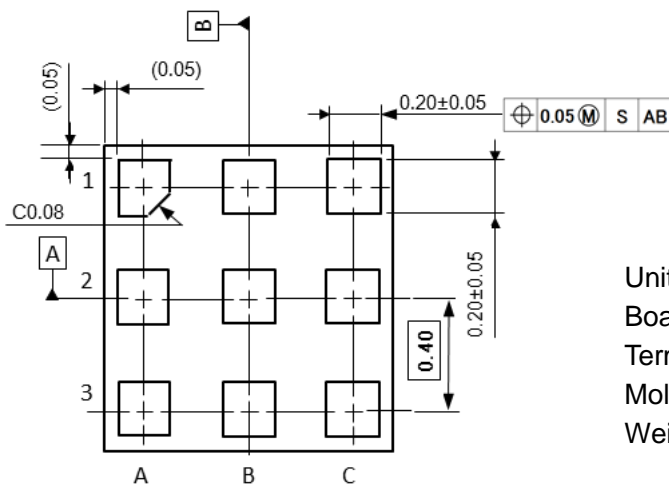
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Unit	: mm
Board	: Copper
Terminal Treat	: Ni/Pd/Au
Molding Material	: Epoxy resin
Weight	: 1.5mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.