47µF AC-Coupling Capacitor Low Voltage Video Driver with LPF

■FEATURES

- ●Operating Voltage 3.0 to 6.0V
- ●Small output coupling capacitor 47µF
- ●6dB Amplifier, 75ohm Driver
- ●Internal LPF 0dBtyp.at 4.5MHz
  -33dBtyp.at 19MHz
- ●Power-save Circuit
- ●Bipolar Technology
- ●Package Outline MSOP8(TVSP8)*

*MEET JEDEC MO-187-DA / THIN TYPE

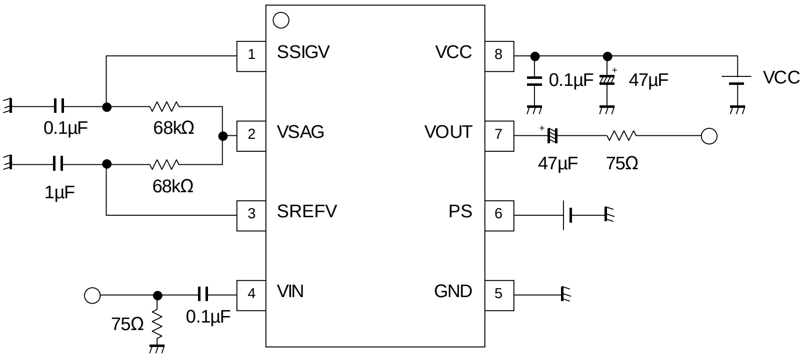
■GENERAL DESCRIPTION

NJM2512 is a Low Voltage Video Amplifier featuring small AC-coupling Capacitor.
The NJRC original Technology "ASC(Advanced SAG Correction)" realizes 47µF AC-Coupling Capacitor which enables to downsize mounting space.
No worrying about beat noise caused by charge-pump circuit, and over-current caused by circuit short out than Capacitor-less video driver.
NJM2512 is suitable for any video application.

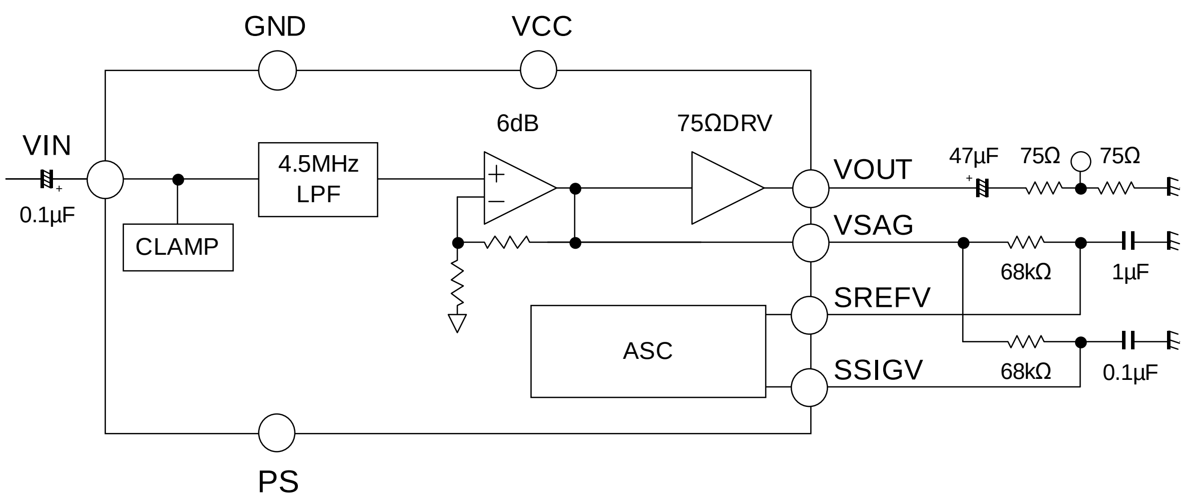
■APPLICATION

- ●Car Camera
- ●Car Navigation

■APPLICATION CIRCUIT



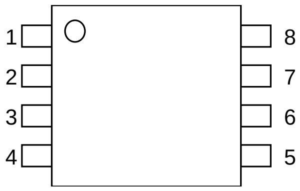
■EQUIVALENT CIRCUIT･BLOCK DIAGRAM



■Voltage Gain Valuation

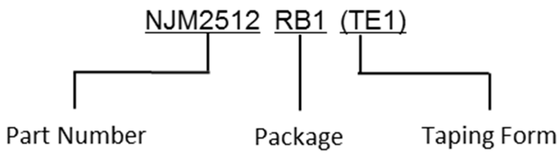
Voltage Gain	Part No.
12dB	NJM2512A

■PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	SSIGV	Sag correction Terminal
2	VSAG	Sag correction Terminal
3	SREFV	Sag correction Terminal
4	VIN	Video Signal Input Terminal
5	GND	GND Terminal
6	PS	Power Save Terminal
7	VOUT	Video Signal Output Terminal
8	VCC	Power Supply Terminal

■MARK INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJM2512RB1	MSOP8	Yes	-(*)	Sn-2Bi	2512	18	2,000

(*): "-" is unevaluated. Please contact your sales representative for more information.

■ABSOLUTE MAXIMUM RATINGS

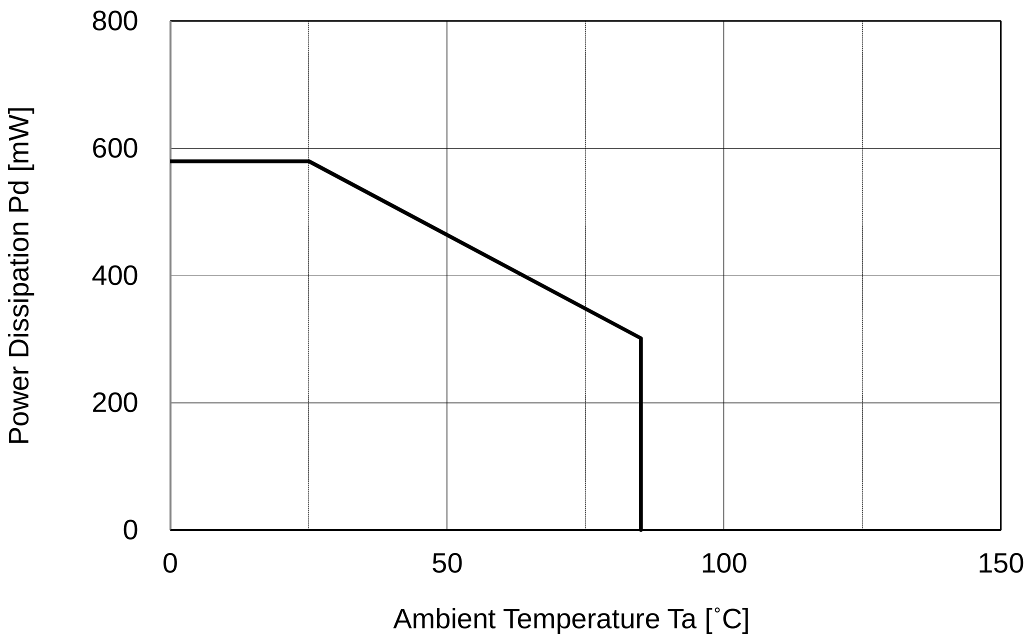
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VCC	7.0	V
Power Dissipation (Ta=25°C)(4)	P_D	580(1)	mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm Two layers, FR-4)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage	Vopr	3.0 to 6.0	V

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



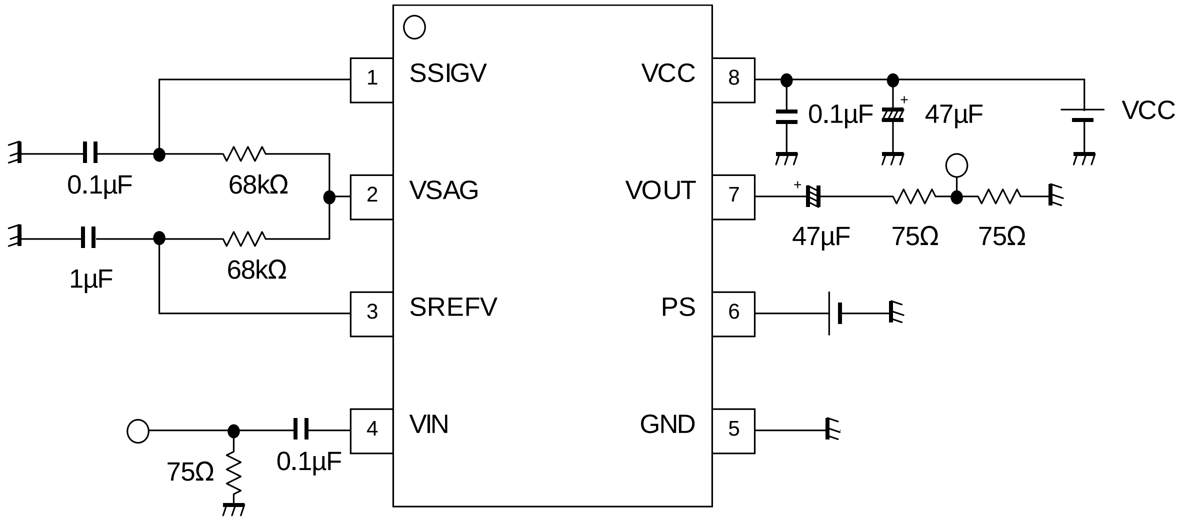
■ELECTRICAL CHARACTERISTICS (Ta=25°C, V^+=3.3V, RL=150Ω, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	Icc	No input signal	-	10	15	mA
Supply Current at Power Save Mode	Isave	Power save mode	-	20	50	µA
Maximum Output Level	Vom	Vin=100kHz,sin-signal, THD=1%,	2.2	-	-	Vp-p
Voltage Gain	Gv	Vin=100kHz, 1.0Vp-p sin- wave	5.5	6.0	6.5	dB
LPF Characteristics	Gf4.5M	Vin=4.5MHz/1MHz, 1.0Vpp sin-signal	-0.6	-0.1	+0.4	dB
	Gf19 M	Vin=19MHz/1MHz, 1.0Vpp sin-signal	-	-33.0	-23.0	
Differential Gain	DG	Vin=1.0Vp-p 10step video signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step video signal	-	0.5	-	deg
S/N Ratio	SN	100kHz to 6MHz, Vin=1.0Vp-p 100% White Video Signal, R_L=75Ω	-	60	-	dB
SW Voltage High Level	VthH	IC: Active mode	1.8	-	V^+	V
SW Voltage Low Level	VthL	IC: Non-Active mode	0	-	0.3	V
SW Sink Current High Level	IthH	V=3V	-	-	300	µA
SW Sink Current Low Level	IthL	V=0.3V	-	-	5	µA

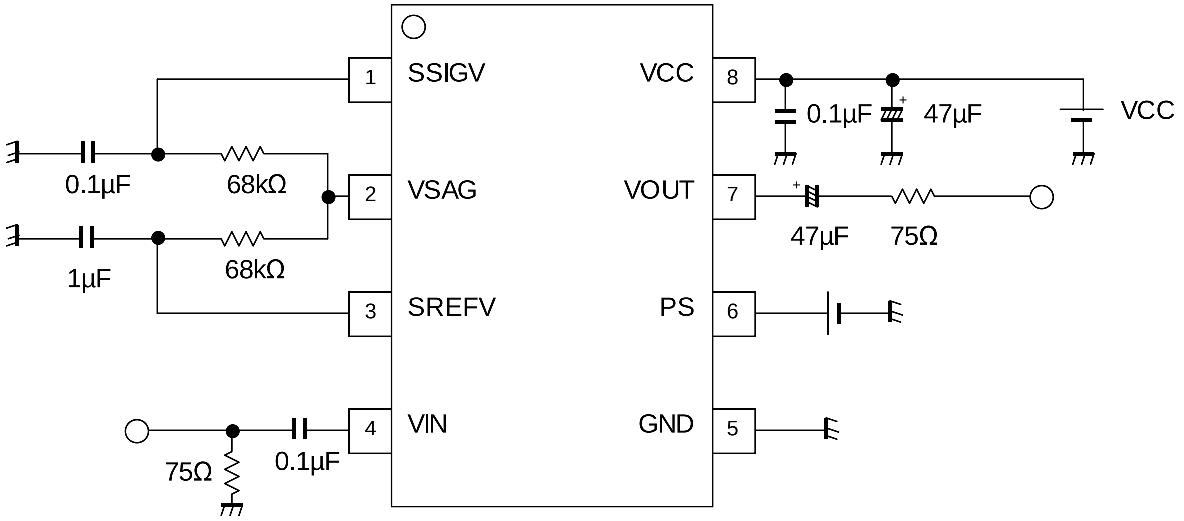
■CONTROL TERMINAL

PARAMETER	STATUS	MODE
PS	H	Power save: OFF Active mode
	L	Power save: ON Non-Active mode(Mute)
	OPEN	Power save: ON Non-Active mode(Mute)

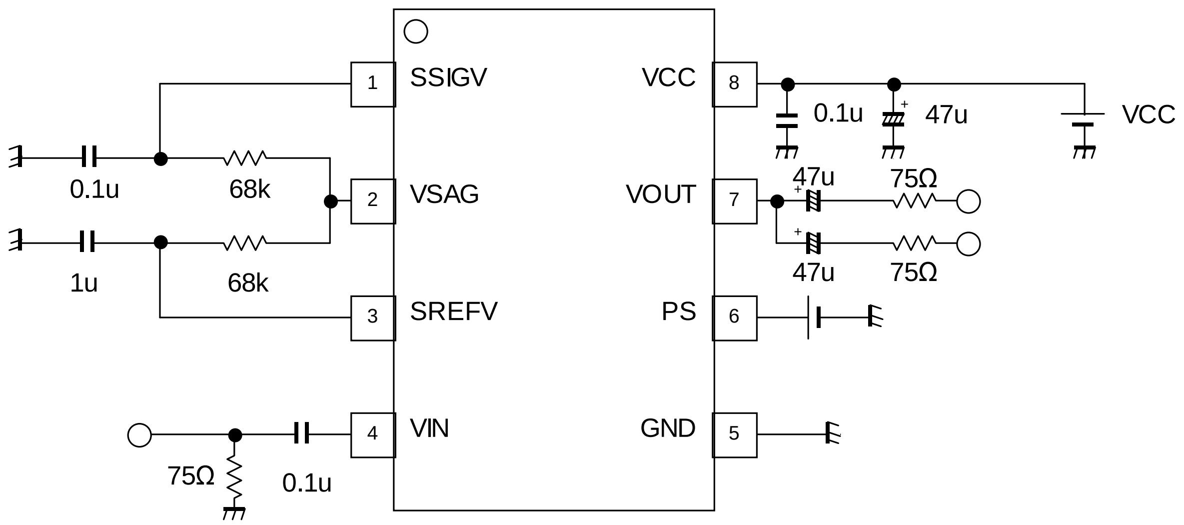
■TEST CIRCUIT 1



■APPLICATION CIRCUIT 1

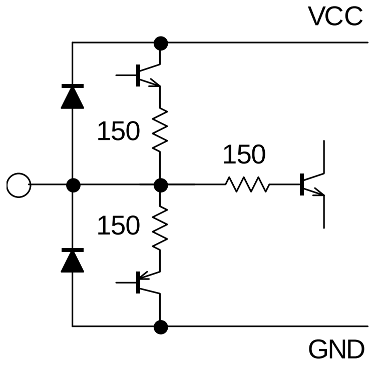
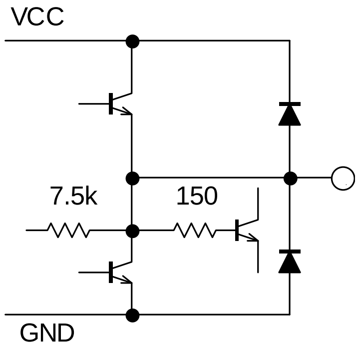
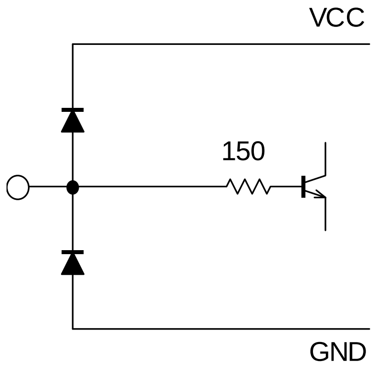
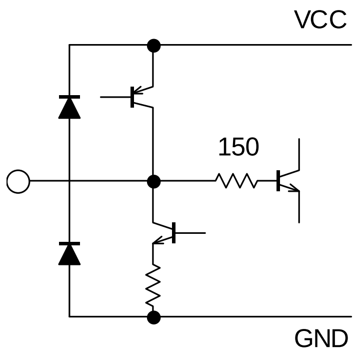


■APPLICATION CIRCUIT 2 (Two-system drive)

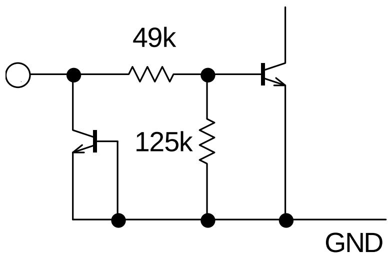
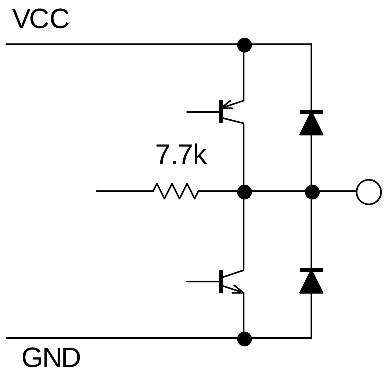


Note) NJM2512 has possibilities that decrease in the capacitance in low-frequency band when the ceramic capacitor is used (pin7). It is a possibility that the sag is generated when the ceramic capacitor decreases capacity.
Please verify it in consideration of the capacity drop of the ceramic capacitor.

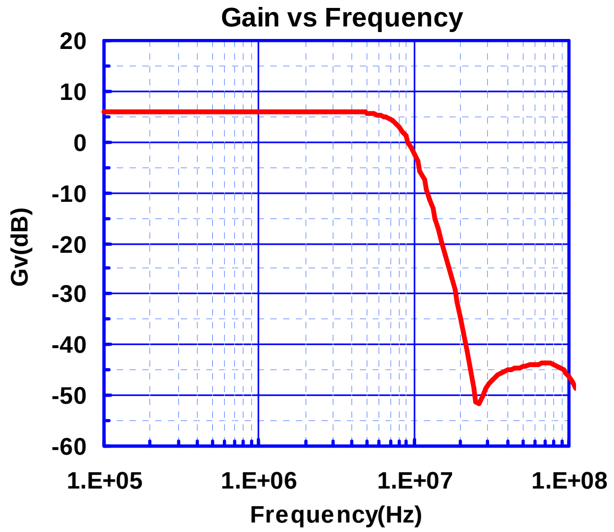
■TERMINAL FUNCTION

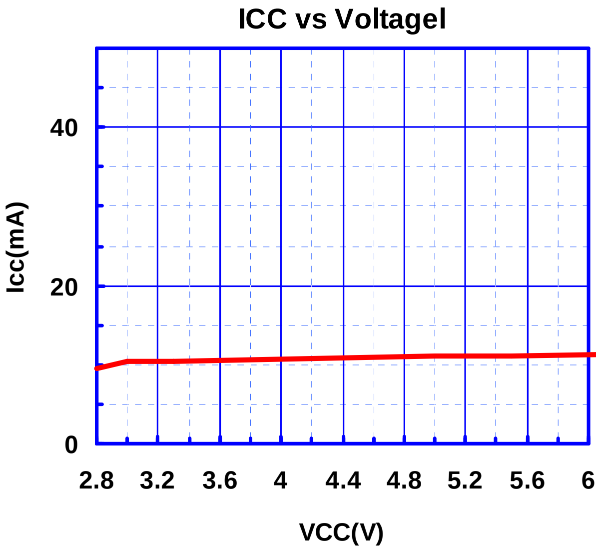
PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1	SSIVG	Sag correction		1.4V
2	VSAG	Sag correction		1.4V
3	SREFV	Sag correction		1.4V
4	VIN	Video signal input		1.4V

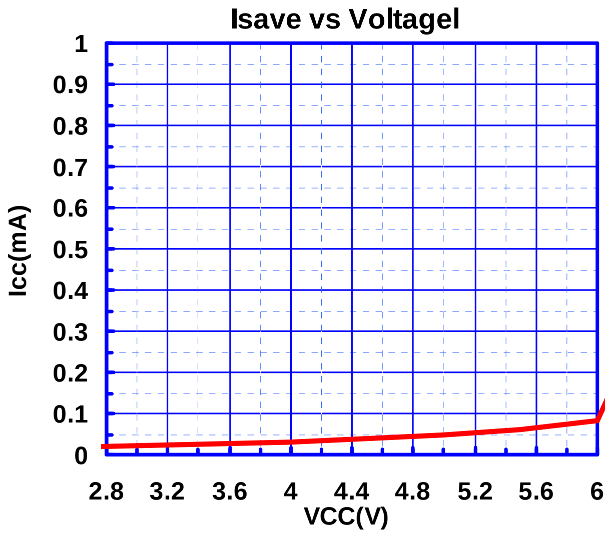
■TERMINAL FUNCTION

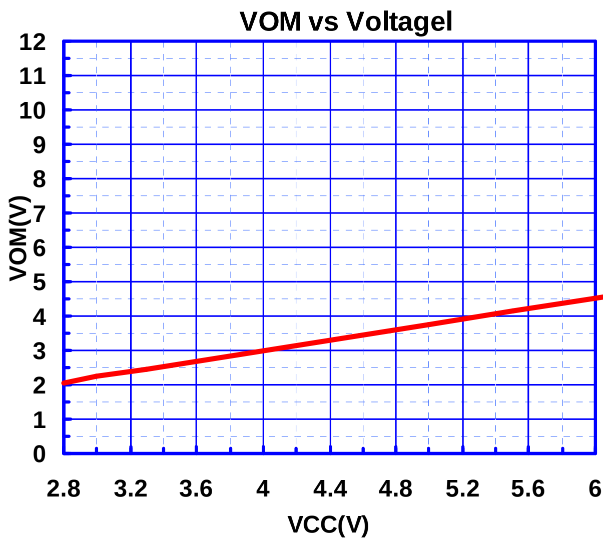
PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
5	GND	GND	-	-
6	PS	Power save control		-
7	VOUT	Video signal output		0.7V
8	VCC	Power supply	-	-

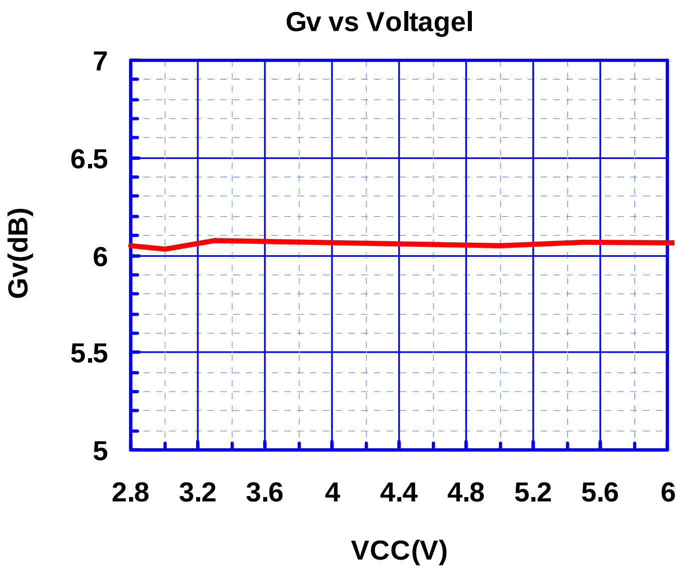
■TYPICAL CHARACTERISTICS



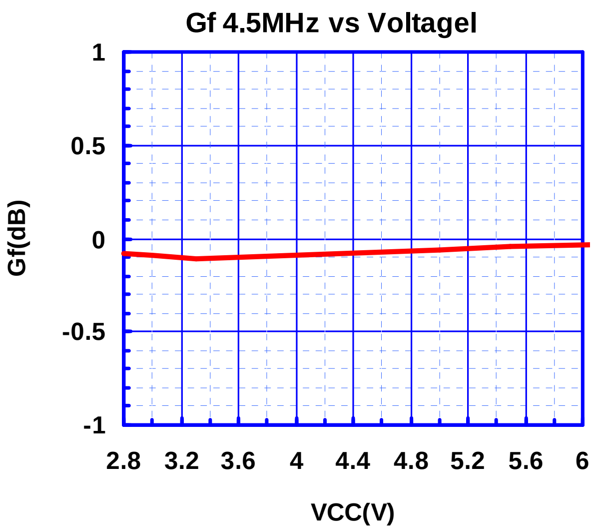


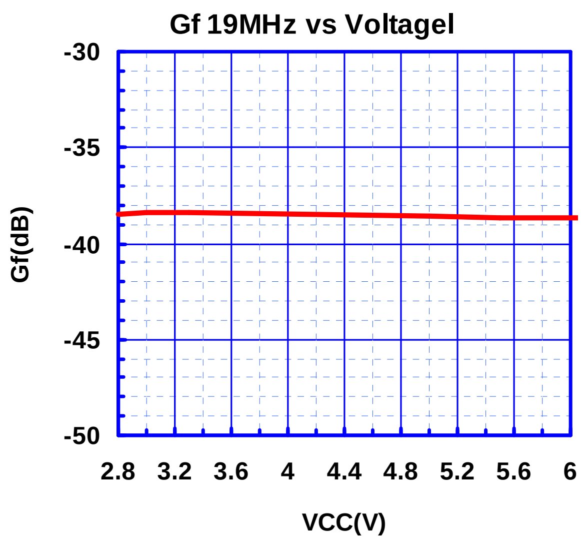


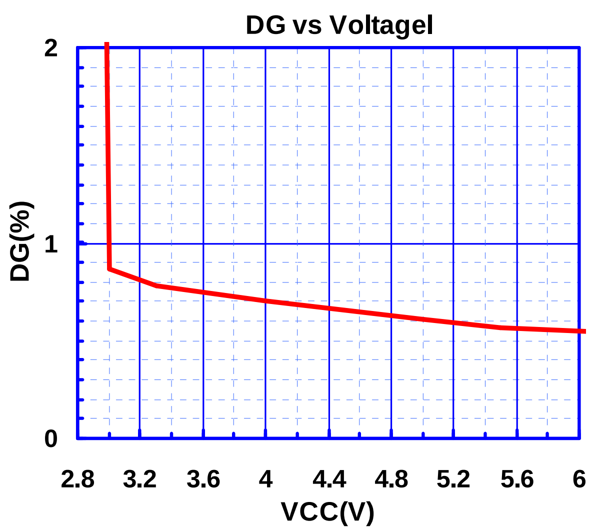


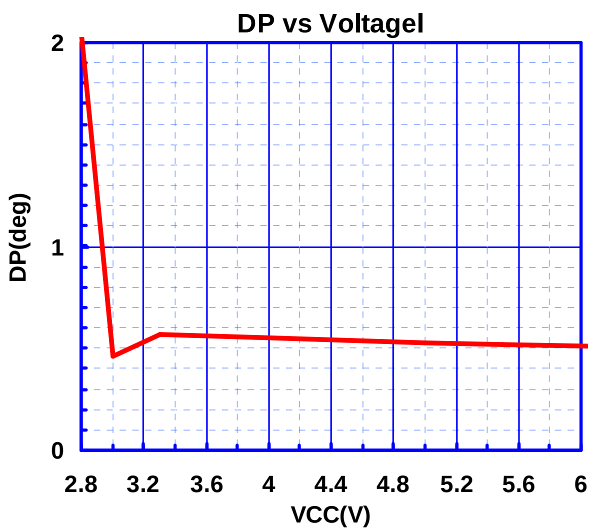


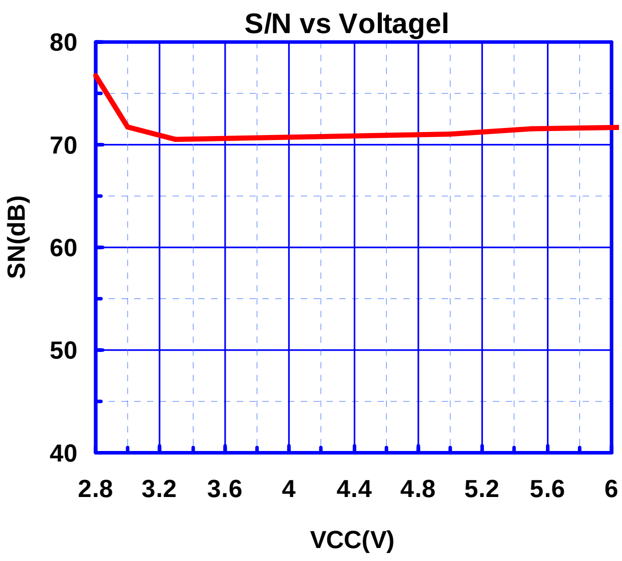
■TYPICAL CHARACTERISTICS



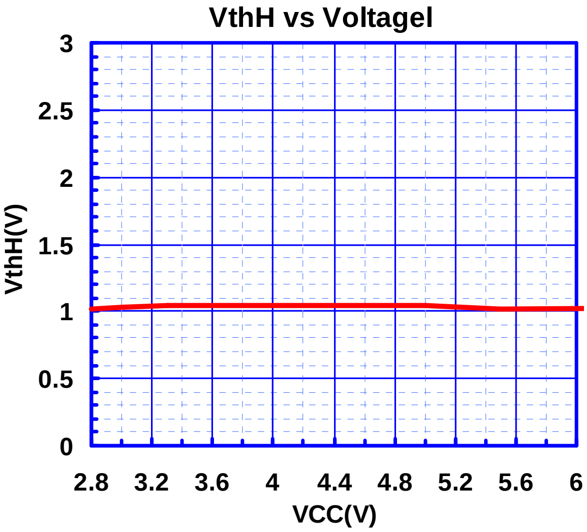


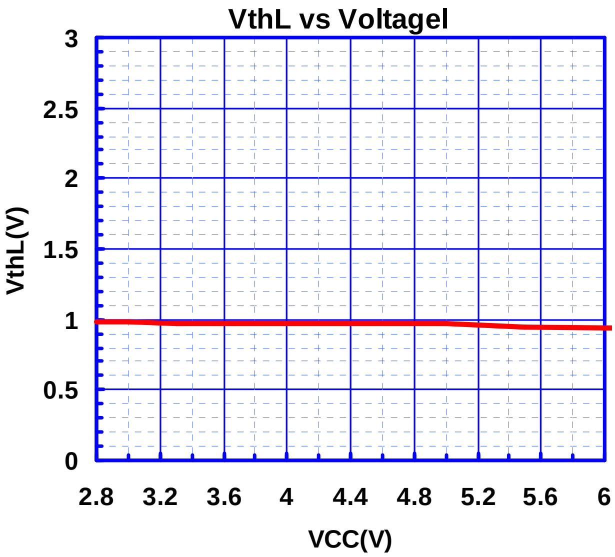


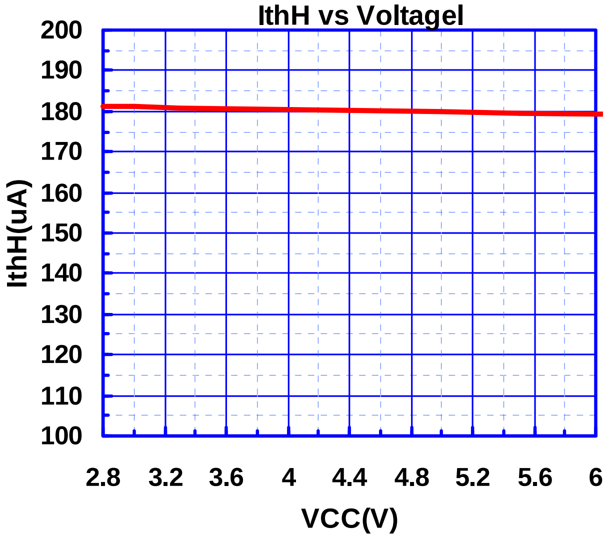


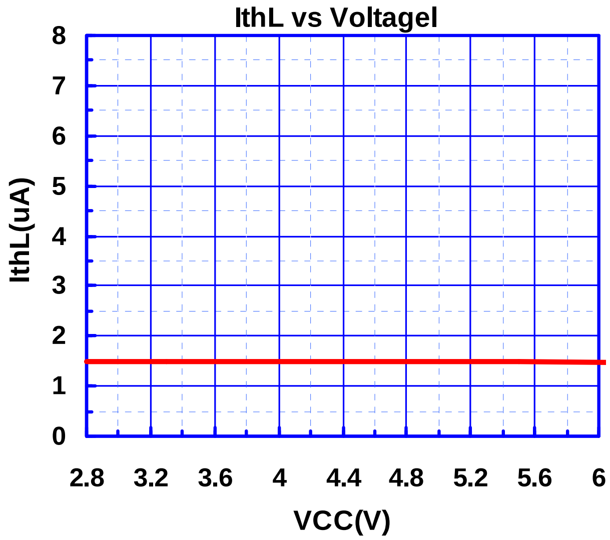


■TYPICAL CHARACTERISTICS

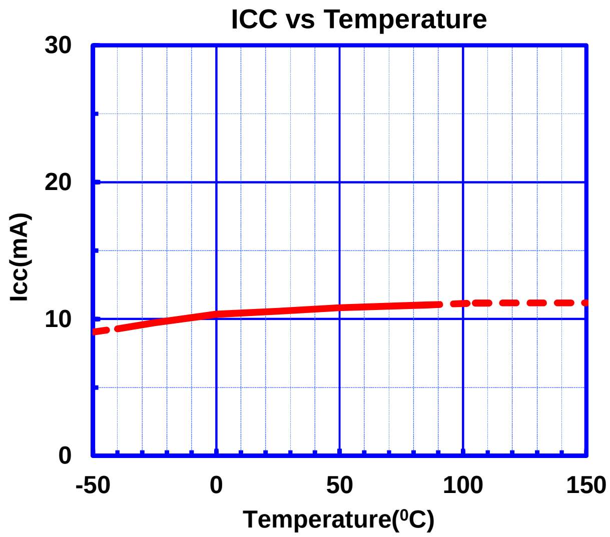


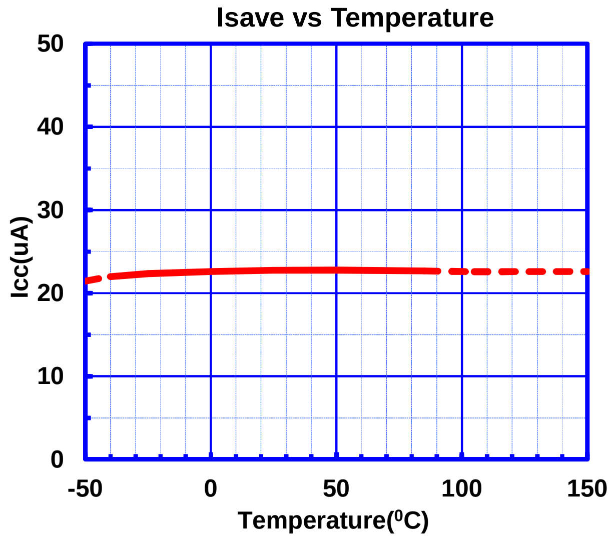


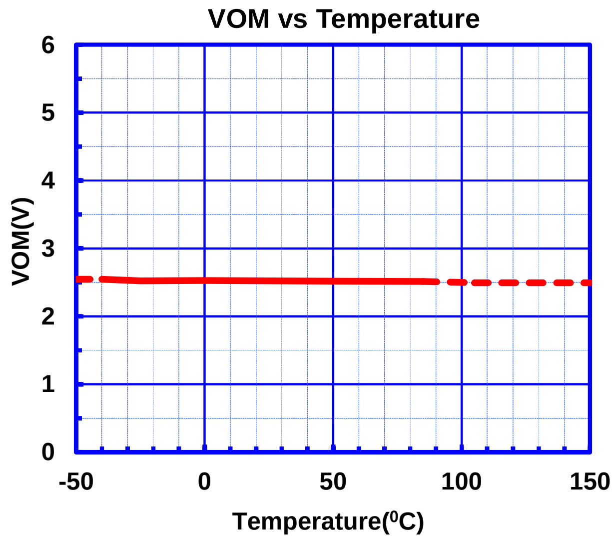


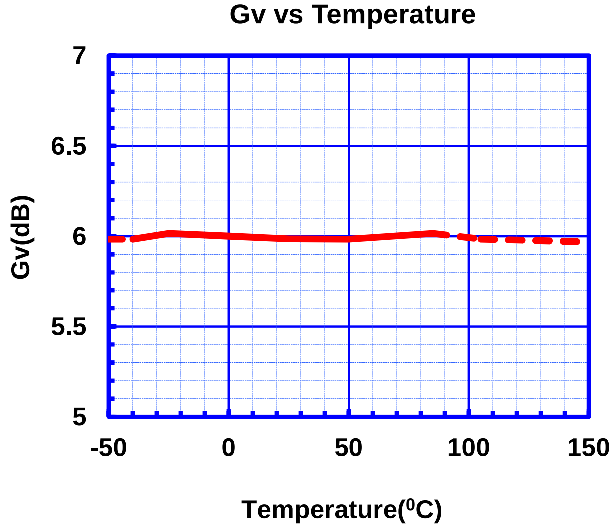


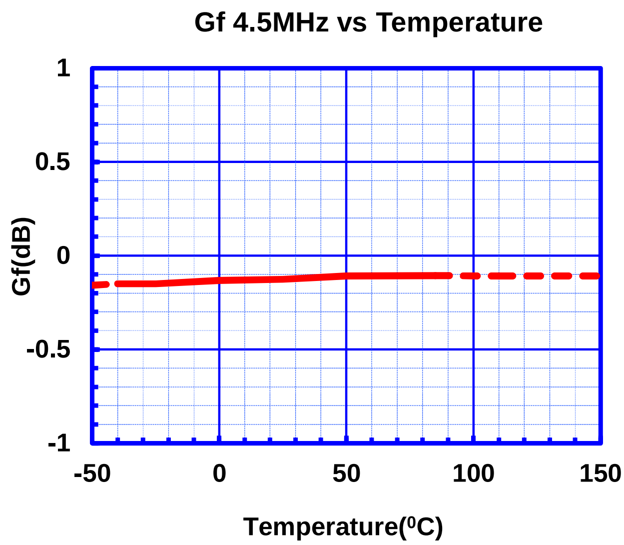
■TYPICAL CHARACTERISTICS

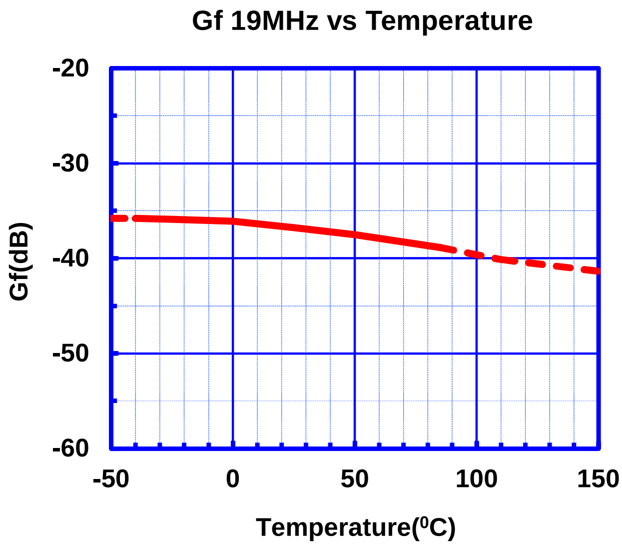




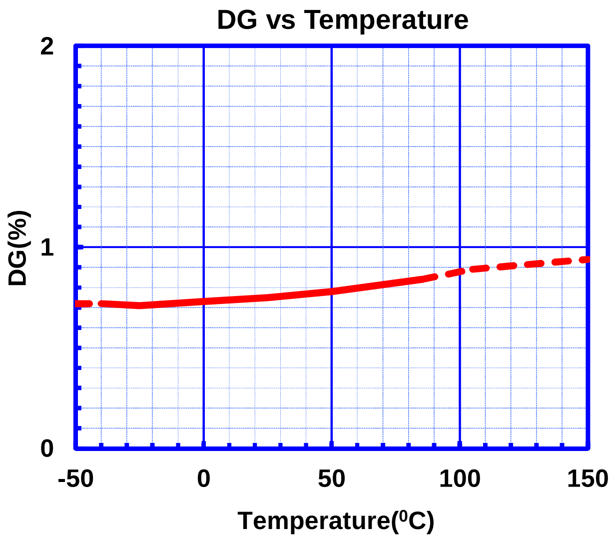


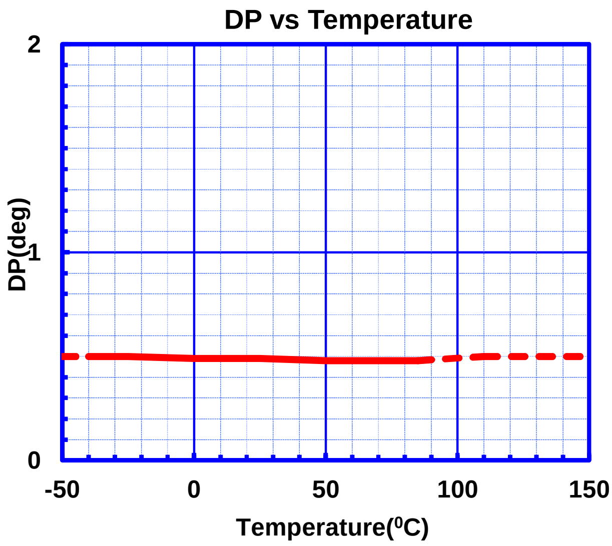


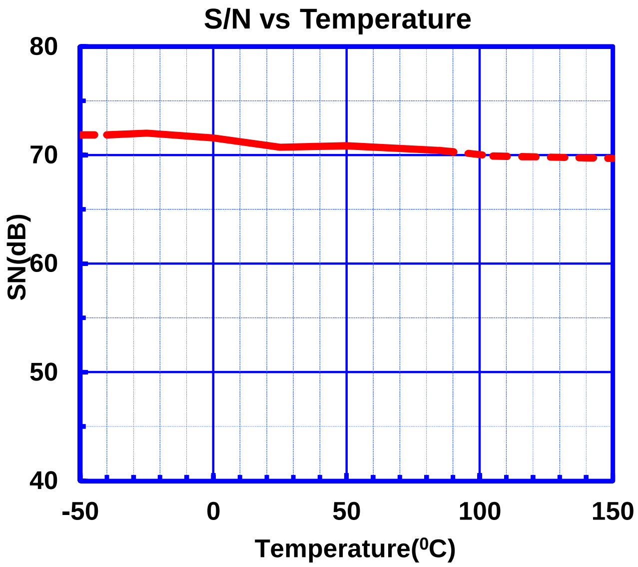


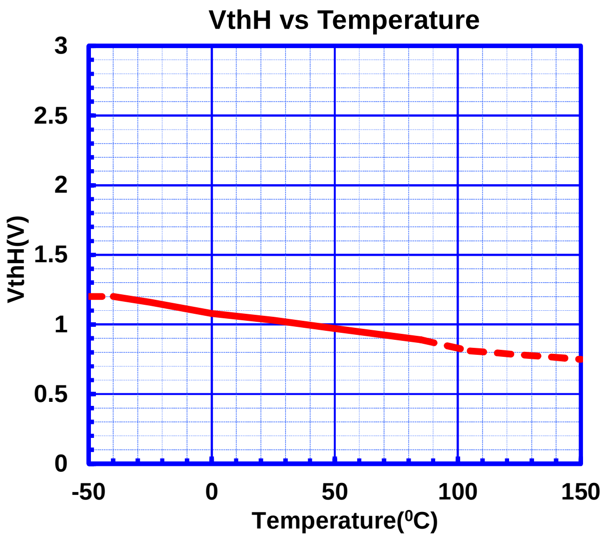


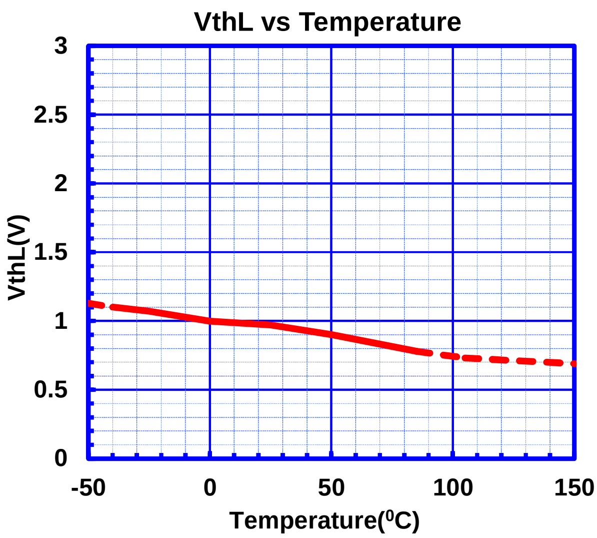
■TYPICAL CHARACTERISTICS



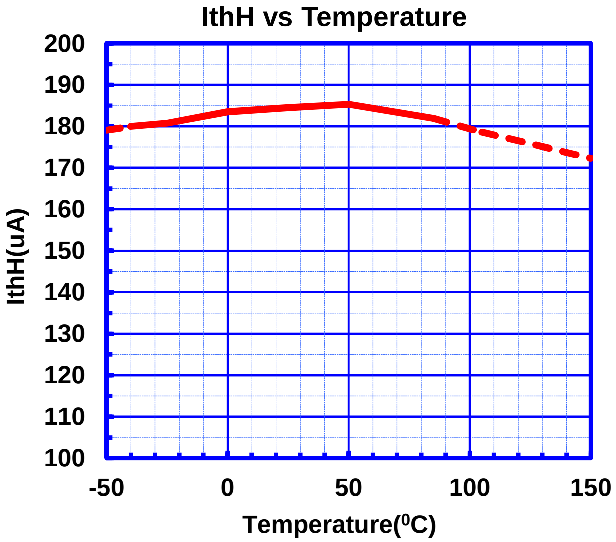


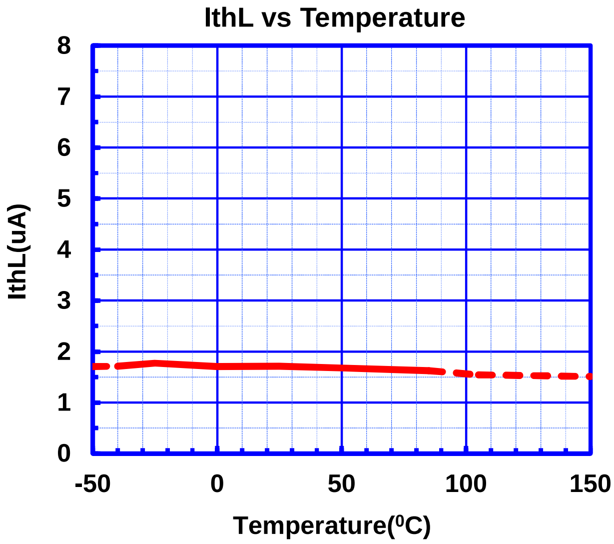






■TYPICAL CHARACTERISTICS





■Clamp circuit

1. Operation of Sync-tip-clamp

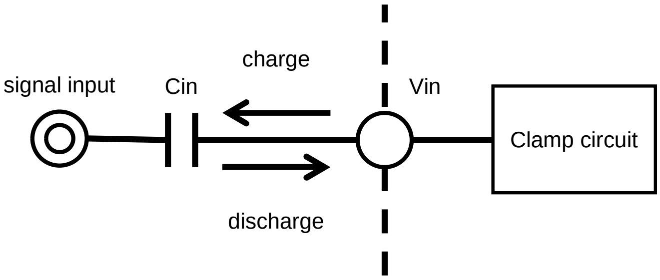
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input Cin. It is charged to the capacitor to the external input Cin at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor Cin at period other than the video signal sync tip. This is due to a small discharge current to the IC.

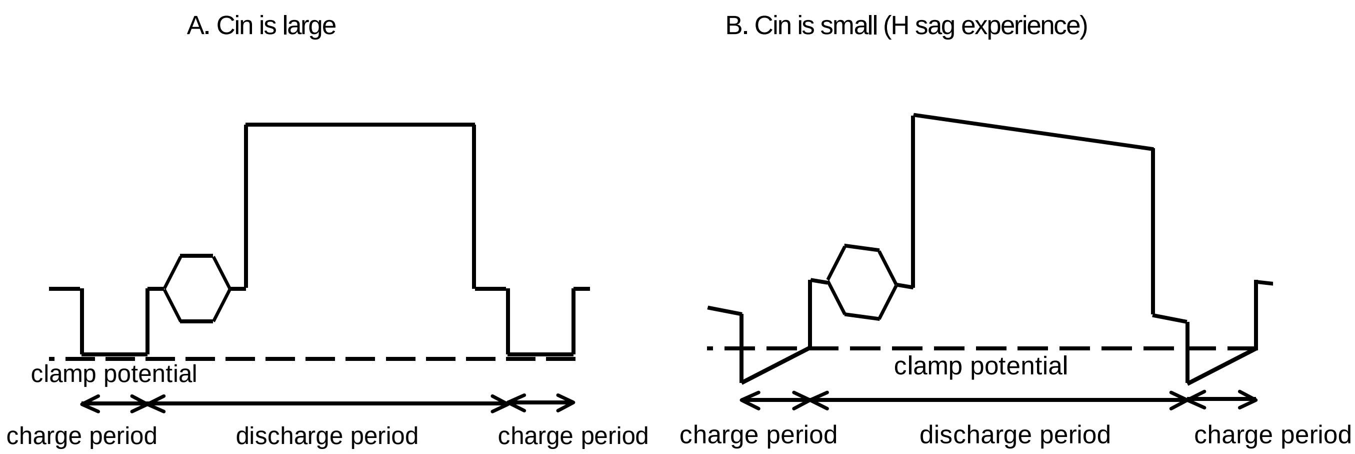
In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of Cin and discharging of Cin at every one horizontal period of the video signal.

The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor Cin.

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1uF.



< Clamp circuit >



< Waveform of input terminal >

2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few kΩ. On the other hand, the input impedance of the discharge period is several MΩ. Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

Source impedance to the input terminal, please lower than 200Ω. A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

■About the ASC(Advanced SAG Correction) circuit

Advanced SAG Correction circuit is our own sag correction technology (patent). It can reduce the output coupling capacitor than conventional sag correction circuit. You can use the ASC circuit, it will contribute to space saving. Also, because it is not in the output capacitor-less, does not have any anxiety which the output is short-circuited.

This section describes the following four items.

1) Overview of the ASC circuit
2) How to set up an external circuit
3) Circuit example of when the two systems drive
4) Notes on Using

1) Overview of the ASC circuit

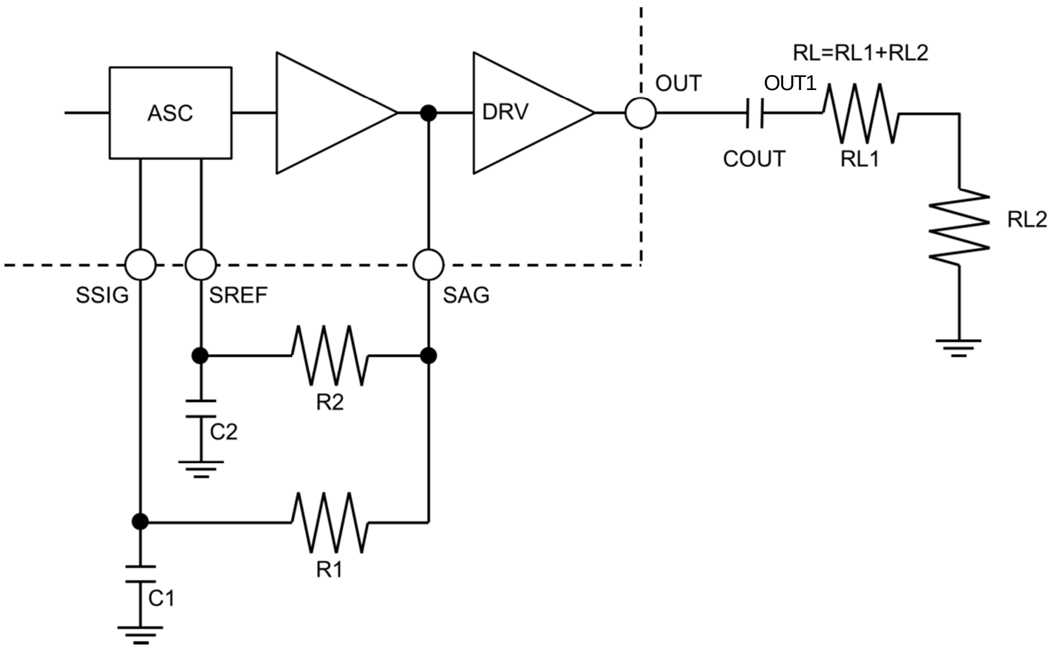
A high-pass filter in the load resistance and output coupling capacitor is configured. Sag occurs because the low-frequency component of the signal is attenuated by this high-pass filter. ASC circuit amplifies the low-frequency component of the signal, corrects for attenuation of the low-frequency component.

The figure below shows ASC around circuit.

SAG terminal is a signal output terminal for correcting the sag. Low pass filter of the resistor R1 and the capacitor C1 will cancel the high-pass filter of the load resistor RL and an output coupling capacitor which is connected to the OUT terminal. And, it is connected to the SSIG terminal. The signal input to the SSIG terminal by processing inside the IC, and generates a signal for correcting the sag.

ASC circuit for amplification the low frequency components of the signal, require a wide dynamic range. The low-pass filter of the resistor R2 and the capacitor C2, to generate a signal of APL (Average Picture Level) voltage. And input to the VREF terminal. Use this voltage of SREF terminal it has to optimize the voltage of the internal IC. ASC circuit generates a sag correction waveform by processing the signal of SSIG terminal and SREF terminal. If sag correction component is large, it may exceed the dynamic range of IC. ASC circuit will stop the operation of the sag correction function if it exceeds the dynamic range by sag correction circuit. Therefore, and preventing that the signal is clipped to fit within the dynamic range.

< ASC around circuit >



2) How to set up an external circuit

This section describes the constant setting steps of the ASC around circuit.

1: First, determine the cut-off frequency: fcout of the high-pass filter to resistance: RL and the output capacitor: COUT of the OUT terminal is configured.
The output capacitor: COUT, please be more than 47uF.

$$fcout = \frac{1}{2\pi \cdot COUT \cdot RL}$$

2: The low-pass filter with a resistor R1 (> 10kΩ) and capacitor C1 is configured. Please refer to the cut-off frequency fc1 the same as fcout.

$$fc1 = \frac{1}{2\pi \cdot C1 \cdot R1} = fcout$$

3: The low-pass filter with a resistor R2 (> 10kΩ) and capacitor C2 is configured. Please do cut-off frequency fc2 is less than or equal to 3Hz.

$$fc2 = \frac{1}{2\pi \cdot C2 \cdot R2} \leq 3$$

4: Please make sure that the combined resistance R1 // R2 of the resistors R1 and R2 is equal to or more than 5kΩ.
And please check the sag characteristics.

Parameter Set example

Set the constant in the case where the output capacitor COUT = 47uF, and a resistor RL = 150Ω.

1. Calculate the cut-off frequency of the high-pass filter formed by capacitor 47uF and resistance 150Ω of OUT terminal.

$$fcout = \frac{1}{2\pi \cdot COUT \cdot RL} = \frac{1}{2\pi \cdot 47u \cdot 150} = 22.6[Hz]$$

2. LPF is configured by a resistor R1 (> 10kΩ) and capacitor C1, and so the cut-off frequency fc1 is the same as fcout.

$$fc1 = \frac{1}{2\pi \cdot C1 \cdot R1} = \frac{1}{2\pi \cdot 0.1u \cdot R1} = 22.6$$

$$R1 = \frac{1}{2\pi \cdot 0.1u \cdot 22.6} = 70.4[k\Omega] \cong 68[k\Omega]$$

Calculation results of the resistor R1 is 70.4kΩ. Here are the 68kΩ available at E6 series.

3. LPF is configured by a resistor R2 (> 10kΩ) and capacitor C2, and cut-off frequency fc2 is set to be less t than 3Hz.
When the capacitor C2 to 1uF, and will be as follows.

$$fc2 = \frac{1}{2\pi \cdot C2 \cdot R2} = \frac{1}{2\pi \cdot 1u \cdot R2} < 3$$

$$R2 > \frac{1}{2\pi \cdot 1u \cdot 3} = 53[k\Omega] \Rightarrow 68[k\Omega]$$

Calculation results of the resistor R2 must be more than or equal to 53kΩ. Therefore, it is the resistor R1 and the same 68kΩ.

4. Make sure that the combined resistance of R1 and R2 is equal to or more than 5kΩ

$$R1 // R2 = 68k // 68k = 34k$$

After constant determination, each characteristic is please makes sure that there is no problem.
This setting example is the same as the test circuit diagram of the data sheet.

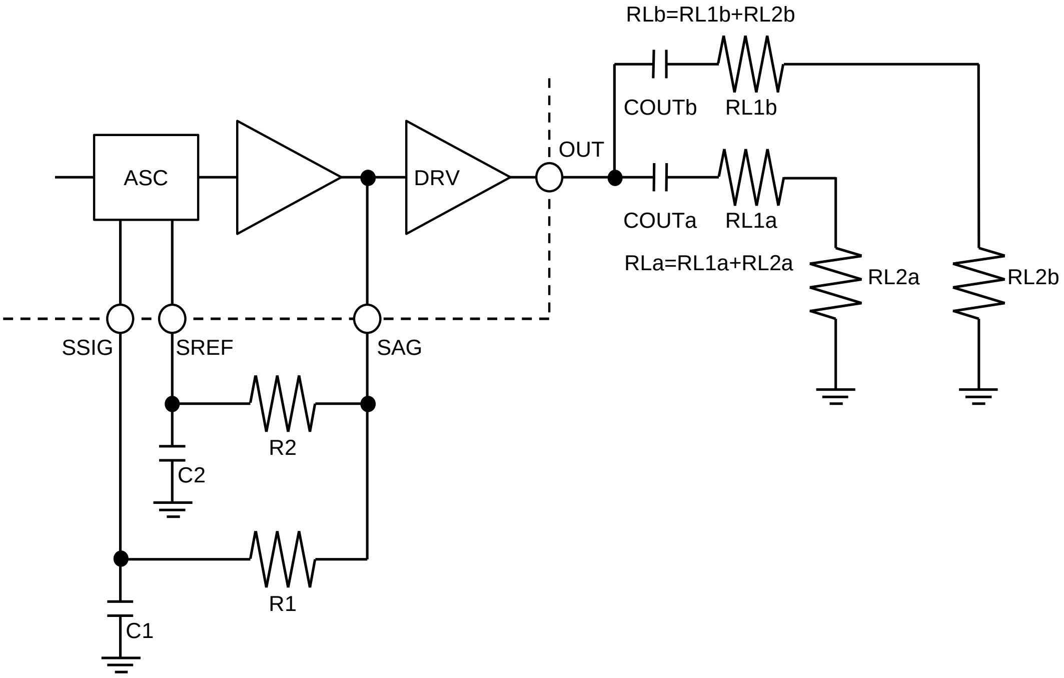
3) Circuit example of two systems drive

An example of a circuit of the two systems drive is shown in the following figure. In the case of a two-system drive, the output capacitor requires COUTa and COUTb. As the cut-off frequency of the high-pass filter is the same, the output capacitor (COUTa, COUTb) and resistance (RLa, RLb) please set.

$$fcout = \frac{1}{2\pi \cdot COUTa \cdot RLa} = \frac{1}{2\pi \cdot COUTb \cdot RLb}$$

Element constant of SAG terminal and SSIG terminal and SREF terminal, please set according to the previous section on how to set up.

< Two system drive circuit >



4) Usage note

Resistance value of SAG terminal R (= R1 // R2), please be more than 5kΩ.
If the resistance is small, the signal to output to the OUT terminal may be distorted.

Wiring of SAG terminal and SREF terminal and SSIG terminal please do as much as possible short.
If the noise is mixed to these terminals, the noise is mixed in signals output to the OUT terminal.

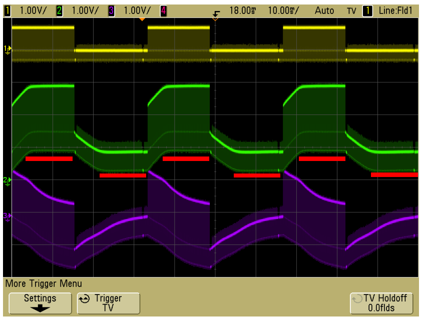
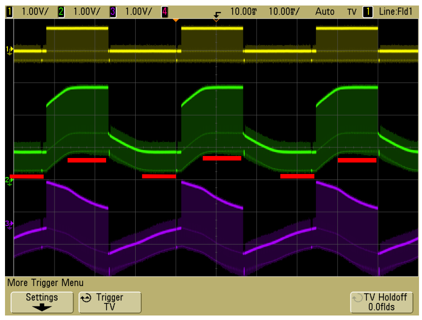
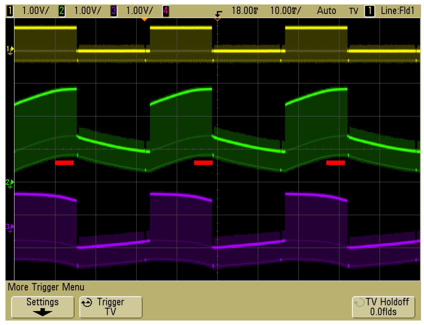
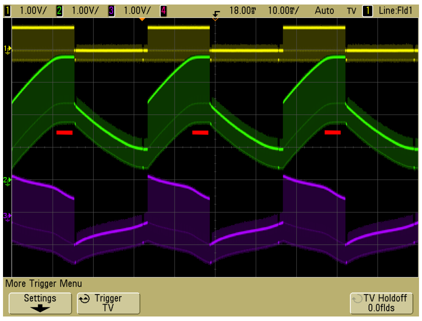
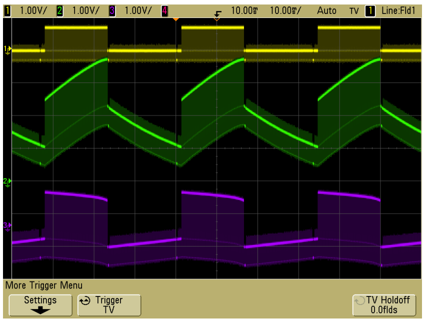
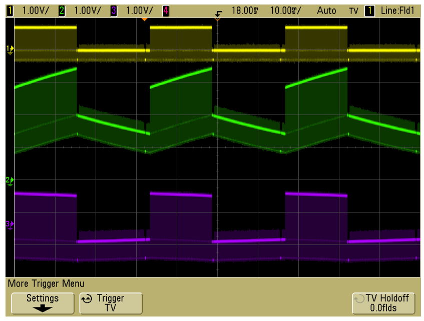
If you want to use a ceramic capacitor, please use a capacitor with good DC bias characteristics.
Ceramic capacitors, capacitance value will vary depending on the DC voltage to be applied. This characteristic is referred to as the DC bias characteristics. There is the actual capacitance value and the desired capacitance value is shifted by this DC bias characteristics. Thereby, it may sag correction function does not work well.

You may also set the constants of external elements does not work sag correction function.
If sag correction component is large, it becomes a waveform signal exceeds the dynamic range of the IC.
In order to prevent that the signal exceeds the dynamic range is to clip, ASC circuit will stop the sag correction function.
In this case, whether to enhance the power supply voltage, or change each element constant by increasing the output capacitor

■Waveform example

Input: Bounce signal (IRE0%, IRE100%, 30Hz), RL=150Ω

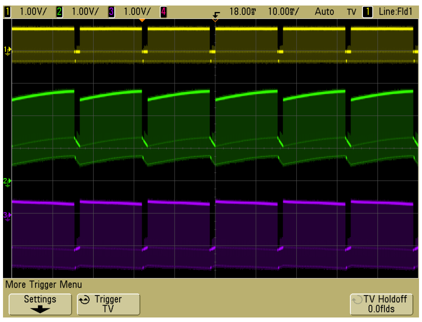
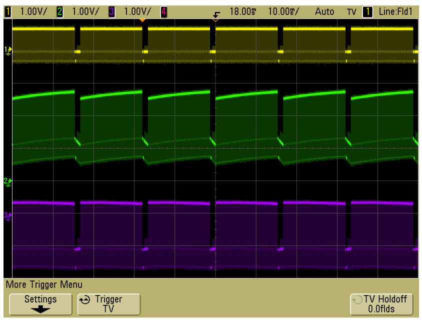
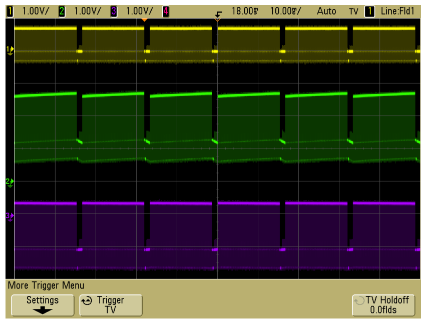
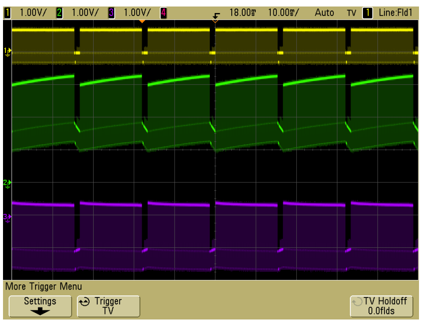
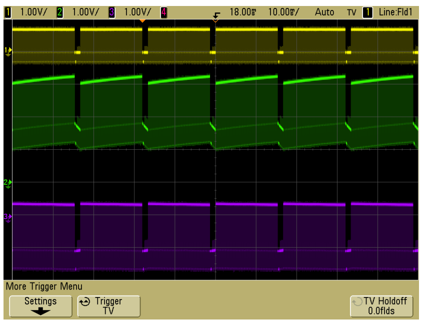
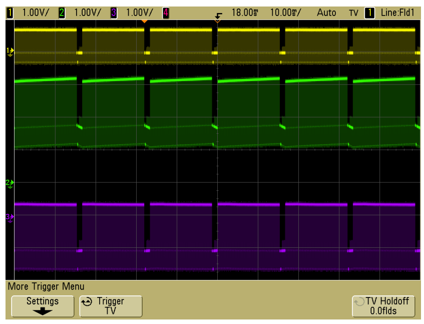
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal, red = Sag correction stop period

	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF	Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF
Vcc=3.0V			
Vcc=5.0V			

If the power supply voltage is low, if the output capacitor is small, to prevent signal clipping beyond the dynamic range of the OUT terminal, sag correction function stops.

Input: White 100%, RL=150Ω

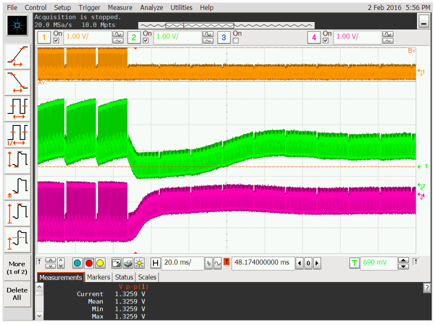
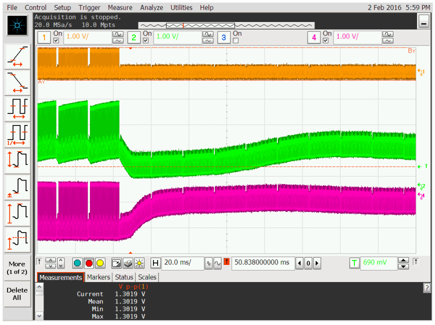
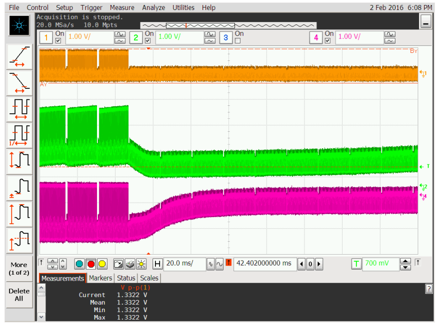
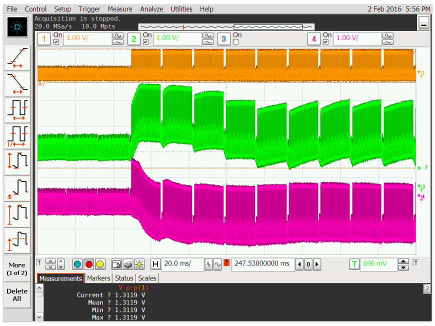
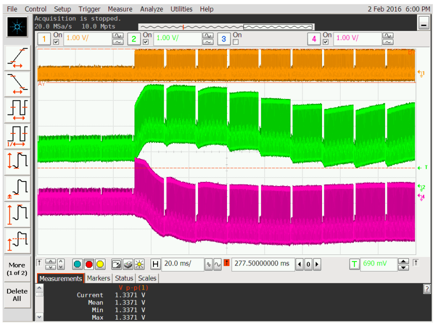
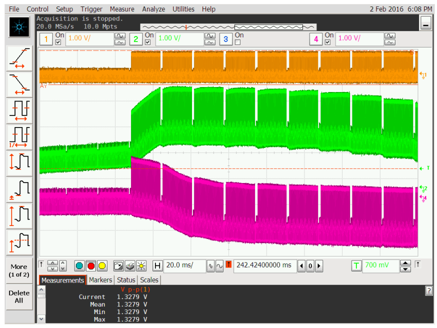
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal

	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF	Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF
Vcc=3.0V			
Vcc=5.0V			

■Waveform example　at Black-and-White change

Input: Black-and-White change signal, RL=150Ω

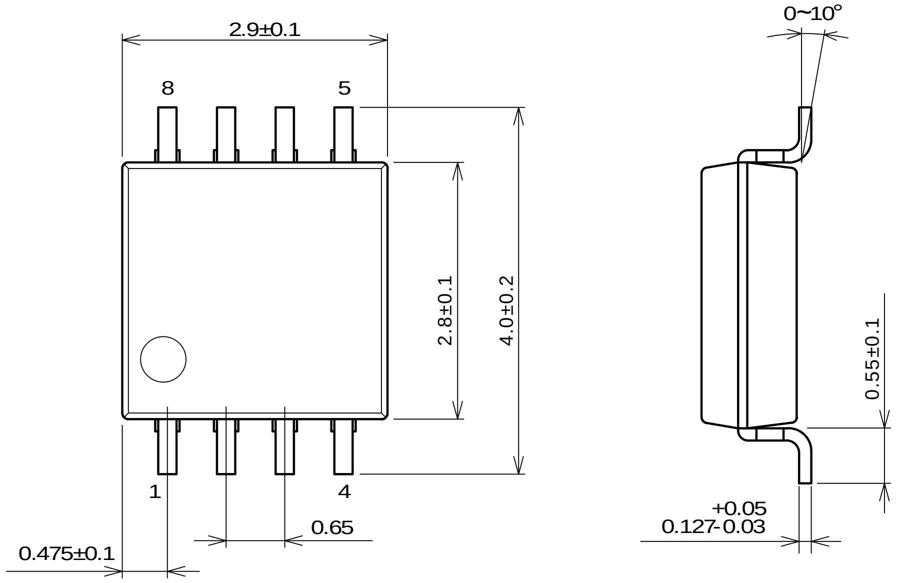
Waveform: yellow = Input signal, green = Output signal, red = OUT1 signal

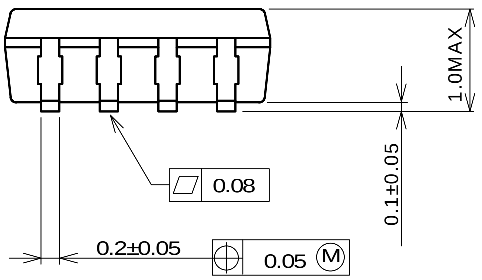
	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF	Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF
Vcc=5.0V 白黒			
Vcc=5.0V 黒白			

DC level will change by APL fluctuation at the black-and-white change.　The rate of change of the DC level is dependent on the capacitance value of Cout.

■PACKAGE OUTLINE

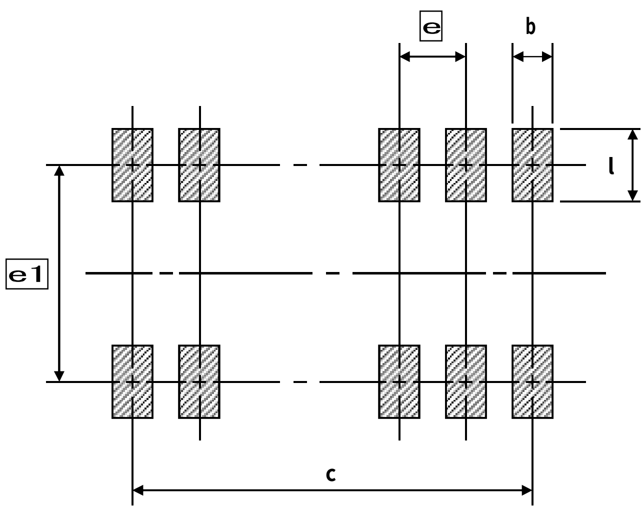
MSOP8





■SOLDER FOOT PRINT

PKG	b	l	c	e1	e
MSOP8	0.23	1.00	1.95	3.50	0.65



Note : These solder foot print dimensions are just examples.
When designing PCB, please estimate the pattern carefully.

Unit : mm

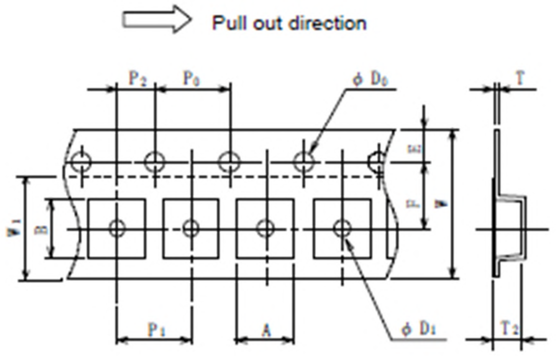
■PACKING SPECIFICATION

General Description

NJRC delivers ICs in 4 methods, plastic tube container, two kinds of Taping, tray and vinyl bag packing. Except adhesive tape treated anti electrostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

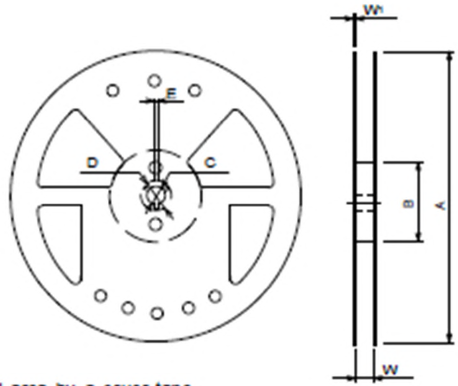
MSOP (VSP/TVSP) Emboss Taping (TE1)

Symbol	MSOP8/10 (TVSP8/10) * *MEETJEDEC MO-187-DA / THIN TYPE	Remark
A	4.4	Bottom size
B	3.2	Bottom size
D_0	1.5+0.1/-0	
D_1	1.5+0.1/-0	
E	1.75±0.1	
F	5.5±0.05	
P_0	4.0±0.1	
P_1	8.0±0.1	
P_2	2.0±0.05	
T	0.3±0.05	
T_2	1.45	
W	12.0±0.3	
W_1	9.5	Thickness 0.1MAX

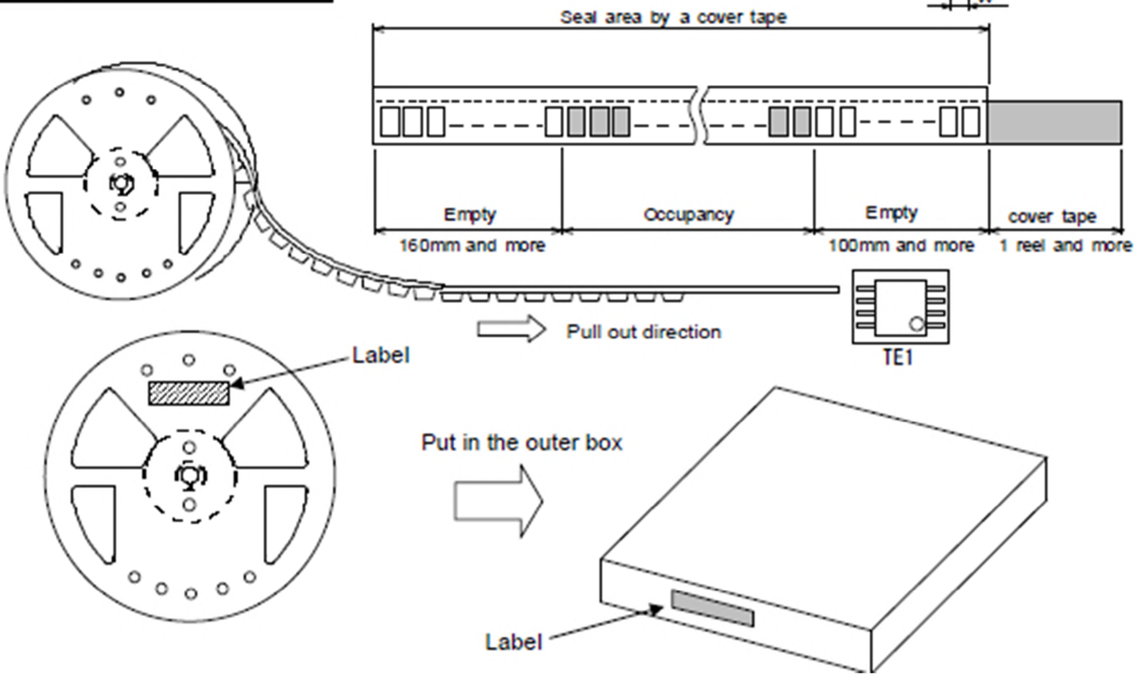


Unit : mm

Symbol	MSOP8/10 (TVSP8/10) * *MEETJEDEC MO-187-DA / THIN TYPE
A	Ø254±2
B	Ø100±1
C	Ø13±0.2
D	Ø21±0.8
E	2±0.5
W	13.5±0.5
W_1	2±0.2
Contents	2,000 pcs

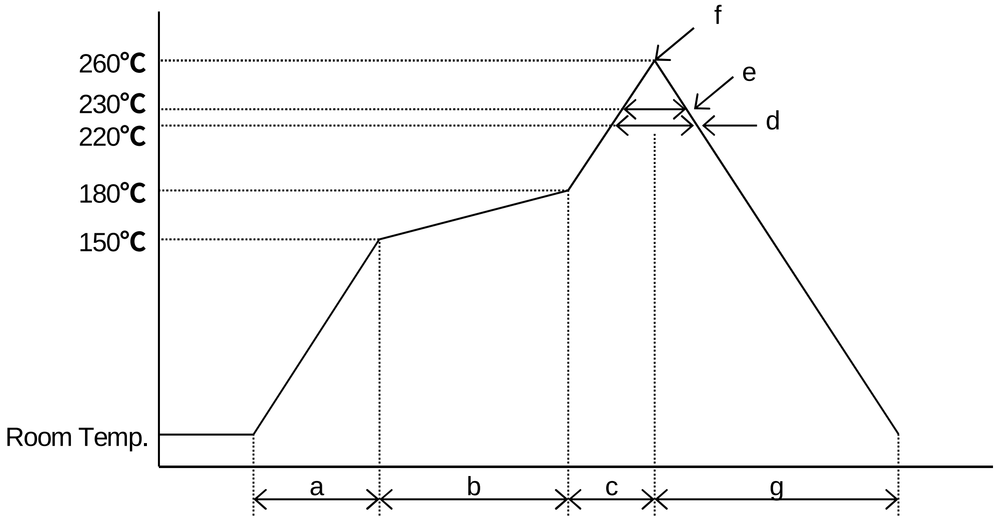


Unit : mm



■RECOMMENDED MOUNTING METHOD

∗Recommended reflow soldering procedure



a:Temperature ramping rate	: 1 to 4°C/s
b:Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c:Temperature ramp rate	: 1 to 4°C/s
d:220°C or higher time	: Shorter than 60s
e:230°C or higher time	: Shorter than 40s
f:Peak temperature	: Lower than 260°C
g:Temperature ramping rate	: 1 to 6°C/s

The temperature indicates at the surface of mold package.

[CAUTION]

1. New JRC strives to produce reliable and high quality semiconductors. New JRC's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of New JRC's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures

2. The specifications on this datasheet are only given for information without any guarantee as regards either mistakes or omissions. The application circuits in this datasheet are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.
All other trademarks mentioned herein are property of their respective companies.

3. To ensure the highest levels of reliability, New JRC products must always be properly handled.
The introduction of external contaminants (e.g. dust, oil or cosmetics) can result in failures of semiconductor products.

4. New JRC offers a variety of semiconductor products intended for particular applications. It is important that you select the proper component for your intended application. You may contact New JRC's Sale's Office if you are uncertain about the products listed in this catalog.

5. Special care is required in designing devices, machinery or equipment which demand high levels of reliability. This is particularly important when designing critical components or systems whose failure can foreseeably result in situations that could adversely affect health or safety. In designing such critical devices, equipment or machinery, careful consideration should be given to amongst other things, their safety design, fail-safe design, back-up and redundancy systems, and diffusion design.

6. The products listed in the catalog may not be appropriate for use in certain equipment where reliability is critical or where the products may be subjected to extreme conditions. You should consult our sales office before using the products in any of the following types of equipment.

   Aerospace Equipment
   Equipment Used in the Deep sea
   Power Generator Control Equipment (Nuclear, Steam, Hydraulic)
   Life Maintenance Medical Equipment
   Fire Alarm/Intruder Detector
   Vehicle Control Equipment (airplane, railroad, ship, etc.)
   Various Safety devices

7. New JRC's products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this catalog. Failure to employ New JRC products in the proper applications can lead to deterioration, destruction or failure of the products. New JRC shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of its products. Products are sold without warranty of any kind, either express or implied, including but not limited to any implied warranty of merchantability or fitness for a particular purpose.

8. Warning for handling Gallium and Arsenic(GaAs) Products (Applying to GaAs MMIC, Photo Reflector). This Products uses Gallium(Ga) and Arsenic(As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed, please follow the related regulation and do not mix this with general industrial waste or household waste.

9. The product specifications and descriptions listed in this catalog are subject to change at any time, without notice.