Low power Single Channel OP-Amp

■FEATURES(V^+=5V, V^-=0V, Ta=25°C)

- ●Guaranteed Temperature -40°C to +125°C
- ●Input Offset Voltage 2mV max.
- ●Input Offset Voltage Drift 17μV/°Cmax.
- ●Supply Current 0.7mA max.
- ●Operating Voltage +3V to +36V or ±1.5V to ±18V
- ●Integrated EMI filter EMIRR=84dB typ. @f=1.8GHz
- ●GBW 1.1MHz typ.
- ●GND sencing
- ●Internal ESD protection Human Body Model ±2000V typ.
- ●Package
  - NJM8020 SOT-23-5, SC-88A
  - NJM8021 SOT-23-5, SC-88A, DFN6-G1(ESON6-G1)

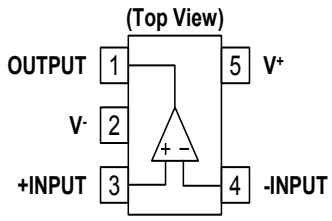
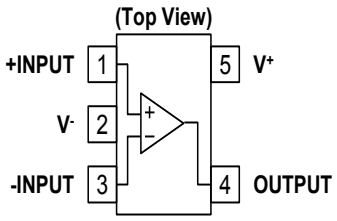
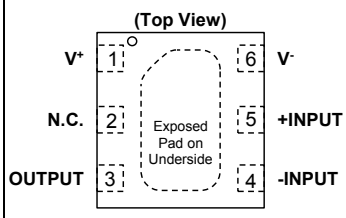
■GENERAL DESCRIPTION

The NJM8020/NJM8021 are single OP-Amps designed specifically to operate wide range of supply voltage and temperature.

These OP-Amps featured low input offset voltage of 2mV max. low supply current of 0.7mA max. DC characteristics are also 100% tested and guaranteed from -40 to 125°C.

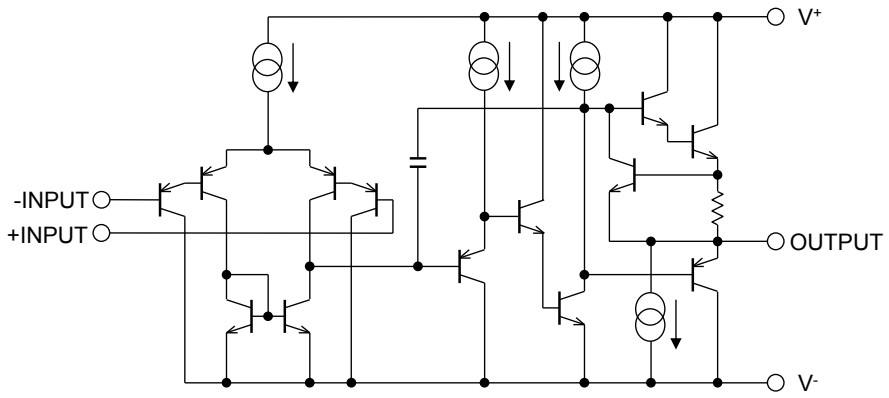
The NJM8020/NJM8021 are available in DFN6-G1 (1616) of small size Package, significantly reducing the required portable application's board area.

■PIN CONFIGURATION

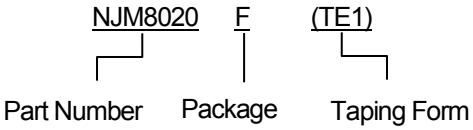
Parts Number	NJM8020F	NJM8020F3	NJM8021F	NJM8021F3	NJM8021KG1
Package Outline	SOT-23-5	SC-88A	SOT-23-5	SC-88A	DFN6-G1(*)
Pin Function					

(*)Connect to exposed pad to V^-

■EQUIVALENT CIRCUIT



■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJM8020F	SOT-23-5	yes	yes	Sn2Bi	A5Z	15	3,000
NJM8020F3	SC-88A	yes	yes	Sn2Bi	2E	7.5	3,000
NJM8021F	SOT-23-5	yes	yes	Sn2Bi	A5Y	15	3,000
NJM8021F3	SC-88A	yes	yes	Sn2Bi	2D	7.5	3,000
NJM8021KG1	DFN6-G1	yes	yes	Sn2Bi	8021	3.5	3,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+ - V^-$	36	V
Input Voltage (1)	V_{IN}	V^- - 0.3 to V^- + 36	V
Output Terminal Input Voltage	V_o	V^- - 0.3 to V^+ + 0.3	V
Differential Input Voltage	V_{ID}	±36	V
Input Current (2)	I_{IN}	5	mA
Power Dissipation(Ta=25°C) SOT-23-5 SC-88A DFN6-G1(ESON6-G1)	P_D	(2-layer / 4-layer) 480(4) / 650(5) 360(4) / 490(5) 330(6) / 1200(7)	mW
Junction Temperature	T_{jmax}	+150	°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C

(1) Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V^+
The normal amplifier operation input voltage is within "Common Mode Input Voltage Range" specified in the Electrical characteristics.

(2) This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-vase junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the OP-Amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.

(3) Short-circuit can cause excessive heating and destructive dissipation. Values are typical.

(4) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)

(5) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2x 74.2mm

(6) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

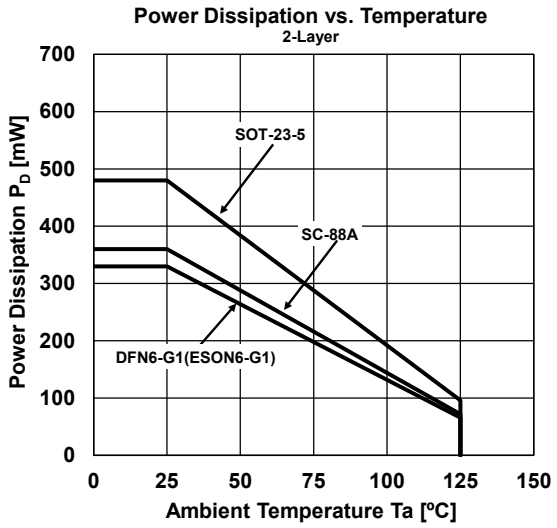
(7) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

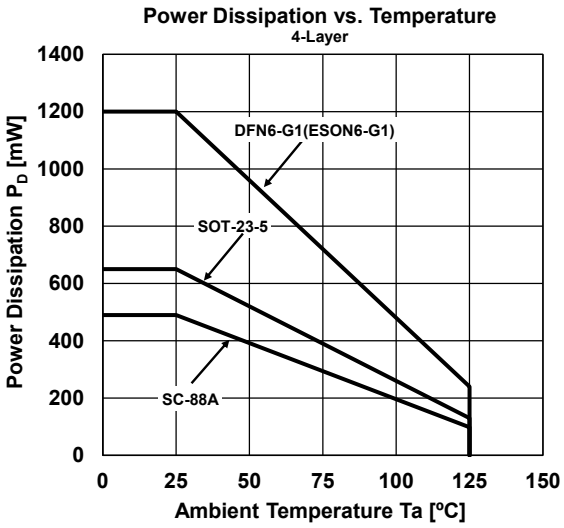
■THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance SOT-23-5(8) SC-88A(8) DFN6-G1(ESON6-G1)(9)	θja	(2-layer / 4-layer) 260 / 195 355 / 260 385 / 110	°C /W
Junction-to-Top of package characterization parameter SOT-23-5(8) SC-88A(8) DFN6-G1(ESON6-G1)(9)	ψjt	(2-layer/ 4-layer) 68 / 58 91 / 74 65 / 26	°C /W

(8) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)
Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2 x 74.2mm
(9) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)
Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

■POWER DISSIPATION vs. AMBIENT TEMPERATURE





■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+ - V^-$	3 to 36	V
Operating Ambient Temperature	T_{opr}	- 40 to +125	°C

■ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V^+=5V, V^-=0V, R_L=OPEN, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage(10)	V_{IO}		—	0.5	2	mV
		Ta=-40°C to 125°C	—	—	3	
Input Offset Voltage Drift (11)	$\Delta V_{IO}/\Delta T$	Ta=-40°C to 125°C	—	5	17	μV/°C
Input Offset Current	I_{IO}		—	2	30	nA
		Ta=-40°C to 125°C	—	—	40	
Input Offset Current Drift (11)	$\Delta I_{IO}/\Delta T$	Ta=-40°C to 125°C	—	—	300	pA/°C
Input Bias Current (12)	I_B		—	20	150	nA
		Ta=-40°C to 125°C	—	—	200	
Open-Loop Voltage Gain	A_V	V^+=15V,R_L=2kΩ, Vo=1.4V to 11.4V	50	100	—	V/mV
		V^+=15V,R_L=2kΩ, Vo=1.4V to 11.4V Ta=-40 to 125°C	25	—	—	
Supply Voltage Rejection Ratio	SVR	V^+=5V to 30V,R_S<10kΩ	65	100	—	dB
		V^+=5V to 30V,R_S<10kΩ Ta=-40 to 125°C	65	—	—	
Supply Current	I_{SUPPLY}	Ta=-40 to 125°C	—	0.45	0.7	mA
		V^+=30V , Ta=-40 to 125°C	—	—	1	
Common Mode Input Voltage Range	V_{ICM}	V^+=30V(13)	0	—	V^+-1.5	V
		V^+=30V, Ta=-40 to 125°C	0	—	V^+-2.0	
Common-Mode Rejection Ratio	CMR	R_S<10kΩ	70	100	—	dB
		R_S<10kΩ,Ta=-40 to 125°C	60	—	—	
Output Source Current	I_{SOURCE}	V^+=15V,V_{IN}+=1V,V_{IN}-=0V, V_o=2V	20	40	—	mA
Output Sink Current	I_{SINK}	V^+=15V,V_{IN}+=0V,V_{IN}-=1V, V_o=2V	10	20	—	mA
		V^+=15V,V_{IN}+=0V,V_{IN}-=1V, V_o=0.2V	12	50	—	μA
High-level Output Voltage	V_{OH}	V^+=30V, R_L=2kΩ	26	27	—	V
		V^+=30V, R_L=2kΩ Ta=-40 to 125°C	26	—	—	
		V^+=30V, R_L=10kΩ	27	28	—	
		V^+=30V, R_L=10kΩ Ta=-40 to 125°C	27	—	—	
Low-level Output Voltage	V_{OL}	R_L=10kΩ Ta=-40 to 125°C	—	5	20	mV
		R_L=10kΩ Ta=-40 to 125°C	—	—	20	

■ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V^+=5V, V^-=0V, R_L=OPEN, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	V^+=15V, V_{IN}=0.5V to 3V, R_L=2kΩ,C_L=100pF Unity gain	—	0.6	—	V/μs
Gain Bandwidth Product	GBW	V^+=30V,f=100kHz, V_{IN}=10mV, R_L=2kΩ,C_L=100pF	—	1.1	—	MHz
Total Harmonic Distortion + Noise	THD+N	f=1kHz,Gv=20dB, R_L=2kΩ V_O=2V_{PP},C_L=100pF	—	0.02	—	%
Equivalent Input Noise Voltage	e_n	f=1kHz, Rs=100Ω V^+=30V	—	30	—	nV/√Hz

(10) 5V < V^+ < 30V, 0 < V_{com} < V^+ - 1.5V.

(11) This parameter is not 100% test.

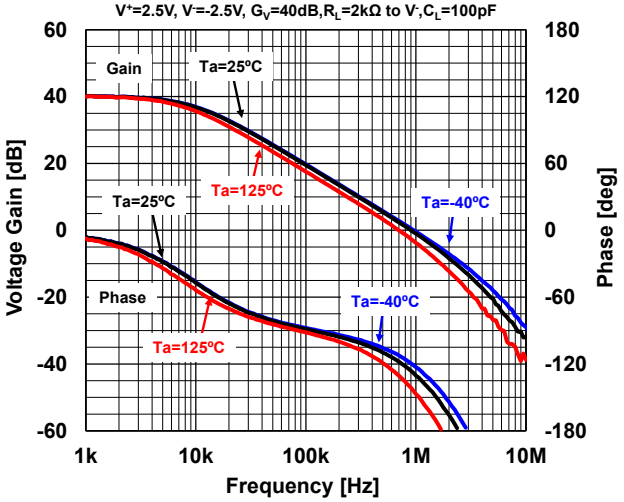
(12) The direction of the input current is out of the IC.

(13) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ - 1.5V, but either or both inputs can go to +36V without damage.

■TYPICAL CHARACTERISTICS

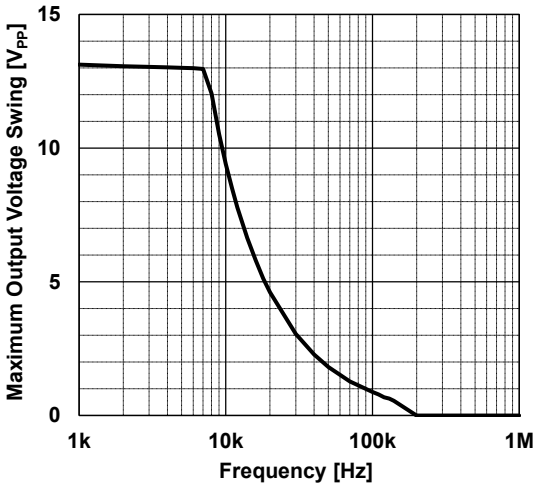
Gain/Phase vs. Frequency

V+=2.5V, V-=-2.5V, G_V=40dB,R_L=2kΩ to V-,C_L=100pF



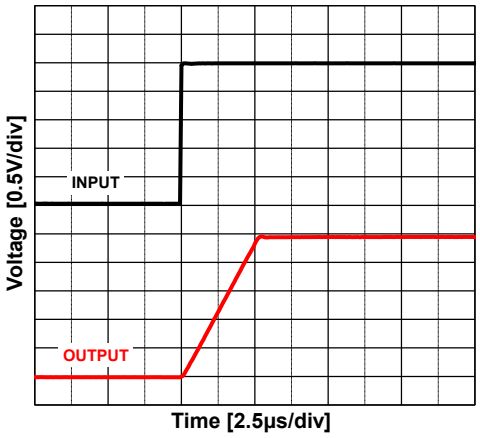
Maximum Output Voltage Swing vs. Frequency

V+=15V, V-=0V, Ta=25ºC



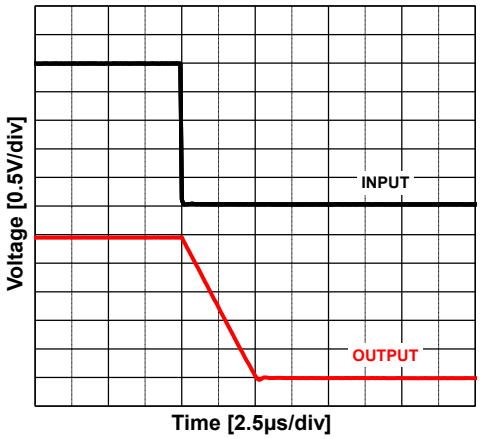
Pulse Response

V+=15V, V-=0V, R_L=2kΩ to V-, C_L=100pF



Pulse Response

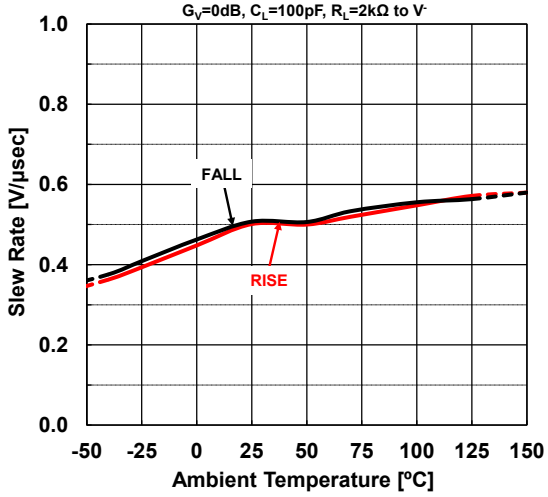
V+=15V, V-=0V, R_L=2kΩ to V-, C_L=100pF



Slew Rate vs. Temperature

V+=15V, V-=0V, f=10kHz

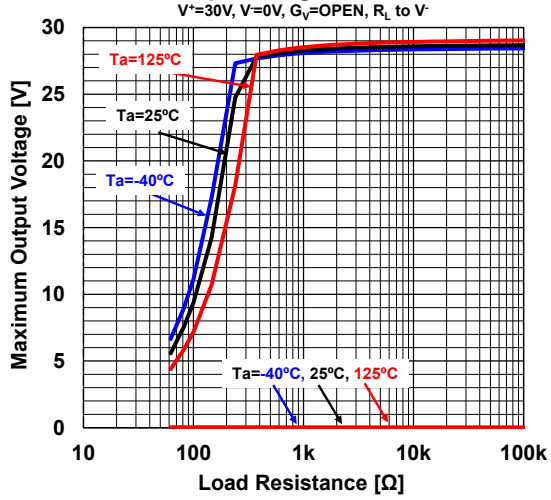
G_V=0dB, C_L=100pF, R_L=2kΩ to V-



■TYPICAL CHARACTERISTICS

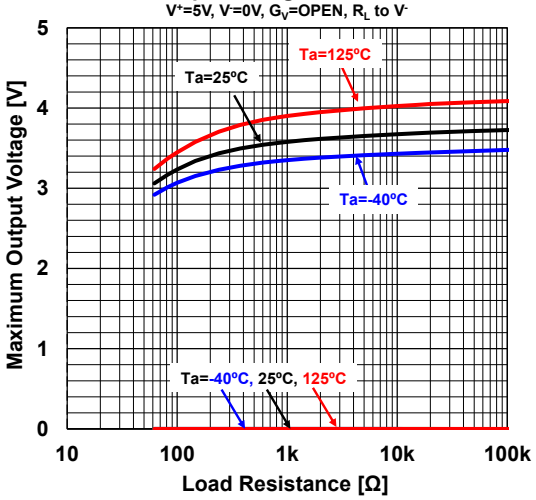
Maximum Output Voltage vs. Load Resistance

V^+=30V, V^-=0V, G_V=OPEN, R_L to V^-



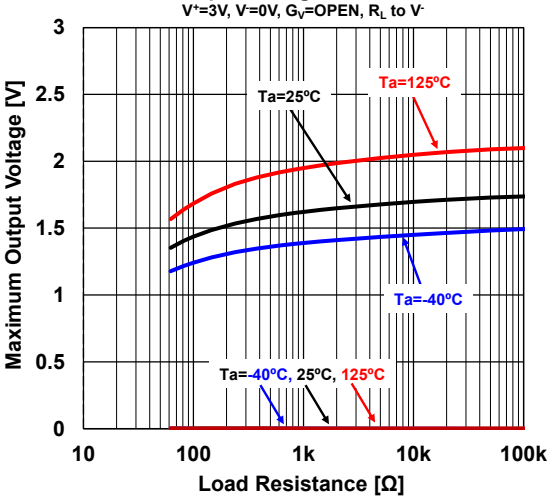
Maximum Output Voltage vs. Load Resistance

V^+=5V, V^-=0V, G_V=OPEN, R_L to V^-



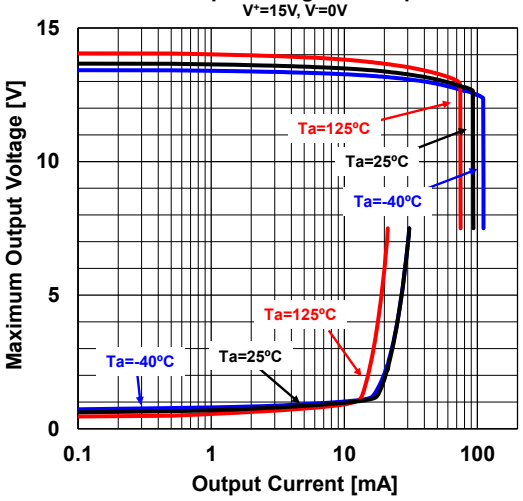
Maximum Output Voltage vs. Load Resistance

V^+=3V, V^-=0V, G_V=OPEN, R_L to V^-



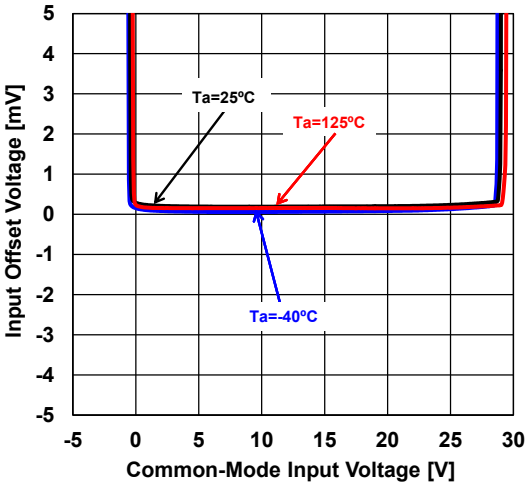
Maximum Output Voltage vs. Output Current

V^+=15V, V^-=0V

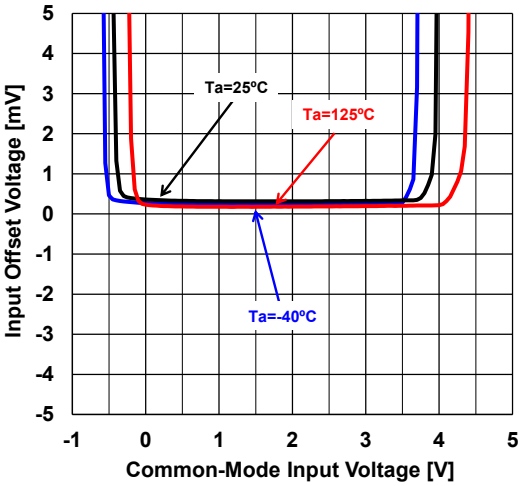


■TYPICAL CHARACTERISTICS

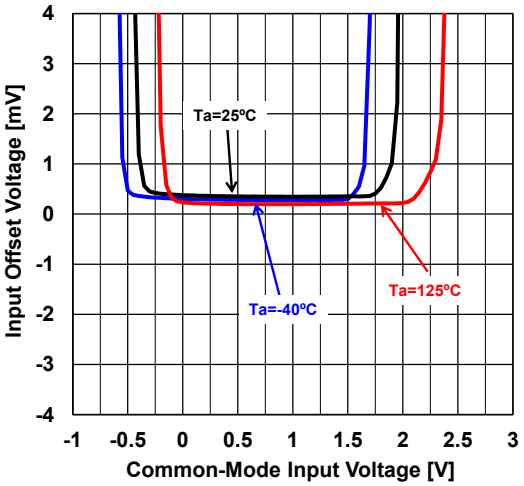
Input Offset Voltage vs. Common-Mode Input Voltage
V⁺=30V, V⁻=0V



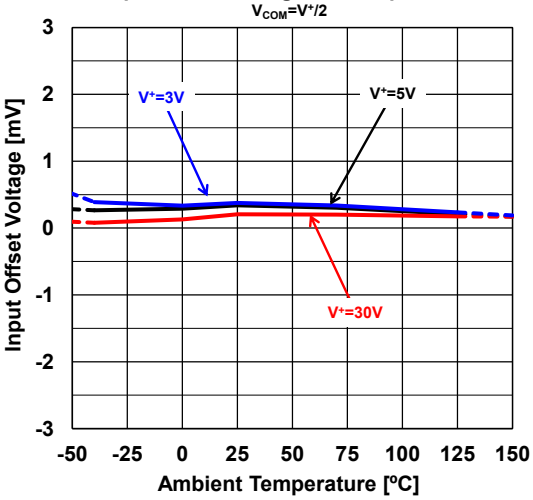
Input Offset Voltage vs. Common-Mode Input Voltage
V⁺=5V,V⁻=0V



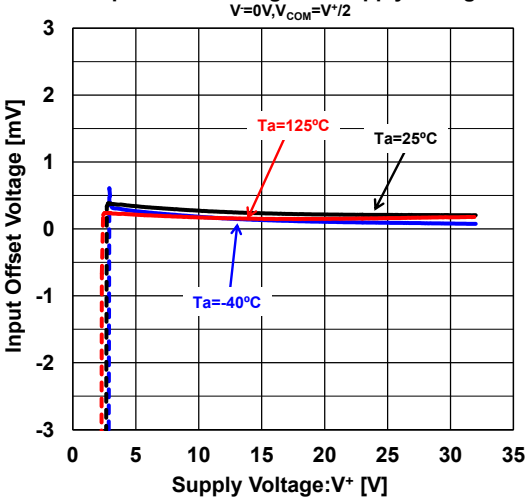
Input Offset Voltage vs. Common-Mode Input Voltage
V⁺=3V,V⁻=0V



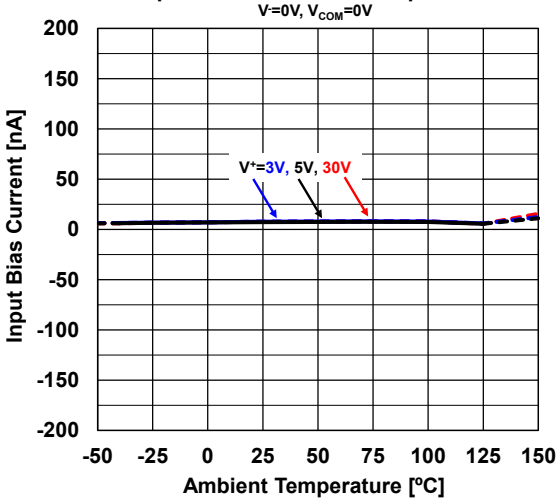
Input Offset Voltage vs. Temperature
V_{COM}=V⁺/2



Input Offset Voltage vs. Supply Voltage
V⁻=0V,V_{COM}=V⁺/2

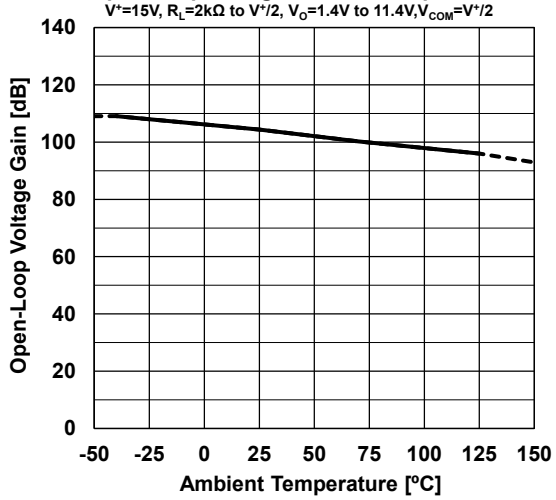


Input Bias Current vs. Temperature
V⁻=0V, V_{COM}=0V

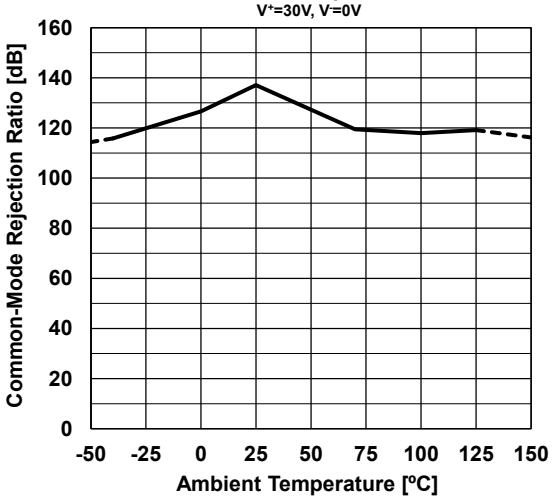


■TYPICAL CHARACTERISTICS

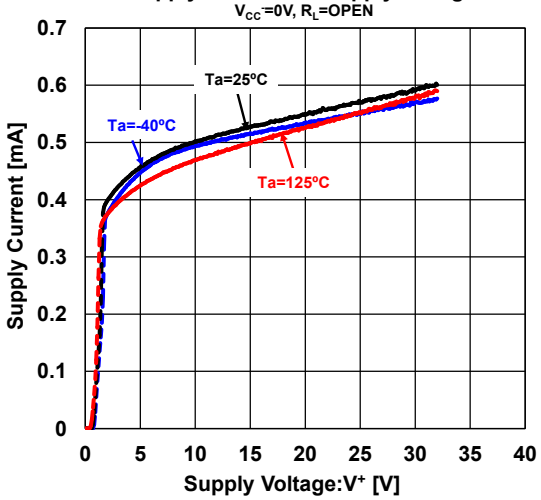
Open-Loop Voltage Gain vs. Temperature
V^+=15V, R_L=2kΩ to V^+/2, V_O=1.4V to 11.4V,V_{COM}=V^+/2



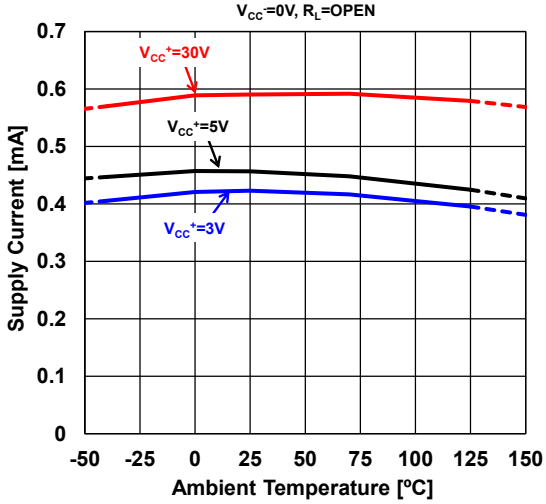
CMR vs. Temperature
V^+=30V, V^-=0V



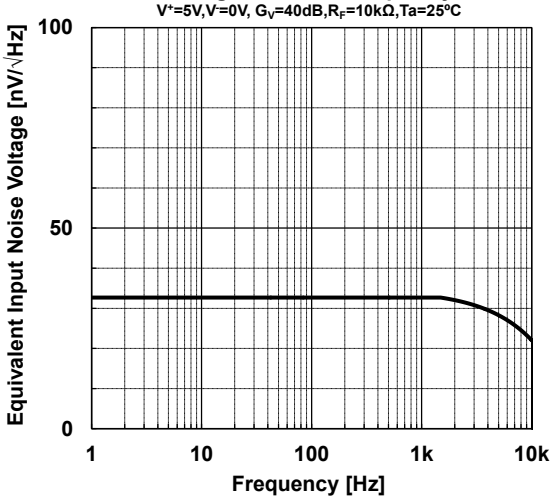
Supply Current vs. Supply Voltage
V_{CC}^-=0V, R_L=OPEN



Supply Current vs. Temperture
V_{CC}^-=0V, R_L=OPEN

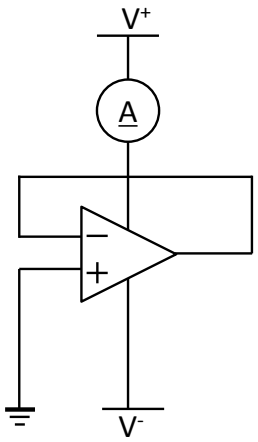


Voltage Noise vs. Frequency
V^+=5V,V^-=0V, G_V=40dB,R_F=10kΩ,Ta=25ºC



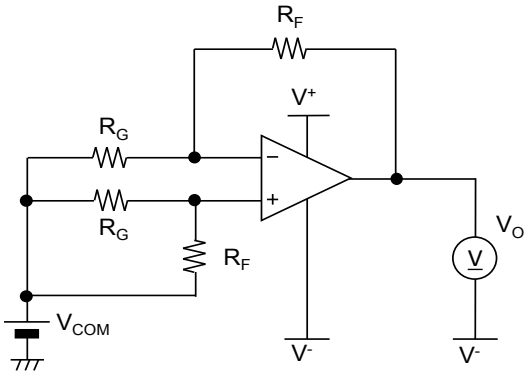
■TYPICAL TEST CIRCUIT

・Supply Current



・Input Offset Voltage

R_G=50Ω, R_F=50kΩ, $V_{IO}=\frac{R_G}{R_G+R_F}\times(V_O-V_{COM})$

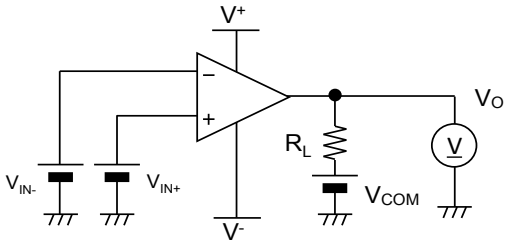


・High-level Output Voltage

$V_{COM}=V^+/2$, V_{IN+}=1V, V_{IN-}=0V, R_L=10kΩ

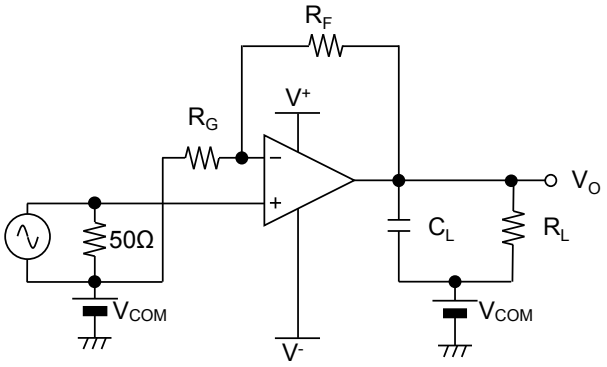
・Low-level Output Voltage

$V_{COM}=V^+/2$, V_{IN+}=0V, V_{IN-}=1V, R_L=10kΩ



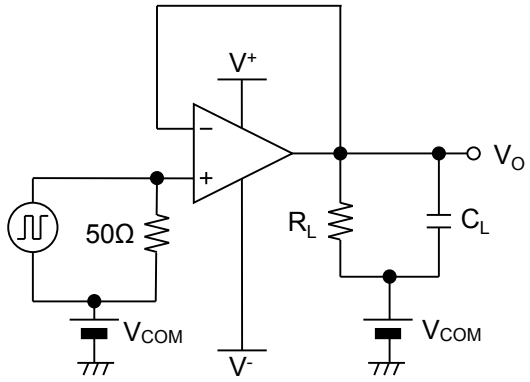
・Gain Bandwidth Product

$V_{COM}=V^+/2$, R_G=20Ω, R_F=2kΩ, R_L=2kΩ, C_L=100pF

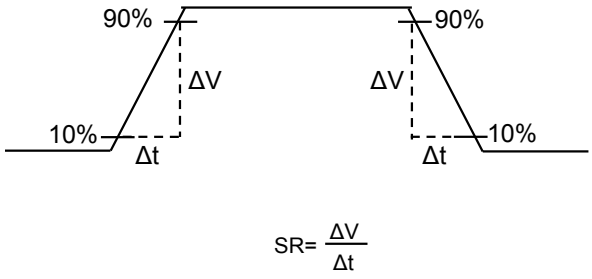


・Slew Rate

$V_{COM}=V^+/2$, R_L=2kΩ, C_L=100pF



Output Wave



$SR=\frac{\Delta V}{\Delta t}$

■APPLICATION NOTE

EMIRR(EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an Op-Amp. The definition of EMIRR is given by the following a formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.

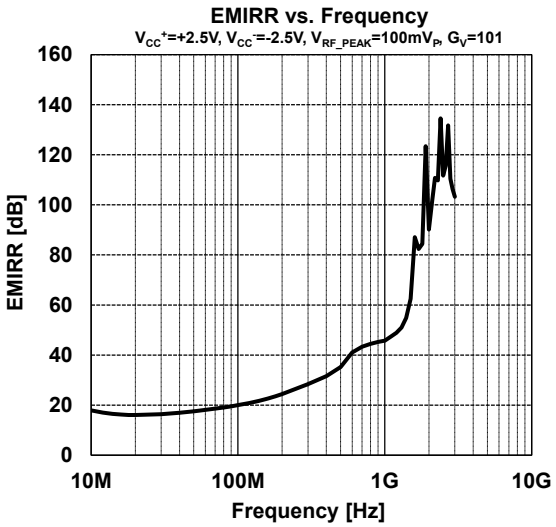
$$EMIRR = 20 \cdot \log\left(\frac{V_{RF\_PEAK}}{|\Delta V_{IO}|}\right) \quad \cdots(1)$$

V_{RF_PEAK} : RF Signal Amplitude [V_P]

ΔV_{IO} : Input offset voltage shift quantity [V]

Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

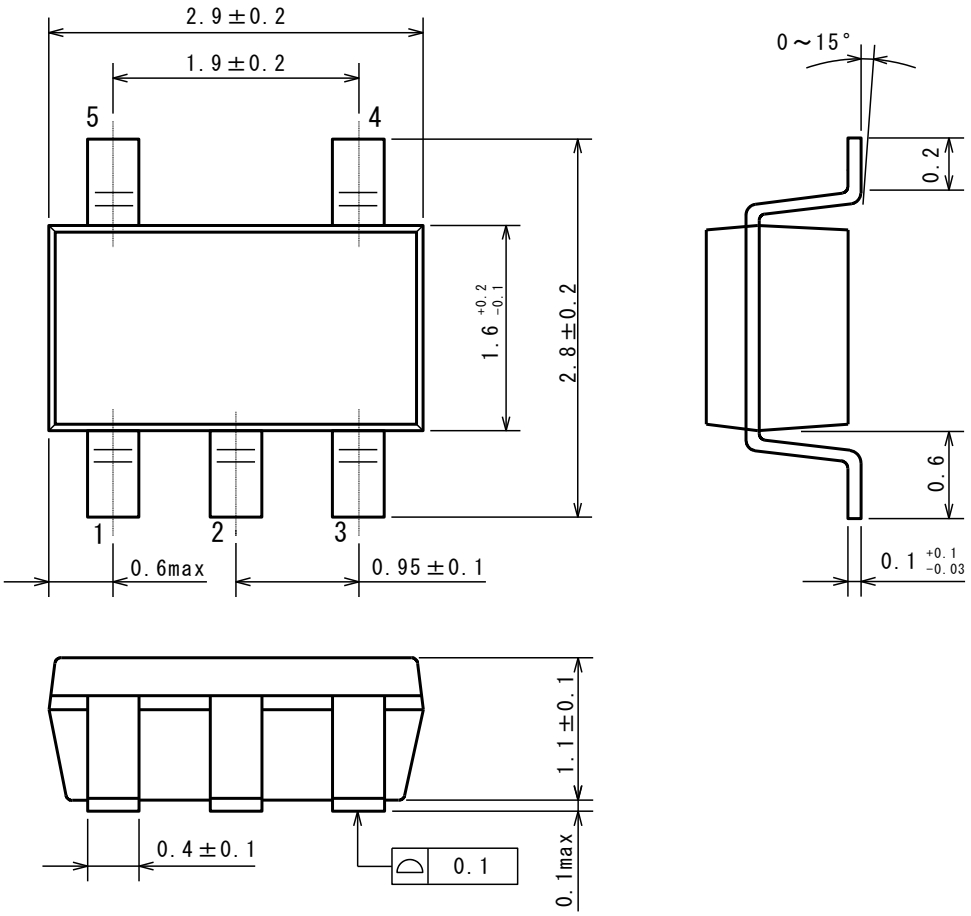
*For details, refer to " Application Note for EMI Immunity" in our HP: http://www.njr.com/



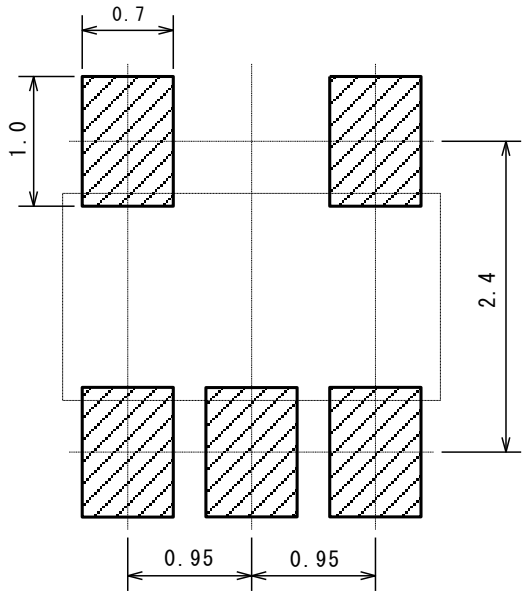
SOT-23-5

Unit: mm

■PACKAGE DIMENSIONS



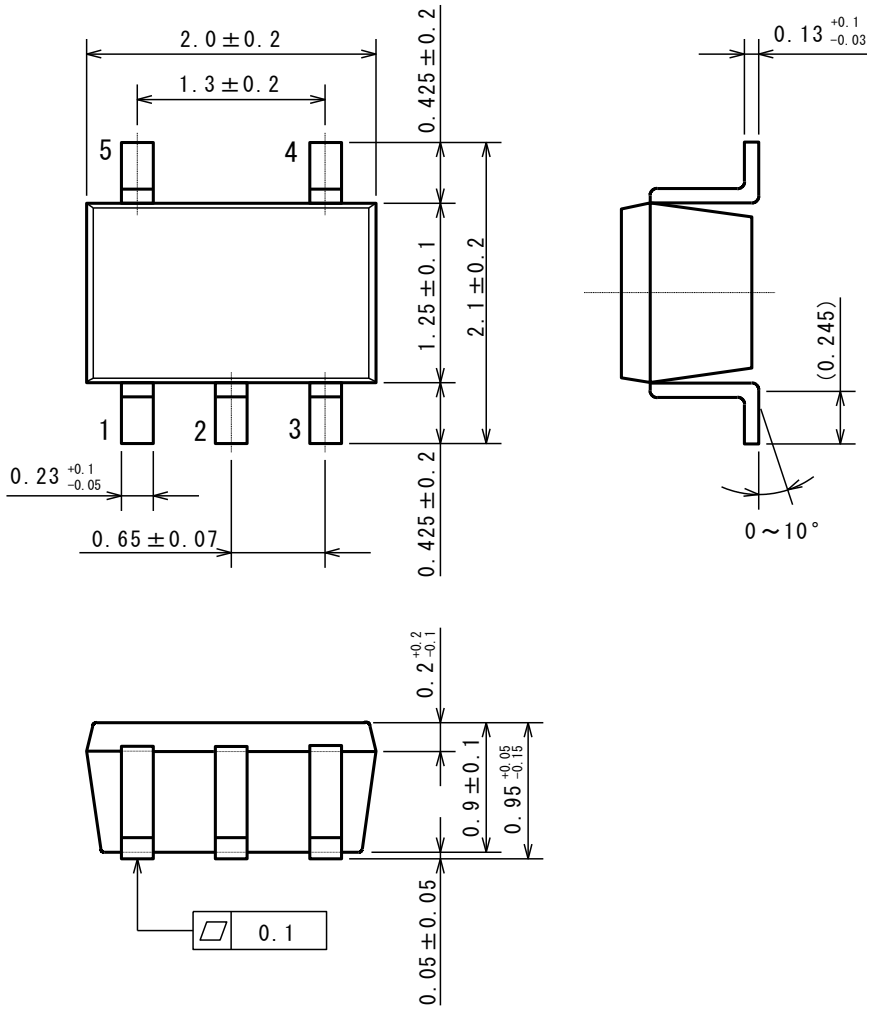
■EXAMPLE OF SOLDER PADS DIMENSIONS



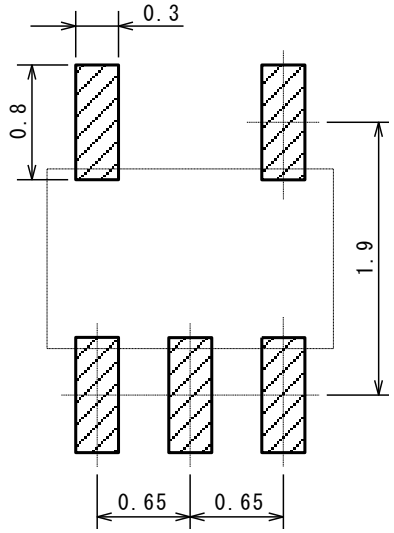
SC-88A

Unit: mm

■PACKAGE DIMENSIONS



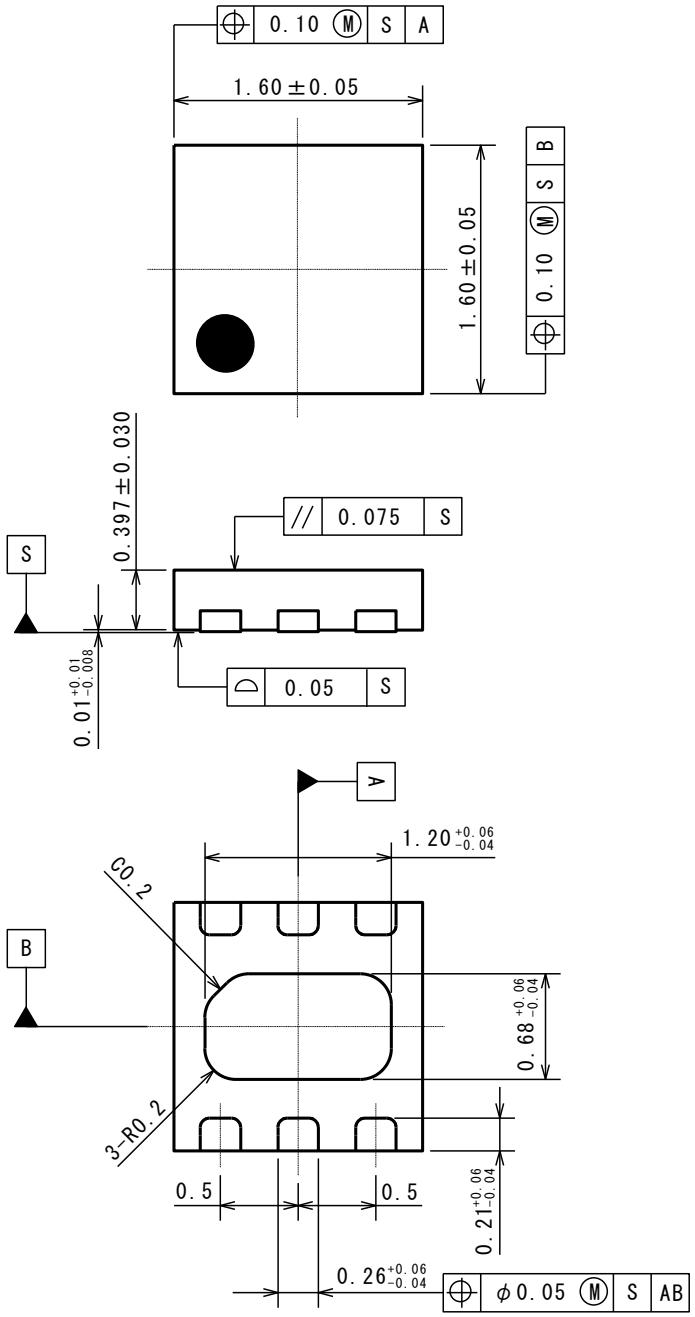
■ EXAMPLE OF SOLDER PADS DIMENSIONS



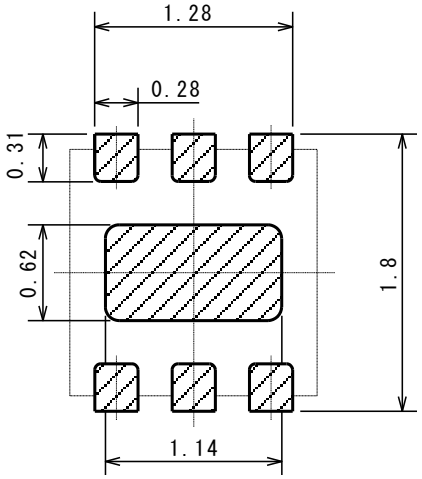
DFN6-G1(ESON6-G1)

Unit: mm

■PACKAGE DIMENSIONS



■EXAMPLE OF SOLDER PADS DIMENSIONS

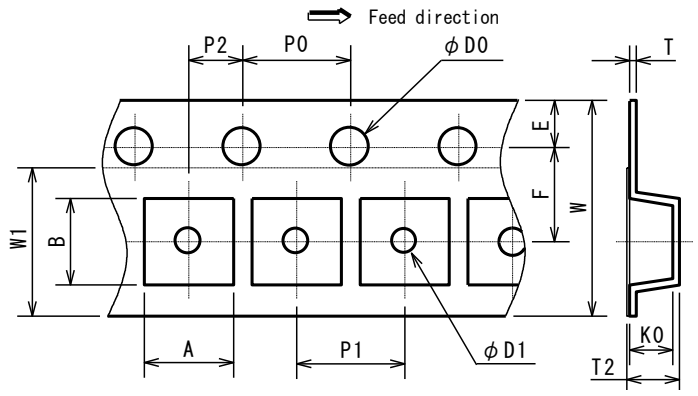


SOT-23-5

Unit: mm

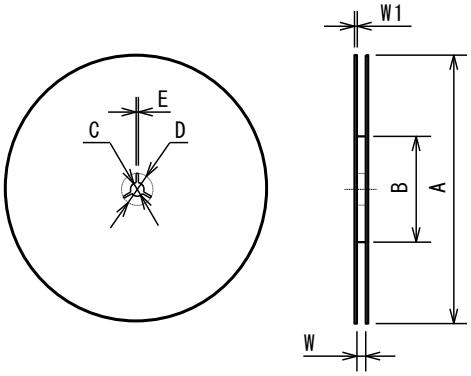
■ PACKING SPEC

TAPING DIMENSIONS



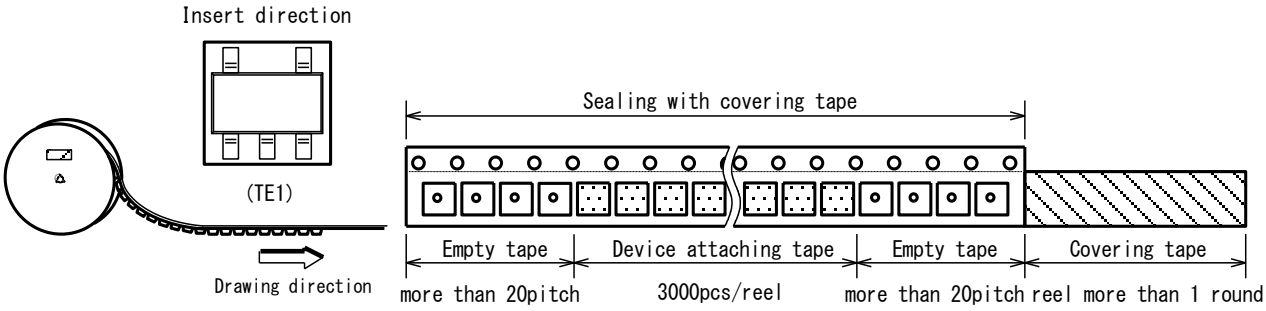
SYMBOL	DIMENSION	REMARKS
A	3.3±0.1	BOTTOM DIMENSION
B	3.2±0.1	BOTTOM DIMENSION
D0	1.55	
D1	1.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.82	
K0	1.5±0.1	
W	8.0±0.3	
W1	5.5	THICKNESS 0.1MAX

REEL DIMENSIONS

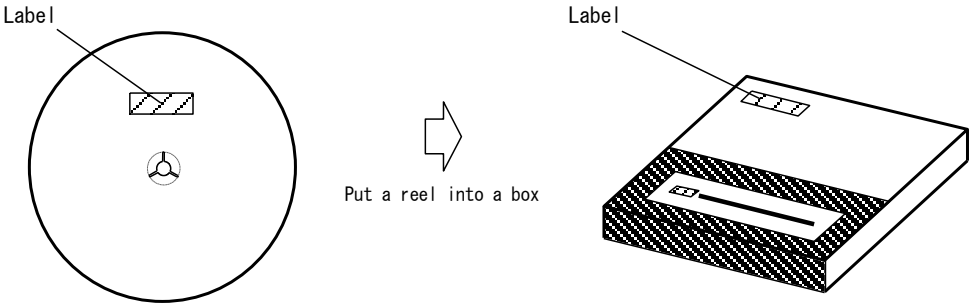


SYMBOL	DIMENSION
A	φ180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE



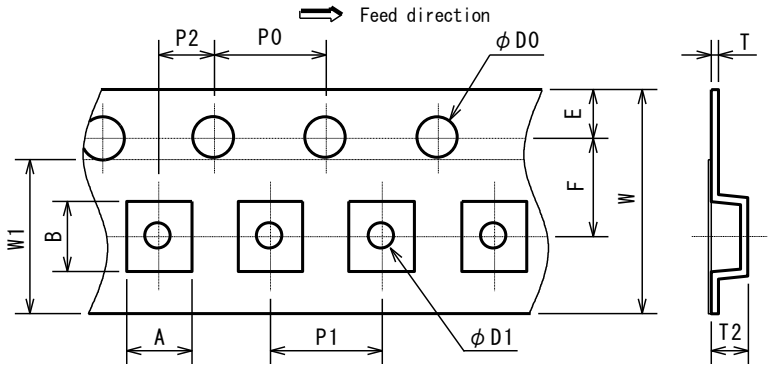
PACKING STATE



Unit: mm

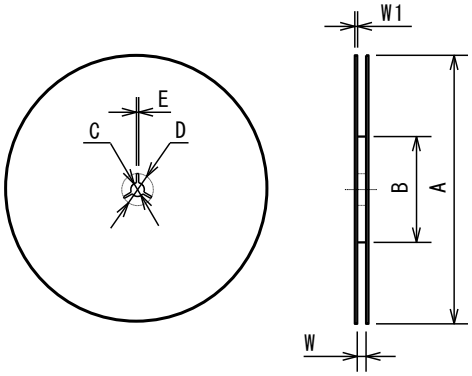
■ PACKING SPEC

TAPING DIMENSIONS



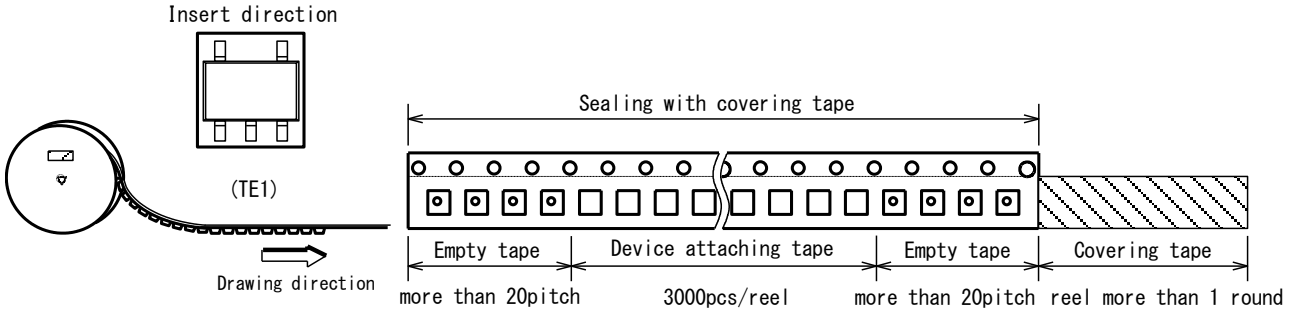
SYMBOL	DIMENSION	REMARKS
A	2.3±0.1	BOTTOM DIMENSION
B	2.5±0.1	BOTTOM DIMENSION
D0	1.55±0.05	
D1	1.05±0.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.3±0.1	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS



SYMBOL	DIMENSION
A	φ180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE



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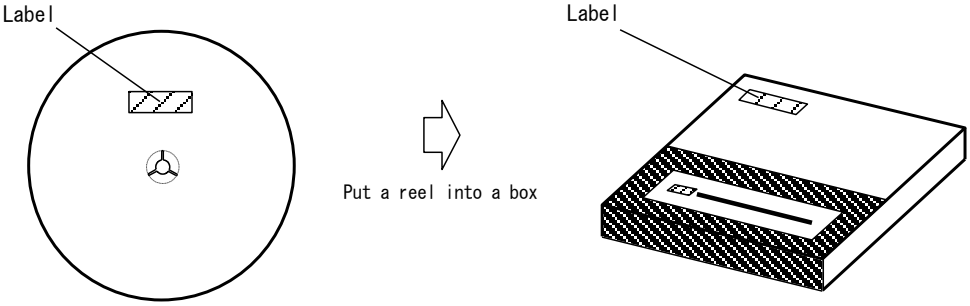
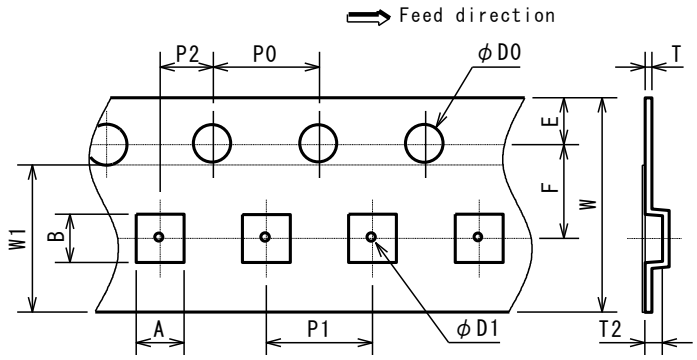


DFN6-G1(ESON6-G1)

■ PACKING SPEC

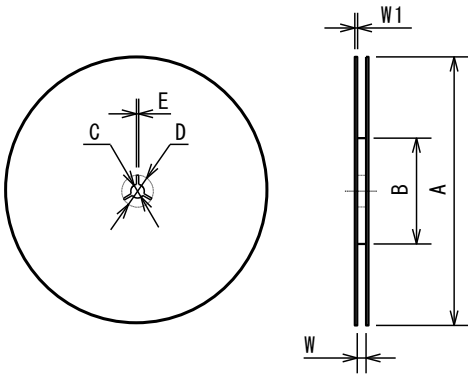
Unit: mm

TAPING DIMENSIONS



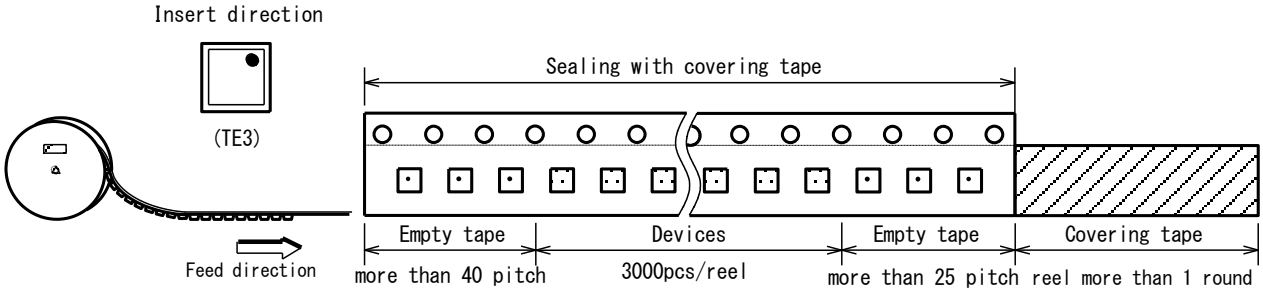
SYMBOL	DIMENSION	REMARKS
A	1.85±0.05	BOTTOM DIMENSION
B	1.85±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

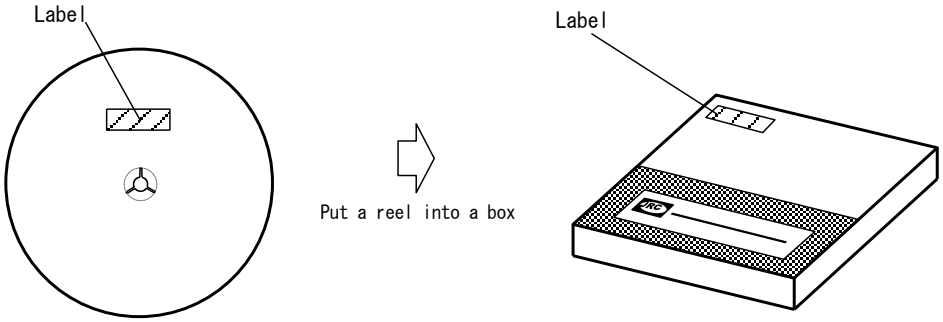


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	$9^{+0.3}_{0}$
W1	1.2

TAPING STATE

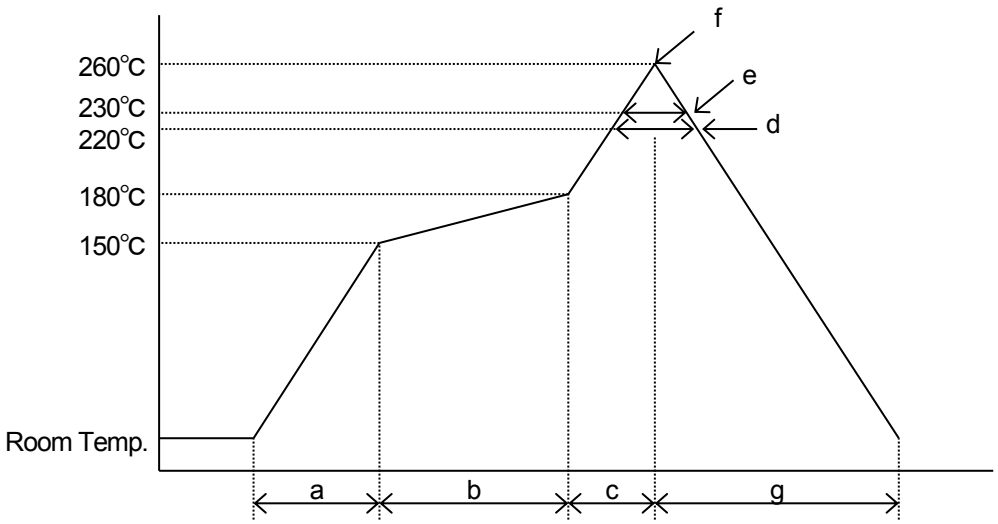


PACKING STATE



■RECOMMENDED MOUNTING METHOD

*Recommended reflow soldering procedure



a : Temperature ramping rate	: 1 to 4℃/s
b : Pre-heating temperature	: 150 to 180℃
time	: 60 to 120s
c : Temperature ramp rate	: 1 to 4℃/s
d : 220℃ or higher time	: Shorter than 60s
e : 230℃ or higher time	: Shorter than 40s
f : Peak temperature	: Lower than 260℃
g : Temperature ramping rate	: 1 to 6℃/s

*The temperature indicates at the surface of mold package.

■REVISION HISTORY

Date	Revision	Changes
1.NOV.2017	Ver.0	Initial Version

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   Vehicle Control Equipment (airplane, railroad, ship, etc.)
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