Digital Signal Processor for TV

■Package

■ General Description

The NJU26041-01A is a high performance 24-bit digital signal processor.

The NJU26041-01A provides 'eala' 3D Surround function, 'ealaBass' Dynamic Bass Boost function, Dialogue Boost, 3-bands 2-stages AGC, and Tone Control.

These kinds of sound functions are suitable for TV, mini-component, CD radio-cassette, speakers system and other audio products.

NJU26041V

■ FEATURES

- Software

- 3D sound : eala(NJRC Original Surround)
- Sound Enhancement: : ealaBass (NJRC Original Dynamic Bass Boost)
  : Dialogue Boost (NJRC Original Dialogue Boost)
- 3-bands 2-stages AGC
- Tone Control
- Master Volume / Balance control
- WatchDog Clock Output

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 1 Input port / 2 Output ports
- Digital Audio Format : I^2S 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode : Master Mode MCK 1/2 fclk, 1/3 fclk
  ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Power Supply : 3.3V
- Input terminal : 5V Input tolerant
- Package : SSOP32 (Pb-Free)
- Two kinds of micro computer interface : I^2C bus (standard-mode/100kbps, Fast-mode/400kbps)
  : Serial interface (4 lines: clock, enable, input data, output data)

The detail hardware specification is described in the " NJU26041 Series Hardware Data Sheet".

■ Function Block Diagram

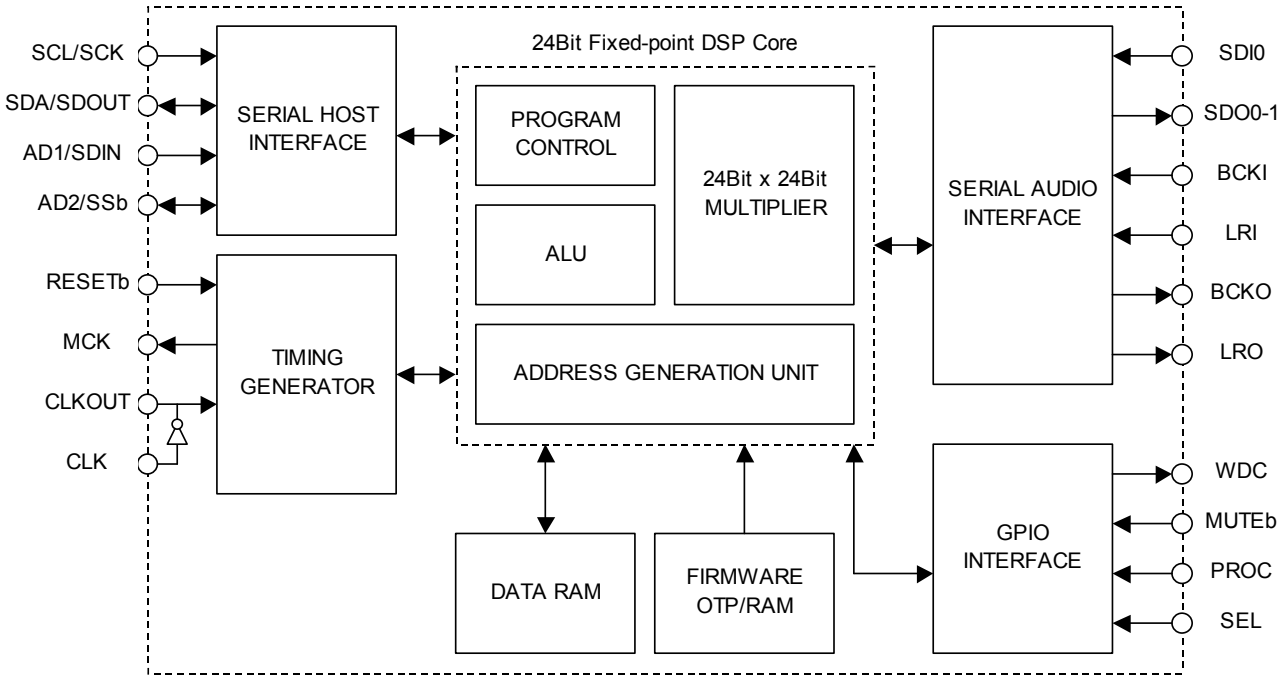


Fig. 1 NJU26041-01A Block Diagram

■ DSP Block Diagram

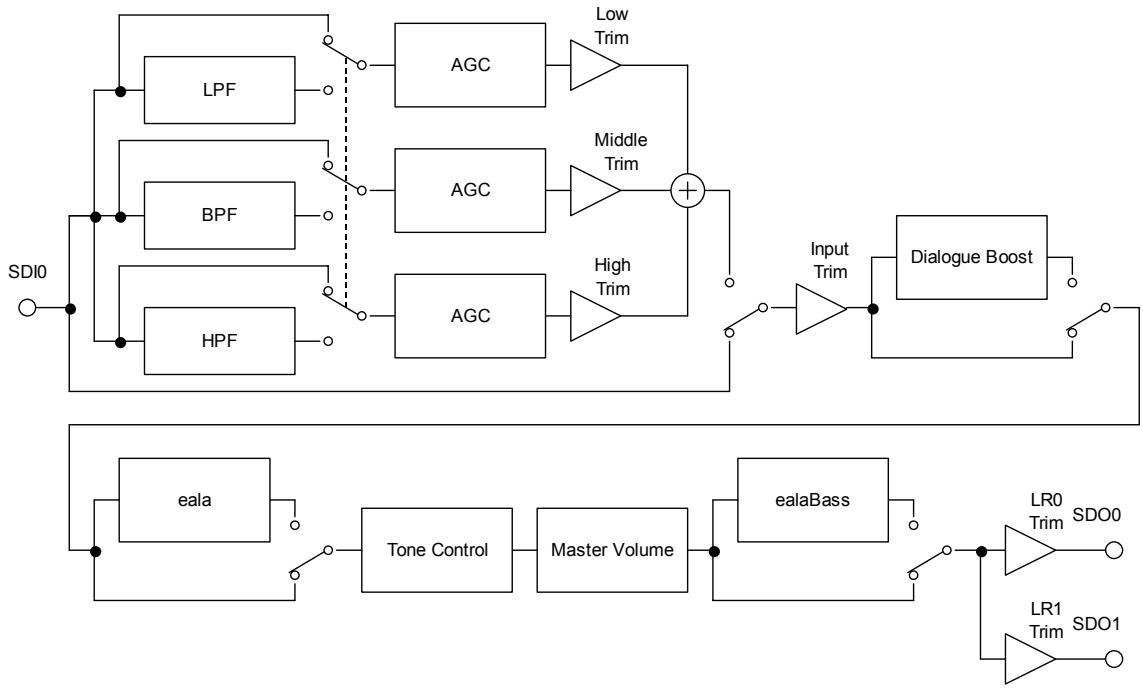


Fig. 2 NJU26041-01A Function Diagram

■ Pin Configuration

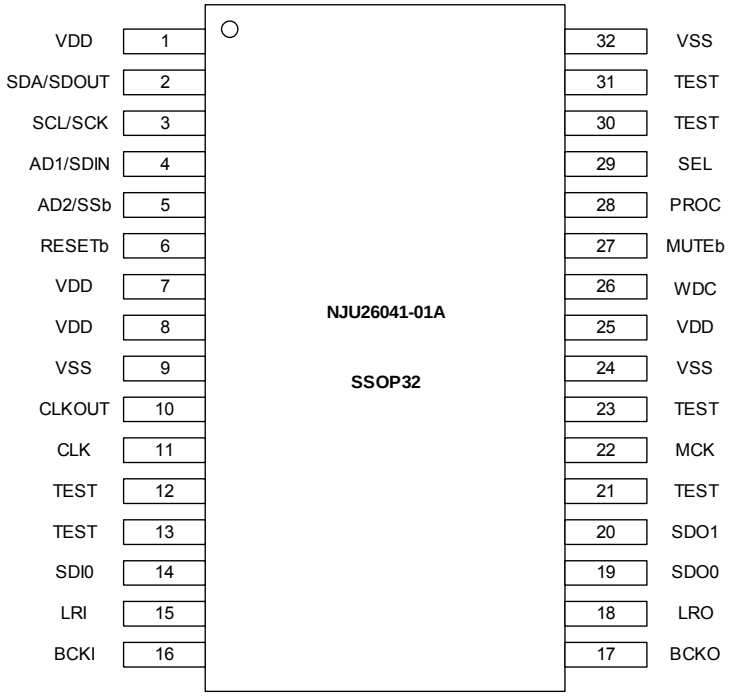


Fig. 3 NJU26041-01A Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Description
1, 7, 8, 25	VDD	-	Power Supply +3.3V
2	SDA / SDOUT	OD	I^2C I/O / 4-Wire Serial Output This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
3	SCL / SCK	I	I^2C Clock / Serial Clock
4	AD1 / SDIN	I	I^2C Address / Serial Input
5	AD2 / SSb	I	I^2C Address / Serial Enable
6	RESETb	I	Reset (RESETb='Low' : DSP Reset)
9, 24, 32	VSS	-	GND
10	CLKOUT	O	OSC Output
11	CLK	I	OSC Clock Input
12, 13	TEST	I	for Test (connected to VSS)
14	SDI0	I	Audio Data Input 0
15	LRI	I	LR Clock Input
16	BCKI	I	Bit Clock Input
17	BCKO	O	Bit Clock Output
18	LRO	O	LR Clock Output
19	SDO0	O	Audio Data Output 0
20	SDO1	O	Audio Data Output 1
21	TEST	O	for Test (Not connected : OPEN)
22	MCK	O	Master Clock Output for A/D, D/A
23, 30, 31	TEST	I -	for Test (connected to VSS)
26	WDC	I/O +	Clock for Watch Dog Timer (Open Drain Output)
27	MUTEb	I/O -	Master Volume level, After Reset DSP ("1" : 0dB "0" : Mute)
28	PROC	I/O -	After Reset DSP. ("1" : Normal "0" : Wait from Command)
29	SEL	I/O -	Select I^2C or Serial bus ('1' : Serial / '0' : I^2C-Bus)

Note : I : Input
I - : Input (Pull-down)
O : Output
OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
I/O+ : Bi-directional (with Pull-up resistance)
I/O - : Bi-directional (with Pull-down resistance)

■ Digital Audio Interface

The NJU26041-01A audio interface provides industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified. The NJU26041-01A audio interface provides one data input, SDI0 and two data outputs, SDO0, SDO1 as shown in table 2, table 3 and Fig.2. An audio interface input and output data format become the same data format.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description
14	SDI0	Audio Data Input 0 L / R

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0 L / R LPF/HPF
20	SDO1	Audio Data Output 1 L / R

■ Host Interface

The NJU26041-01A can be controlled via Serial Host Interface (SHI) using either of two serial bus formats: I^2C bus or 4-Wire serial bus.(Table 4) Data transfers are in 8 bit packets (1 byte) when using either format.
Serial Host Interface Pin Description.(Table 5)

Table 4 Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
29	SEL	"Low"	I^2C bus
		"High"	4-Wire serial bus

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus / Serial)	I^2C bus Format	4-Wire Serial bus Format
2	SDA / SDOUT *	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (Open-Drain Output)
3	SCL / SCK *	Serial Clock	Serial Clock
4	AD1 / SDIN *	I^2C bus address Bit1	Serial Data Input
5	AD2 / SSb *	I^2C bus address Bit2	Serial enable

Note : SDA /SDOUT pin is a bi-directional open drain.
This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
* When the power supply (V_{DD}= +3.3V) is supplied to NJU26041, these pins become +5.0V Input tolerant.

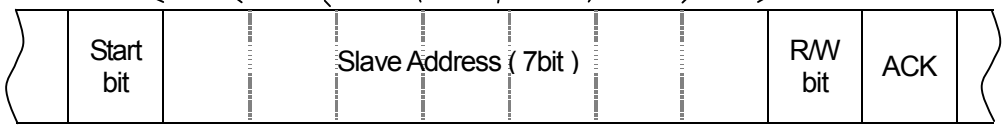
■ I²C bus

When the NJU26041-01A is configured for I²C bus communication during the Reset initialization sequence. I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26041-01A. An address can be arbitrarily set up by the AD1 and AD2 pins. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

Table 6 I²C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is “Low”. SLAVE address is 1 when AD1/2 is “High”.

* SLAVE address is 0 when R/W is “W”. SLAVE address is 1 when R/W is “R”.

Note : The serial host interface supports “Standard-Mode (100kbps)” and “Fast-Mode (400kbps)” I²C bus data transfer.

The NJU26041-01A can transmit multiple-bytes (I²C address -> Command -> Parameter1 -> Parameter2).

The end of the transmission must end by “P (stop)”.

■ 4-Wire Serial Interface

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb=0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = “High”. SDOUT is Open-drain output in case of SSb = “Low”. SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

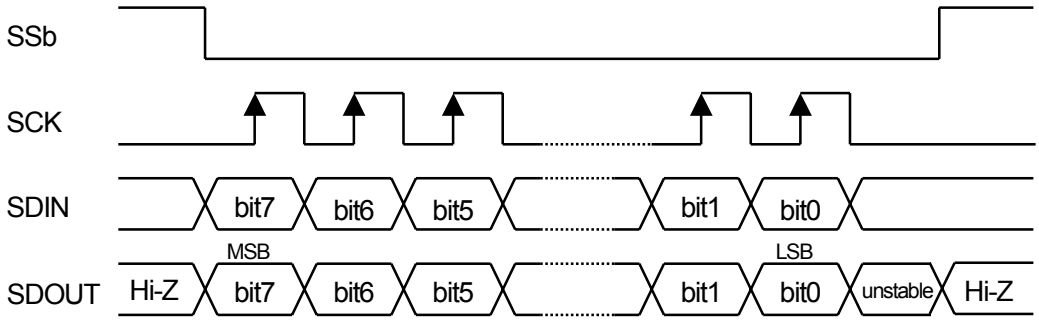


Fig. 4 4-Wire Serial Interface Timing

Note: When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb=”High”. When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes “High”.

■ Pin setting

The NJU26041-01A operates default command setting after resetting the NJU26041-01A. In addition, the NJU26041-01A restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No.	Symbol	Setting	Function
28	PROC	"High"	The NJU26041-01A operates default setting after reset.
		"Low"	The NJU26041-01A does not operate after reset. Sending start command is required for starting operation.
27	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26041-01A outputs clock pulse through WDC (No.26) pin during normal operation. (Table 8)

Table8 WatchDog Clock Output Cycle

WDC Output Cycle (Low/High) Time
100msec

The NJU26041-01A generates a clock pulse through the WDC terminal after resetting the NJU26041-01A. The WDC clock is useful to check the status of the NJU26041-01A operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26041-01A. When the WDC clock pulse is lost or not normal clock cycle, the NJU26041-01A does not operate correctly. Then reset the NJU26041-01A and set up the NJU26041-01A again.

Note: If input and output of an audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.

■ NJU26041-01A Command Table

Table 9 NJU26041-01A Command

No.	Command
1	System State
2	Firmware mode select
3	SW select
4	Master Volume Smooth Control
5	Master Volume Setup
6	Master Volume Balance
7	AGC Start Level
8	AGC Threshold Level
9	AGC Boost Trim
10	AGC Ratio
11	AGC Output Trim
12	AGC Attack Time / Release Time
13	AGC Low Frequency
14	AGC Middle-Low Frequency
15	AGC Middle-High Frequency
16	AGC High Frequency
17	Input Trim

No.	Command
18	Dialogue Boost
19	Tone Control Bass Gain
20	Tone Control Treble Gain
21	L0/R0 Channel Trim
22	L1/R1 Channel Trim
23	eala Surround Gain
24	ealaBass LPF fc
25	ealaBass LPF Gain
26	ealaBass Treble fc
27	ealaBassTreble Gain
28	ealaBass Output Gain
29	ealaBass Attack Time / Release Time
30	Version No. Request
31	Revision No. Request
32	Start Command
33	No Operation

Notes : In respect to detail command information, request New Japan Radio Co., Ltd.

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