



## Digital Signal Processor for TV

### ■ Package


**NJU26107FR1**

### ■ General Description

The NJU26107 is a high performance 24-bit digital signal processor.

The NJU26107 provides 'eala' 3D Surround function, 'eala BASS' Dynamic Bass Boost function, SRS 3D, TruBass, AGC, Tone Control, and LPF/HPF. These kinds of sound functions are suitable for TV, mini-component, CD radio-cassette, speakers system and other audio products.

### ■ FEATURES

#### - Software

- 3D sound : eala(NJRC Original Surround), SRS 3D
- Sound Enhancement: : ealaBASS (NJRC Original Dynamic Bass Boost), SRS TruBass
- AGC
- Tone Control
- Master Volume / Balance control
- LPF/HPF crossover network
- WatchDog Clock Output

#### - Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 2 Input ports / 3 Output ports
- Digital Audio Format : I<sup>2</sup>S 24bit, Left- justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode : Master Mode MCK 1/2 fclk, 1/3 fclk  
ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Power Supply : 2.5V
- Input terminal : 3.3V Input tolerant
- Package : QFP32-R1 (Pb-Free)
- Two kinds of micro computer interface : I<sup>2</sup>C bus (standard-mode/100kbps)  
: Serial interface (4 lines: clock, enable, input data, output data)

The detail hardware specification is described in the "NJU26100 Series Hardware Data Sheet".

## Function Block Diagram

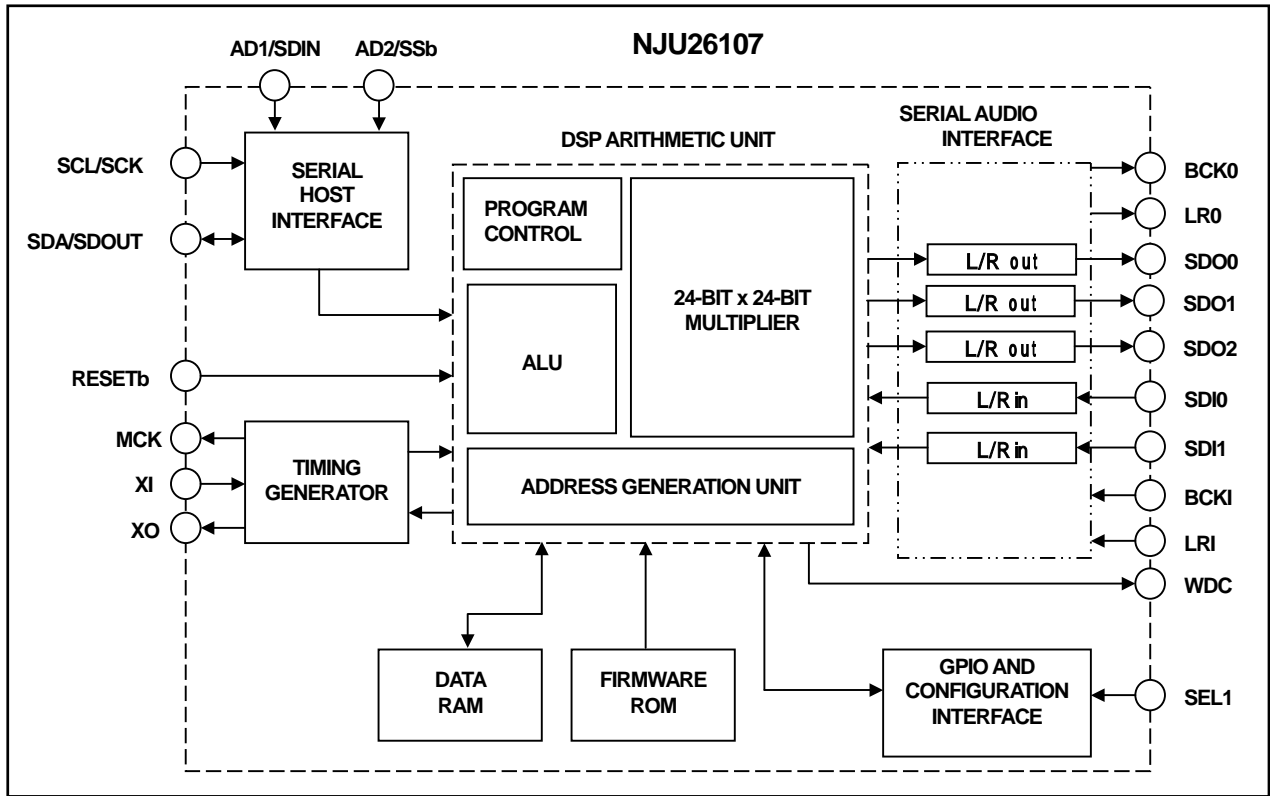


Fig. 1 NJU26107 Block Diagram

## DSP Block Diagram

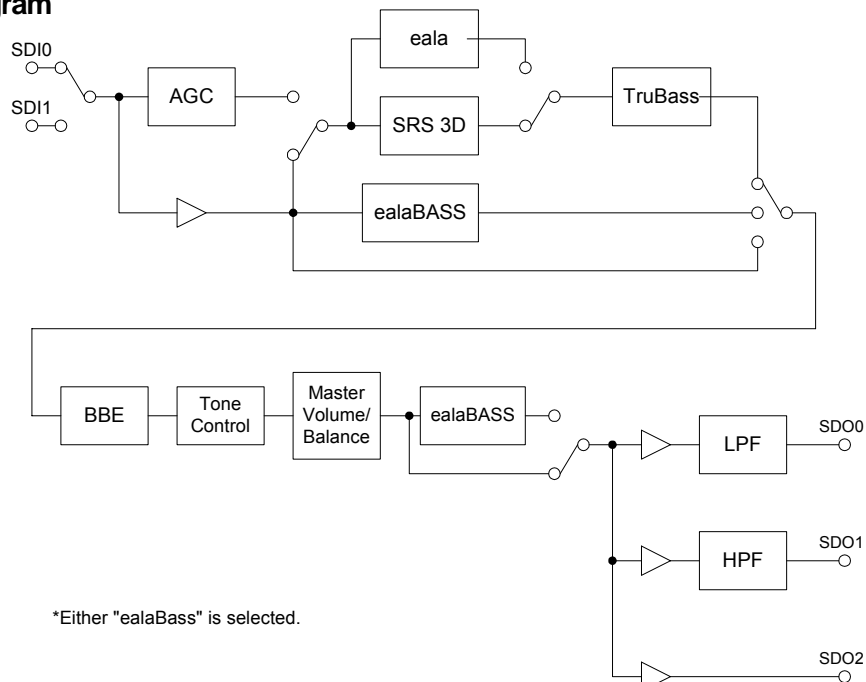
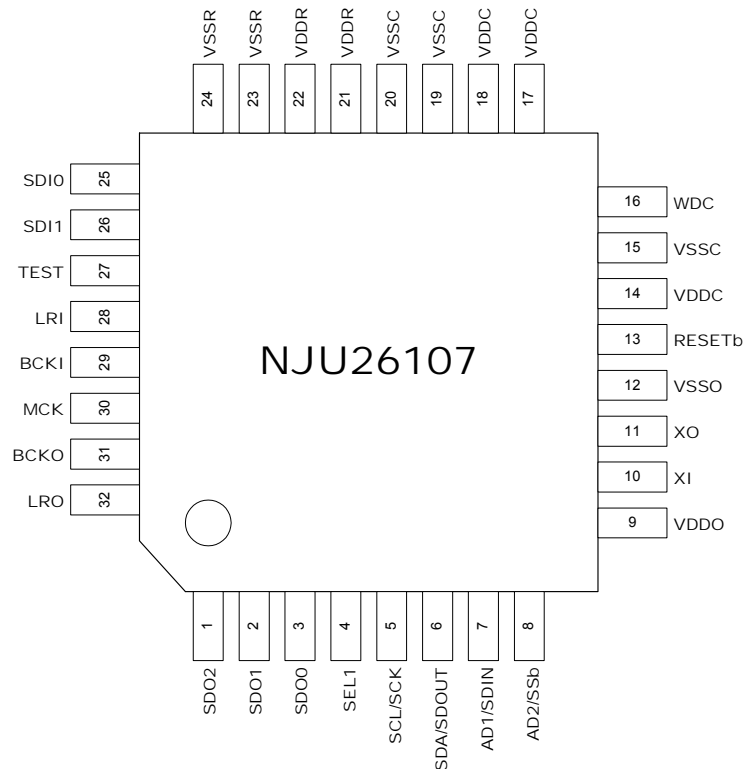


Fig. 2 NJU26107Function Diagram

## ■ Pin Configuration



**Fig. 3 NJU26107 Pin Configuration**

## ■ Pin Description

**Table 1 Pin Description**

No.	Symbol	I/O	Description	No.	Symbol	I/O	Description
1	SDO2	O	Audio Data Output 2 L/R	17	VDDC	--	Core Power Supply +2.5V
2	SDO1	O	Audio Data Output 1 L/R HPF	18	VDDC	--	Core Power Supply +2.5V
3	SDO0	O	Audio Data Output 0 L/R LPF	19	VSSC	--	Core GND
4	SEL1 *1	I	Select I <sup>2</sup> C or Serial bus	20	VSSC	--	Core GND
5	SCL/SCK	I	I <sup>2</sup> C Clock / Serial Clock	21	VDDR	--	I/O Power Supply +2.5V
6	SDA/SDOUT	I/O	I <sup>2</sup> C I/O / Serial Output This pin requires a pull-up resistance.	22	VDDR	--	I/O Power Supply +2.5V
7	AD1/SDIN	I	I <sup>2</sup> C Address / Serial Input	23	VSSR	--	I/O GND
8	AD2/SSb	I	I <sup>2</sup> C Address / Serial Enable	24	VSSR	--	I/O GND
9	VDDO	--	OSC Power Supply +2.5V	25	SDI0	I	Audio Data Input 0 L/R
10	XI	I	X'tal Clock Input	26	SDI1	I	Audio Data Input 1 L/R
11	XO	O	OSC Output	27	TEST	I	Connect to GND
12	VSSO	--	OSC GND	28	LRI	I	LR Clock Input
13	RESETb	I	RESET (active Low)	29	BCKI	I	Bit Clock Input
14	VDDC	--	Core Power Supply +2.5V	30	MCK	O	Master Clock Output
15	VSSC	--	Core GND	31	BCKO	O	Bit Clock Output
16	WDC *2	O	Clock for Watch Dog Timer	32	LRO	O	LR Clock Output

- \* I : Input,
- O : Output,
- I/O: Bi-directional
- \*1 SEL1 : Input
- \*2 WDC : Output

## ■ Digital Audio Interface

The NJU26107 audio interface provides industry standard serial data formats of I<sup>2</sup>S, MSB-first left-justified or MSB-first right-justified. The NJU26107 audio interface provides two data inputs, SDI0, SDI1 and three data outputs, SDO0, SDO1, SDO2 as shown in table 2, table 3 and Fig.2. An audio interface input and output data format become the same data format.

**Table 2 Serial Audio Input Pin**

Pin No.	Symbol	Description
25	SDI0	Audio Data Input 0 L / R
26	SDI1	Audio Data Input 1 L / R

**Table 3 Serial Audio Output Pin**

Pin No.	Symbol	Description
3	SDO0	Audio Data Output 0 L / R LPF
2	SDO1	Audio Data Output 1 L / R HPF
1	SDO2	Audio Data Output 2 L / R

## ■ Host Interface

The NJU26107 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I<sup>2</sup>C bus.(Table 4) Data transfers are in 8 bit packets (1 byte) when using either format. Serial Host Interface Pin Description.(Table 5)

**Table 4 Serial Host Interface Pin Description**

Pin No.	Symbol	Setting	Host Interface
4	SEL1	"Low"	I <sup>2</sup> C bus
		"High"	4-Wire serial bus

**Table 5 Serial Host Interface Pin Description**

Pin No.	Symbol (I <sup>2</sup> C bus / Serial)	I <sup>2</sup> C bus Format	4-Wire Serial bus Format
5	SCL / SCK	Serial Clock	Serial Clock
6	SDA / SDOUT	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (CMOS)
7	AD1 / SDIN	I <sup>2</sup> C bus address Bit1	Serial Data Input
8	AD2 / SSb	I <sup>2</sup> C bus address Bit2	Serial enable

**Note :** SDA/SDOUT pin is a bi-directional open drain.

SDA/SDOUT output is normal CMOS output in case of 4-Wire Serial bus mode and SSb="Low".

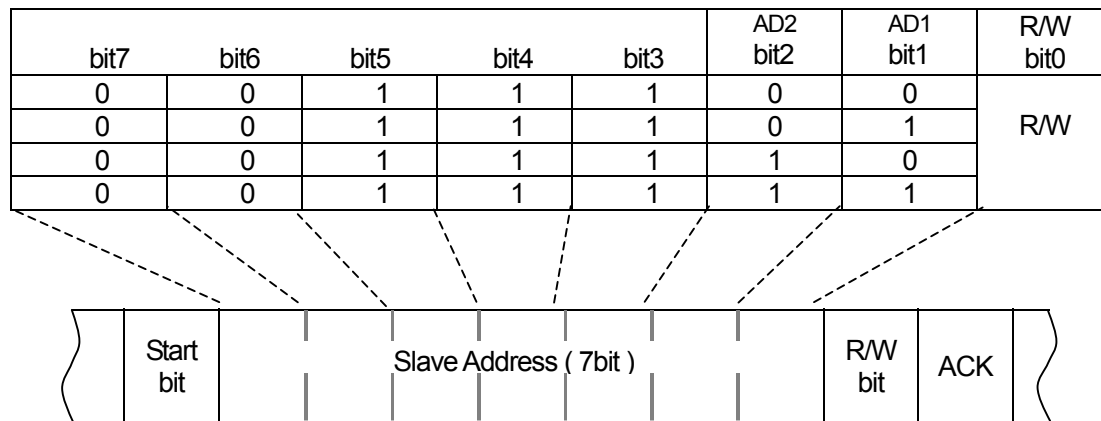
SDA /SDOUT output is Hi-Z state in case of 4-Wire Serial bus mode and SSb="High". This pin requires a pull-up resistor in both 4-Wire serial and I<sup>2</sup>C bus mode.

## ■ I<sup>2</sup>C bus

When the NJU26107 is configured for I<sup>2</sup>C bus communication during the Reset initialization sequence. I<sup>2</sup>C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26107. An address can be arbitrarily set up by the AD1 and AD2 pins. The I<sup>2</sup>C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

**Table 6 I<sup>2</sup>C bus SLAVE Address**



\* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

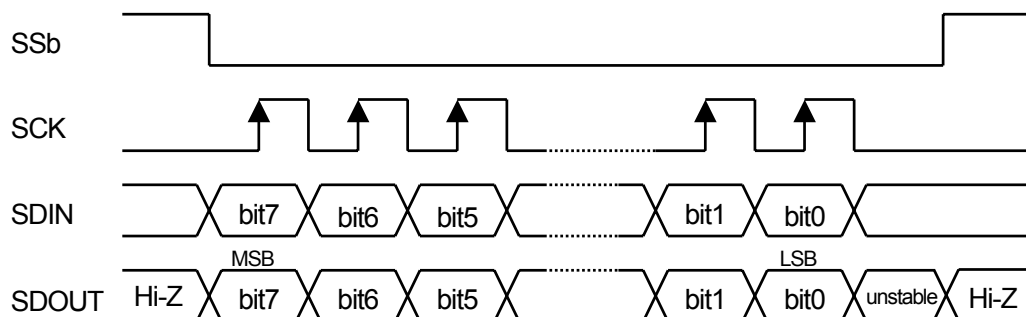
**Note :** In case of the NJU26107 only single-byte transmission is available. The serial host interface supports "Standard-Mode (100kbps)" I<sup>2</sup>C bus data transfer.

## ■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1 pin ="High" during the Reset initialization sequence.

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low ( SSb=0 ). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = "High". SDOUT is CMOS output in case of SSb = "Low". SDOUT needs a pull-up resistor when SDOUT is Hi-Z.



**Fig. 4 4-Wire Serial Interface Timing**

**Note:** When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High". When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High". SDOUT is Hi-Z in case of SSb = "High". SDOUT is CMOS output in case of SSb = "Low". SDOUT needs a pull-up resistor to prevent SDOUT from becoming floating level.

## ■ WatchDog Clock

The NJU26107 outputs clock pulse through WDC (No.16) pin during normal operation. (Table 7)

**Table7 WatchDog Clock Output Cycle**

WDC Output Cycle (Low/High) Time
100ms

The NJU26107 generates a clock pulse through the WDC terminal after resetting the NJU26107. The WDC clock is useful to check the status of the NJU26107 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26107. When the WDC clock pulse is lost or not normal clock cycle, the NJU26107 does not operate correctly. Then reset the NJU26107 and set up the NJU26107 again.

**Note:** If input and output of a audio signal stop and an audio interface stops, WDC can't output.  
That is because it has controlled based on the signal of an audio interface.


## ■ NJU26107 Command Table

**Table 8 NJU26107 Command**

No.	Command	No.	Command
1	System State	23	BBE Contour
2	Firmware mode select	24	BBE Process
3	SW select	25	Tone Control Bass Gain
4	Fs Select / Input Select	26	Tone Control Treble Gain
5	AGC Threshold Level	27	Master Volume Smooth Control
6	AGC Noise Compressor Threshold Level	28	Master Volume Setup
7	AGC Attack Time / Release Time	29	Master Volume Balance
8	AGC Ratio	30	LPF order mode
9	AGC Output Trim	31	LPF1 f0
10	AGC BYPASS Trim	32	LPF2 f0
11	eala Surround Gain	33	HPF order mode
12	SRS 3D Stereo Center Gain	34	HPF f0
13	SRS 3D Stereo Space Gain	35	L0/R0 Channel Trim
14	ealaBass LPF fo	36	L1/R1 Channel Trim
15	ealaBass LPF Gain	37	L2/R2 Channel Trim
16	ealaBass Treble fo	38	Version No. Request
17	ealaBass Treble Gain	39	Revision No. Request
18	ealaBass Output Trim	40	AGC Input Level Request
19	eala Bass Attack Time / Release Time	41	AGC Gain Reduction Level Request
20	SRS TruBass Speaker Size	42	Start Command
21	SRS TruBass Punch Control	43	No Operation
22	SRS TruBass Bass Control		

**Notes :** In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs. Inc. and BBE Sound, Inc.) is required.

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