Digital Signal Processor for Car Audio

■ General Description

The NJU26202 is a digital signal processor that provides the function of Circle Surround Automotive, Hall Simulator, 7Band PEQ / GEQ, and Time Alignment. The applications of NJU26202 are suitable for multi-channel products such as Car Audio small speakers system.

■Package

NJU26202FR3

■ Features

-Software

- SRS Circle Surround Automotive
- TruBass
- FOCUS
- Hall Simulator
- 7Band PEQ / GEQ
- Time Alignment
- Sampling Frequency
  - 16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz (Stereo Input Mode and Multi Input Mode)
  - 32kHz/44.1kHz/48kHz (CS Auto Mode)

-Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 3 Output ports
- Digital Audio Format : I^2S 24bit, left-justified, right-justified, BCK : 32fs/64fs
- Master / Slave Mode
- Microcomputer Interface
  - I^2C Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  - 4 -Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Operating Voltage : V_{DD} = V_{DDPLL} = 1.8V
  : V_{DDIO} = 3.3V
- Input Terminal : 5.0V Input tolerant
- Package : LQFP48-R3 (Pb-Free)

* The detail hardware specification of the NJU26202 is described in the " NJU26200 Series Hardware Data Sheet".

■ Block Diagram

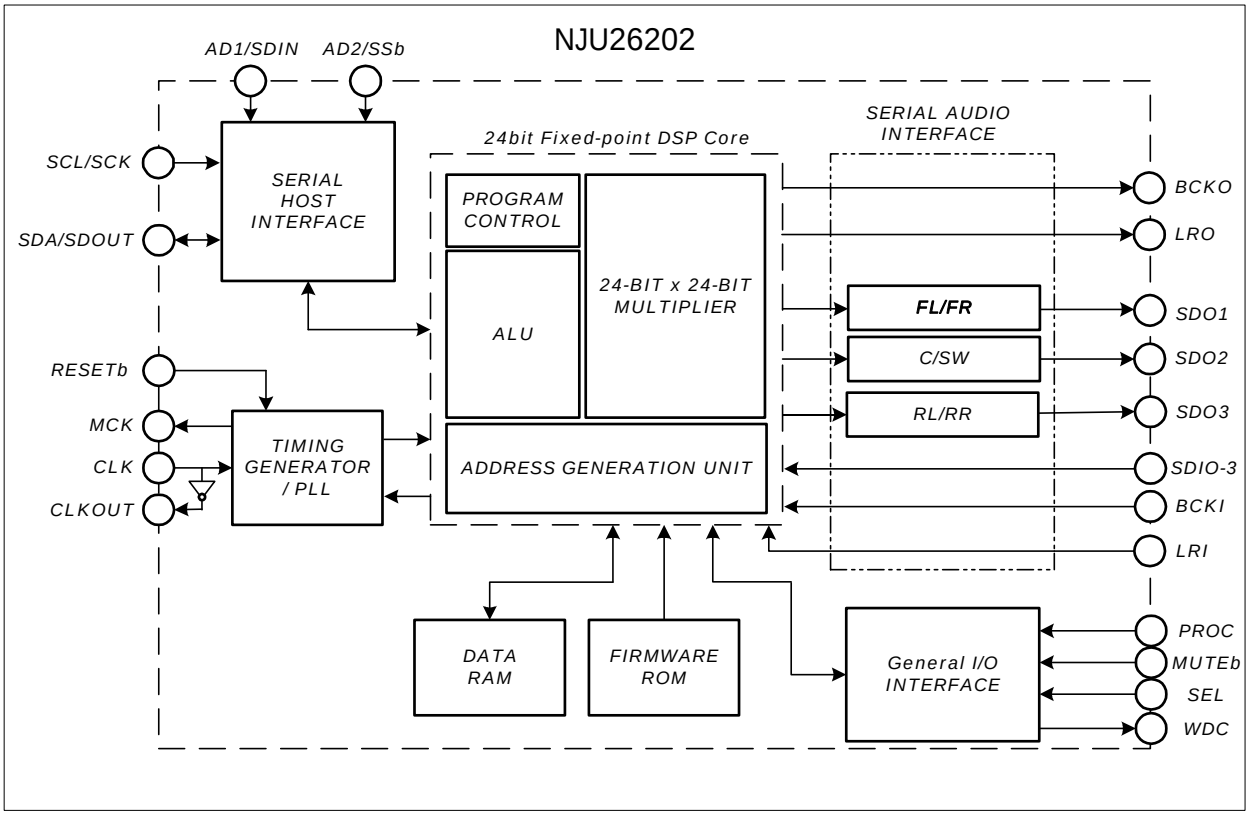
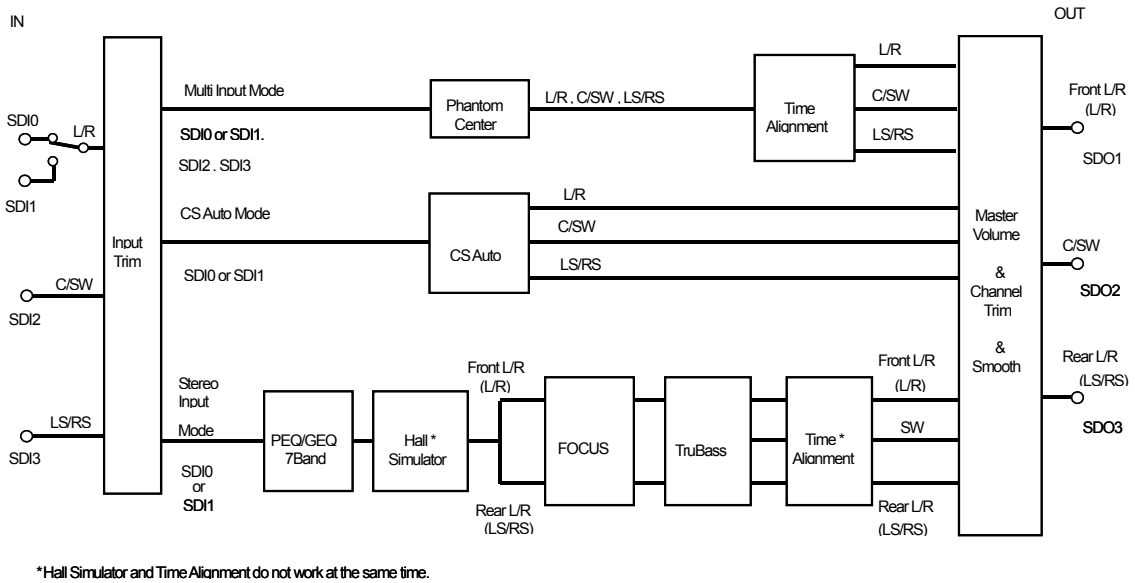


Fig. 1 NJU26202 Hardware Block Diagram

■ Function Block Diagram



*Hall Simulator and Time Alignment do not work at the same time.

Fig. 2 NJU26202 Block Diagram

■ Pin Configuration

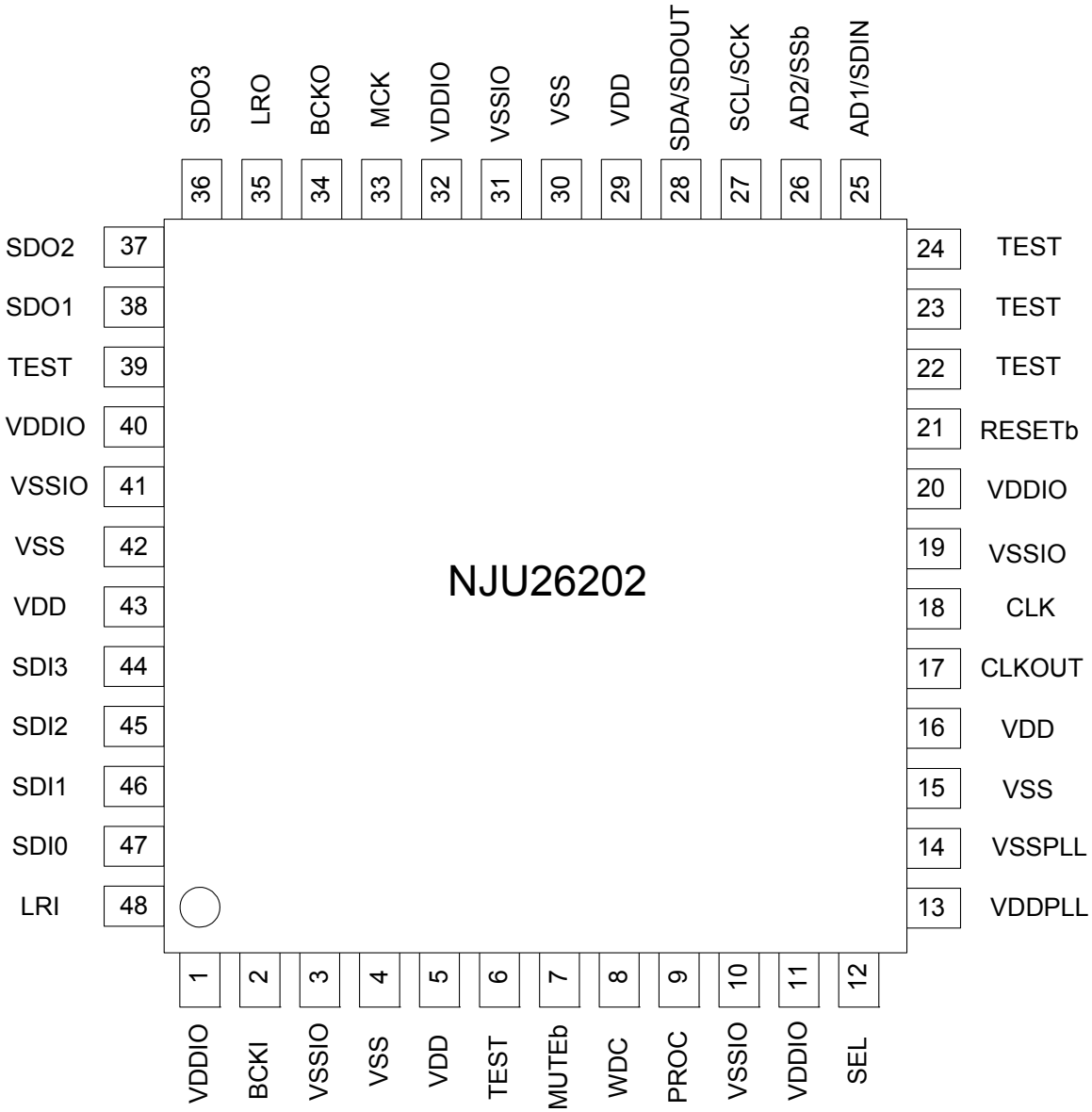


Fig. 3 NJU26202 Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Function
1,11,20,32,40	VDDIO	-	I/O Power Supply +3.3V
2	BCKI	I	Bit Clock Input
3,10,19,31,41	VSSIO	-	I/O GND
4,15,30,42	VSS	-	Core GND
5,16,29,43	VDD	-	Core Power Supply +1.8V
6	TEST	I	for test (connected to VSSIO through 3.3kΩ resistance.)
7	MUTEb *	I	Master Volume level, After Reset DSP ("1" : 0dB "0" : Mute)
8	WDC *	OD	Clock for Watch Dog Timer (Open Drain Output)
9	PROC *	I	After Reset DSP. ("1" : Normal "0" : Wait from Command)
12	SEL	I	Select I^2C or Serial bus ('1' : Serial / '0' : I^2C-Bus)
13	VDDPLL	-	PLL Analog Power Supply +1.8V
14	VSSPLL	-	PLL Analog GND
17	CLKOUT	O	OSC Output
18	CLK	I	X'tal Clock Input (12.288MHz)
21	RESETb	I	Reset (RESETb='0' : DSP Reset)
22	TEST	I	for Test (Connect to VDDIO)
23,24	TEST	I	for Test (Connect to VSSIO)
25	AD1/SDIN	I	I^2C Address / Serial Input
26	AD2/SSb	I	I^2C Address / Serial Enable
27	SCL/SCK	I	I^2C Clock / Serial Clock
28	SDA/SDOUT	I/O	I^2C I/O (Open Drain output) / Serial Output (CMOS output) I^2C Bus mode : SDA pin requires a pull-up resistance. 4-wire Serial mode : SDOUT does not require a pull-up resistance.
33	MCK	O	Master Clock Output (CLK Terminal=27pin Buffer Out)
34	BCKO	O	Bit Clock Output
35	LRO	O	LR Clock Output
36	SDO3	O	Audio Data Output 3 (Rear Lch / Rch)
37	SDO2	O	Audio Data Output 2 (Center / Subwoofer)
38	SDO1	O	Audio Data Output 1 (Front Lch / Rch)
39	TEST	O	for Test (No connect : OPEN)
44	SDI3	I	Audio Data Input 3 (SL / SR)
45	SDI2	I	Audio Data Input 2 (Center / Subwoofer)
46	SDI1	I	Audio Data Input 1 (Front Lch / Rch)
47	SDI0	I	Audio Data Input 0 (Front Lch / Rch)
48	LRI	I	LR Clock Input

Note : I : Input
O : Output
OD : Open Drain Output
I/O : Bi-directional
Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance

■ Audio Interface

The NJU26202 audio interface provides industry serial data formats of I^2S, MSB-first Left-justified or MSB-first Right-justified. The NJU26202 audio interface provides two data inputs, SDI0 and SDI1, and three data outputs, SDO0, SDO1 and SDO2, as shown in table 2 and 3. The input serial data is selected by the firmware command.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description
47	SDI0	Lch / Rch Audio Data Input 0
46	SDI1	Lch / Rch Audio Data Input 1
45	SDI2	Cch / SWch Audio Data Input 2
44	SDI3	LSch / RSch Audio Data Input 3

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
38	SDO1	Front Lch/Rch Audio Data Output 1
37	SDO2	Cch / SWch Audio Data Output 2
36	SDO3	Rear Lch/Rch Audio Data Output 3

■ Host Interface

The NJU26202 can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : I^2C bus or 4-Wire serial bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The detail I^2C bus and 4-Wire Serial bus information are described in the 'NJU26200 Series Hardware Data Sheet'.

Table 4 Serial Host Interface Pin Descriptions

Pin No.	Symbol	Setting	Host Interface
12	SEL	Low	I^2C Bus Interface
		High	4-Wire Serial Interface

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C /Serial)	I^2C bus Interface	4-Wire Serial Interface
25	AD1/SDIN	I^2C Address Select Bit1	Serial data input
26	AD2/SSb	I^2C Address Select Bit2	Slave select
27	SCL/SCK	Serial Clock	Serial Clock
28	SDA/SDOUT	Serial Data Input/Output (Open Drain output)	Serial data output (CMOS Output)

Note: When 4-Wire Serial bus is selected, The SDA/SDOUT pin is CMOS output. The SDOUT pin does not require a pull-up resistance.

When I^2C Bus is selected, this pin is a bi-directional Open Drain output. This pin, which is assigned for I^2C Bus, requires a pull-up resistance.

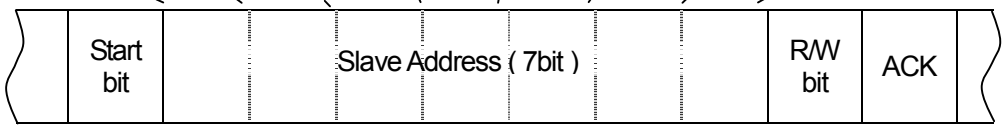
The SDA/SDOUT pin isn't 5.0V Input tolerant.

■ I²C Bus

When the NJU26202 is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

Table 6 I²C-Bus Interface Slave address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note: The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer. Moreover, after sending S ("START" condition), Sr (repeated "START" condition) is not received but it becomes the waiting for the P ("STOP" condition). Therefore, please be sure to send P ("STOP" condition).

■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. The SDOUT pin is always CMOS output. This pin does not require a pull-up resistance.

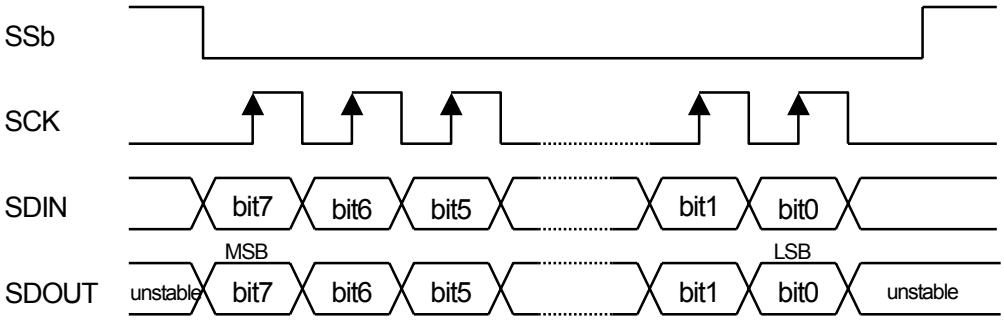


Fig. 4 4-Wire Serial Interface Timing

Note : When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".
When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
After sending LSB data, SDOUT transmits the MSB data that is received via SDIN until SSb becomes "High".

■ Pin setting

The NJU26202 operates default command setting after resetting the NJU26202. In addition, the NJU26202 restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No.	Symbol	Setting	Function
9	PROC	"High"	The NJU26202 operates default setting after reset.
		"Low"	The NJU26202 does not operate after reset. Sending start command is required for starting operation.
7	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ WatchDog Clock

The NJU26202 outputs clock pulse through WDC (Pin No.8) during normal operation. The WDC clock is useful to check the status of the NJU26202 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26202. When the WDC clock pulse is lost or not normal clock cycle, the NJU26202 does not operate correctly. Then reset the NJU26202 and set up the NJU26202 again.
The output toggle cycle from a WDC pin is set as about 100ms.

The WDC pin is open drain output. The WDC pin setting (Table 8)

Table 8 WDC pin setting

Pin No.	Symbol	Setting	
8	WDC	WDC pin is used.	Connect with V_{DDIO} through 3.3kΩ resistance
		WDC pin is not used.	Connect with V_{SSIO} through 3.3kΩ resistance. Do not open WDC pin.

Note: The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, the WDC pin can't output.
It is required to set up a sampling rate correctly.

■ Firmware Command Table

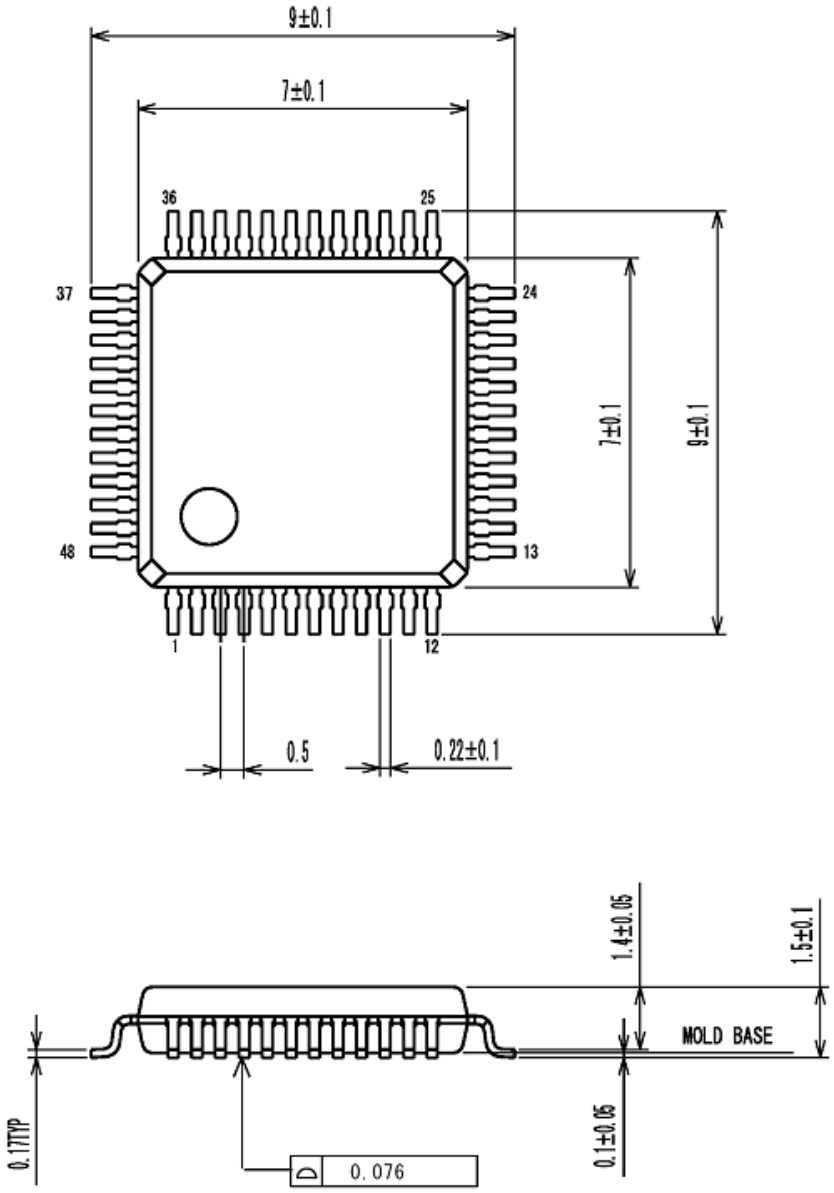
Table 9 NJU26202 Command

No.	Command
1	Set Task
2	Circle Surround Config
3	Circle Surround Automotive Config
4	TruBass Config
5	TruBass Size Select
6	TruBass Gain Control
7	FOCUS Config
8	FOCUS Gain Control
9	Input Trim Control
10	Master Volume Control
11	Channel Trim Control
12	Delay Control
13	Stereo Input Mode Config
14	Hall Simulator Input Select
15	Hall Simulator HPF fc
16	Hall Simulator LPF fc
17	Hall Simulator Early Reflection Start Time
18	Hall Simulator Early Reflection End Time
19	Hall Simulator Reverb Start Time
20	Hall Simulator HF Dump
21	Hall Simulator Reverb Time

No.	Command
22	Hall Simulator Surround
23	Hall Simulator Effect Output Trim
24	Hall Simulator Balance Trim
25	EQ Mode Select
26	EQ f0 Control
27	EQ Q Control
28	EQ Gain Control
29	Time Alignment
30	SW LPF fc
31	Sample rate Select
32	Smooth Control Config
33	Input Select
34	Phantom Center Config
35	TruBass Input Select
36	Input Mode Config
37	System State
38	Firmware Version Number Request
39	DSP Reset
40	Start
41	Nop

Notes : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs. Inc.) is required.

■ Package Dimensions (LQFP48-R3, Pb-Free)



MOLD MATERIAL : EPOXY RESIN

UNIT : mm
Lead Plating : SnBi

■ License Information

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