# Dolby Virtual Speaker / Dolby Headphone Decoder

## ■ General Description

The NJU26220 simulates a highly realistic 5.1-speaker surround sound listening environment from as few as two speakers or headphone by Dolby® Virtual Speaker/Dolby® Headphone technology.
The NJU26220 processes the Dolby® Virtual Speaker and Dolby® Headphone technology that combined with Pro Logic II processing. It includes Pro Logic II decoder. Moreover, multi-channel signal inputs from an external decoder are possible.
It is suitable for digital TVs, stereo mini-components, PCs, and any audio/visual products.

■Package

NJU26220FR3

## ■ Features

**-Software**

- Dolby® Virtual Speaker
- Dolby® Headphone
- Dolby® Pro Logic II® (Max 5.1ch Output)
- Multi-channel signals input (Max 5.1ch Input)
- Monitor output
- Lip-Sync Delay function (Digital Audio Delay)

**-Hardware**

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 12.288MHz(Standard), built-in PLL Circuit
- Digital Audio Interface : 4 Input ports / 4 Output ports
- Digital Audio Format : $I^2S$ 24bit, left-justified, right-justified, BCK : 32fs/64fs
- Master / Slave Mode
  - In Master mode, MCK : 256fs @fs=48kHz / 384fs @fs=32kHz
- Microcomputer Interface
  - $I^2C$ Bus (Standard-mode/100kbps, Fast-mode/400kbps)
  - 4 -Wire Serial Bus (4-Wire: Clock, Enable, Input data, Output data)
- Operating Voltage : $V_{DD}$ = $V_{DDPLL}$ = 1.8V
  : $V_{DDIO}$ = 3.3V
- Input Terminal : 5.0V Input tolerant
- Package : LQFP48-R3 (Pb-Free)

* The detail hardware specification of the NJU26220 is described in the " NJU26200 Series Hardware Data Sheet".

## ■ Block Diagram

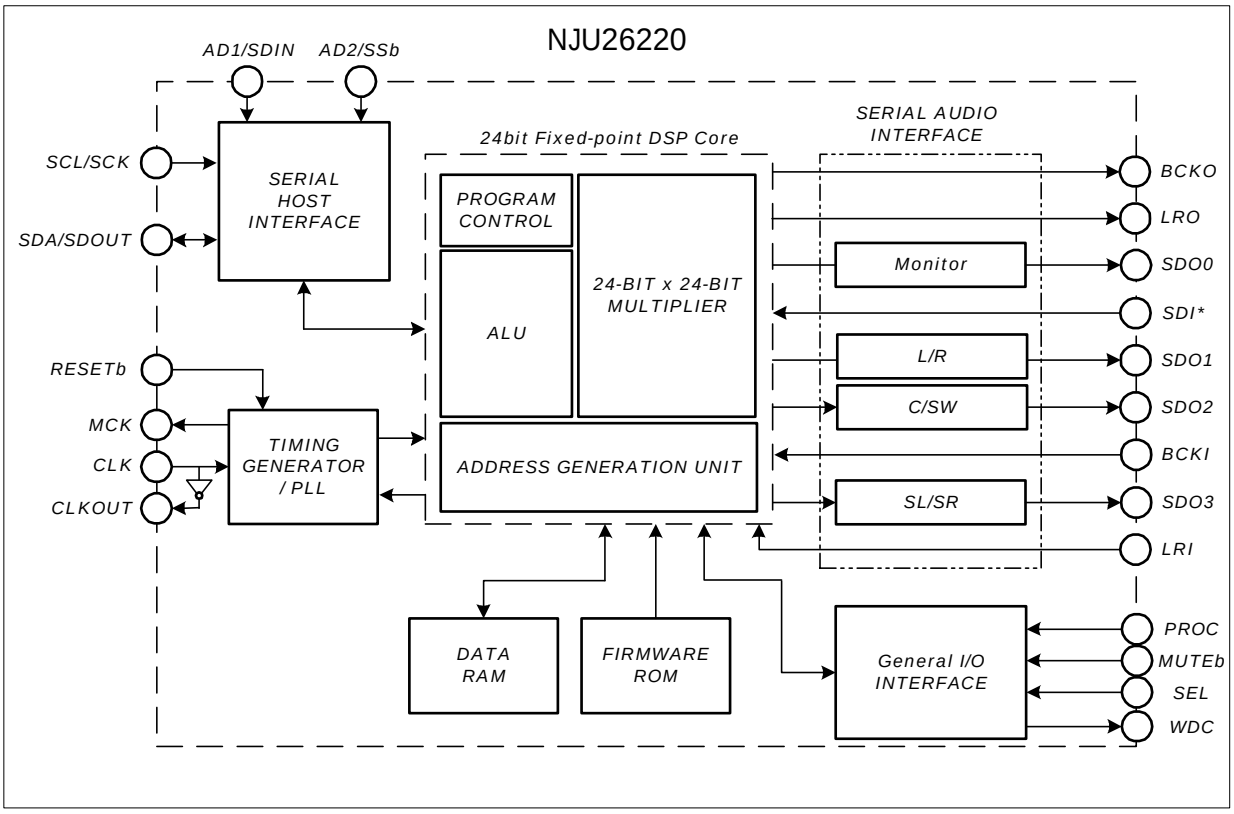



**Fig. 1 NJU26220 Hardware Block Diagram**

## ■ Function Block Diagram

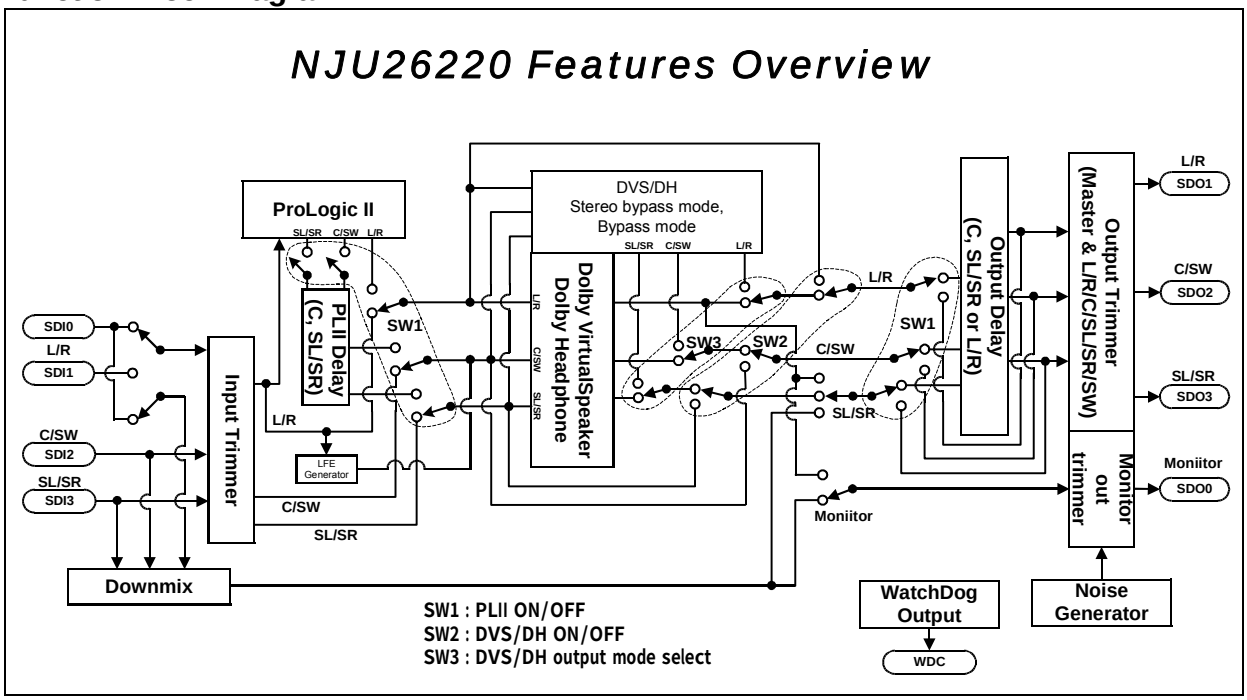



**Fig. 2 NJU26220 Block Diagram**

## ■ Pin Configuration

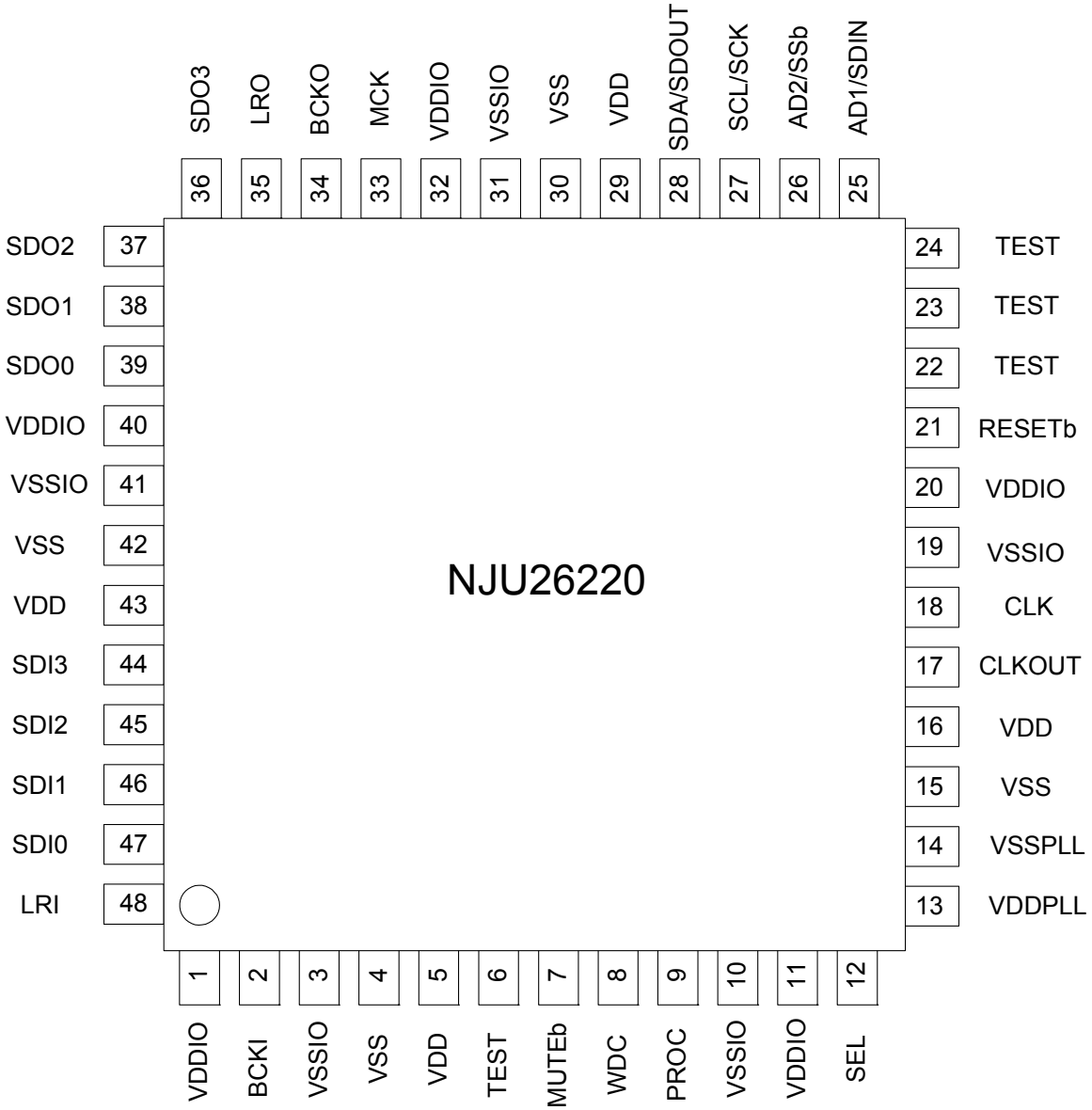



**Fig. 3 NJU26220 Pin Configuration**

## ■ Pin Description

**Table 1 Pin Description**

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1,11,20,32,40 | VDDIO | - | I/O Power Supply +3.3V |
| 2 | BCKI | I | Bit Clock Input |
| 3,10,19,31,41 | VSSIO | - | I/O GND |
| 4,15,30,42 | VSS | - | Core GND |
| 5,16,29,43 | VDD | - | Core Power Supply +1.8V |
| 6 | TEST | I | for test (connected to VSSIO through 3.3kΩ resistance.) |
| 7 | MUTEb * | I | Master Volume level, After Reset DSP ("1" : 0dB , "0" : Mute) |
| 8 | WDC * | OD | Clock for Watch Dog Timer (Open Drain Output) |
| 9 | PROC * | I | After Reset DSP. ( "1" : Normal , "0" : Wait from Command ) |
| 12 | SEL | I | Select $I^2C$ or Serial bus ( '1' : Serial , '0' : $I^2C$-Bus) |
| 13 | VDDPLL | - | PLL Analog Power Supply +1.8V |
| 14 | VSSPLL | - | PLL Analog GND |
| 17 | CLKOUT | O | OSC Output |
| 18 | CLK | I | X'tal Clock Input (12.288MHz) |
| 21 | RESETb | I | Reset (RESETb='0' : DSP Reset) |
| 22 | TEST | I | for Test (Connect to VDDIO) |
| 23,24 | TEST | I | for Test (Connect to VSSIO) |
| 25 | AD1/SDIN | I | $I^2C$ Address / Serial Input |
| 26 | AD2/SSb | I | $I^2C$ Address / Serial Enable |
| 27 | SCL/SCK | I | $I^2C$ Clock / Serial Clock |
| 28 | SDA/SDOUT | I/O | $I^2C$ I/O (Open Drain output) / Serial Output (CMOS output)<br>$I^2C$ Bus mode : SDA pin requires a pull-up resistance.<br>4-wire Serial mode : SDOUT does not require a pull-up resistance. |
| 33 | MCK | O | Master Clock Output (CLK Terminal=27pin Buffer Out) |
| 34 | BCKO | O | Bit Clock Output |
| 35 | LRO | O | LR Clock Output |
| 36 | SDO3 | O | Audio Data Output 3 (SL/SR) |
| 37 | SDO2 | O | Audio Data Output 2 (C/ SW) |
| 38 | SDO1 | O | Audio Data Output 1 (L/R) |
| 39 | SDO0 | O | Audio Data Output 0 (Monitor output) |
| 44 | SDI3 | I | Audio Data Input 3 |
| 45 | SDI2 | I | Audio Data Input 2 |
| 46 | SDI1 | I | Audio Data Input 1 |
| 47 | SDI0 | I | Audio Data Input 0 |
| 48 | LRI | I | LR Clock Input |

I : Input
O : Output
OD : Open Drain Output
I/O : Bi-directional

**Note:** Pins symbol with * : Connect with VDDIO or VSSIO through 3.3kΩ resistance

## ■ Audio Interface

The NJU26220 audio interface provides industry serial data formats of $I^2S$, MSB-first Left-justified or MSB-first Right-justified. The NJU26220 audio interface provides four data inputs, SDI0, SDI1, SDI2 and SDI3, and four data outputs, SDO0, SDO1, SDO2 and SDO3, as shown in table 2 and 3. The input serial data is selected by the firmware command.

**Table 2 Serial Audio Input Pin**

| Pin No. | Symbol | Description |
|---|---|---|
| 47 | SDI0 | Stereo L/R input (Pin select) |
| 46 | SDI1 | |
| 45 | SDI2 | C/SW |
| 44 | SDI3 | SL/SR |

**Table 3 Serial Audio Output Pin**

| Pin No. | Symbol | Description |
|---|---|---|
| 39 | SDO0 | Monitor output |
| 38 | SDO1 | L/R |
| 37 | SDO2 | C/SW |
| 36 | SDO3 | SL/SR |

**Note:** L/R : Front channel
C/SW : Center channel and Sub woofer
SL/SR: Surround channel

## ■ Host Interface

The NJU26220 can be controlled via Serial Host Interface (SHI) using either of two serial bus formats : $I^2C$ bus or 4-Wire serial bus. Data transfers are in 8 bits packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The detail $I^2C$ bus and 4-Wire Serial bus information are described in the 'NJU26200 Series Hardware Data Sheet'.

**Table 4 Serial Host Interface Pin Descriptions**

| Pin No. | Symbol | Setting | Host Interface |
|---|---|---|---|
| 12 | SEL | Low | $I^2C$ Bus Interface |
| | | High | 4-Wire Serial Interface |

**Table 5 Serial Host Interface Pin Description**

| Pin No. | Symbol ($I^2C$ /Serial) | $I^2C$ bus Interface | 4-Wire Serial Interface |
|---|---|---|---|
| 25 | AD1/SDIN | $I^2C$ Address Select Bit1 | Serial data input |
| 26 | AD2/SSb | $I^2C$ Address Select Bit2 | Slave select |
| 27 | SCL/SCK | Serial Clock | Serial Clock |
| 28 | SDA/SDOUT | Serial Data Input/Output (Open Drain output) | Serial data output (CMOS Output) |

**Note:** When 4-Wire Serial bus is selected, The SDA/SDOUT pin is CMOS output. The SDOUT pin does not require a pull-up resistance.

When $I^2C$ Bus is selected, this pin is a bi-directional Open Drain output. This pin, which is assigned for $I^2C$ Bus, requires a pull-up resistance.

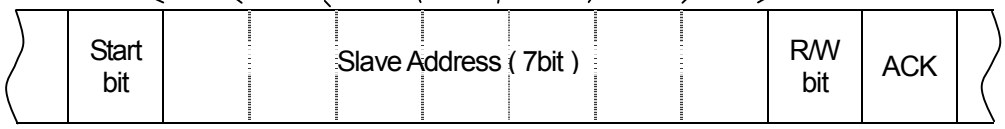
The SDA/SDOUT pin isn't 5.0V Input tolerant. Please note the voltage level (Max voltage is $V_{DDIO}$).

## ■ I²C Bus

When the NJU26220 is configured for I²C bus communication in SEL="Low", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring a pull-up resistance. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6)

**Table 6 I²C-Bus Interface Slave address**

| bit7 | bit6 | bit5 | bit4 | bit3 | AD2 bit2 | AD1 bit1 | R/W bit0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | R/W |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | |




* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

**Note:** The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer. Moreover, after sending S ("START" condition), Sr (repeated "START" condition) is not received but it becomes the waiting for the P ("STOP" condition). Therefore, please be sure to send P ("STOP" condition).

## ■ 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="High" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin.

Data transfers are MSB first and are enabled by setting SSb = "Low". Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte(MSB) which is latched on the falling transitions of SSb. The SDOUT pin is always CMOS output. This pin does not require a pull-up resistance.

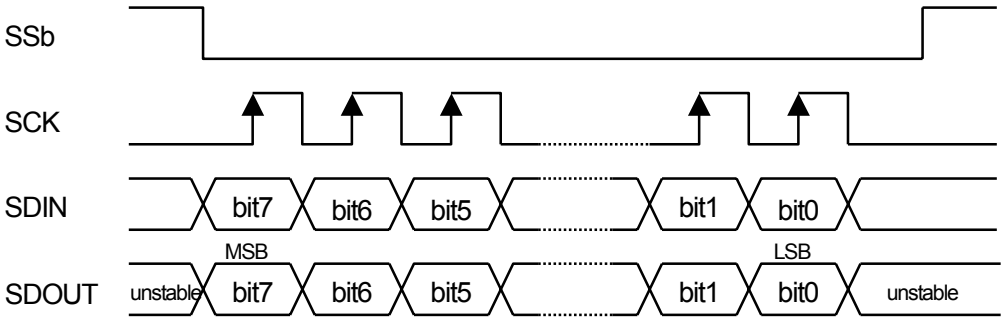



**Fig. 4 4-Wire Serial Interface Timing**

**Note :** When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High".
When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

## ■ Pin setting

The NJU26220 operates default command setting after resetting the NJU26220. In addition, the NJU26220 restricts operation at power on by setting PROC pin and MUTEb pin (Table 7). These pins are input pin. However, these pins operate as bi-directional pins. Connect with $V_{DDIO}$ or $V_{SSIO}$ through 3.3kΩ resistance.

**Table 7 Pin setting**

| Pin No. | Symbol | Setting | Function |
|---|---|---|---|
| 9 | PROC | "High" | The NJU26220 operates default setting after reset. |
| | | "Low" | The NJU26220 does not operate after reset. Sending start command is required for starting operation. |
| 7 | MUTEb | "High" | Master volume is set 0dB after reset. |
| | | "Low" | Master volume is set mute after reset. |

## ■ WatchDog Clock

The NJU26220 outputs clock pulse through WDC (Pin No.8) during normal operation. The WDC clock is useful to check the status of the NJU26220 operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26220. When the WDC clock pulse is lost or not normal clock cycle, the NJU26220 does not operate correctly. Then reset the NJU26220 and set up the NJU26220 again. The WDC clock is able to be variable for 10ms to 640ms by command. Default setting of WDC clock is 200ms.

The WDC pin is open drain output. The WDC pin setting (Table 8)

**Table 8 WDC pin setting**

| Pin No. | Symbol | Setting | |
|---|---|---|---|
| 8 | WDC | WDC pin is used. | Connect with $V_{DDIO}$ through 3.3kΩ resistance |
| | | WDC pin is not used. | Connect with $V_{SSIO}$ through 3.3kΩ resistance.<br>Do not open WDC pin. |

**Note:** The cycle of WDC output is rough. Because WDC output inserts in the process of sound processing.
In slave mode, when there is no input of BCKI/LRI, the WDC pin can't output.
It is required to set up a sampling rate correctly.

## ■ Firmware Command Table

**Table 9 NJU26220 Command**

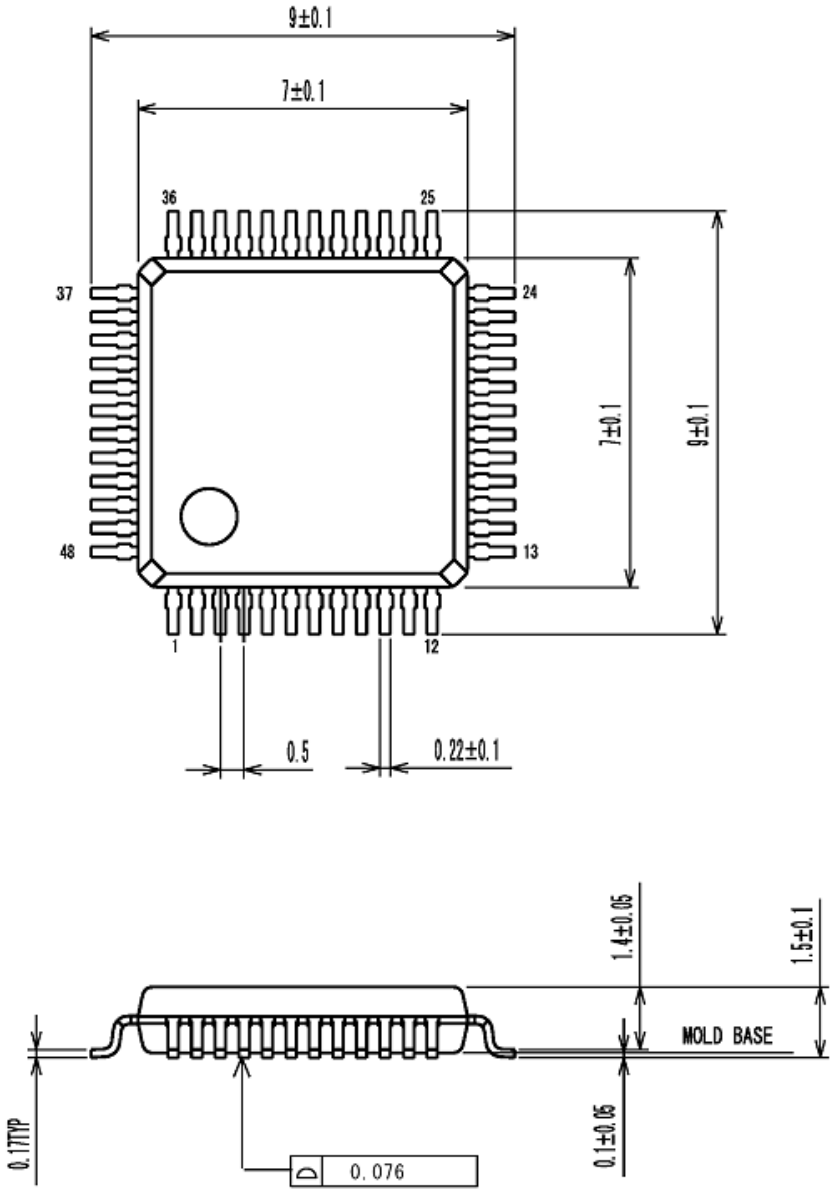
| No. | Command |
|---|---|
| 1 | SET_TASK_CMD |
| 2 | PRO2MODE_CMD |
| 3 | PRO2CDCFG_CMD |
| 4 | PRO2FLAGS_CMD |
| 5 | DVS_DH_CMD |
| 6 | SAMPLERATE_CMD |
| 7 | PNG_MODE_CMD |
| 8 | DELAY_CMD |
| 9 | GAIN_CMD |
| 10 | SYSTEM_STATE_CMD |
| 11 | WATCHDOG_CMD |
| 12 | SMOOTH_CMD |
| 13 | OUTPUT_SEL_CMD |
| 14 | LFE_CONFIG_CMD |
| 15 | REINIT_CMD |
| 16 | SOFTWARE_RESET_CMD |
| 17 | START_CMD |
| 18 | NOP_CMD |

**Notes :** In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (Dolby) is required.

## ■ License Information

The Word “DOLBY”, “Pro Logic” and the double D mark are trademarks of Dolby Laboratories.
The NJU26220 can only be delivered to licensees of Dolby Laboratories.
Please refer to the licensing application manual issued by Dolby Laboratories.

## ■ Package Dimensions ( LQFP48-R3, Pb-Free )




**MOLD MATERIAL : EPOXY RESIN**

UNIT : mm
Lead Plating : SnBi