PRELIMINARY

# 4-BIT SINGLE CHIP OTP TINY CONTROLLER

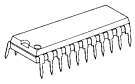
## ■ GENERAL DESCRIPTION

The **NJU3152** is the C-MOS 4-bit Single Chip OTP type Micro Controller with programmable Flash Memory.

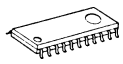
It is completely compatible with the **NJU3102** in function and the pin configuration. Therefore, the **NJU3152** is suitable for the final evaluation before **NJU3102** mask generation, the small quantity production and short lead-time.

* *In this data sheet, only OTP programming and the difference between **NJU3152** and **NJU3102** are mentioned mainly.*
*Therefore the detail function and specification should be referred on the **NJU3102** data sheet.*

## ■ PACKAGE OUTLINE



NJU3152L

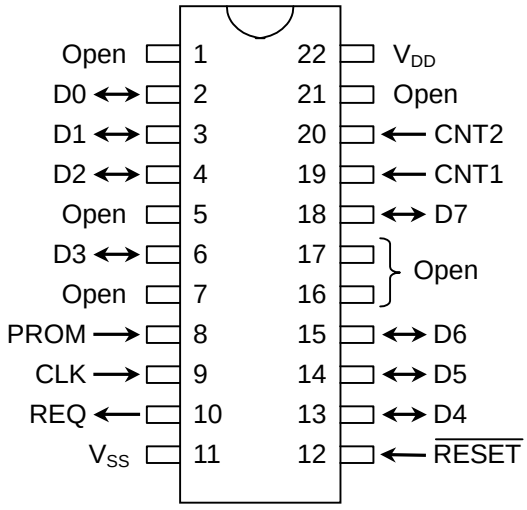


NJU3152G

## ■ FEATURES

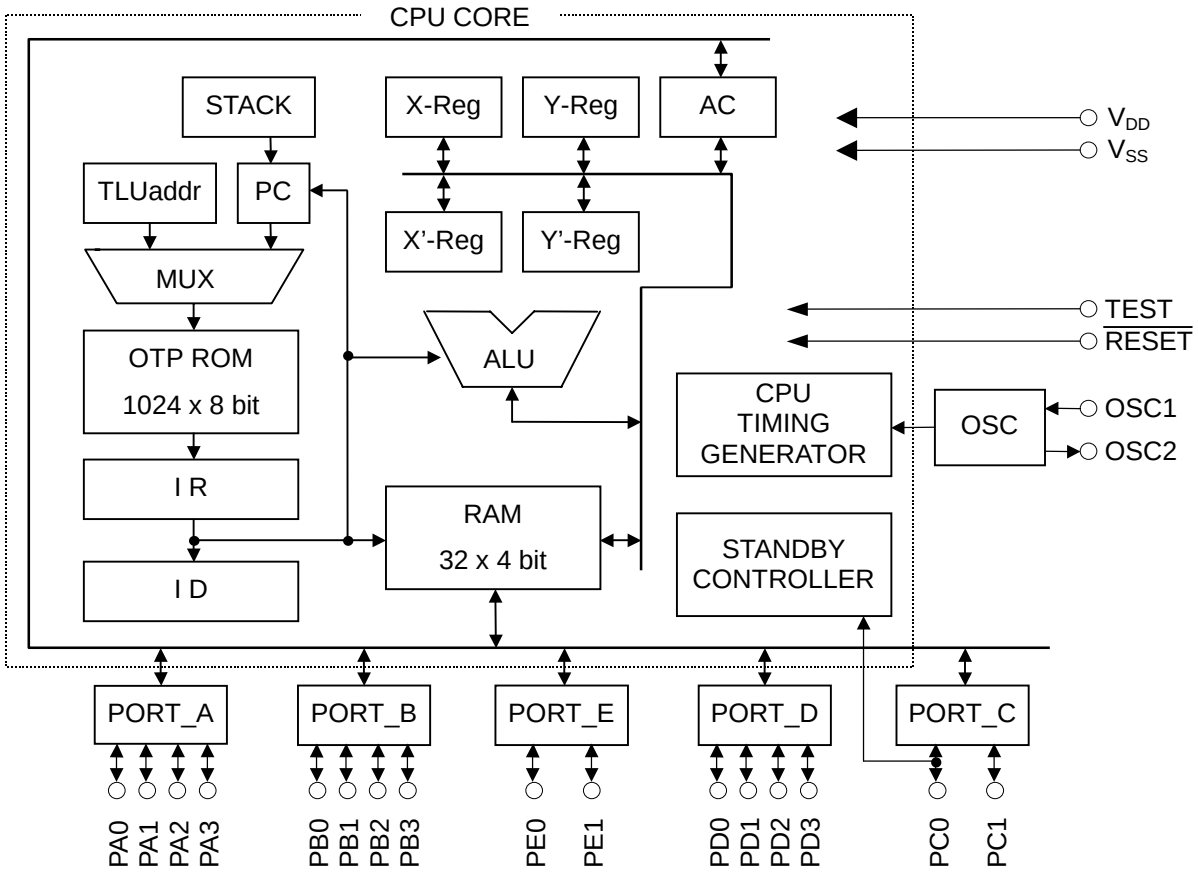
- Internal One Time Programmable ROM 1,024 X 8bits
- Internal Data RAM 32 X 4bits
- Wide operating voltage range 2.7V ~ 5.5V
- Package outline SDIP22 / SOP22
- ROM programmer “SUPERPRO/L” by XELTEK co,.

## ■ PIN CONFIGURATION IN OTP PROGRAMMING MODE




Note) The pin configuration in Normal operating mode is the same as **NJU3102**.

## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION IN OTP PROGRAMMING MODE

| No. | SYMBOL | INPUT/OUTPUT | F U N C T I O N |
|---|---|---|---|
| 12 | $\overline{\text{RESET}}$ | INPUT | RESET terminal.<br>When the low-level input-signal, the system is initialized. |
| 2 - 4,<br>6,<br>13 - 15,<br>18 | D0 - D7 | INPUT/OUTPUT | Data bus |
| 19,<br>20 | CNT1<br>CNT2 | INPUT<br>INPUT | OTP control input terminal |
| 10 | REQ | OUTPUT | Request output terminal |
| 9 | CLK | INPUT | Clock input terminal |
| 8 | PROM | INPUT | OTP programming enable terminal |
| 22 | $V_{DD}$ | - | Power Source (5V) |
| 11 | $V_{SS}$ | - | Power Source (0V) |

Note 1) Use at $V_{DD}$=5V in OTP programming mode.
2) Non connect anything to the other terminals.

## ■ Difference between NJU3152 (OTP version) and NJU3102 (MASK version)

● Operating mode

**NJU3152** has two operating modes. One is "Normal operating mode" and the other is "OTP programming mode".

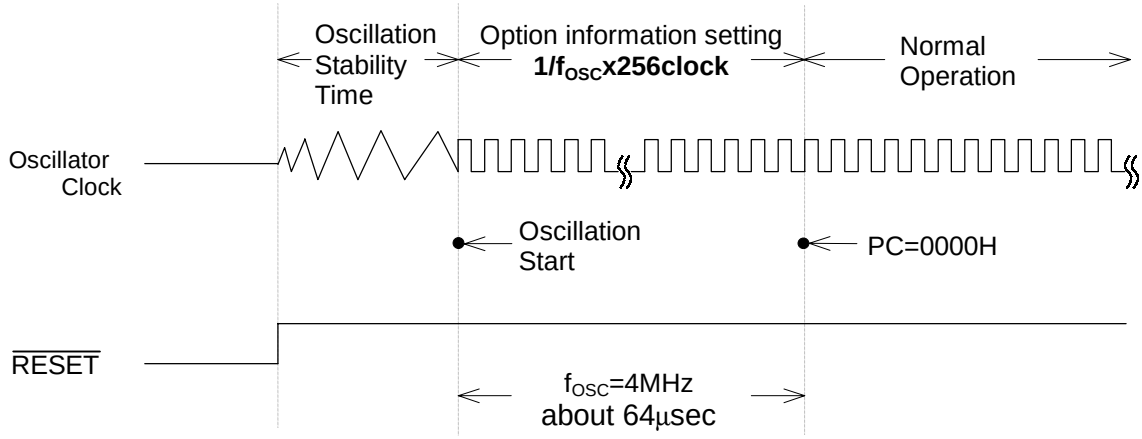
- Normal operating mode
  The "TEST" terminal is set to low level. (The terminal is recommended to connect to GND.)
  Operating voltage range; 2.7V ~ 5.5V.

- OTP Programming mode
  User program is read out from or written into the OTP by the universal programmer "SUPERPRO/L" and converting adapter made by XELTEK co,.(USA).

● Option information set in the initialization

When the initialization is performed($\overline{\text{RESET}}$ terminal is "L"), the operation information stored in option area is set as shown in the following timing chart . The option information is set in the term of **1 / $f_{osc}$ x 256clock** after RESET releasing and oscillation stability time. After information set, the program counter is set to 0000H and the **NJU3152** operates in normal.

**[ TIMING CHART ]**



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.3 ~ +7.0 | V |
| Input Voltage | $V_{IN}$ | -0.3 ~ $V_{DD}$ + 0.3 | V |
| Output Voltage | $V_{OUT}$ | -0.3 ~ $V_{DD}$ + 0.3 | V |
| Operating Temperature | $T_{opr}$ | -20 ~ +75 | °C |
| Storage Temperature | $T_{stg}$ | -55 ~ +125 | °C |

Note)

The difference of electrical characteristics between **NJU3152** (OTP version) and **NJU3102** (MASK version)

| | | **NJU3102** | | **NJU3152** |
|---|---|---|---|---|
| •Supply Voltage ($V_{DD}$) MIN. | | 2.4V | → | 2.7V |
| •Supply Current | | | | |
| 5V | ($I_{DD1}$) Max. | 4.5mA | → | 30mA |
| | ($I_{DD2}$) Max. | 4.5mA | → | 30mA |
| | ($I_{DD3}$) Max. | 4.3mA | → | 30mA |
| | ($I_{DD4}$) Max. | 5.0μA | | 20μA |
| 3V | ($I_{DD1}$) Max. | 2.3mA | → | 20mA |
| | ($I_{DD2}$) Max. | 2.3mA | → | 20mA |
| | ($I_{DD3}$) Max. | 2.1mA | | 20mA |
| | ($I_{DD4}$) Max. | 3.0μA | → | 20μA |

## ■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 1

($V_{DD}$=3.6~5.5V, $V_{SS}$=0V, Ta=-20~75°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{DD}$ | 3.6 | | 5.5 | V | |
| Supply Current | $I_{DD1}$ | $V_{DD}$<br>$V_{DD}$=5V, $f_{OSC}$=2MHz<br>X'tal Oscillation in Reset | | | 30 | mA | *3 |
| | $I_{DD2}$ | $V_{DD}$<br>$V_{DD}$=5V, $f_{OSC}$=2MHz<br>Ceramic Oscillation in Reset | | | 30 | mA | *3 |
| | $I_{DD3}$ | $V_{DD}$<br>$V_{DD}$=5V, $f_{OSC}$=2MHz<br>CR Oscillation in Reset | | | 30 | mA | *3 |
| | $I_{DD4}$ | $V_{DD}$<br>$V_{DD}$=5V, STANDBY Mode | | | 20 | μA | *3 |
| | $I_{DD5}$ | $V_{DD}$<br>$V_{DD}$=5V, $f_{OSC}$=4MHz, Operating | | | 30 | mA | *3 |
| High-Level Input Voltage | $V_{IH1}$ | PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3 | $0.7V_{DD}$ | | $V_{DD}$ | V | *1 |
| | $V_{IH2}$ | PE0, PE1, $\overline{RESET}$ | $0.8V_{DD}$ | | $V_{DD}$ | V | *1 |
| | $V_{IH3}$ | OSC1 | $V_{DD}$-1.0 | | $V_{DD}$ | V | |
| Low-level Input Voltage | $V_{IL1}$ | PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3 | 0 | | $0.3V_{DD}$ | V | *1 |
| | $V_{IL2}$ | PE0, PE1, $\overline{RESET}$ | 0 | | $0.2V_{DD}$ | V | *1 |
| | $V_{IL3}$ | OSC1 | 0 | | 1.0 | V | |
| High-Level Input Current | $I_{IH}$ | $V_{DD}$=5.5V, $V_{IN}$=5.5V<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1, $\overline{RESET}$ | | | 10 | μA | *1 |
| Low-Level Input Current | $I_{IL1}$ | $V_{DD}$=5.5V, $V_{IN}$=0V<br>Without pull-up resistance<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1, $\overline{RESET}$ | | | -10 | μA | *1 |
| | $I_{IL2}$ | $V_{DD}$=5.5V, $V_{IN}$=0V<br>With pull-up resistance<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1 | | | -100 | μA | *1 |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$=-100μA<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1 | $V_{DD}$-0.5 | | | V | *2 |
| Low-Level Output Voltage | $V_{OL1}$ | $I_{OL1}$=400μA<br>PA0~PA3, PB0~PB3, PC0, PC1, PE0, PE1 | | | 0.5 | V | *2 |
| | $V_{OL2}$ | $I_{OL2}$=15mA<br>PD0~PD3 | | | 2.0 | V | *2 |
| Output Leakage Current | $I_{OD}$ | $V_{DD}$=5.5V, $V_{OH}$=5.5V<br>PD0~PD3 | | | 10 | μA | *2 |
| Input Capacitance | $C_{IN}$ | Except $V_{DD}$, $V_{SS}$ terminals<br>$f_{OSC}$=1MHz<br>Other terminals : 0V | | 10 | 20 | pF | |

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

## ■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 2

($V_{DD}$=2.7~3.6V, $V_{SS}$=0V, Ta=-20~75°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{DD}$ | 2.7 | | 3.6 | V | |
| Supply Current | $I_{DD1}$ | $V_{DD}$<br>$V_{DD}$=3V, $f_{OSC}$=1MHz<br>X'tal Oscillation in Reset | | | 20 | mA | *3 |
| | $I_{DD2}$ | $V_{DD}$<br>$V_{DD}$=3V, $f_{OSC}$=1MHz<br>Ceramic Oscillation in Reset | | | 20 | mA | *3 |
| | $I_{DD3}$ | $V_{DD}$<br>$V_{DD}$=3V, $f_{OSC}$=1MHz<br>CR Oscillation in Reset | | | 20 | mA | *3 |
| | $I_{DD4}$ | $V_{DD}$<br>$V_{DD}$=3V, STANDBY Mode | | | 20 | μA | *3 |
| | $I_{DD5}$ | $V_{DD}$<br>$V_{DD}$=3V, $f_{OSC}$=4MHz, Operating | | | 20 | mA | *3 |
| High-Level Input Voltage | $V_{IH1}$ | PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3 | $0.8V_{DD}$ | | $V_{DD}$ | V | *1 |
| | $V_{IH2}$ | PE0, PE1, $\overline{RESET}$ | $0.85V_{DD}$ | | $V_{DD}$ | V | *1 |
| | $V_{IH3}$ | OSC1 | $V_{DD}$-0.3 | | $V_{DD}$ | V | |
| Low-level Input Voltage | $V_{IL1}$ | PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3 | 0 | | $0.2V_{DD}$ | V | *1 |
| | $V_{IL2}$ | PE0, PE1, $\overline{RESET}$ | 0 | | $0.15V_{DD}$ | V | *1 |
| | $V_{IL3}$ | OSC1 | 0 | | 0.3 | V | |
| High-Level Input Current | $I_{IH}$ | $V_{DD}$=3.6V, $V_{IN}$=3.6V<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1, $\overline{RESET}$ | | | 10 | μA | *1 |
| Low-Level Input Current | $I_{IL1}$ | $V_{DD}$=3.6V, $V_{IN}$=0V<br>Without pull-up resistance<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1, $\overline{RESET}$ | | | -10 | μA | *1 |
| | $I_{IL2}$ | $V_{DD}$=3.6V, $V_{IN}$=0V<br>With pull-up resistance<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1 | | | -100 | μA | *1 |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$=-80μA<br>PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0, PE1 | $V_{DD}$-0.5 | | | V | *2 |
| Low-Level Output Voltage | $V_{OL1}$ | IOL1=350μA<br>PA0~PA3, PB0~PB3, PC0, PC1, PE0, PE1 | | | 0.5 | V | *2 |
| | $V_{OL2}$ | $I_{OL2}$=5mA<br>PD0~PD3 | | | 1.0 | V | *2 |
| Output Leakage Current | $I_{OD}$ | $V_{DD}$=3.6V, $V_{OH}$=3.6V<br>PD0~PD3 | | | 10 | μA | *2 |
| Input Capacitance | $C_{IN}$ | Except $V_{DD}$, $V_{SS}$ terminals<br>$f_{OSC}$=1MHz<br>Other terminals : 0V | | 10 | 20 | pF | |

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

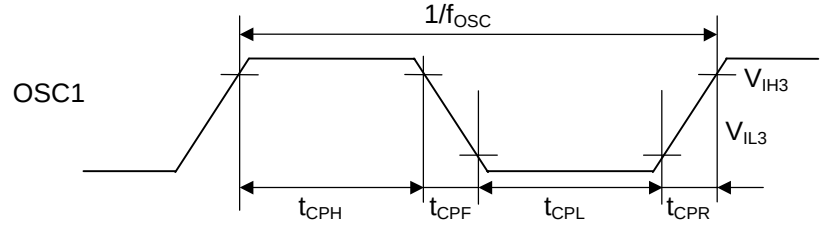
## ■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 1

($V_{SS}$=0V, Ta= -20~75°C)

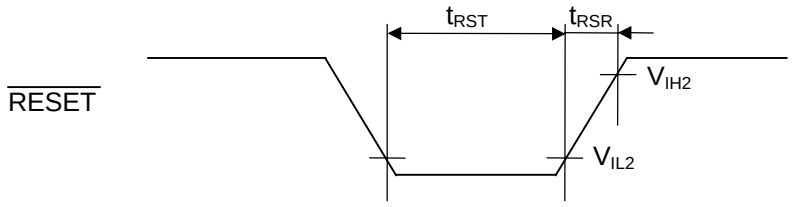
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Operating Frequency | $f_{OSC}$ | $V_{DD}$=2.7~3.6V | X'tal Resonator | 0.03 | | 2.0 | MHz |
| | | | Ceramic Resonator | 0.03 | | 2.0 | |
| | | | External Resistor Oscillation | 0.03 | | 1.0 | |
| | | | External Clock | 0.03 | | 2.0 | |
| | | $V_{DD}$=3.6~5.5V | X'tal Resonator | 0.03 | | 4.0 | |
| | | | Ceramic Resonator | 0.03 | | 4.0 | |
| | | | External Resistor Oscillation | 0.03 | | 2.0 | |
| | | | External Clock | 0.03 | | 4.0 | |
| Instruction Cycle Time | $t_C$ | | | | $6/f_{OSC}$ | | s |
| External Clock Pulse Width | $t_{CPH}$ | $V_{DD}$=2.7~3.6V | | 250 | | 16600 | ns |
| | $t_{CPL}$ | $V_{DD}$=3.6~5.5V | | 125 | | 16600 | |
| External Clock Rise Time / Fall Time | $t_{CPR}$ / $t_{CPF}$ | $V_{DD}$=2.7~5.5V | | | | 20 | ns |
| $\overline{RESET}$ Low-Level Width | $t_{RST}$ | $V_{DD}$=2.7~5.5V | | $4/f_{OSC}$ | | | s |
| $\overline{RESET}$ Rise Time | $t_{RSR}$ | $V_{DD}$=2.7~5.5V | | | | 20 | ms |
| Port Input Level Width | $t_{PIN}$ | $V_{DD}$=2.7~5.5V | | $6/f_{OSC}$ | | | s |
| Edge Detection (PC1) Rise Time / Fall Time | $t_{EDR}$ / $t_{EDF}$ | $V_{DD}$=2.7~5.5V | | | | 200 | ns |
| Restart Signal (PC0) Rise Time | $t_{STR}$ | $V_{DD}$=2.7~5.5V | | | | 200 | ns |

## ■ AC CHARACTERISTICS 1 TIMING CHART

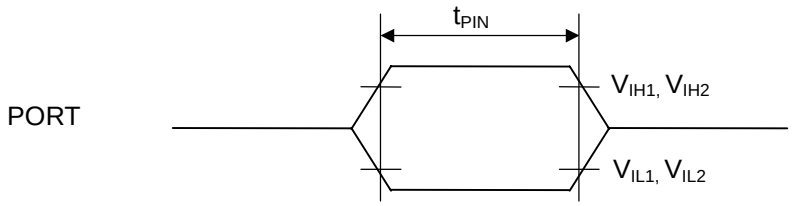
EXTERNAL CLOCK



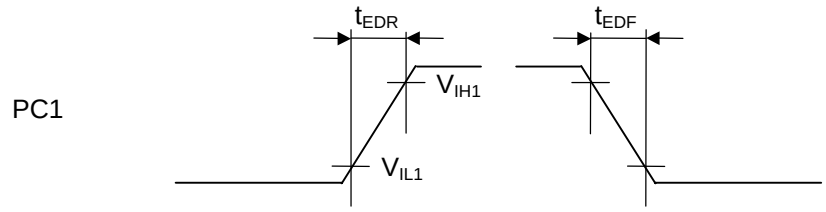

RESET INPUT



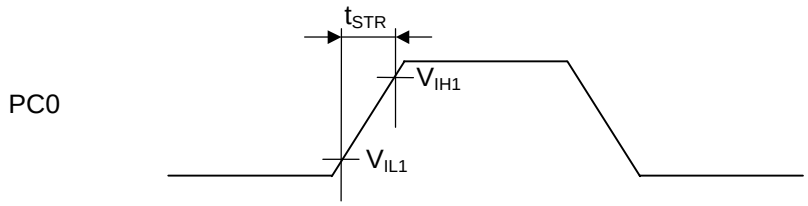

PORT INPUT




EDGE DETECTOR INPUT




RESTART SIGNAL INPUT



## ■ OPTION as same as mask version (NJU3102)

1) INPUT OUTPUT Terminal Selection
All of input-output terminals select a terminal type from the following table for each group as a PORT by the mask option.

**[ CIRCUIT TYPE TABLE ]**

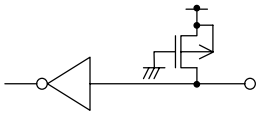
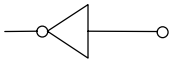
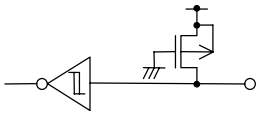
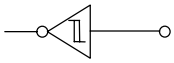
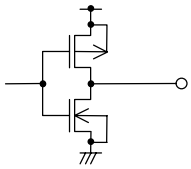
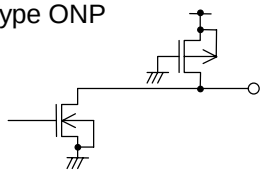
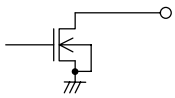
| SYMBOL | TERMINAL TYPES | | | | REMARKS | |
|---|---|---|---|---|---|---|
| | Input / Output Terminal*1 | | EXTRA FUNCTION | | | |
| | Port of Input | Port of Output | | | | |
| Port A (PA0～PA3) | ICP IC | OC | | | | |
| Port B (PB0～PB3) | ICP IC | OC | | | | |
| Port C (PC0, PC1) | ICP IC | OC | | Restart signal input *2 | | |
| | | | | Edge detection *2 | R<br>F | Rise edge detection<br>Fall edge detection |
| Port D (PD0～PD3) | ICP IC | ONP ON | | | | |
| Port E (PE0, PE1) | ISP IS | OC | | | | |

Note) The symbol in the above table is the same as in mask option generator software.
*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.
*2) When the PORTC(PHY3) is set as the input, the extra function are added for terminals.

**[MASK OPTION LIST]**

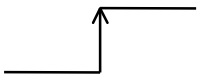
| 記号 | 機 能 |
|---|---|
| ICP | C-MOS input with pull-up resistance |
| ISP | C-MOS Schmitt trigger input with pull-up resistance |
| IC | C-MOS input |
| IS | C-MOS Schmitt trigger input |
| ONP | Nch-FET Open-Drain output with pull-up resistance |
| OC | C-MOS output |
| ON | Nch-FET Open-Drain output |
| R | Rise edge detection |
| F | Fall edge detection |

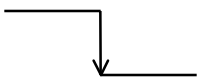
**[ INPUT OUTPUT TERMINAL TYPE ]**

| | Types | With Pull-up | Without Pull-up | Terminals |
|---|---|---|---|---|
| INPUT TERMINAL | C-MOS | Type ICP  | Type IC  | PA0~PA3, PB0~PB3, PC0, PC1, PD0~PD3 |
| | SCHMITT TRIGGER | Type ISP  | Type IS  | PE0, PE1 |
| OUTPUT TERMINAL | C-MOS | | Type ON  | PA0~PA3, PB0~PB3, PC0, PC1, PE0, PE1 |
| | N-channel(Nch) OPEN DRAIN | Type ONP  | Type ON  | PD0~PD3 |

2) Edge Detector Selection

PC1 terminal is added the “Edge detect function” by the mask option.

Rising edge 

Falling edge 

# MEMO