

36 Outputs VFD Controller/Driver

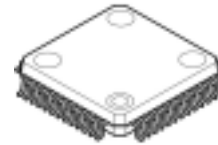
■ GENERAL DESCRIPTION

The NJU3427 is a 36-output VFD (Vacuum Fluorescent Display) controller/driver.

The NJU3427 consists of high-voltage driving circuit, Timing/ Segment driver select circuit, display data RAM (DDRAM), address counter, instruction register, reset circuit serial interface and oscillator.

The direct control from the MPU and high voltage drivers make the NJU3427 well suited for various VFD displays

■ Package

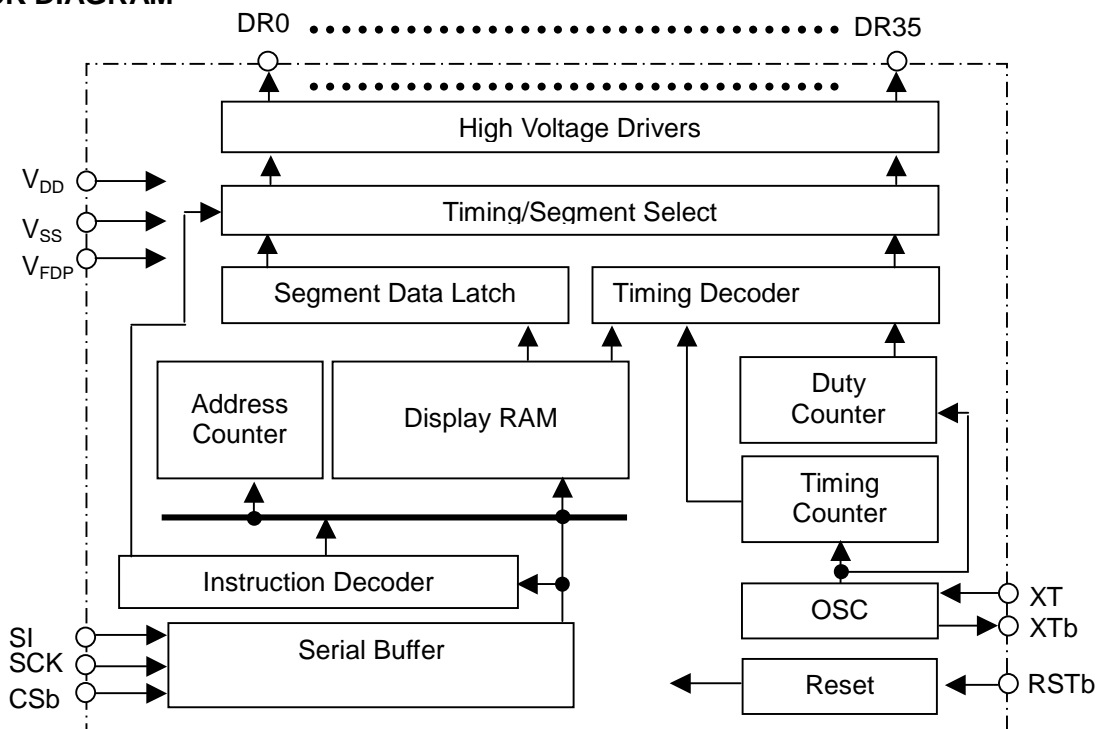


NJU3427F

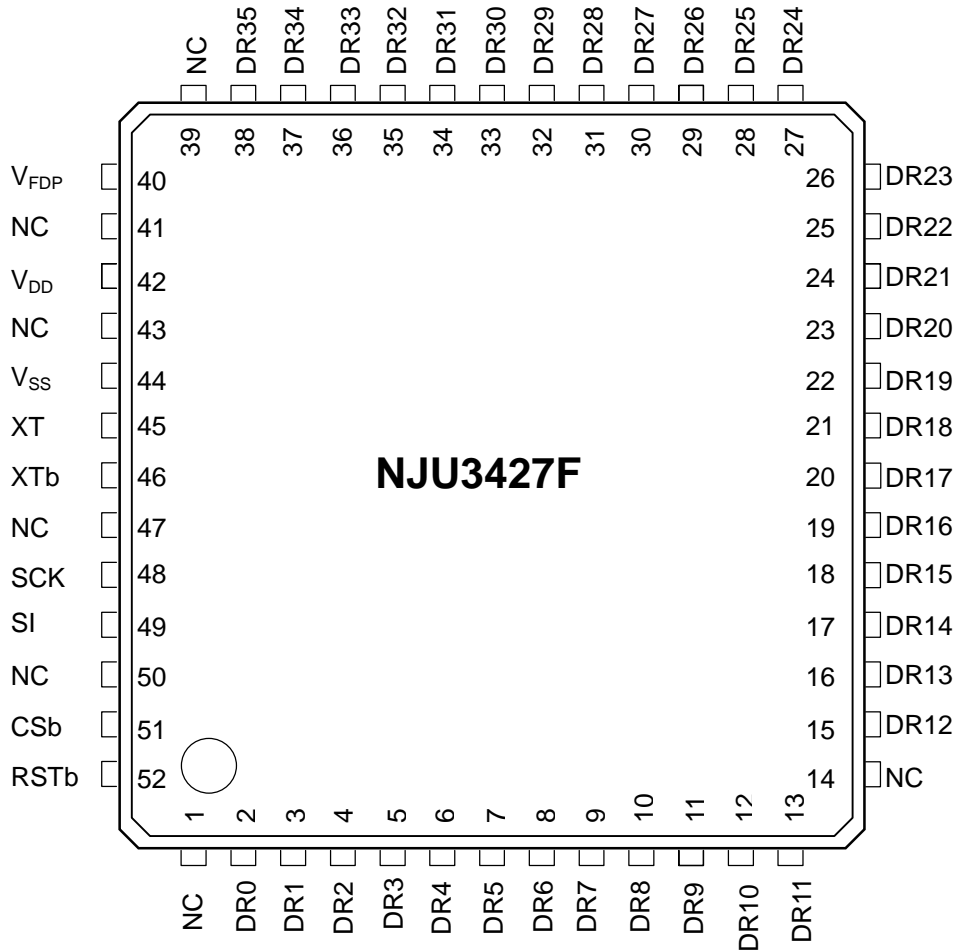
■ FEATURES

- Display Capability From 20-Seg x16-Timing to 28-Seg x 4-Timing
- DR0 Pin (I_{S01}) 20mA($V_{DD}=5V$)
- DR1~DR35 Pins (I_{S02}) 10mA($V_{DD}=5V$)
- Segment and Timing Driver Configure 4 patterns
- High VFD Driving Voltage $|V_{DD}-V_{FDP}| \leq 40V$
- Programmable Display Duty Ratio 1/4, 1/8, 1/12 or 1/16
- Programmable Timing Signal Duty Ratio 2/16, 4/16, 6/16, 8/16, 10/16, 12/16, 14/16, 15/16
- Display ON/OFF
- Display Data RAM 47x8 bits
- CR Oscillator External CR and capable of clock input from outside
- Serial Data Transfer Clock frequency: 2MHz Max.
- Logic Power Supply 3.0V / 5.0V
- C-MOS
- Package QFP52

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

No.	Symbol	Function
42	V _{DD}	Logic power supply 3.0V / 5.0V
44	V _{SS}	GND V _{SS} =0V
40	V _{FDP}	Power supply for VFD driving
2 ~ 13, 15 ~ 38	DR0~ DR35	Driving signal output The configure of the Segment and Timing drivers is determined by the instruction, refer to (2) Instruction Register.
52	RSTb	Reset If RSTb="L", reset occurs, but data on DDRAM not changing.
51	CSb	Chip select If CSb="L", data transmission is enabled.
48	SCK	Serial clock
49	SI	Serial data input (8-bit/one word)
45, 46	XT, XTb	Connecting external capacitor and resistor, or input clock via this pin If using external clock, input clock signal via XT and keep XTb open.
1, 14, 39, 41, 43, 47, 50	NC	No connect Usually open.

■ FUNCTION DESCRIPTION

(1) Address Counter

The address counter specifies the RAM address, and the display data from CPU is written to the specified address.

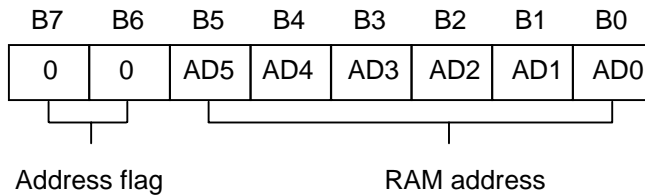
If the upper 2 bits (B7, B6) of the 1st word are “0,0”, the rest 6 bits (B5~B0) will be interpreted as RAM address. The 2nd word will be interpreted as display data and saved on the RAM which address is specified by the B5~B0 of the 1st data.

Once the RAM address is determined by the 1st data, the address counter will automatically increase (+1) for every following word. So there is no need to specify the address for every word for a consecutive data transfer.

During display data writing, even there is unused or not-existing RAM area, be sure to input 8-bit serial data. The data allocated to the above mentioned area is invalid.

The RAM address range varies with programmable duty ratios. For 1/4 duty, the address range is from “00H~0FH”. For 1/8 duty, the range is from “00H~1FH”. For 1/12 duty, the range is from “00H~23H”. For 1/16 duty, the range is from “00H~2FH”. When automatically increased address excess the address range and display data is still transferred from CPU, the address counter will return to “00H” and count up again.

Address Data



DDR4 MAP1

- 1/16 duty (T=16, S=20)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00 _H							
T1	03 _H							
T2	06 _H							
T3	09 _H							
T4	0C _H							
T5	0F _H							
T6	12 _H							
T7	15 _H							
T8	18 _H							
T9	1B _H							
T10	1E _H							
T11	21 _H							
T12	24 _H							
T13	27 _H							
T14	2A _H							
T15	2D _H							
S0	S1	S2	S3	S4	S5	S6	S7	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
01 _H								
04 _H								
07 _H								
0A _H								
0D _H								
10 _H								
13 _H								
16 _H								
19 _H								
1C _H								
1F _H								
22 _H								
25 _H								
28 _H								
2B _H								
2E _H								
S8	S9	S10	S11	S12	S13	S14	S15	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
02 _H								
05 _H								
08 _H								
0B _H								
0E _H								
11 _H								
14 _H								
17 _H								
1A _H								
1D _H								
20 _H								
23 _H								
26 _H								
29 _H								
2C _H								
2F _H								
S16	S17	S18	S19	S20	S21	S22	S23	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
-								
-								
-								
-								
-								
-								
-								
-								
-								
S24	S25	S26	S27					

- 1/12 duty (T=12, S=24)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
T0	00 _H							
T1	03 _H							
T2	06 _H							
T3	09 _H							
T4	0C _H							
T5	0F _H							
T6	12 _H							
T7	15 _H							
T8	18 _H							
T9	1B _H							
T10	1E _H							
T11	21 _H							
T12	-							
T13	-							
T14	-							
T15	-							
S0	S1	S2	S3	S4	S5	S6	S7	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
01 _H								
04 _H								
07 _H								
0A _H								
0D _H								
10 _H								
13 _H								
16 _H								
19 _H								
1C _H								
1F _H								
22 _H								
-								
-								
-								
S8	S9	S10	S11	S12	S13	S14	S15	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
02 _H								
05 _H								
08 _H								
0B _H								
0E _H								
11 _H								
14 _H								
17 _H								
1A _H								
1D _H								
20 _H								
23 _H								
-								
-								
-								
S16	S17	S18	S19	S20	S21	S22	S23	

RAM address	D0	D1	D2	D3	D4	D5	D6	D7
-								
-								
-								
-								
-								
-								
-								
-								
-								
S24	S25	S26	S27					

Not-using RAM area
 Not-existing RAM area

RAM MAP 2

- 1/8 duty (T=8, S=28)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	S3	S4	S5	S6	S7
T0	00 _H															
T1	04 _H															
T2	08 _H															
T3	0C _H															
T4	10 _H															
T5	14 _H															
T6	18 _H															
T7	1C _H															
T8	-															
T9	-															
T10	-															
T11	-															
T12	-															
T13	-															
T14	-															
T15	-															

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S8	S9	S10	S11	S12	S13	S14	S15
01 _H																
05 _H																
09 _H																
0D _H																
11 _H																
15 _H																
19 _H																
1D _H																
-																
-																
-																
-																
-																
-																

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S16	S17	S18	S19	S20	S21	S22	S23
02 _H																
06 _H																
0A _H																
0E _H																
12 _H																
16 _H																
1A _H																
1E _H																
-																
-																
-																
-																
-																

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S24	S25	S26	S27
03 _H												
07 _H												
0B _H												
0F _H												
13 _H												
17 _H												
1B _H												
1F _H												
-												
-												
-												
-												
-												

- 1/4 duty (T=4, S=28)

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S8	S9	S10	S11	S12	S13	S14	S15
01 _H																
05 _H																
09 _H																
0D _H																
-																
-																
-																
-																
-																
-																

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S16	S17	S18	S19	S20	S21	S22	S23
02 _H																
06 _H																
0A _H																
0E _H																
-																
-																
-																
-																
-																

RAM address	D0	D1	D2	D3	D4	D5	D6	D7	S24	S25	S26	S27
03 _H												
07 _H												
0B _H												
0F _H												
-												
-												
-												
-												
-												

Not-using RAM area
 Not-existing RAM area

(2) Instruction Register 1

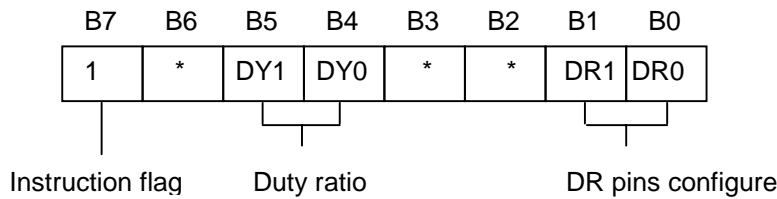
The Instruction Register 1 is used for setting duty ratio and driver (DR) pins configure. If B7 of the 1st word is “1”, the rest 4 bits (B5, B4, B1, B0) is interpreted as instruction 1.

The value on register is initialized to the default by reset signal. But, during power on, the value of register 1 is unspecified, it is necessary to set value in register 1.

The contents of the “Instruction register 1” is initially set up by reset signal, as shown below. Because the NJU3427 is unstable during power on, reset shall be executed.

Instruction Register 1 Default

Duty ratio 1/16
DR pins pattern 1



DY1	DY0	Duty Ratio
0	0	1/16
0	1	1/12
1	0	1/8
1	1	1/4

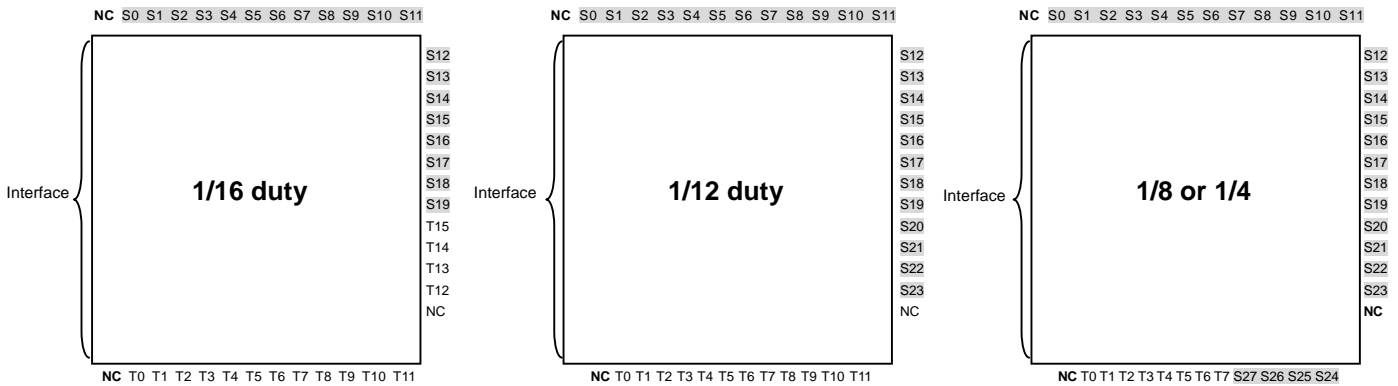
Note): For Segment and Timing pins configure, please refer to “The Relationship Between Duty Ratio and Segment/Timing Pins”. When select 1/4 and 1/8 duty, configures of segment and timing pins are the same.

DR1	DR0	DR configure
0	0	Pattern 1
0	1	Pattern 2
1	0	Pattern 3
1	1	Pattern 4

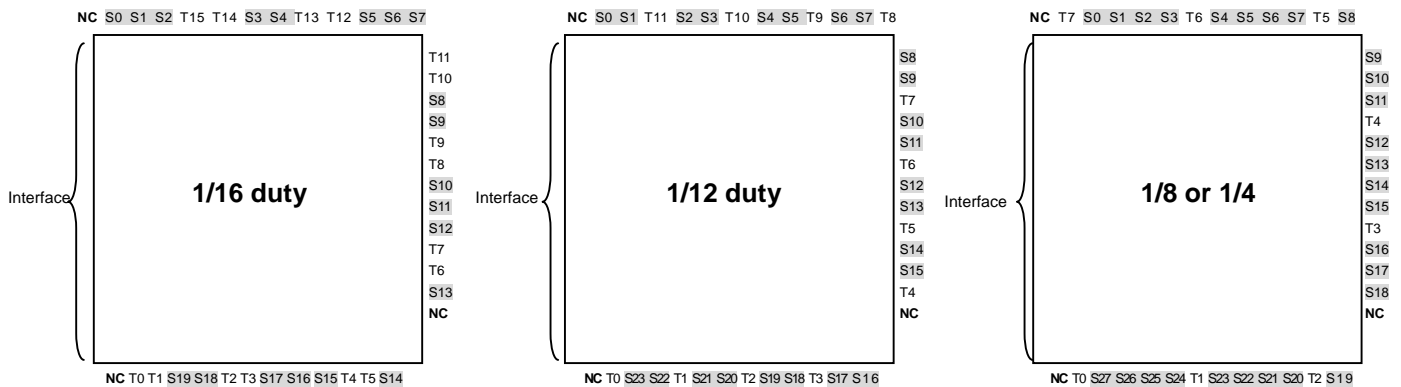
Note): For Segment and Timing pins configure, please refer to “The relationship Between Duty Ratio and Segment/Timing Pins”.

The Relationship Between Duty Ratio and Segment (S)/Timing (T) Pins Configure

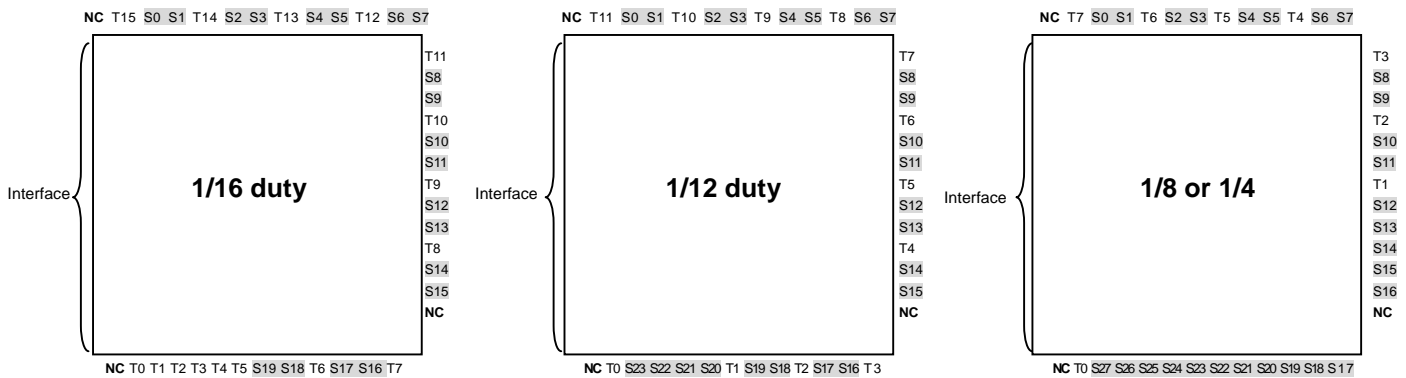
- Pattern 1



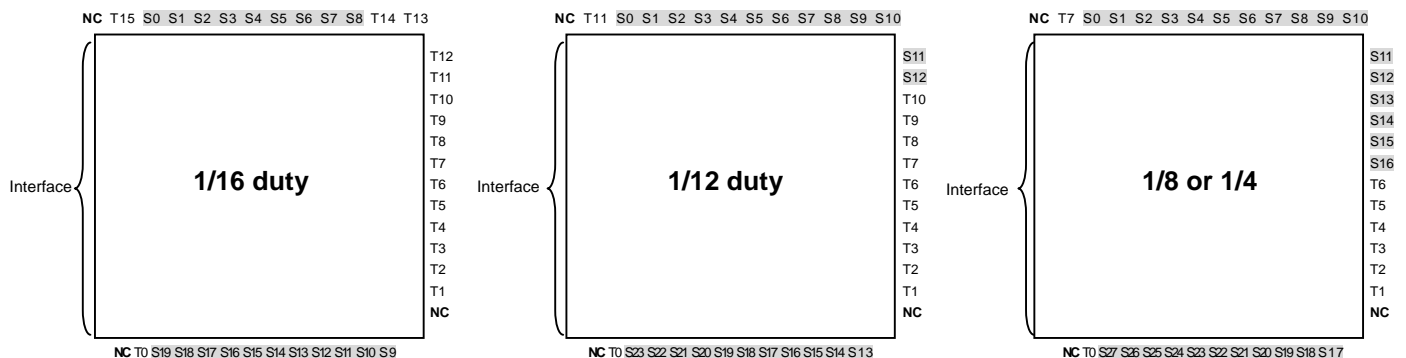
- Pattern 2



- Pattern 3



- Pattern 4



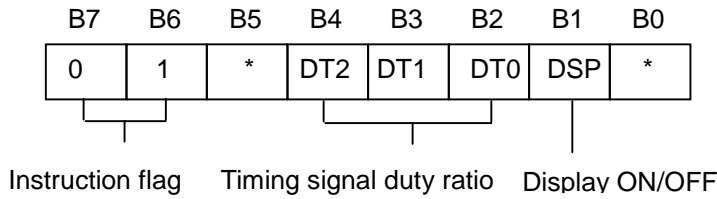
(3) Instruction Register 2

The Instruction Register 2 is used for setting Timing signal duty ratio and controlling display ON/OFF. If B7 and B6 of the 1st word are “0, 1”, the rest 4 bits (B4~B1) is interpreted as instruction 2.

When power on or reset signal input, the Register 2 is initialized as below: Because the NJU3427 is unstable during power on, reset shall be executed.

Instruction Register 2 Default

Timing duty ratio 2/16
 Display ON/OFF OFF



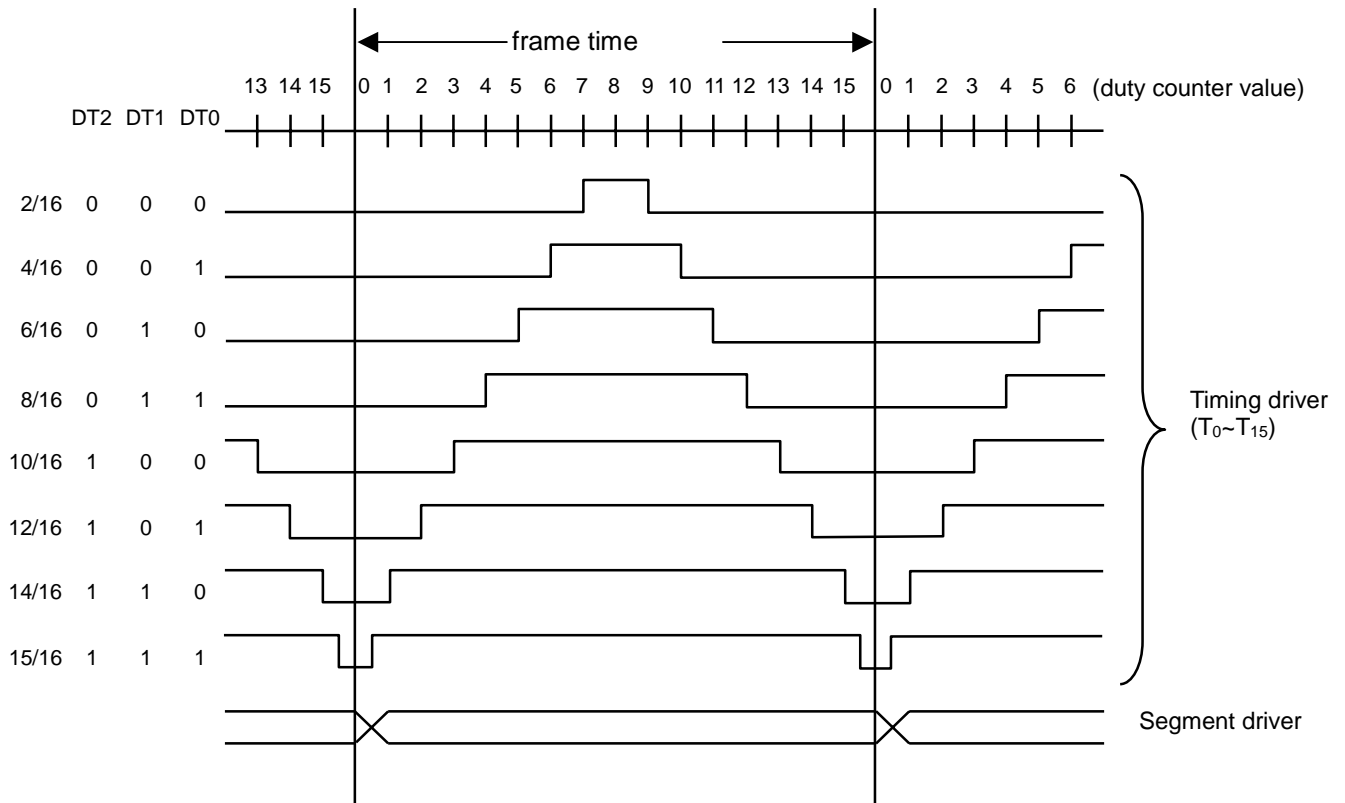
DT2	DT1	DT0	Timing duty ratio
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

Note): For the output waveform, refer to “Timing Signal Duty Ratio”.

DSP	Display control
0	OFF
1	ON

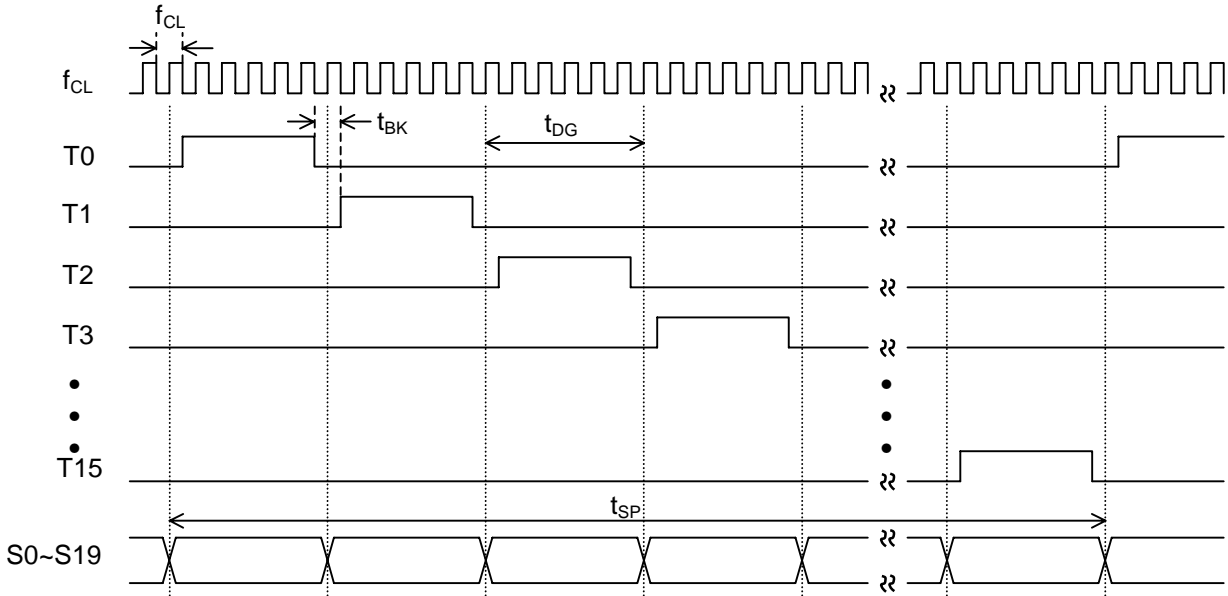
Note): During display off, there is no signal from Timing pins and Segment pins.

● Timing Signal and Duty Ratio



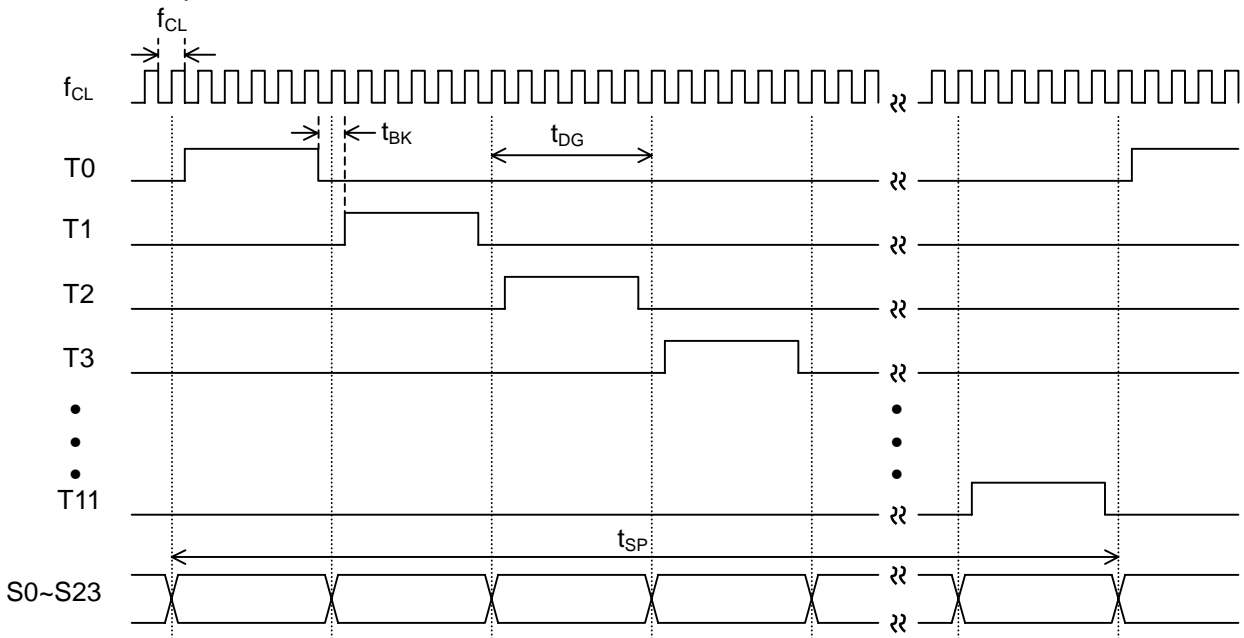
● Display Timing Charter

- Duty ratio 1/16



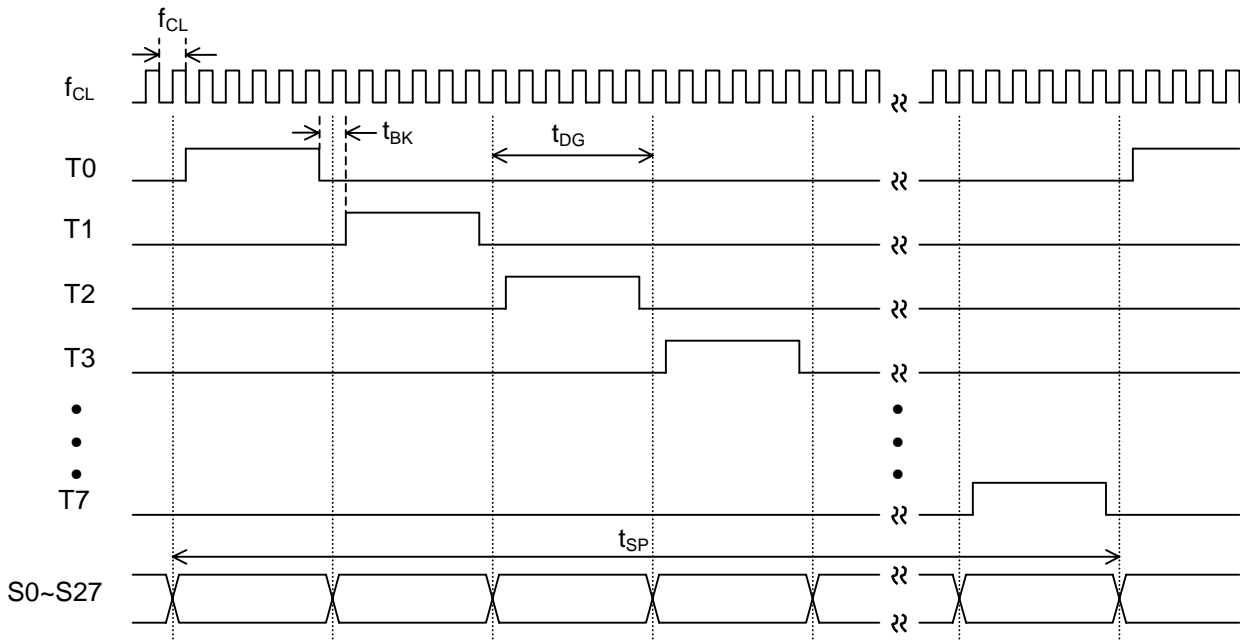
External Clock Frequency	800kHz~2.5MHz	f_{CL}
Minimum Blinking Time (Timing Signal Duty Ratio = 15/16)	40 μ s~12.8 μ s	$t_{BK}=(1/f_{CL}) \times 16 \times 2$
1-character display time	640 μ s ~204.8 μ s	$t_{DG}=t_{BK} \times 16$
Frame time	10.24ms~3.2768ms	$t_{SP}=t_{DG} \times 16$

- Duty ratio 1/12



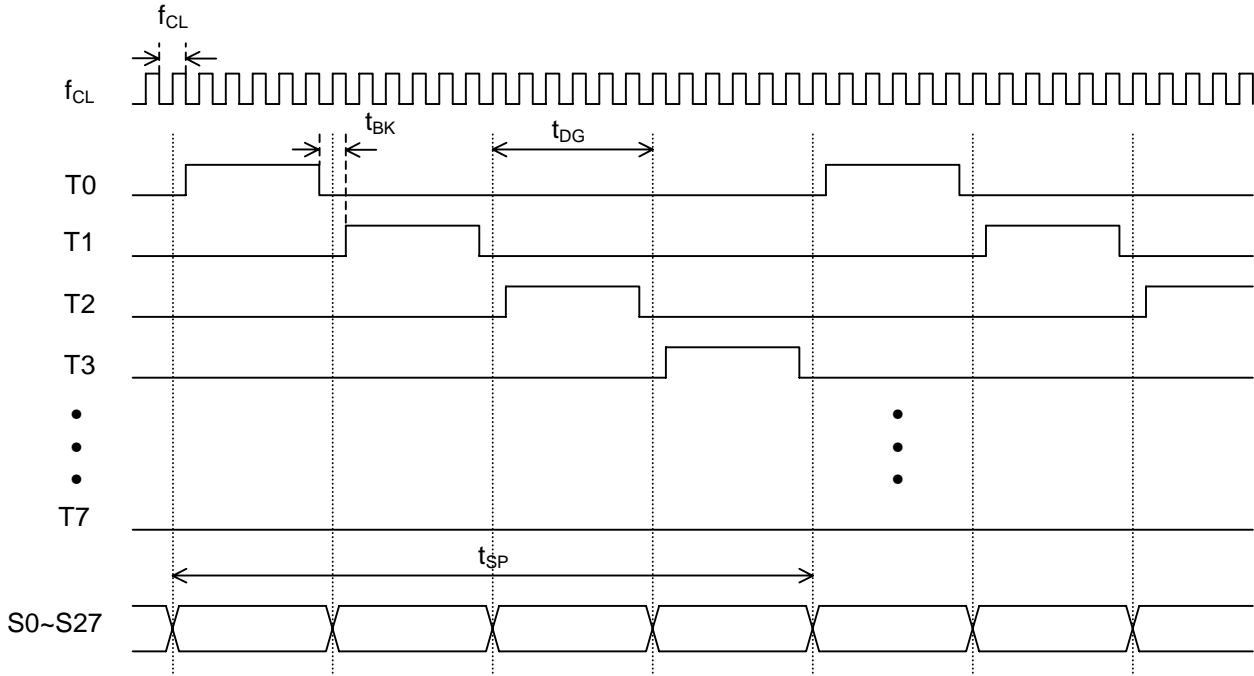
External Clock Frequency	800kHz~2.5MHz	f_{CL}
Minimum Blinking Time (Timing Signal Duty Ratio = 15/16)	55 μ s~17.6 μ s	$t_{BK}=(1/f_{CL}) \times 22 \times 2$
1-character display time	880 μ s ~281.6 μ s	$t_{DG}=t_{BK} \times 16$
Frame time	10.56ms~3.3792ms	$t_{SP}=t_{DG} \times 12$

- Duty Ratio 1/8



External Clock Frequency	800kHz~2.5MHz	(f_{CL})
Minimum Blanking Time (Timing Signal Duty Ratio = 15/16)	80 μ s~25.6 μ s	$t_{BK} = (1/f_{CL}) \times 32 \times 2$
1-character display time	1.28ms~409.6 μ s	$t_{DG} = t_{BK} \times 10$
Frame time	10.24ms~3.2768ms	$t_{SP} = t_{DG} \times 8$

- Duty ratio 1/4 (T4~T7 output pins)

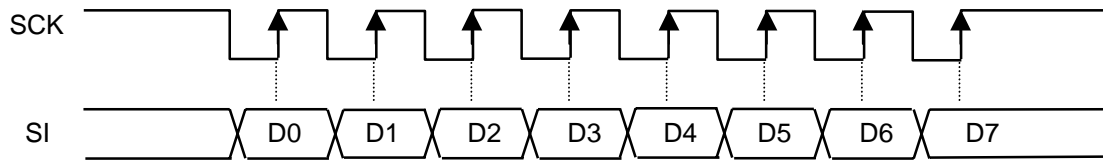


External Clock Frequency	800kHz~2.5MHz	(f_{CL})
Minimum Blanking Time (Timing Signal Duty Ratio = 15/16)	160 μ s~51.2 μ s	$t_{BK} = (1/f_{CL}) \times 64 \times 2$
1-character display time	2.56ms~819.2 μ s	$t_{DG} = t_{BK} \times 16$
Frame time	10.24ms~3.2768ms	$t_{SP} = t_{DG} \times 4$

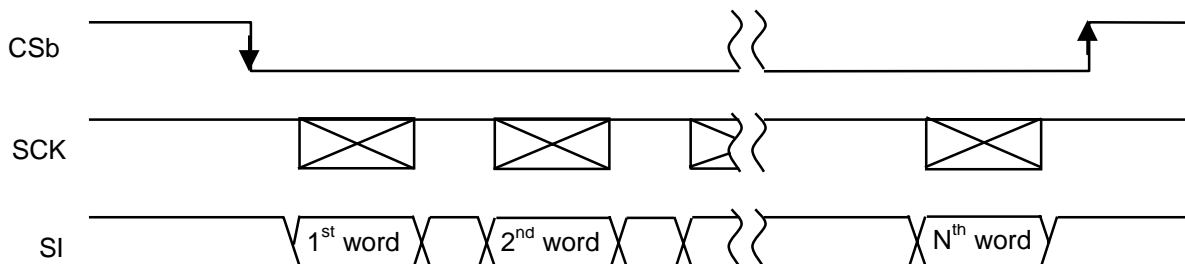
(4) Serial Interface

8-bit per word serial data is transferred from CPU to NJU3427 with synchronous clock signal (SCK). At the every rising edge of the SCK, data is taken in, and at the rising edge of CSb, the data of words are latched.

If the 1st data is address data when CSb becoming “L”, without changing CSb, the following data will be interpreted as display data. If the 1st data is instruction, without changing CSb signal, all the following data is invalid.



Serial data transmission



Serial data transmission format

- Serial Data
1st word

Address data

B7	B6	B5	B4	B3	B2	B1	B0
0	0	AD5	AD4	AD3	AD2	AD1	AD0

Instruction 1

B7	B6	B5	B4	B3	B2	B1	B0
1	*	DY1	DY0	*	*	DR1	DR0

*:don't care

Instruction 2

B7	B6	B5	B4	B3	B2	B1	B0
0	1	*	DT2	DT1	DT0	DSP	*

*:don't care

From the 2nd word

- If the 1st word is address data display data
- If the 1st word is instruction data invalid data

(5) Reset Circuit

If RSTb="L", reset circuit functions, and the following default is set up. Because the NJU3427 is unstable during power on, reset shall be executed.

Address Data

(AD0, AD1, AD2, AD3, AD4, AD5): (0, 0, 0, 0, 0, 0)

Instruction Register 1

Duty ratio	1/16
DR pins configure	Pattern 1

Instruction Register 2

Timing signal duty ratio	2/16
Display ON/OFF	OFF

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Conditions
Power Supply	V_{DD}	-0.3~+7.0	V	
Input Voltage	V_{IN}	-0.3~ $V_{DD}+0.3$	V	
VFD Driving Voltage	V_{FDP}	$V_{DD}-45\sim V_{DD}+0.3$	V	V_{DD} as reference voltage
H Level Output Current 1	I_{OH1}	-35	mA	DR ₀ output, signal pin
H Level Output Current 2	I_{OH2}	-15	mA	DR ₁ ~ DR ₃₅ output, signal pin
L Level Output Current	I_{OL}	20	mA	
Operating Temperature	Topr	-40 ~ 85	°C	
Storage Temperature	Tstg	-55 ~ 125	°C	
Power Dissipation	PD	900	mW	Glass epoxy board (76.2 x114.3x1.6mm)

Note 1): The IC must be used within the Absolute Maximum Ratings, otherwise, an electrical or physical stress may cause a permanent damage to it.

Note 2): De-coupling capacitors should be placed between $V_{DD}-V_{SS}$ and $V_{FDP}-V_{SS}$.

Note 3): The condition of $V_{DD} > V_{SS} \geq V_{FDP}$ and $V_{SS}=0$ must be maintained.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics 1

($V_{DD}=5.0V$, $V_{SS}=0V$, $T_a=-40 \sim 85^\circ C$)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Power Supply (1)	V_{DD}	V_{DD} pin	4.5	-	5.5	V	
Power Supply (2)	V_{FDP}	V_{FDP} pin and V_{DD} as reference	-40	-	V_{SS}	V	
H Level Input Voltage	V_{IH}	XT, RSTb, CSb, SCK, SI pins	$0.8V_{DD}$	-	-	V	
L Level Input Voltage	V_{IL}		-	-	$0.2V_{DD}$		
Input off-leak current	I_{IZ}	CSb, SCK, SI pins $V_{DD}=5.5V$, $V_I=0$ or $5.5V$	-	-	± 1	μA	
Display Current	I_{OH}	DR ₀ pin	$V_{DD}=4.5V$, $V_{FDP}=V_{DD}-40$	-11.5	-20	-	mA
		DR ₁ ~ DR ₃₅ pin	V_I , $V_{OH}=V_{DD}-2.25V$	-5.5	-10	-	mA
Pull-up Resistance	R_{UR}	RSTb pin, $T_a=25^\circ C$, $V_I=V_{SS}$	100	-	300	k Ω	
Pull-down Resistance	R_{DST}	DR ₀ ~ DR ₃₅ pins, $T_a=25^\circ C$ $V_I=V_{DD}$, $V_{FDP}=V_{DD}-40V$	75	-	195	k Ω	
Logic Circuit Power Supply	I_{SS}	V_{SS} pin CR oscillation ($R=6.8k\Omega$, $C=100pF$), All Segment/Timing pins open, RSTb open All Segment/Timing pins output display OFF signal.	-	0.6	0.8	mA	
Operation Current	I_{FDP}	V_{FDP} pin, $V_{FDP}=V_{DD}-40V$, CR oscillation ($R=6.8k\Omega$, $C=100pF$), All driving pins output display ON signal	-	12	16.5	mA	
CR Oscillation Frequency	f_{CR}	$T_a=25^\circ C$ $R=6.8k\Omega$, $C=100pF$	1.05	1.13	1.21	MHz	

• AC Characteristics 1

($V_{DD}=5.0V$, $V_{SS}=0V$, $T_a=-40 \sim 85^\circ C$)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External Clock Frequency	f_{CL}	Fig 1	0.8	-	2.5	MHz
Width of External Clock Pulse	t_{CLH} , t_{CLL}	Fig 1	200			ns
Data Setup Time	t_{SIS}	Fig2	35			ns
Data Hold Time	t_{SIH}	Fig2	35			ns
Clock Frequency	f_{SCK}	Fig3			2.0	MHz
Clock Pulse Width	t_{SCKH} , t_{SCKL}	Fig3	200			ns
External Clock Rising Time, Falling Time	t_{CLH} , t_{CLL}	Fig2			250	ns
Clock Interval Time	t_{SCI}	Fig3	10			μs
Reset Pulse Width	t_{RSTb}	Fig4	10			μs

• DC Characteristics 2

(V_{DD}=3.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Power Supply (1)	V _{DD}	V _{DD} pin	2.7	-	3.6	V	
Power Supply (2)	V _{FDP}	V _{FDP} pin and V _{DD} as reference	-40	-	V _{SS}	V	
H Level Input Voltage	V _{IH}	XT, RSTb, CSb, SCK, SI pins	0.8V _{DD}	-	-	V	
L Level Input Voltage	V _{IL}		-	-	0.2V _{DD}		
Input off-leak current	I _{IZ}	CSb, SCK, SI pins V _{DD} =3.6V, V _I =0 or 3.6V	-	-	±1	μA	
Display Current	I _{OH}	DR ₀ pin	V _{DD} =2.7V, V _{FDP} =V _{DD} -40	-5.0	-9.0	-	mA
		DR ₁ ~ DR ₃₅ pin	V _I , V _{OH} =V _{DD} -1.35V	-2.5	-4.0	-	mA
Pull-up Resistance	R _{UR}	RSTb pin, Ta=25°C, V _I =V _{SS}	100	-	300	kΩ	
Pull-down Resistance	R _{DST}	DR ₀ ~ DR ₃₅ pins, Ta=25°C V _I =V _{DD} , V _{FDP} =V _{DD} -40V	75	-	195	kΩ	
Logic Circuit Power Supply	I _{SS}	V _{SS} pin CR oscillation (R=4.7kΩ, C=100pF), All Segment/Timing pins open, RSTb open All Segment/Timing pins output display OFF signal.	-	0.25	0.35	mA	
Operation Current	I _{FDP}	V _{FDP} pin, V _{FDP} =V _{DD} -40V, CR oscillation (R=4.7kΩ, C=100pF), All driving pins output display ON signal	-	12	16.5	mA	
CR Oscillation Frequency	f _{CR}	Ta=25°C R=4.7kΩ, C=100pF	1.05	1.13	1.21	MHz	

• AC Characteristics 2

(V_{DD}=3.0V, V_{SS}=0V, Ta=-40 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External Clock Frequency	f _{CL}	Fig 1	0.8	-	2.5	MHz
Width of External Clock Pulse	t _{CLH} , t _{CLL}	Fig 1	200			ns
Data Setup Time	t _{SIS}	Fig2	35			ns
Data Hold Time	t _{SIH}	Fig2	35			ns
Clock Frequency	f _{SCK}	Fig3			2.0	MHz
Clock Pulse Width	t _{SCKH} , t _{SCKL}	Fig3	200			ns
External Clock Rising Time, Falling Time	t _{CLH} , t _{CLL}	Fig2			250	ns
Clock Interval Time	t _{SCI}	Fig3	10			μs
Reset Pulse Width	t _{RSTb}	Fig4	10			μs

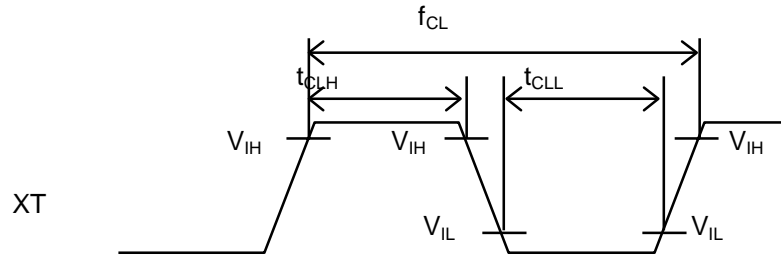


Fig1

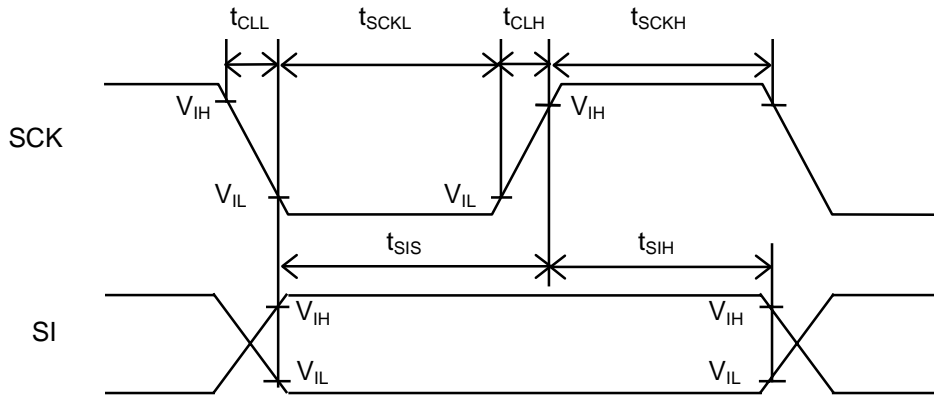


Fig2

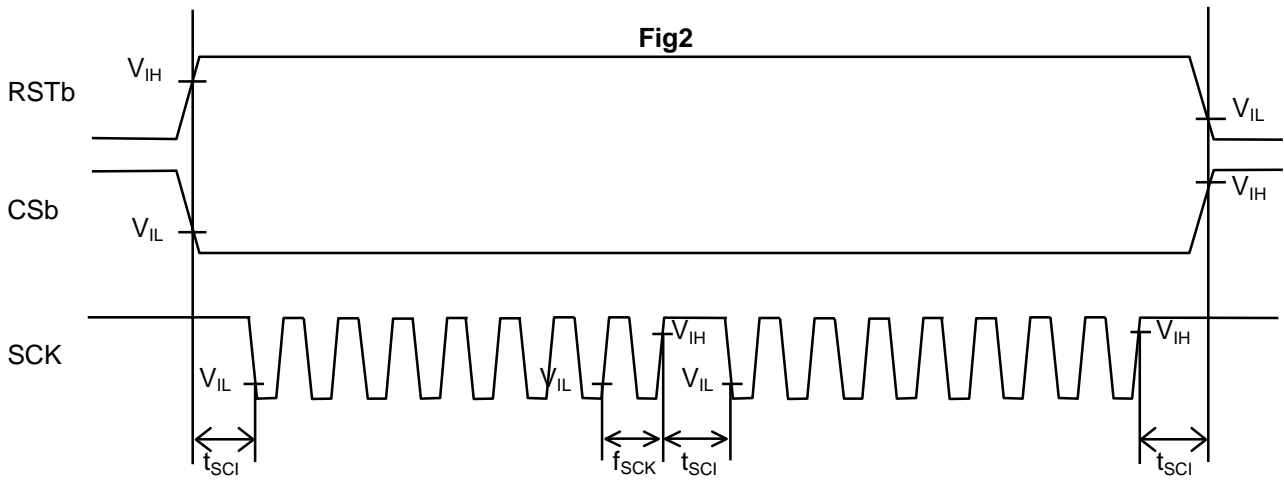


Fig3

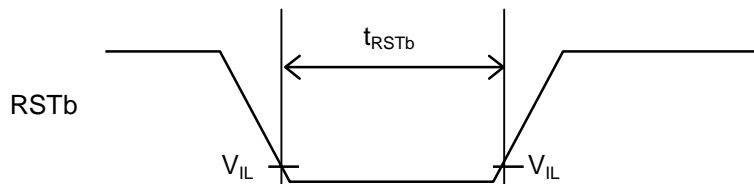
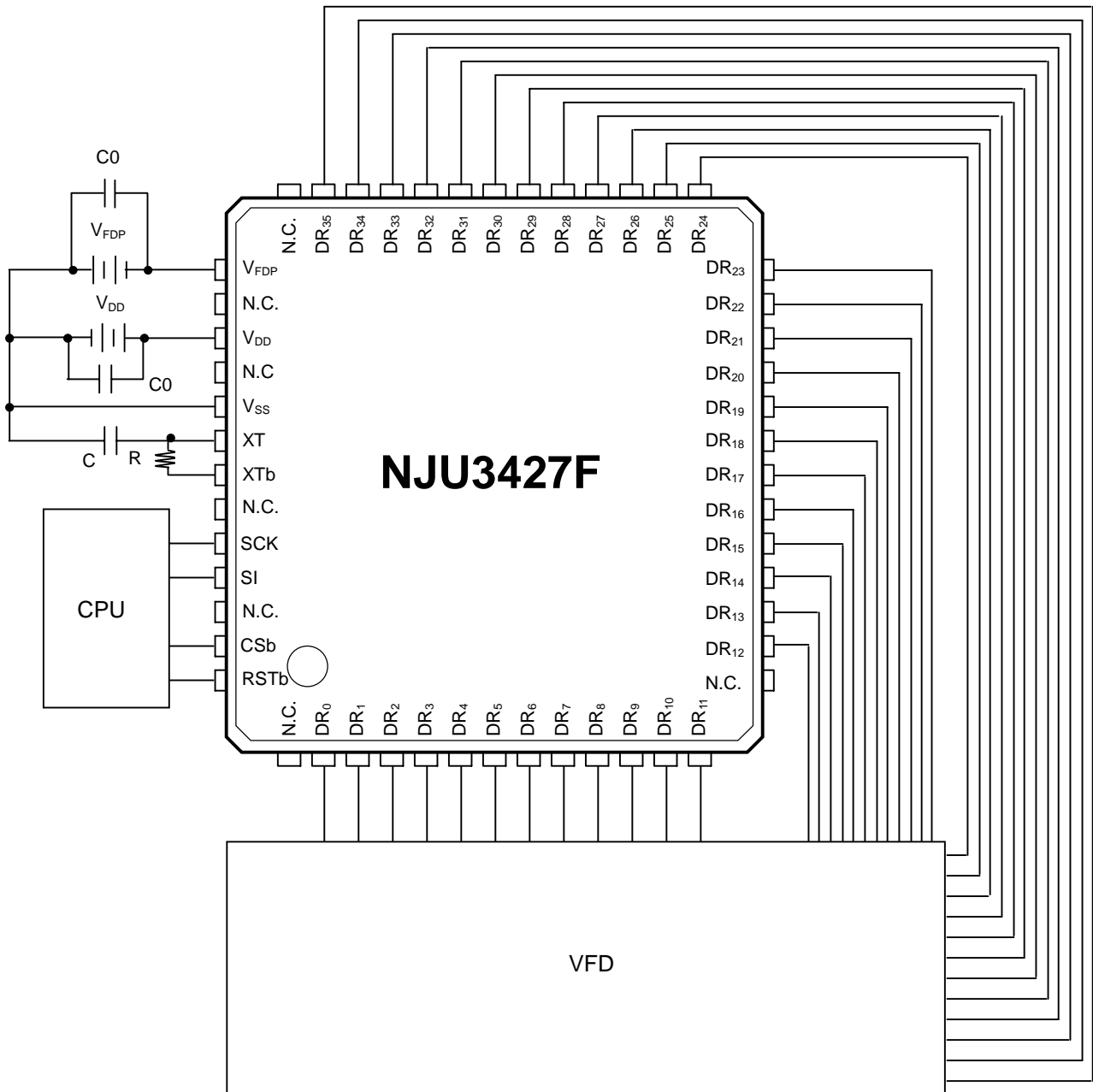


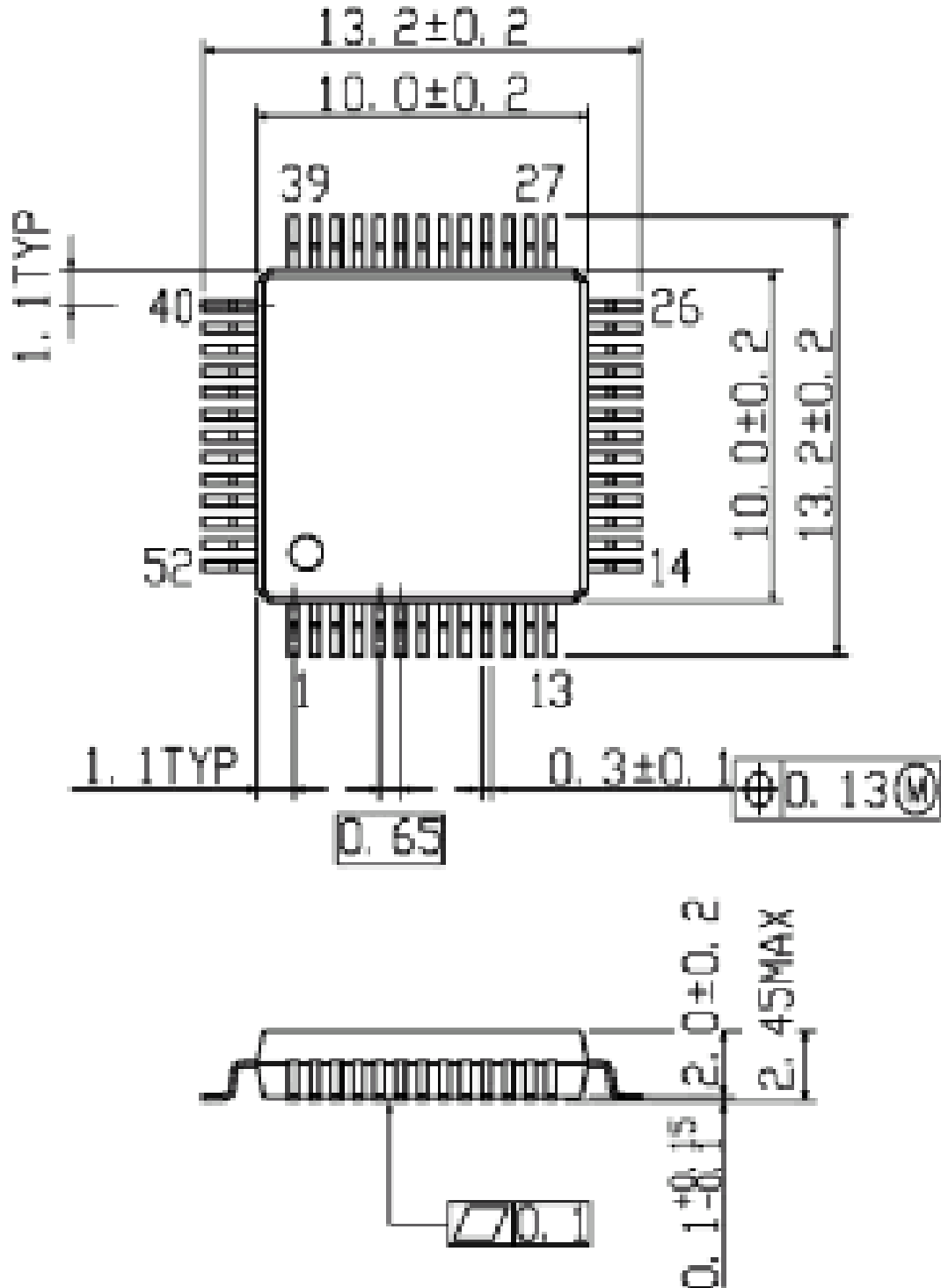
Fig4

■ APPLICATION CIRCUIT (CR OSCILLATION)



* Pay careful attention to reduce the noise from power supply and interface pins.

■ QFP52 PACKAGE



[CAUTION]
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