

20-BIT SERIAL TO PARALLEL CONVERTER

■ GENERAL DESCRIPTION

The NJU3718 is a 20-bit serial to parallel converter especially apply to MPU output expander.

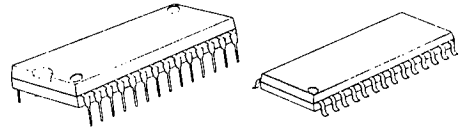
The effective output assignment of MPU is available as the connection between NJU3718 and MPU is required only 4 lines.

Up to 5MHz signal can be input to the serial data input terminal and the data is output from parallel output buffer through serial in parallel out shift register and parallel data latches.

Furthermore, the NJU3718 output the serial data from SO terminal through the shift register, therefore output bit number can increase by cascade connection.

The hysteresis input circuit realized wide noise margin and high drivability output buffer (25mA) can drive LED directly.

■ PACKAGE OUTLINE



NJU3718L

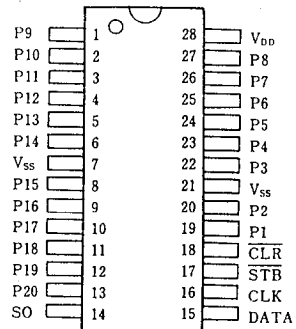
NJU3718G

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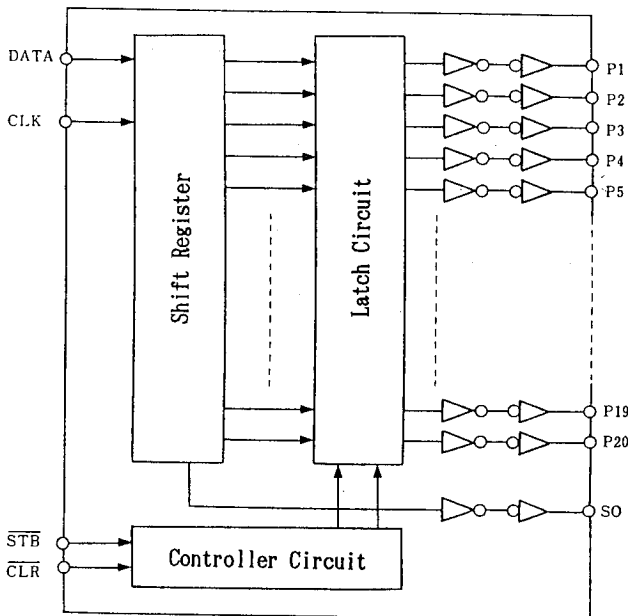
■ FEATURES

- 20-Bit Serial In Parallel Out
- Cascade Connection
- Hysteresis Input ---- 0.5V typ
- Operating Voltage ---- 5V±10%
- Operating Frequency ---- 5MHz or more
- Output Current ---- 25mA
- C-MOS Technology
- Package Outline ---- SDIP/SOP 28

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

| NO. | SYMBOL | F U N C T I O N | NO. | SYMBOL | F U N C T I O N |
|-----|-----------------|--|-----|-------------------------|--|
| 1 | P9 | Parallel Converts Data Output Terminals | 15 | DATA | Serial Data Input Terminal |
| 2 | P10 | | 16 | CLK | Clock Signal Input Terminal |
| 3 | P11 | | 17 | $\overline{\text{STB}}$ | Strobe Signal Input Terminal |
| 4 | P12 | | 18 | $\overline{\text{CLR}}$ | Clear Signal Input Terminal |
| 5 | P13 | | 19 | P1 | Parallel Converts Data Output Terminals |
| 6 | P14 | | 20 | P2 | |
| 7 | V _{SS} | GND | 21 | V _{SS} | GND |
| 8 | P15 | Parallel Converts Data Output Terminals | 22 | P3 | Parallel Converts Data Output Terminals |
| 9 | P16 | | 23 | P4 | |
| 10 | P17 | | 24 | P5 | |
| 11 | P18 | | 25 | P6 | |
| 12 | P19 | | 26 | P7 | |
| 13 | P20 | | 27 | P8 | |
| 14 | S0 | Serial Data Output Terminal | 28 | V _{DD} | Power Supply Terminal |

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■ FUNCTIONAL DESCRIPTION
(1) Reset

When the "L" level is input to the $\overline{\text{CLR}}$ terminal, all latches are reset and all parallel conversion output are "L" level.

Normally, the $\overline{\text{CLR}}$ terminal should be "H" level.

(2) Data Transmission

In the $\overline{\text{STB}}$ terminal is "H" level and input the clock signal to the CLK terminal, the serial data input from DATA terminal shift in the shift register by synchronizing at rising edge of the clock signal.

When the $\overline{\text{STB}}$ terminal change to "L" level, the data in the shift register transfer to the latch.

Even if the $\overline{\text{STB}}$ terminal is "L" level, the input clock signal shift the data in the shift register, therefore, the clock signal control is needed.

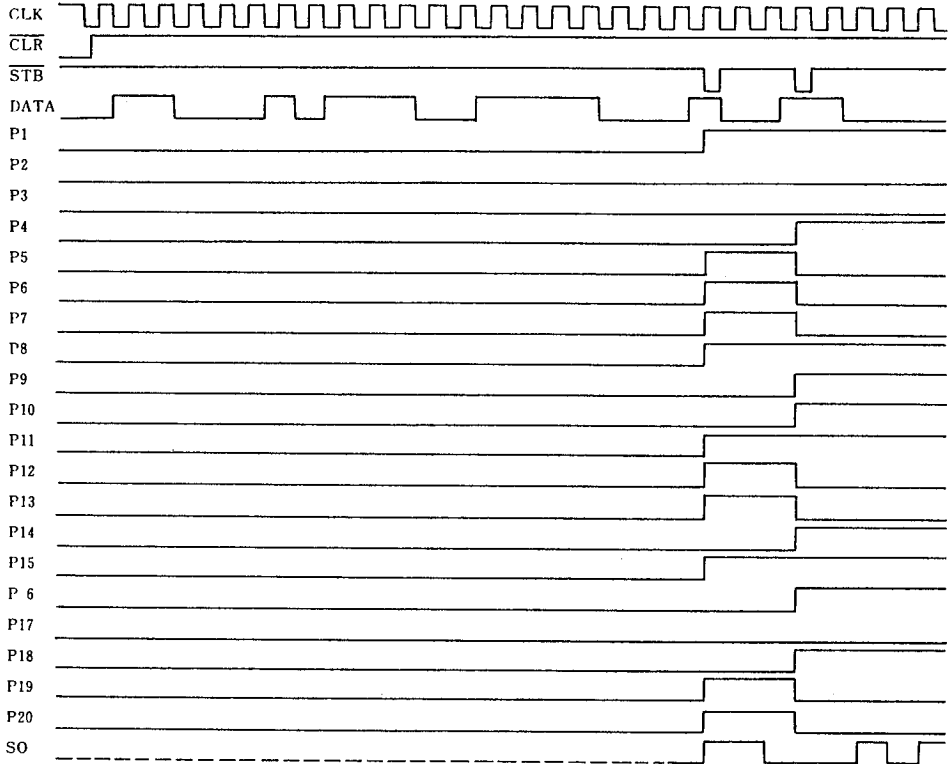
(3) Cascade Connection

The serial data input from DATA terminal output from the S0 terminal through internal shift register unrelated the $\overline{\text{CLR}}$ and $\overline{\text{STB}}$ status.

Furthermore, the 4 input terminals have a hysteresis characteristics by using the schmitt trigger structure to protect the noise.

| CLK | $\overline{\text{STB}}$ | $\overline{\text{CLR}}$ | O P E R A T I O N |
|-----|-------------------------|-------------------------|--|
| X | X | L | All latch are reset (the data in the shift register is no change). All of Parallel convert output are "L". |
| | H | H | The serial data input from DATA terminal input to the shift register. In this stage, the data in the latch is no change. |
| L | L | H | The data in the shift register transfer to the latch. And the data in the latch output from parallel output. |
| H | | | |
| | L | H | The CLK input in the $\overline{\text{STB}}$ ="L" and $\overline{\text{CLR}}$ ="H" state, the data shift in the shift register and latched data also change in accordance with the shift register. |

Note) X: Don't care

■ TIMING CHART

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-----------------------------|------------------|---|------|
| Supply Voltage Range | V _{DD} | - 0.5 ~ + 7.0 | V |
| Input Voltage Range | V _I | V _{SS} -0.5 ~ V _{DD} +0.5 | V |
| Output Voltage Range | V _O | V _{SS} -0.5 ~ V _{DD} +0.5 | V |
| Output Current | I _O | ±25 | mA |
| Power Dissipation | P _D | 700 (SDLP) 500 (SDP) | mW |
| Operating Temperature Range | T _{OPR} | -25 ~ +85 | °C |
| Storage Temperature Range | T _{STG} | -65 ~ +150 | °C |

DC ELECTRICAL CHARACTERISTICS

 (V_{DD}=4.5~5.5V, V_{SS}=0V, T_a=25°C)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|---------------------------|------------------|---|---------------------------------|----------------------|--------------------|------|
| Operating Current | I _{DDs} | V _{IH} =V _{DD} , V _{IL} =V _{SS} | | | 0.1 | mA |
| Output Voltage | High-Level | V _{OH} | I _{OH} =-0.4mA | SO Terminal | V _{DD} | V |
| | Low-Level | V _{OL} | I _{OL} =+3.2mA | | V _{SS} | |
| Input Voltage | High-Level | V _{IH} | | 0.7V _{DD} | V _{DD} | V |
| | Low-Level | V _{IL} | | V _{SS} | 0.3V _{DD} | |
| Input Leakage Current | I _{LI} | V _I =0~V _{DD} | -10 | | 10 | μA |
| High-Level Output Voltage | V _{OHD} | I _{OH} =-25mA | P1~P20 Terminals (Note 1) | V _{DD} -1.5 | V _{DD} | V |
| | | I _{OH} =-15mA | | V _{DD} -1.0 | V _{DD} | |
| | | I _{OH} =-10mA | | V _{DD} -0.5 | V _{DD} | |
| Low-Level Output Voltage | V _{OLD} | I _{OL} =+25mA | (Note 1) | V _{SS} | 1.5 | V |
| | | I _{OL} =+15mA | | V _{SS} | 0.8 | |
| | | I _{OL} =+10mA | | V _{SS} | 0.4 | |
| Output Short Current | I _{OS} | V _O =7V, V _I =0V | SO Terminal (Note 2) | | 10 | mA |
| | | V _O =0V, V _I =7V | | | -10 | |
| | I _{OSD} | V _O =7V, V _I =0V | P1~P20 Terminals (Note 2) | | 20 | mA |
| | | V _O =0V, V _I =7V | | | -20 | |

Note 1) Specified value represent output current per pin. When use, total current consideration and less than power dissipation rating operation should be required.

Note 2) V_{DD}=7V, V_{SS}=0V, 1 second per pin.

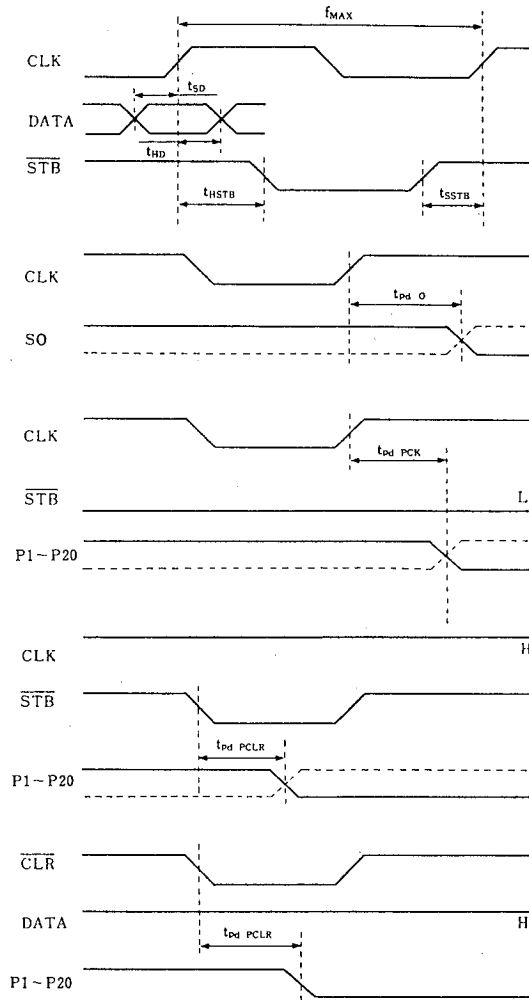
SWITCHING CHARACTERISTICS

 (V_{DD}=4.5V~5.5V, V_{SS}=0V, T_a=-20~75°C)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------|---------------------|--------------|-----|-----|-----|------|
| Set-Up Time | t _{SD} | DATA - CLK | 20 | | | ns |
| Hold Time | t _{HD} | CLK - DATA | 20 | | | ns |
| Set-Up Time | t _{SSTB} | STB - CLK | 30 | | | ns |
| Hold Time | t _{HSTB} | CLK - STB | 30 | | | ns |
| Output Delay Time | t _{pdO} | CLK - SO | | | 70 | ns |
| | t _{pdPCK} | CLK - P1~P20 | | | 100 | ns |
| | t _{pdPSTB} | STB - P1~P20 | | | 80 | ns |
| | t _{pdPCLR} | CLR - P1~P20 | | | 80 | ns |
| Max. Operating Frequency | f _{MAX} | | 5 | | | MHz |

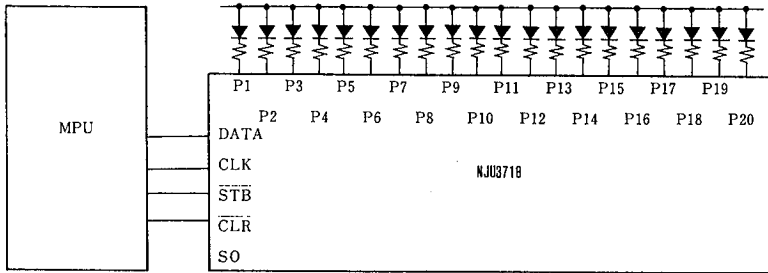
*) C_{OUT}=50pF

■ SWITCHING CHARACTERISTICS TEST WAVEFORM



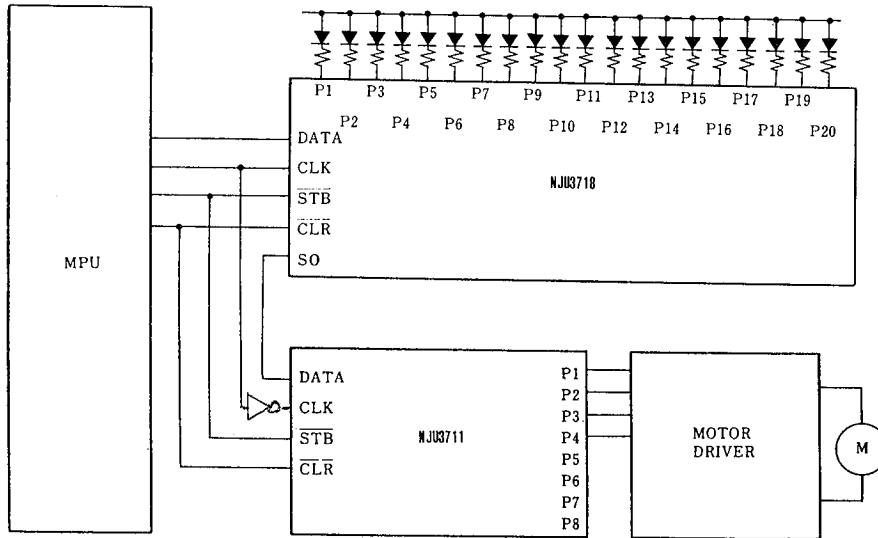
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■ APPLICATION CIRCUIT (1)



■ APPLICATION CIRCUIT (2) (Combined with NJU3711)

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MEMO

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