PRELIMINARY

SERIAL I/O REAL TIME CLOCK WITH WAKE-UP OUTPUT for EXTERNAL CLOCK

■ GENERAL DESCRIPTION

The NJU6359 series is serial I/O and external clock using Real Time Clock with wake-up function suitable for microprocessor.

It contains timer counter, shift register, and interface controller.

It is able to simplify of the external crystal because of the external clock signal using for 32kHz or 384kHz.

The operating voltage is as wide as 2.0V to 5.5V, consequently, the NJU6359 can count accurate time data even if the back up period. And also the wake-up signal outputs by fixed cycle of 720 μS.

The data transfer with MPU operated by 2-wire serial transfer.

Furthermore, the long time back up is available as the current consumption during the back up period is a few.

■ PACKAGE OUTLINE

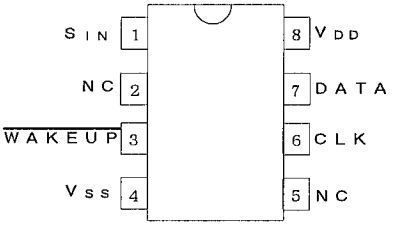
NJU6359V

NJU6359C

■ FEATURES

- Operating Voltage : 3.0V±20%
  2.0V to 5.5V(The clock operation)
- Low operating current : 0.25μA (Typ.) at 3.0V(NJU6359A)
  1.0 μA (Max.) at 3.0V(NJU6359A)
- BCD Counts of Seconds, Minutes, Hours, Days of week, Date, Month and Year
- Required only 2-port for MCU interface (DATA and CLK)
- Automatic Leap Year Compensation: Up to AD 2099
- WAKE-UP function :720 μs cycle
- Package Outline : SSOP 8/Chip
- C-MOS Technology

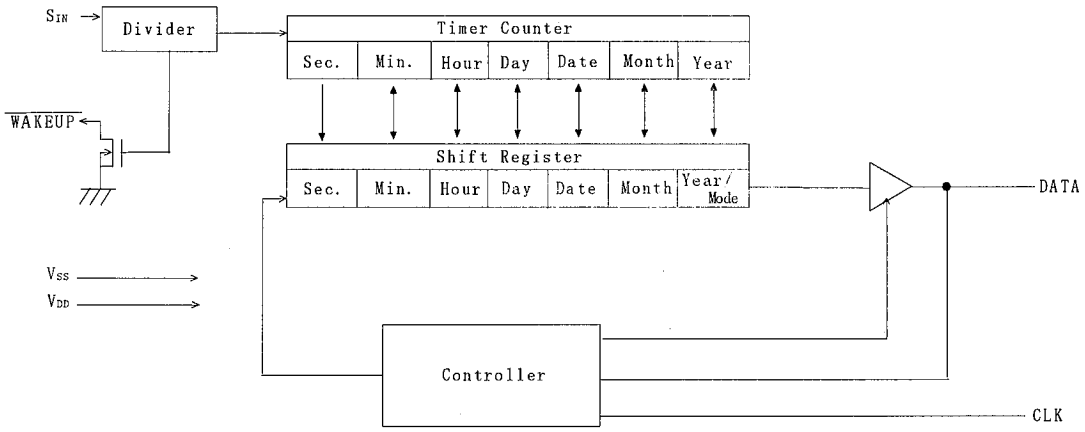
■ PIN CONFIGURATION



■ LINE UP

Device Name	Input frequency
NJU6359A	32kHz
NJU6359B	384kHz

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	F U N C T I O N
1	SIN	I	32kHz or 384kHz input terminal It is different 32kHz and 384kHz by line up. Note)If the accuracy clock is needed, 32.0kHz or 384.0kHz shuold input. Because, It makes the 1Hz by the dividing clock input from this terminal.
3	$\overline{\text{WAKE-UP}}$	O	WAKE-UP Output terminal(N-channel open-drain.) It Outputs the "L" level signal in 720μ S cycle.
4	VSS	Power	GND
6	CLK	I	Clock Input Terminal.(with a pull-down resistor.) The Data Input/Output is synchronized by this clock. When the no accessing, this terminal should be connected to VSS.
7	DATA	I/O	Serial timer data input/output terminal. (with a pull-down resistor.) When the no accessing, this terminal should be connected to VSS. Because the pull-down resistor is valid at the input mode, and, this terminal is VSS. The pull-down resistor is invalid at the output mode.
8	VDD	Power	Power supply
2,5	NC	-	Non connection (Normally open)

■ FUNCTIONAL DESCRIPTION

1.Timer and System control data format

The NJU6359 using BCD code which consisting of 4 bits per 1 digit.

The calendar function including the last data of each month and the leap year calculation is executed automatically.

The system control data is operated wake-up control.

The unused bit for the Timer and System control data is "0".

Only the system control data can be set instead of setting whole timer data.

< System control data format >

	MSB			LSB
System control data block	0	0	0	WK

WK : WAKE-UP control bit

< Timer data format >

	MSB						LSB	Range
				0	0	0	WK	
Second	0	S6	S5	S4	S3	S2	S1	S0	0～59
Minute	0	m6	m5	m4	m3	m2	m1	m0	0～59
Hour	0	0	H5	H4	H3	H2	H1	H0	0～23
Days of week					0	W2	W1	W0	1～ 7
Date	0	0	D5	D4	D3	D2	D1	D0	1～31
Month	0	0	0	M4	M3	M2	M1	M0	1～12
Year	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0～99

2.Start bit, Stop bit

The NJU6359 is decided "Start bit, Stop bit" in order to recognize the start and stop of the Data Input/Output. The fix data needs to input about the timer data write/read, only the system control data write. But, in case of the Stop bit of the timer data read, The NJU6359 generated and outputs. The data is changed over from Output to Input by output of Stop bit. There "Start bit, Stop bit" is using the unused arrangement in BCD code.

< Start bit format >

① Timer data writing

MSB							LSB	
0	1	0	1	1	1	1	1	(5F)H

② Timer data reading

MSB							LSB	
1	1	0	1	1	1	1	1	(DF)H

③ Only the system control data writing

MSB							LSB	
1	0	0	1	1	1	1	1	(9F)H

< Stop bit format >

① Timer data writing/reading, Only the system control data writing

MSB							LSB	
0	0	0	1	1	1	1	1	(1F) H

3. Only the system control data writing

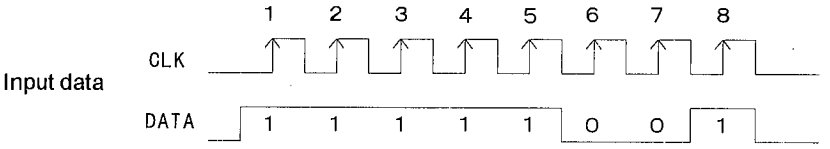
The data can be written into the shift register in the NJU6359 from the DATA terminal synchronized with the rising edge of the clock signal input from the CLK terminal.

At first, Start bit for writing of only the system control data is writing into NJU6359, Therefore into the writing mode.

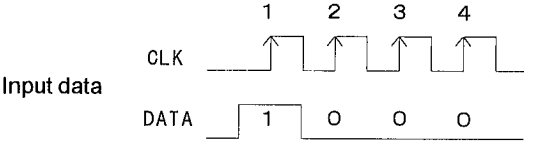
At second, System control data is writing into NJU6359, and the last 4 bits is effective.

At last, Stop bit is writing, after the Writing system control data concluded. The system control data is written into the internal register with the falling edge of the clock signal, after the writing stop bit. The data writing is operated from LSB first.

< Writing start bit timing >

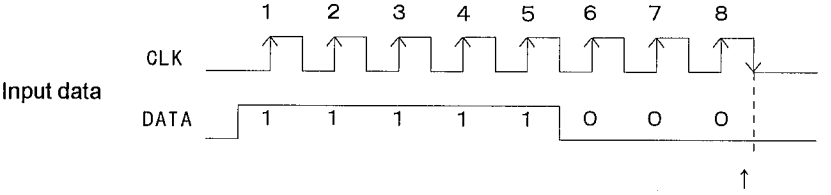


< Writing system control data timing >



(In case of using the wake-up output)

< Writing stop bit timing >



(The system control data is written into the internal register with the falling edge of the 8th clock.)

4.Timer data writing

The timer data can be written into the shift register in the NJU6359 from the DATA terminal synchronized with the rising edge of the clock signal input from the CLK terminal.

At first, Start bit for writing of the timer data is writing into NJU6359, Therefore into the writing mode. And then, the divider is stop, and the contents of data is cleared.

At second, Timer data is writing into NJU6359, and the last 56 bits is effective.

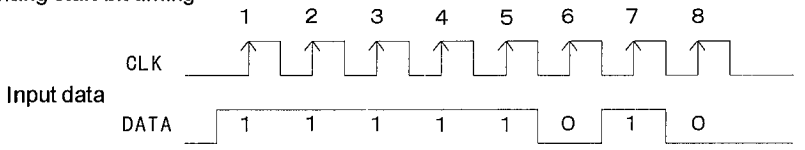
At last, Stop bit is writing, after the Writing timer data concluded. The timer data is written into the internal register with the falling edge of the clock signal, after the writing stop bit. And the divider starts operation. The data writing is operated from LSB first. The writing timer data must execute from the beginning, after the power supply turn on.

Rise time of power supply should be less than 10mS when the power supply turn on. (at V_{DD}=3V)

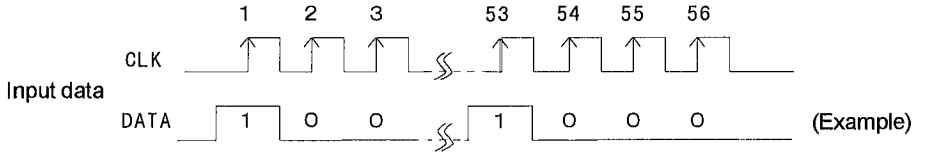
The input data strings are shown below :

Year	Month	Date	Day	Hour	Min.	Sec.	System control

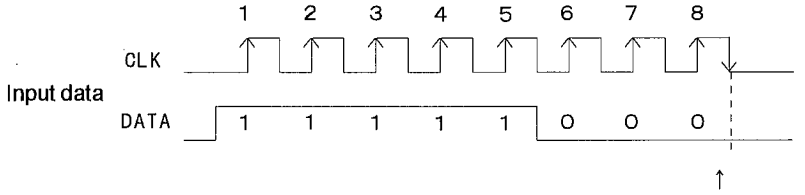
< Writing start bit timing >



< Writing timer data timing >



< Writing stop bit timing >



(The timer data is written into the internal register with the falling edge of the 8th clock, and the divider starts operation.)

5.Timer data reading

The timer data in the shift register shift by synchronized at the falling edge of the clock signal on CLK terminal and output from the DATA terminal.

At first, Start bit for reading of the timer data is writing into NJU6359. The timer data becomes reading mode by the falling edge of the CLK after the writing. And then, the data terminal is output.

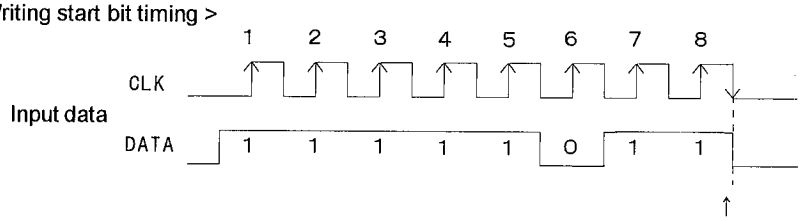
When the timer data becomes reading mode, the timer data is read from the shift register. The timer data is 56 bits.

The stop bit is reading continuously, after the reading timer data concluded. The DATA terminal is changed over from output to input by the falling edge of the CLK after the stop bit writing. The data reading is operated from LSB first.

The input data strings are shown below :

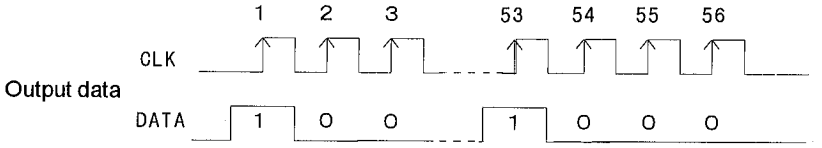
Year	Month	Date	Day	Hour	Min.	Sec.	System control

< Writing start bit timing >



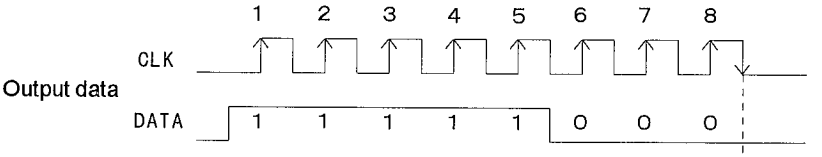
(The DATA terminal is output by the falling edge of the 8th clock.)

< Reading timer data timing >



(Example)

< Reading stop bit timing >



(The DATA terminal is input by the falling edge of the 8th clock.)

6.Data correction

The NJU6359 have the function of the data correction. This function prevent the error operation of the internal counter by wrong data.

When the in effective data is input, the data is corrected as show below table. However, the data correction is not executed for the system control data. Even if the data "1" is written into the unused bit, the data correction is executed to "0" automatically.

	The ineffective data	The object data of the correction	The corrected data
Second	The data except 0 to 59	S0 to S6	0
Minute	The data except 0 to 59	m0 to m6	0
Hour	The data except 0 to 23	H0 to H5	0
Day	The data except 1 to 7	W0 to W2	1
Date	Jan., Mar., May, Jul., Aug., Oct., Dec. : The data except 1 to 31 Apr., Jun., Sep., Nov. : The data except 1 to 30 Feb. : The data except 1 to 28 Feb. in the leap year : The data except 1 to 29	D0 to D5	1
Month	The data except 1 to 12	M0 to M4	1
Year	The data except 0 to 99	Y0 to Y7	0

Note) The data correction is not executed for the "start bit, stop bit". Therefore, the wrong data is recognized as "start bit, stop bit".

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	-0.3 ~ +6.0	V
Input Voltage		V_I	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operating Temperature		T_{opr}	-30 ~ +80	°C
Storage Temperature		T_{stg}	-40 ~ +125	°C
Power Dissipation	SSOP	P_D	250	mW

Note 1) Decoupling capacitor should be connected between V_{DD} and Vss due to the stabilized operation of the circuit.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics (Unless Otherwise Specified V_{DD}=3V±20%, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
Operating Voltage	V_{DD}			2.0		5.5	V	
Operating Current	I_{DD1}	Apply to the NJU6359A			0.25	1.0	μA	2
	I_{DD2}	Apply to the NJU6359B			0.85	2.0		3
Output off Leakage Current	I_{OL}	$\overline{WAKEUP}$ Terminal		-2.0		2.0	μA	
Input Current	I_{IN}	CLK, DATA Terminals	At the Input mode V_{DD},CLK,DATA=3.6V			12.0	μA	
Input Voltage 1	V_{IH1}	SIN Terminal		V_{DD}x0.8		V_{DD}	V	
	V_{IL1}	SIN Terminal		0		0.2		
Input Voltage 2	V_{IH2}	CLK,DATA Terminals		V_{DD}x0.8		V_{DD}	V	
	V_{IL2}	CLK,DATA Terminals		V_{SS}		V_{DD}x0.2		
Output Current	V_{OH}	DATA Terminal	V_{DD}=2.4V,V_{OH}=1.8V	0.4			mA	
	V_{OL1}	DATA Terminal	V_{DD}=2.4V,V_{OL}=0.4V	1.0				
	V_{OL2}	$\overline{WAKEUP}$ Terminal	V_{DD}=2.4V,V_{OL}=0.4V	1.0				

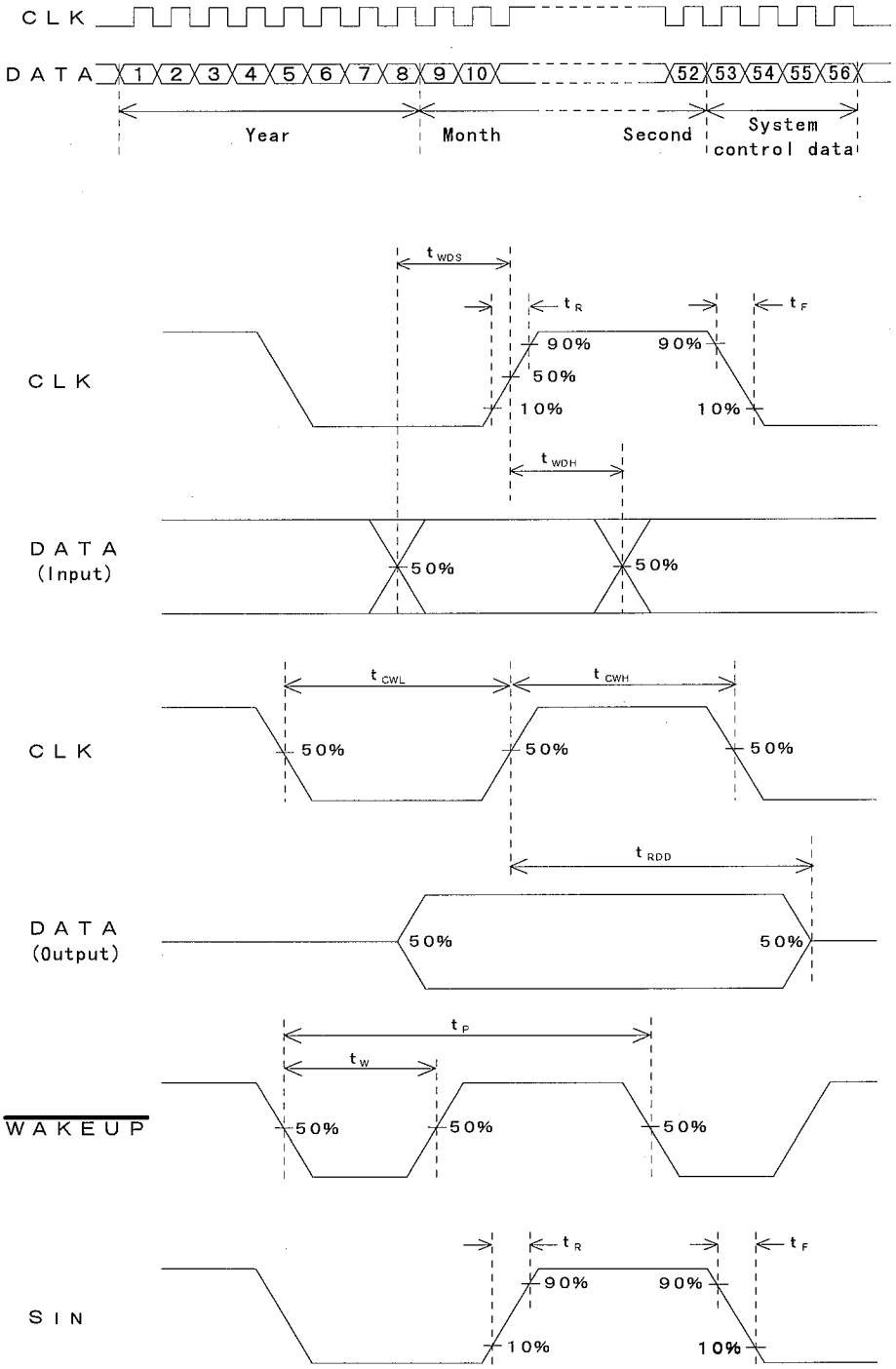
Note 2) SIN=32KHz, CLK/DATA=0V, The data is input mode, and the unused wake-up.
Note 3) SIN=384KHz, CLK/DATA=0V, The data is input mode, and the unused wake-up.

AC Characteristics (Unless Otherwise Specified V_{DD}=3V±20%, V_{SS}=0V, Ta=25°C)

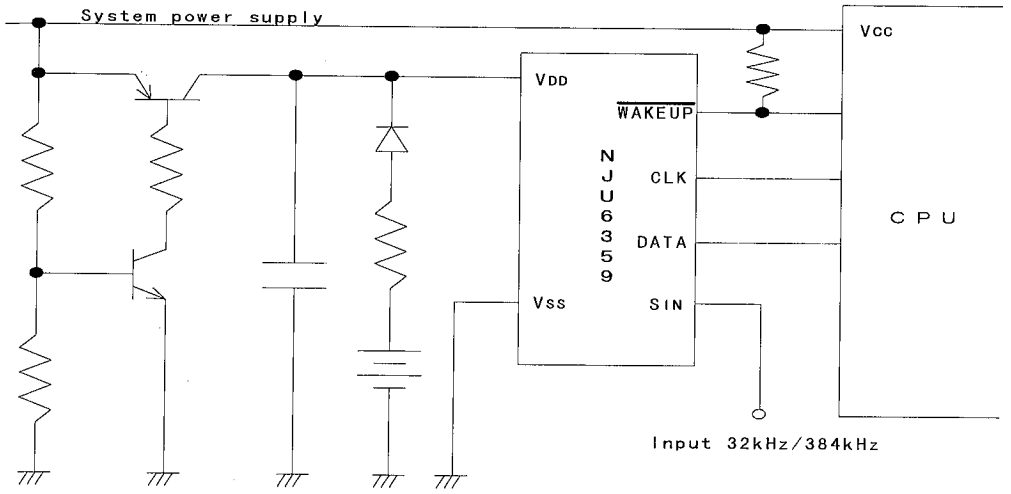
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
SIN Input Frequency	FR_{32}			32		KHz	4
	FR_{384}			384			5
SIN Input Operating Frequency	FRD_{32}		30	32	34	KHz	6
	FRD_{384}		382	384	386		7
SIN Input Signal Duty Ratio	DUTY		40	50	60	%	
CLK Pulse "H" Period	t_{CWH}		0.47		5000	μS	
CLK Pulse "L" Period	t_{CWL}		0.47		5000	μS	
DATA Set-up Time Before CLK Rising	t_{WDS}		200			nS	
DATA Hold Time After CLK Rising	t_{WDH}		200			nS	
DATA Delay Time After CLK Rising	t_{RDD}	CL=50pF			200	nS	
Wake-up Cycle	t_P		690	720	750	μS	8
Wake-up Pulse "L" Period	t_W		90	120	150	μS	8
Input Rise/Fall Time	t_{RF}				40	nS	
Power Supply Rising Time	t_{VON}				10	mS	

Note 4) Apply to the NJU6359A. If the accuracy clock is needed, 32.0kHz should input, because a second is made with the input signal is divided by 32,000.
Note 5) Apply to the NJU6359B. If the accuracy clock is needed, 384.0kHz should input, because a second is made with the input signal is divided by 384,000.
Note 6) Apply to the NJU6359A. The regulations guarantees operation, but the accuracy is not available.
Note 7) Apply to the NJU6359B. The regulations guarantees operation, but the accuracy is not available.
Note 8) Measurement conditions : The $\overline{WAKEUP}$ terminal is pulled-up to the V_{DD} terminal connected by 470kΩ resister. The 32kHz (NJU6359A) or 384kHz (NJU6359B) inputs to the SIN terminal.

■ TIMING CHART of Real Time Clock Block



■ APPLICATION CIRCUIT



MEMO