

QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6395 series is a low voltage operation C-MOS quartz crystal oscillator which is possible to 65MHz. It consists of an oscillation amplifier and a 3-state output buffer.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors (Cg, Cd), therefore it requires no external component except quartz crystal.

The driverbility of the 3-state output buffer is 6mA, thus it can drive C-MOS load.

■ FEATURES

- Low Operating Voltage — 2.2~2.8V
- Recommended Oscillation Frequency — 45 to 65MHz
- High Fan-out — $I_{OL}/I_{OH}=6mA$ @2.5V
- Oscillation Stop and Output Buffer Stand-by Function
- 3-state Output Buffer
- Oscillation Capacitors Cg and Cd on-chip
- Package Outline — Chip/Thin-Chip
- C-MOS Technology

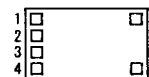
■ PACKAGE OUTLINE



NJU6393C/CT

■ PAD LOCATION

Chip/Thin-Chip



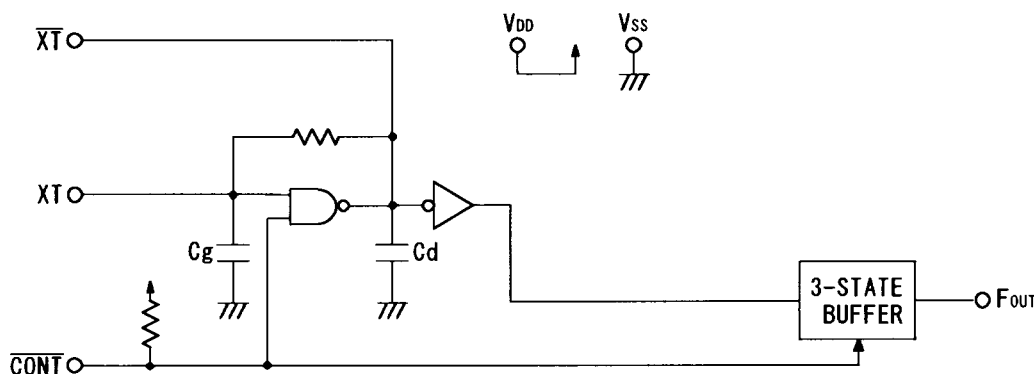
■ COORDINATES

UNIT: μm

No.	PAD	X	Y
1	\overline{CONT}	-428	258
2	XT	-428	86
3	\overline{XT}	-428	-86
4	V _{SS}	-428	-258
5	F _{OUT}	478	-258
8	V _{DD}	478	258

Chip Center : X=0 μm , Y=0 μm
 Chip Size : 1.24x0.8 mm
 Chip Thickness : 400 \pm 30 μm
 Thin-Chip Thickness: 260 \pm 20 μm
 Note1) No. 6 and 7 are no pad.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N	
1	$\overline{\text{CONT}}$	Oscillation and 3-State Output Buffer Control	
		$\overline{\text{CONT}}$	F_{OUT}
		H or Open	Output Frequency f_o
		L	Oscillation Stop and High Impedance Output
2	XT	Quartz Crystal Connecting terminals	
3	$\overline{\text{XT}}$		
4	V_{SS}	GND : $V_{\text{SS}}=0\text{V}$	
5	F_{OUT}	Output Frequency f_o	
8	V_{DD}	$V_{\text{DD}}=2.5\text{V}$	

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	$V_{\text{SS}}-0.5 \sim V_{\text{DD}}+0.5$	V
Output Voltage	V_o	-0.5 ~ $V_{\text{DD}}+0.5$	V
Input Current	I_{IN}	± 10	mA
Output Current	I_o	± 25	mA
Operating Temperature Range	Topr	-40 ~ + 85	°C
Storage Temperature Range	Tstg	-55 ~ +125	°C

Note2) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

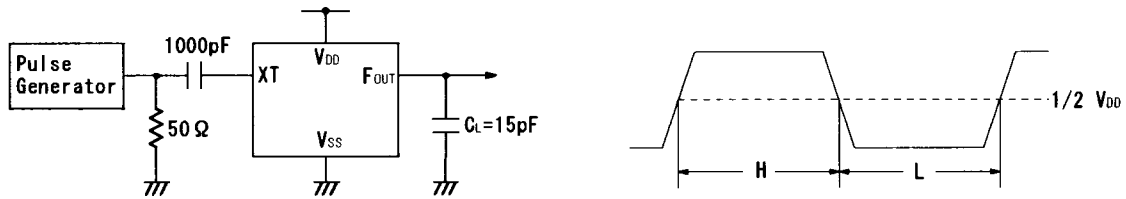
 (V_{DD}=3.0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V _{DD}		2.2		2.8	V
Operating Current	I _{DD1}	f _{OSC} =48MHz, No Load		8	15	mA
Stand-by Current	I _{st}	CONT=XT=V _{SS} , No load Note3			1	uA
Input Voltage	V _{IH}		2.0		2.5	V
	V _{IL}		0		0.5	
Output Current	I _{OH}	V _{OH} =2.25V	6			mA
	I _{OL}	V _{OL} =0.25V	6			
Input Current	I _{IN}	CONT=V _{SS}	62	125	250	uA
3-state Off-leakage Current	I _{oz}	CONT=V _{SS} , F _{OUT} =V _{DD} or V _{SS}			±0.1	uA
Internal Capacitor	C _s /C _d	f _{OSC} =48MHz		12/14		pF
Maximum Oscillation Frequency	F _{MAX}		65			MHz
Output Signal Symmetry	SYM	C _L =15pF, @1/2·V _{DD}	45	50	55	%
Output Signal Rise Time	t _r	C _L =15pF, 10%~90%		2.6	6	ns
Output Signal Fall Time	t _f	C _L =15pF, 90%~10%		2.6	6	
Output Disable Time	T _{PLZ}	C _L =15pF, R _{UP} =10kΩ			200	ns
Output Enable Time	T _{PZL}	C _L =15pF, R _{UP} =10kΩ			200	

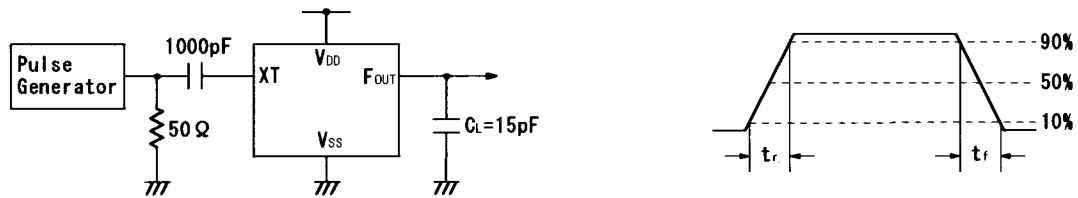
Note3) Excluding input current on CONT terminal.

■ MEASUREMENT CIRCUITS

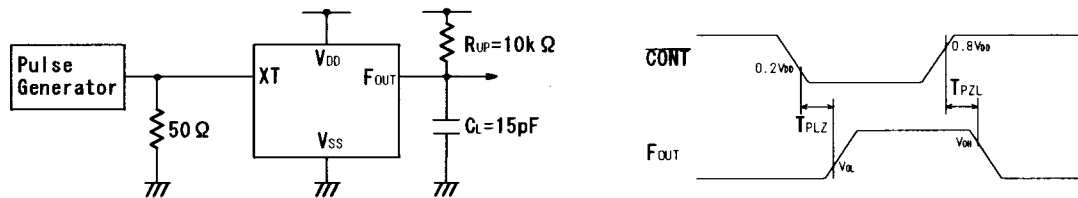
(1) Output Signal Symmetry ($C_L=15\text{pF}$)



(2) Output Signal Rise/Fall Time ($C_L=15\text{pF}$)



(3) Output Disable/Enable Time ($C_L=15\text{pF}, R_{UP}=10\text{k}\Omega$)



[CAUTION]
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