

## DOT MATRIX LCD 64-OUT SEGMENT DRIVER

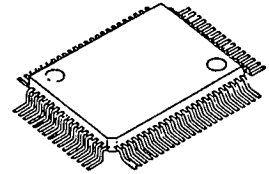
**■ GENERAL DESCRIPTION**

The NJU6417C is a serial input, 64-out segment driver for dot matrix LCDs, especially useful as extension driver for LCD controller drivers like NJU6408B.

It consists of 64-bit (two of 32-bit) shift register, 64-bit latch, and 64 high voltage LCD drivers.

The shift direction of each 32-bit shift register can be set independently to each other, consequently the efficient extension driver allocation according to the number of characters and easy wiring with the LCD panel can be performed.

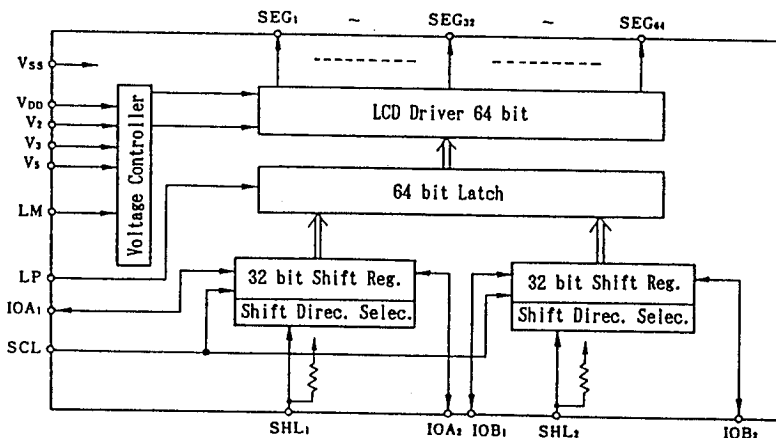
As the 64-driver have 4 level voltage inputs to drive the LCD, adjustable driving voltage according to the LCD panel can be supplied from the external power source.

**■ PACKAGE OUTLINE**


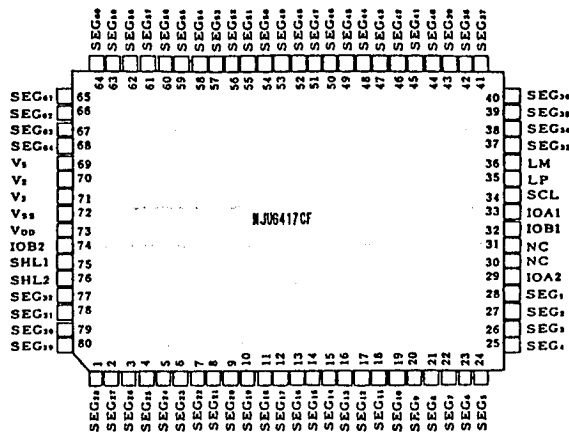
NJU6417CF

**■ FEATURES**

- 64 Segment Drivers
- 64-bit Shift Register
  - ( Two of 32-bit Shift Registers )
- Shift Direction of each 32-bit
  - Shift Registers Selection
- Two of Shift Direction Select Terminal
- Duty Ratio 1/8 to 1/16
- Fast Data Transmission ( Shift Clock 6 MHz max.)
- External Power Supply for LCD Driving Voltage
- LCD Driving Voltage ---  $V_{DD} - 3V \sim V_{DD} - 13.5V$
- Operating Voltage ---  $5V \pm 10\%$
- Package Outline --- QFP 80
- C-MOS Technology

**■ BLOCK DIAGRAM**


## ■ PIN CONFIGURATION



## ■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N
1~28 37~68 77~80	SEG <sub>1</sub> ~ SEG <sub>64</sub>	LCD segment driving terminal. Each terminal corresponds to each bit of shift register
29 33	IOA <sub>2</sub> IOA <sub>1</sub>	Data input/output terminals for 1st to 32nd bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL <sub>1</sub> terminal.
32 74	IOB <sub>1</sub> IOB <sub>2</sub>	Data input/output terminals for 33rd to 64th bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL <sub>2</sub> terminal.
34	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time (T <sub>RS</sub> ) and falling time (T <sub>FS</sub> ) should be set less than 50ns respectively.
35	LP	Latch pulse input terminal. The data in the shift register is latched to the latch by this signal. "H": Data writing, "L": Data latch
36	LM	Alternate signal input for LCD driving.
69, 71 70	V <sub>5</sub> , V <sub>3</sub> V <sub>2</sub>	LCD driving power source terminals. V <sub>DD</sub> ≥ V <sub>2</sub> ≥ V <sub>3</sub> ≥ V <sub>5</sub> , V <sub>DD</sub> ≥ V <sub>SS</sub> ≥ V <sub>5</sub>
72 73	V <sub>DD</sub> V <sub>SS</sub>	Power supply terminal (connect to the controller's V <sub>DD</sub> terminal) Power supply terminal (connect to the controller's V <sub>SS</sub> terminal)
75	SHL <sub>1</sub>	Shift direction and input/output control terminal (Pull-up R). "H" or Open: Shift direction is from 1st bit to 32nd bit. "L": Shift direction is from 32nd bit to 1st bit.
76	SHL <sub>2</sub>	Shift direction and input/output control terminal (Pull-up R). "H" or Open: Shift direction is from 33rd bit to 64th bit. "L": Shift direction is from 64th bit to 33rd bit.
54	NC	Non connection.

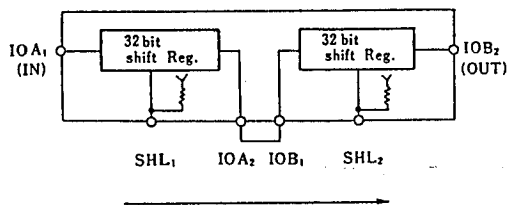
**FUNCTIONAL DESCRIPTION**
**(1) Shift register control**

The 64-bit shift register is divided into two of 32-bit shift register.

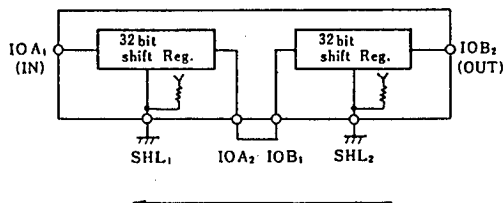
The shift direction of each 32-bit shift register can be set independently to each other shown in below.

Control Terminal	Input	Shift Direction
SHL <sub>1</sub>	"H" or Open	IOA <sub>1</sub> → IOA <sub>2</sub>
	"L"	IOA <sub>1</sub> ← IOA <sub>2</sub>
SHL <sub>2</sub>	"H" or Open	IOB <sub>1</sub> → IOB <sub>2</sub>
	"L"	IOB <sub>1</sub> ← IOB <sub>2</sub>

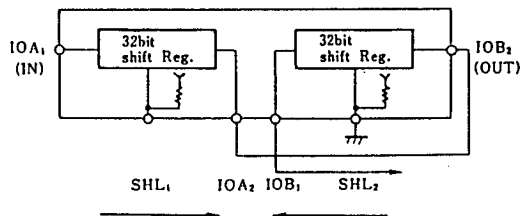
(1-1) When the terminals SHL<sub>1</sub> and SHL<sub>2</sub> are "H" or open, the data shift from SEG<sub>1</sub> to SEG<sub>64</sub>.



(1-2) When the terminals SHL<sub>1</sub> and SHL<sub>2</sub> are "L", the data shift from SEG<sub>64</sub> to SEG<sub>1</sub>.



(1-3) Reversed shift direction to each other is also available. SEG<sub>1</sub> → SEG<sub>32</sub> → SEG<sub>64</sub> → SEG<sub>33</sub> example is shown in below:



## (2) LCD driver output truth table.

Input Data	Selection/Non-selection	LM	Driver Output (SEG <sub>1</sub> to SEG <sub>6,4</sub> )
"H"	Selection	H	V <sub>5</sub>
		L	V <sub>DD</sub>
"L"	Non-selection	H	V <sub>3</sub>
		L	V <sub>2</sub>

## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage ( 1 )	V <sub>DD</sub>	- 0.3 ~ + 7.0	V
Supply Voltage ( 2 ) Note 1)	V <sub>DD</sub> ~ V <sub>5</sub>	V <sub>DD</sub> -13.5 ~ V <sub>DD</sub> +0.3	V
Input Voltage	V <sub>IN</sub>	- 0.3 ~ V <sub>DD</sub> +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 150	°C

 Note 1) The relation : V<sub>DD</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>5</sub> must be maintained.

## ■ ELECTRICAL CHARACTERISTICS

## • DC Characteristics

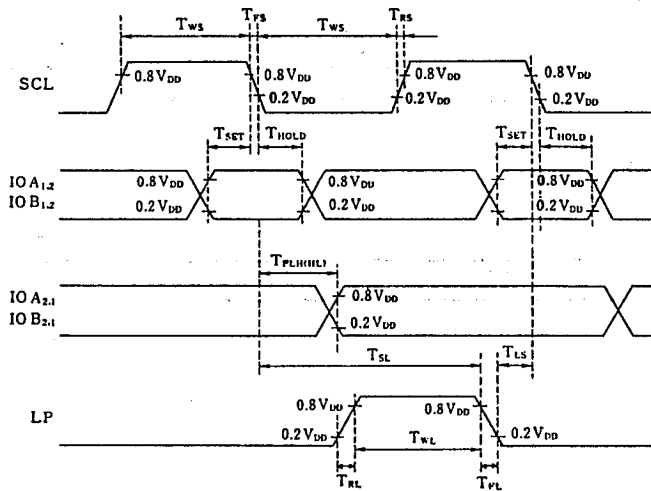
 ( V<sub>DD</sub>=5V±10% , Ta=-20 ~ +75°C )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Input Voltage	V <sub>IH</sub>	LM, LP, SHL <sub>1</sub> , SHL <sub>2</sub> Terminals	0.8V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IL</sub>				0.2V <sub>DD</sub>		
Input Current	I <sub>IH1</sub>	V <sub>IH</sub> =V <sub>DD</sub>			1	μA	
	I <sub>IL1</sub>	V <sub>IL</sub> =0V			- 1		
	I <sub>IH2</sub>	V <sub>IH</sub> =V <sub>DD</sub>	SHL <sub>1</sub> , SHL <sub>2</sub> Terminals				1
	I <sub>IL2</sub>	V <sub>IL</sub> =0V		- 10	- 15		- 25
Output Voltage	V <sub>OH</sub>	I <sub>O</sub> =- 40μA	10A <sub>1</sub> , 10A <sub>2</sub> , 10B <sub>1</sub> , 10B <sub>2</sub> Terminals	4.2		V	
	V <sub>OL</sub>	I <sub>O</sub> = 400μA					0.4
Driver On-resistance	R <sub>ON</sub>	I <sub>d</sub> =0.05mA	SEG <sub>1</sub> ~ SEG <sub>6,4</sub> Terminals		30	kΩ	
Operating Current ( Logic Part )	I <sub>SSO</sub>	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.		0.85	1.2	mA	
Operating Current ( LCD Driver Part )	I <sub>SSHO</sub>	LM,LP=130us cycle, SCL=1.5MHz Every one bit Inverted Data. No Load.		70	100	μA	
LCD Driving Voltage	V <sub>LCD</sub>	V <sub>DD</sub> - V <sub>5</sub>	V <sub>DD</sub> - 3.0		V <sub>DD</sub> - 13.5	V	

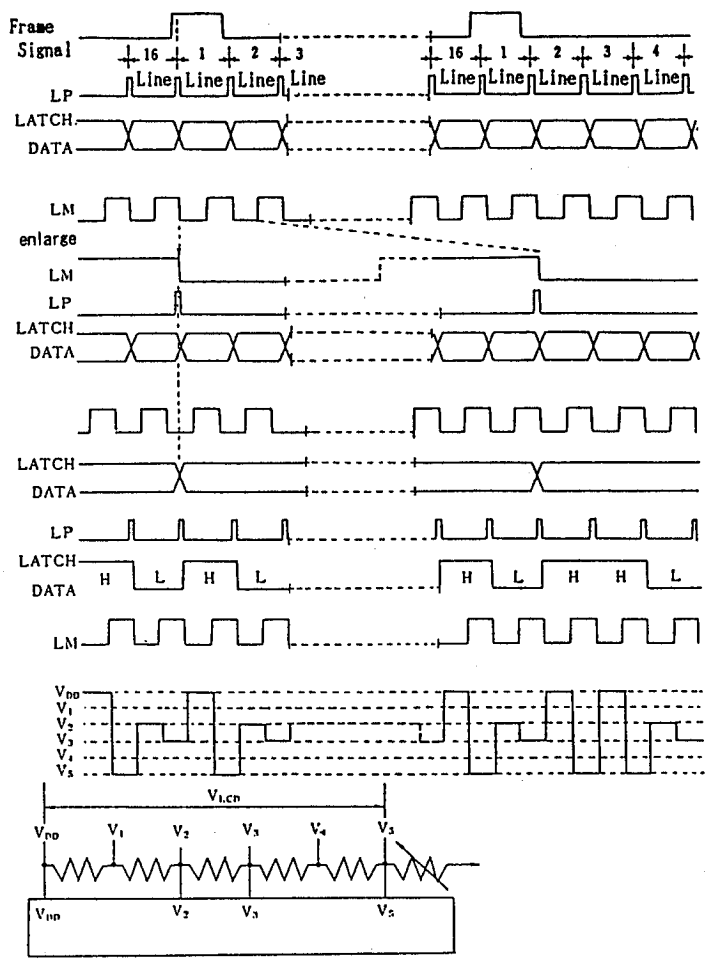
## • AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$T_{PLH(HL)}$				150	ns
Maximum Operating Frequency	$f_{SCL}$	Duty = 50 %			6	MHz
SCL Pulse Width	$T_{WS}$		63			ns
LP Pulse Width	$T_{WL}$		110			ns
Set up Time	$T_{SET}$		50			ns
SCL → LP Time	$T_{SL}$		100			ns
LP → SCL Time	$T_{LS}$		0			ns
Data Hold Time	$T_{HOLD}$		30			ns
SCL Rise, Fall Time	$T_{RS}, T_{FS}$				50	ns
LP Rise, Fall Time	$T_{RL}, T_{FL}$				1	us

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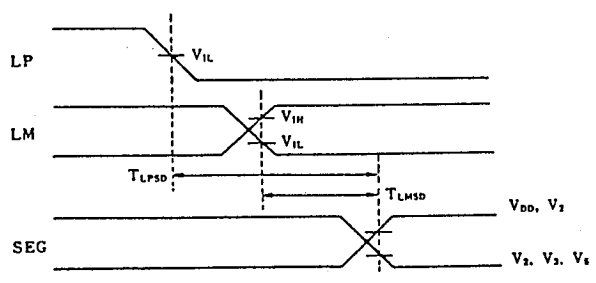


■ TIMING CHART 1/5 Bias, 1/16 Duty Ratio



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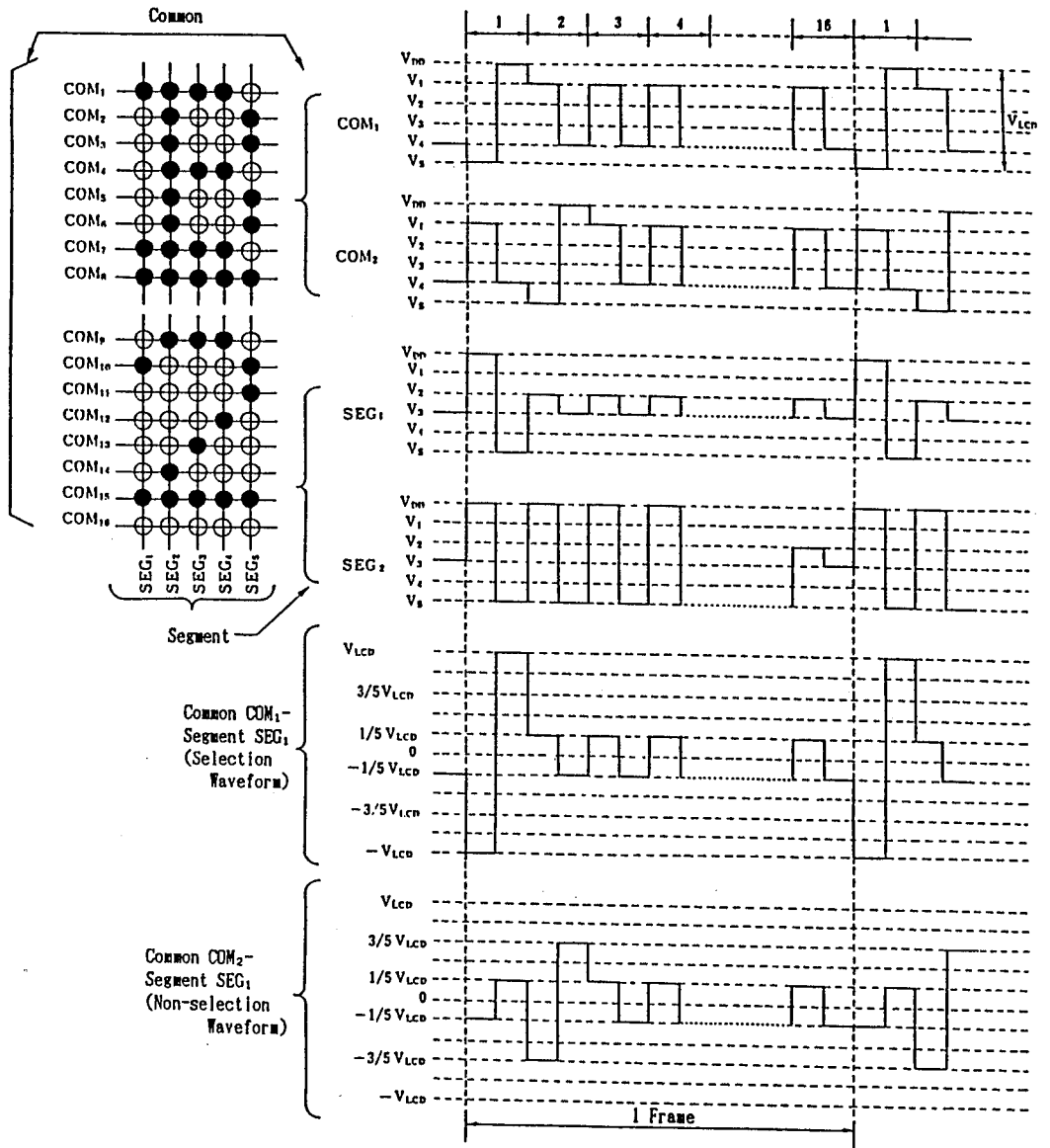
■ SEGMENT SIGNAL OUTPUT TIMING



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP - SEG Output Delay Time	$T_{LPDS}$	$C_L = 100pF$			4.5	us
LM - SEG Output Delay Time	$T_{LMDS}$	$C_L = 100pF$			4.5	

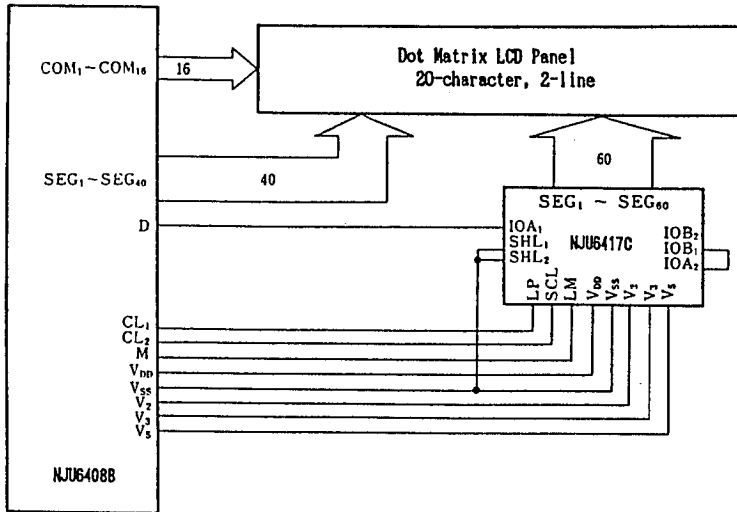
■ LCD DRIVING WAVEFORM EXAMPLE

1/5 Bias, 1/16 Duty Ratio

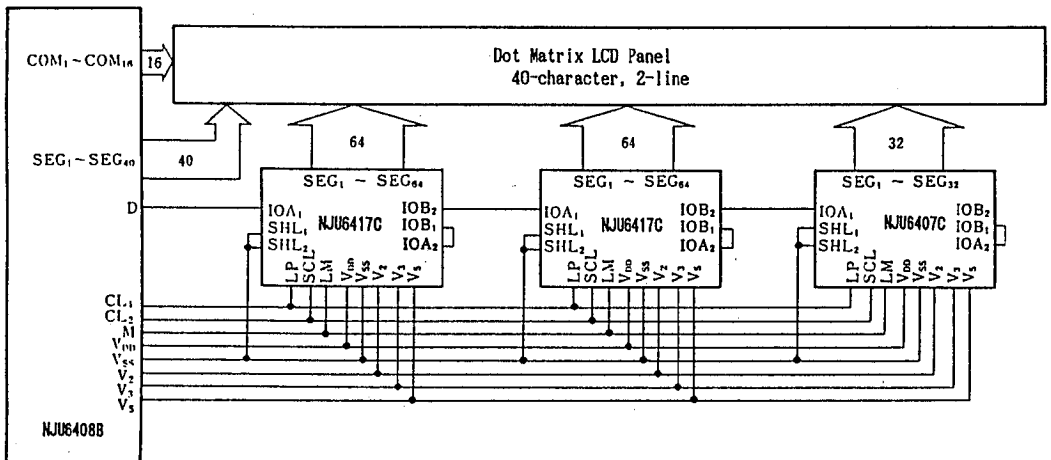


■ APPLICATION CIRCUITS

(1) 20-character 2-line Display Example ( Combine with NJU6408B )



(2) 40-character 2-line Display Example ( NJU6408B + NJU6417C x 2 + NJU6407C )





## MEMO

[CAUTION]

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