

1/4 DUTY LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6433B is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6433B is useful for the digital tuning system or others segment type display driver.

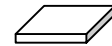
■ PACKAGE OUTLINE



NJU6433BFG1



NJU6433BFH1

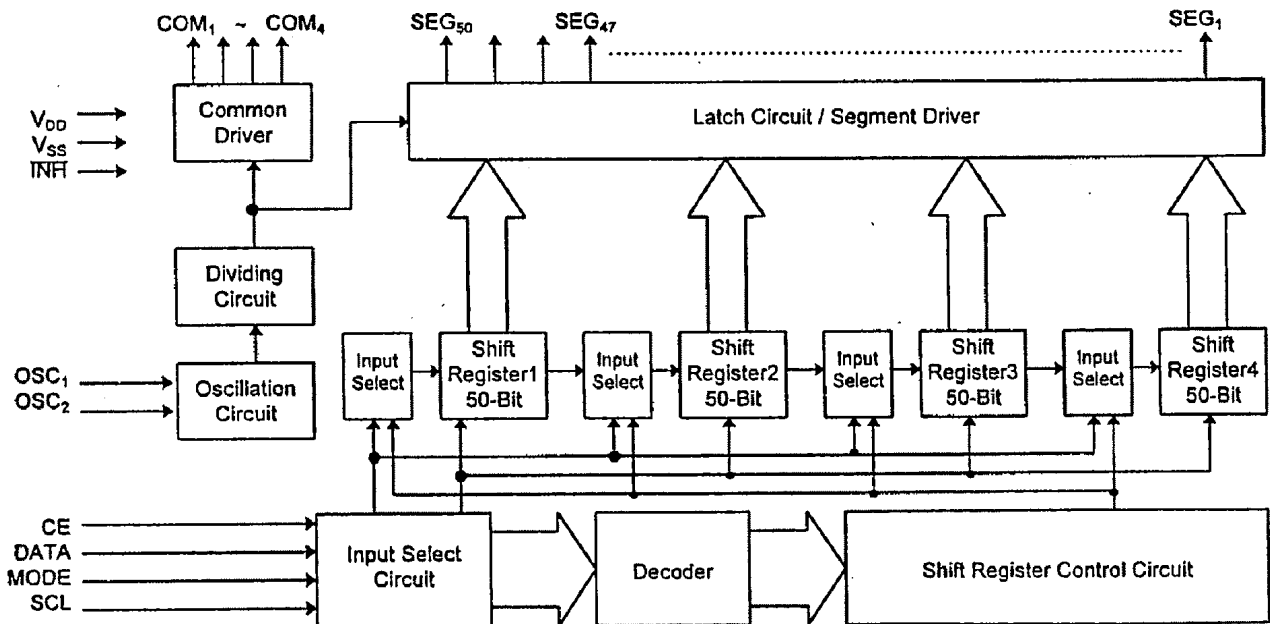


NJU6433BC/BCH

■ FEATURES

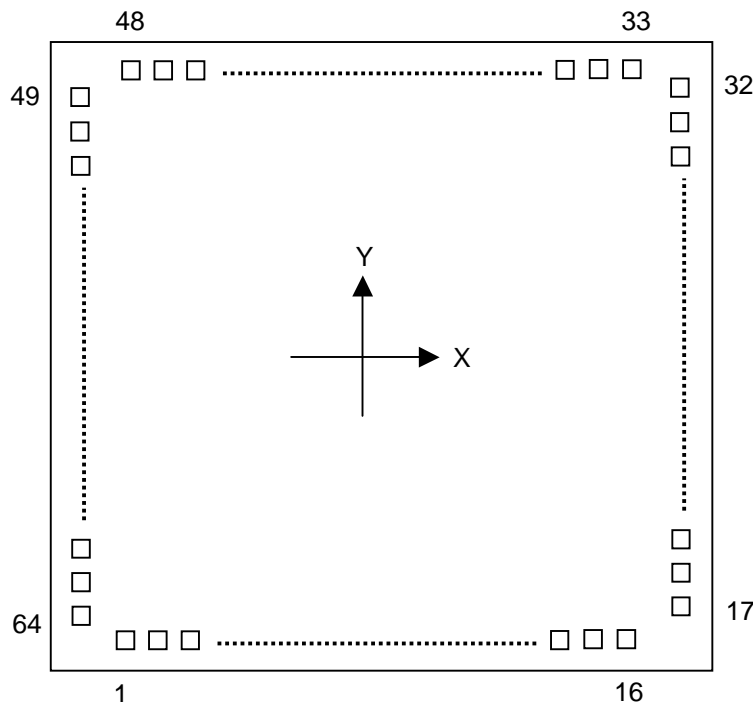
- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required)
- Display Off Function (INHb Terminal)
- Operating Voltage 2.4 to 5.5V
- LCD Driving Voltage 6.5V Max.
- Package Outline Bump Chip, Chip, QFP 64-G1, QFP64-H1
- C-MOS Technology

■ BLOCK DIAGRAM



NJU6433B

■ PAD LOCATION



Chip Center : X=0 μ m, Y=0 μ m
 Chip Size : X=3.20 mm, Y=3.20 mm
 Chip Thickness : 400 μ m
 PAD Size : X=99.2 μ m, Y=99.2 μ m
 PAD Pitch : 171.2 μ m
 Bump Height : 25 μ m

■ PAD COORDINATES

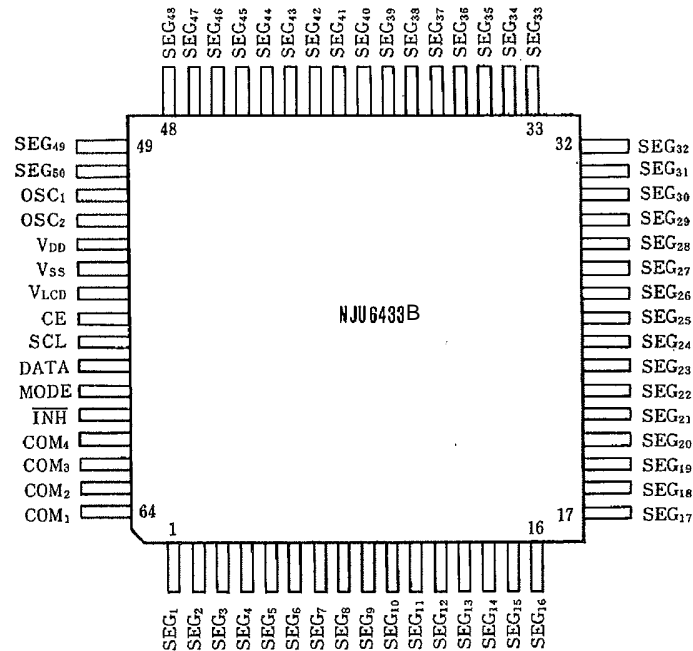
Chip Size 3.20 x 3.20 mm(Chip Center X=0 μ m, Y=0 μ m)

PAD No.	Terminal	X= μ m	Y= μ m
1	SEG ₁	-1279	-1437
2	SEG ₂	-1107	-1437
3	SEG ₃	-936	-1437
4	SEG ₄	-765	-1437
5	SEG ₅	-594	-1437
6	SEG ₆	-423	-1437
7	SEG ₇	-251	-1437
8	SEG ₈	-80	-1437
9	SEG ₉	91	-1437
10	SEG ₁₀	262	-1437
11	SEG ₁₁	433	-1437
12	SEG ₁₂	605	-1437
13	SEG ₁₃	776	-1437
14	SEG ₁₄	947	-1437
15	SEG ₁₅	1118	-1437
16	SEG ₁₆	1289	-1437
17	SEG ₁₇	1437	-1288
18	SEG ₁₈	1437	-1117
19	SEG ₁₉	1437	-946
20	SEG ₂₀	1437	-775
21	SEG ₂₁	1437	-603
22	SEG ₂₂	1437	-432
23	SEG ₂₃	1437	-261
24	SEG ₂₄	1437	-90

PAD No.	Terminal	X= μ m	Y= μ m
25	SEG ₂₅	1437	81
26	SEG ₂₆	1437	253
27	SEG ₂₇	1437	424
28	SEG ₂₈	1437	595
29	SEG ₂₉	1437	766
30	SEG ₃₀	1437	937
31	SEG ₃₁	1437	1109
32	SEG ₃₂	1437	1280
33	SEG ₃₃	1280	1437
34	SEG ₃₄	1109	1437
35	SEG ₃₅	937	1437
36	SEG ₃₆	766	1437
37	SEG ₃₇	595	1437
38	SEG ₃₈	424	1437
39	SEG ₃₉	253	1437
40	SEG ₄₀	81	1437
41	SEG ₄₁	-90	1437
42	SEG ₄₂	-261	1437
43	SEG ₄₃	-432	1437
44	SEG ₄₄	-603	1437
45	SEG ₄₅	-775	1437
46	SEG ₄₆	-946	1437
47	SEG ₄₇	-1117	1437
48	SEG ₄₈	-1288	1437

PAD No.	Terminal	X= μ m	Y= μ m
49	SEG ₄₉	-1437	1280
50	SEG ₅₀	-1437	1109
51	OSC ₁	-1437	937
52	OSC ₂	-1437	766
53	V _{DD}	-1437	595
54	V _{SS}	-1437	424
55	V _{LCD}	-1437	253
56	CE	-1437	81
57	SCL	-1437	-90
58	DATA	-1437	-261
59	MODE	-1437	-432
60	INHX	-1437	-603
61	COM ₄	-1437	-775
62	COM ₃	-1437	-946
63	COM ₂	-1437	-1117
64	COM ₁	-1437	-1288

■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
1~50	SEG ₁ ~SEG ₅₀	LCD Segment Output Terminals
51	OSC ₁	Oscillation Terminals : External resistance is connected to these terminals.
52	OSC ₂	
53	V _{DD}	Power Supply (+5V)
54	V _{SS}	Power Supply (0V)
55	V _{LCD}	Power Supply for LCD Driving The relation : $1.3V_{DD} \geq V_{DD} - V_{LCD} $, $V_{SS} \geq V_{LCD}$ must be maintained.
56	CE	Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch
57	SCL	Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge.
58	DATA	Serial Data Input Terminal Data input timing : SCL clock rise edge
59	MODE	Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (Refer the mode setting table for mode setting contents)
60	INHb	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off
61~64	COM ₄ ~COM ₁	LCD Common Output Terminals

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

The oscillation circuit operate by connecting external resistance (capacitance is incorporated).
This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(2) Data Input Format

(2-1) Input Data Correspond to Segment Status

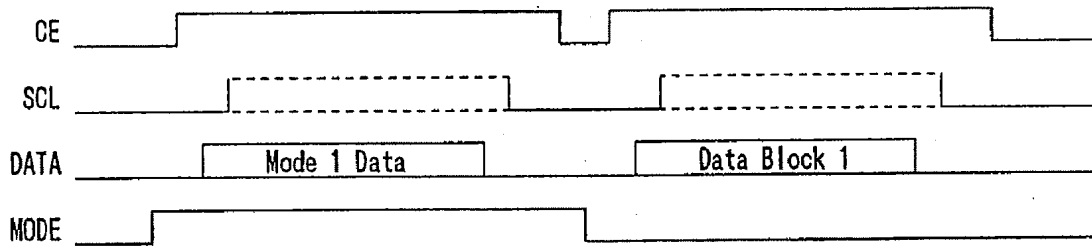
The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data Dxxx	Segment Status
"H"	ON
"L"	OFF

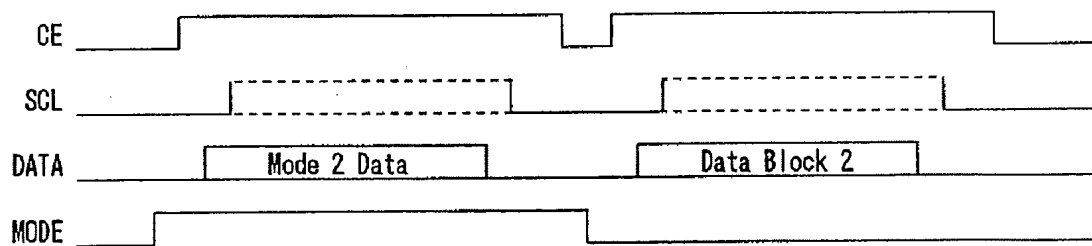
(2-2) Write to Shift-register

Write to shift-register performs Mode setting data writing and LCD display data writing.

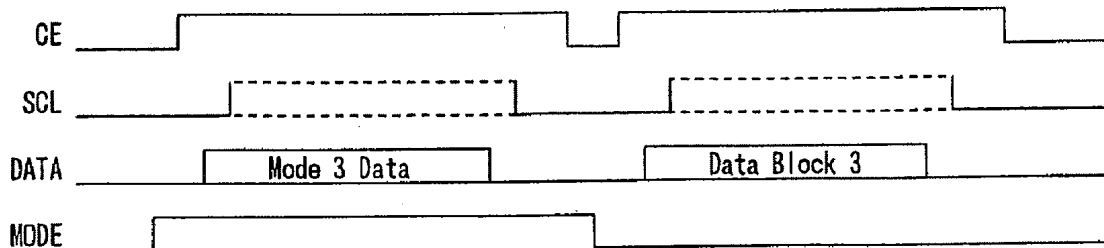
Example 1 (Mode 1): Write to Shift-register 1 (1 to 50-bit)



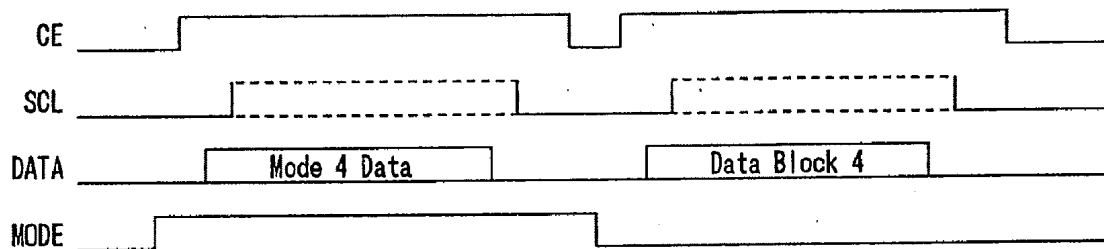
Example 2 (Mode 2): Write to Shift-register 2 (51 to 100-bit)



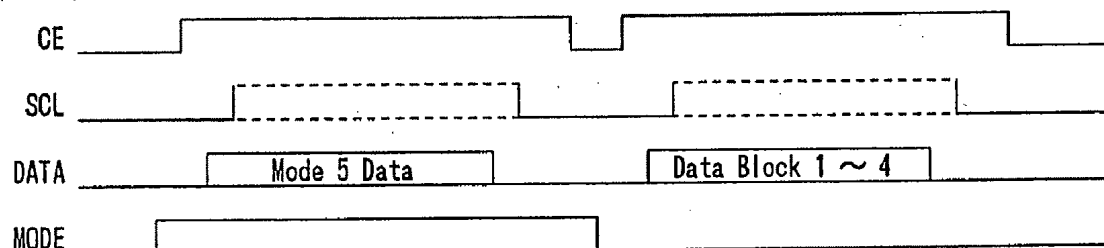
Example 3 (Mode 3): Write to Shift-register 3 (101 to 150-bit)



Example 4 (Mode 4): Write to Shift-register 4 (151 to 200-bit)



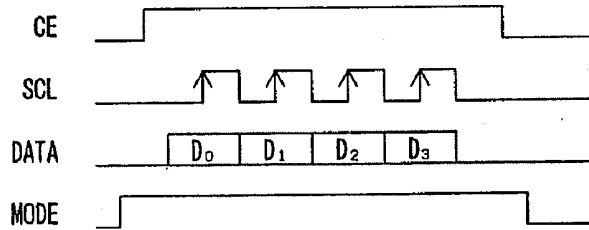
Example 5 (Mode 5): Write to Shift-register 5 (1 to 200-bit)



(2-3) Mode Setting

Transfer register selection and all clear of the shift register are performed by writing 4-bit code shown below to the decoder in CE = "H" and MODE = "H" state.

<Input Timing Chart>



<Mode Setting Table>

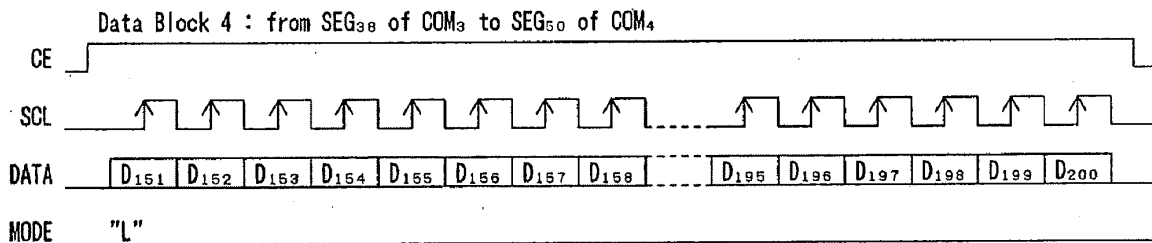
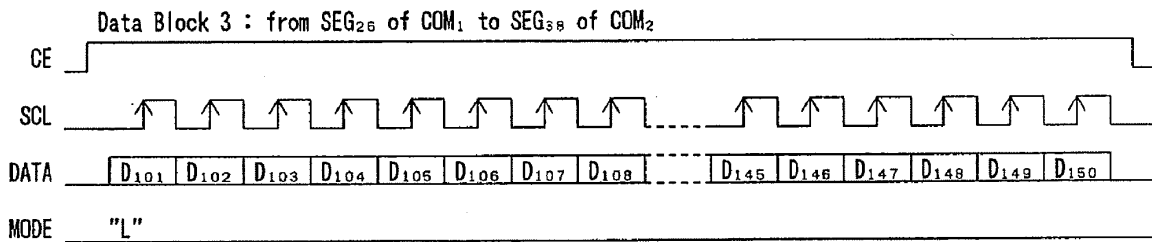
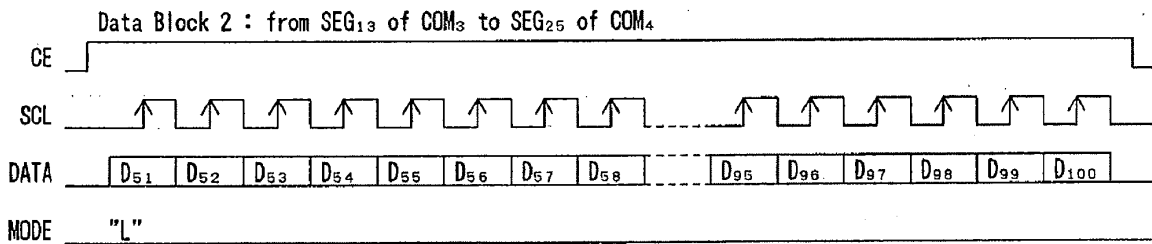
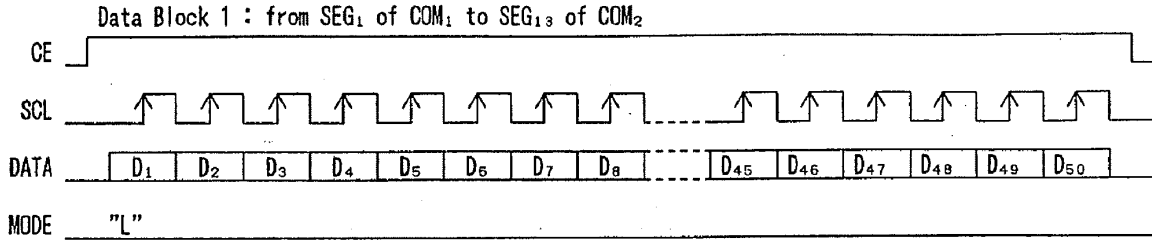
CE Terminal	MODE Terminal	DATA Terminal	MODE # Data (HEX)	Mode Set Up
"H"	"H"	D ₃ D ₂ D ₁ D ₀	0 0 0 1 (01 _H)	Select the shift-register 1
		D ₃ D ₂ D ₁ D ₀	0 0 1 0 (02 _H)	Select the shift-register 2
		D ₃ D ₂ D ₁ D ₀	0 0 1 1 (03 _H)	Select the shift-register 3
		D ₃ D ₂ D ₁ D ₀	0 1 0 0 (04 _H)	Select the shift-register 4
		D ₃ D ₂ D ₁ D ₀	0 1 0 1 (05 _H)	Select the all shift-register (1 to 4)
		D ₃ D ₂ D ₁ D ₀	1 1 1 1 (0F _H)	All shift-register is "L"

Note) The internal decoder is data through type. Therefore, the 8 bits data also can write though only 4 bits data from the CE falling are validated.

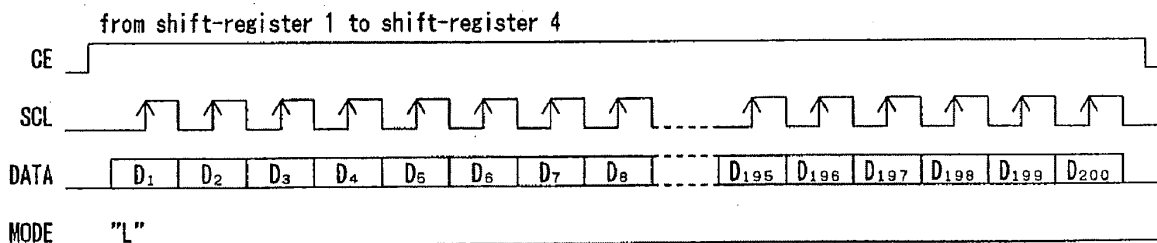
(2-4) Block Data and Whole Data transfer

a. Block Data (50-bit) transfer

In this mode, each 50 bits data block send to the each register.



b. Whole Data (200-bit) transfer



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(2-5) Display Data Correspond to Segment and Common Terminals

Mode	Data	Segment	COM ₁	COM ₂	COM ₃	COM ₄	Data Block
Mode 1	D ₁ D ₂ D ₃ D ₄	SEG ₁	○	○	○	○	Data Block 1
	D ₅ D ₆ D ₇ D ₈	SEG ₂	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D ₄₅ D ₄₆ D ₄₇ D ₄₈	SEG ₁₂	○	○	○	○	
	D ₄₉ D ₅₀	SEG ₁₃	○	○			
Mode 2	D ₅₁ D ₅₂	SEG ₁₃			○	○	Data Block 2
	D ₅₃ D ₅₄ D ₅₅ D ₅₆	SEG ₁₄	○	○	○	○	
	⋮	⋮	⋮	⋮	⋮	⋮	
	D ₉₇ D ₉₈ D ₉₉ D ₁₀₀	SEG ₂₅	○	○	○	○	
	D ₁₀₁ D ₁₀₂ D ₁₀₃ D ₁₀₄	SEG ₂₆	○	○	○	○	
Mode 3	D ₁₀₅ D ₁₀₆ D ₁₀₇ D ₁₀₈	SEG ₂₇	○	○	○	○	Data Block 3
	⋮	⋮	⋮	⋮	⋮	⋮	
	D ₁₄₅ D ₁₄₆ D ₁₄₇ D ₁₄₈	SEG ₃₇	○	○	○	○	
	D ₁₄₉ D ₁₅₀	SEG ₃₈	○	○			
	D ₁₅₁ D ₁₅₂	SEG ₃₈			○	○	
D ₁₅₃ D ₁₅₄ D ₁₅₅ D ₁₅₆	SEG ₃₉	○	○	○	○		
⋮	⋮	⋮	⋮	⋮	⋮		
D ₁₉₇ D ₁₉₈ D ₁₉₉ D ₂₀₀	SEG ₅₀	○	○	○	○		

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Operating Voltage (1)	V_{DD}	-0.3~+7.0	V	
Operating Voltage (2)	V_{LCD}	$V_{DD}-6.5\sim V_{SS}$	V	1
Input Voltage (1)	$V_{1(1)}$	-0.3~+7.0	V	2
Input Voltage (2)	$V_{1(2)}$	-0.3~ $V_{DD}+0.3$	V	3
Output Voltage	V_O	-0.3~ $V_{DD}+0.3$	V	3
Output Current (1)	$I_{O(1)}$	100	uA	4
Output Current (2)	$I_{O(2)}$	1.0	mA	5
Power Dissipation	P_D	300	mW	
Operating Temperature	T_{opr}	-30~+85	°C	
Storage Temperature	T_{stg}	-40~+125	°C	

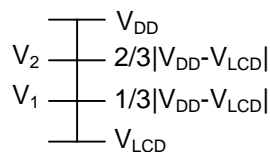
- Note 1) $V_{DD} \times 1.3 \geq |V_{DD}-V_{LCD}|$, $V_{SS} \geq V_{LCD}$
 Note 2) CE, SCL, DATA, MODE, INHb Terminals
 Note 3) OSC₁, OSC₂ Terminals
 Note 4) SEG₁~SEG₅₀ Terminals
 Note 5) COM₁~COM₄ Terminals

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (Ta= 25°C, V_{DD}=5.0V, V_{SS}=0V, V_{LCD}=V_{DD}-6.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NO TE
Operating Voltage (1)	V_{DD}	V_{DD} Terminal	2.4	5.0	5.5	V	
Operating Voltage (2)	V_{LCD}	V_{LCD} Terminal	V_{SS}		$V_{DD}-6.5$	V	1
"H" Input Voltage	V_{IH}	CE, SCL, DATA, MODE, INHb	$0.7V_{DD}$		V_{DD}	V	
"L" Input Voltage	V_{IL}		V_{SS}		$0.3V_{DD}$	V	
"H" Input Current	I_{IH}	CE, SCL, DATA, MODE, INHb	$V_1=V_{DD}$		5	uA	
"L" Input Current	I_{IL}		$V_1=V_{SS}$		5	uA	
"H" Output Voltage (1)	$V_{OH(1)}$	SEG ₁ ~SEG ₅₀	$I_O=-10\mu A$	$V_{DD}-1.0$		V	
"L" Output Voltage (1)	$V_{OL(1)}$		$I_O=+10\mu A$			$V_{LCD}+1.0$	V
Middle Level Voltage 1/3(1)	$V_{MS1/3}$	SEG ₁ ~SEG ₅₀	$I_O=\pm 10\mu A$	$V_1-1.0$	V_1	$V_1+1.0$	V
Middle Level Voltage 2/3(1)	$V_{MS2/3}$		$I_O=\pm 10\mu A$	$V_2-1.0$	V_2	$V_2+1.0$	V
"H" Output Voltage (2)	$V_{OH(2)}$	COM ₁ ~COM ₄	$I_O=-100\mu A$	$V_{DD}-0.6$		V	
"L" Output Voltage (2)	$V_{OL(2)}$		$I_O=+100\mu A$			$V_{LCD}+0.6$	V
Middle Level Voltage 1/3(2)	$V_{MC1/3}$	COM ₁ ~COM ₄	$I_O=\pm 100\mu A$	$V_1-0.6$	V_1	$V_1+0.6$	V
Middle Level Voltage 2/3(2)	$V_{MC2/3}$		$I_O=\pm 100\mu A$	$V_2-0.6$	V_2	$V_2+0.6$	V
Oscillating Frequency Range	f_{OSC}	OSC ₁ , OSC ₂ Terminals	25		200	kHz	
Oscillating Frequency	f_{OSC}	OSC ₁ , OSC ₂ , R=140kΩ	115	130	145	kHz	
Operating Current (1)	I_{DD}	V_{DD} Terminal		50	80	uA	
Operating Current (2)	I_{LCD}	V_{LCD} Terminal		15	25	uA	
Hysteresis Voltage	V_H	CE, SCL, DATA, MODE, INHb	0.3			V	

- Note 1) The relation : $V_{DD} \times 1.3 \geq |V_{DD}-V_{LCD}|$, $V_{SS} \geq V_{LCD}$ must be maintained.
 Note 2) $V_1=1/3|V_{DD}-V_{LCD}|$, $V_2=2/3|V_{DD}-V_{LCD}|$



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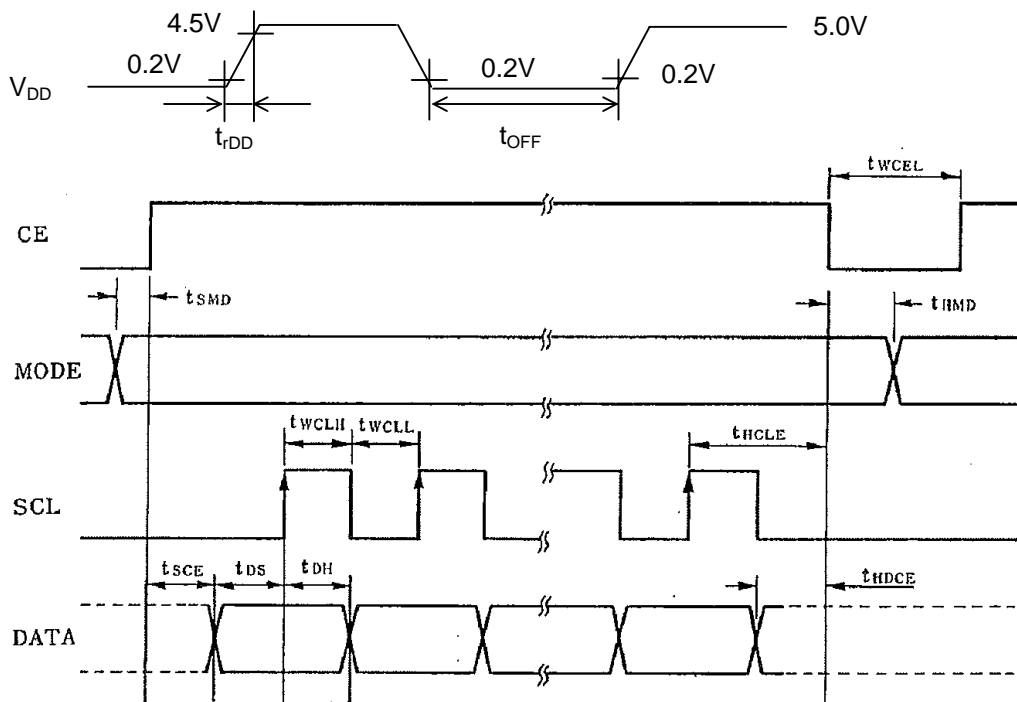
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(Ta= 25°C, V_{DD}=5.0V, V_{SS}=0V, V_{LCD}=V_{DD}-6.5V)

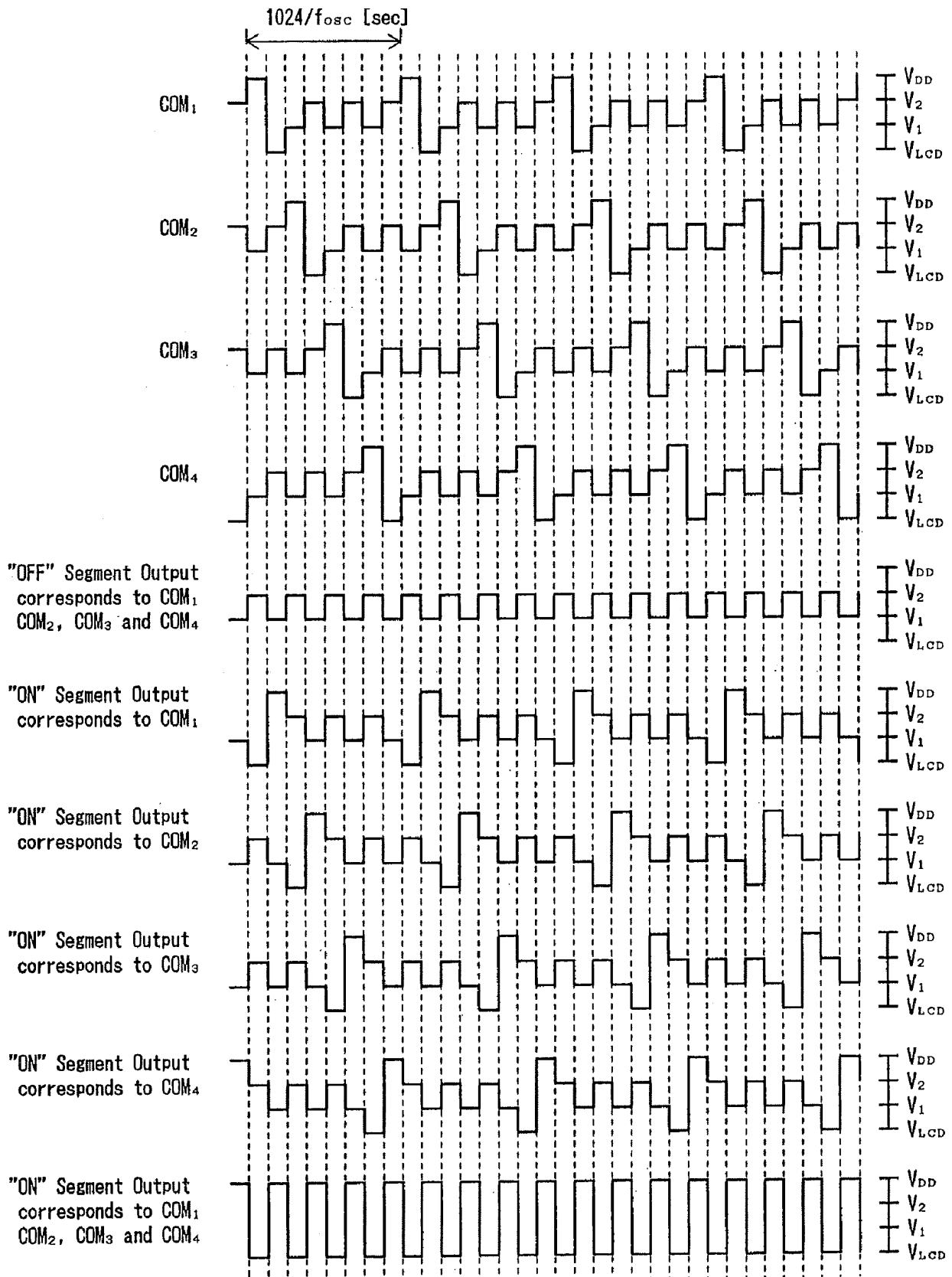
AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t _{WCLL}	SCL	0.25			US
"H" Clock Pulse Width	t _{WCLH}	SCL	0.25			US
DATA Set-up Time	t _{DS}	SCL, DATA	0.25			US
DATA Hold Time	t _{DH}	SCL, DATA	0.25			US
CE Set-up Time	t _{SCE}	CE, DATA	1.0			US
CE Hold Time (1)	t _{HDCE}	CE, DATA	1.0			US
CE Hold Time (2)	t _{HCLE}	CE, SCL T	1.25			US
MODE Set-up Time	t _{SMD}	MODE, CE	0.25			US
MODE Hold Time	t _{HMD}	MODE, CE	0.25			US
"L" Chip Enable Pulse Width	t _{WCEL}	CE	4.0			US
Power Supply Rise Time	t _{rDD}	V _{DD}	0.1		10	ms
Power Supply OFF Time	t _{OFF}	V _{DD}	1			ms

Input Timing Characteristics



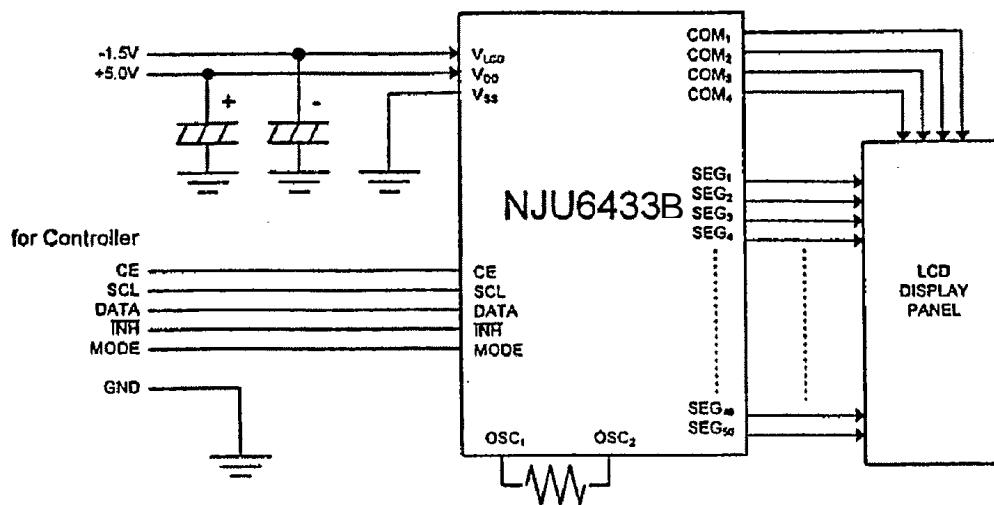
• LCD Driving Waveform(1/4DUTY · 1/3BIAS)



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APPLICATION CIRCUIT



Note) The internal display data is undefined when V_{DD} is just turned on. To avoid the meaningless display, please keep the INHb terminal at "L" until proper display data has been transferred. In order to set the initial condition, 200-bit blank data or the first 200-bit data to be displayed should be transferred.

[CAUTION]

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