PRELIMINARY

12-CHARACTER 4-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6465 is a Dot Matrix LCD controller driver for 12-character 4-line with icon display in single chip.

It contains voltage converter and regulator, bleeder resistance, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.

The voltage converter generates high voltage(about 8V) from the supply voltage(3V) and it is regulated by the regulator. The bias level of LCD driving voltage is generated of high value of bleeder resistance and the buffer amplifire convert its impedance. The 16th gray scale contrast control function is incorporated for its adjustment. Therefore, simple power supply circuit and easy contrast adjustment are available.

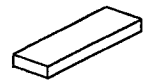
The complete CR oscillator is incorporated, therefore no external components for oscillation circuit are required.

The microprocessor interface circuits which operate by 1MHz, can be selected serial, 4 or 8 bit interface.

The character generator ROM consists of 10,080 bits stores 252 kinds of character Font. Each 160 bits CG RAM and Icon display RAM can stores 4 kinds of special character displayed on the dot matrix display area or 152 kind of Icon on the Icon display area.

The 37-common (32 for character, 4 for icon and 1 for static) and 63-segment (60 for character, 2 for icon and 1 for static) drivers operated up to 13.5V drives 12-character 4-line with 128 Icon and static segment LCD display.

■ PACKAGE OUTLINE

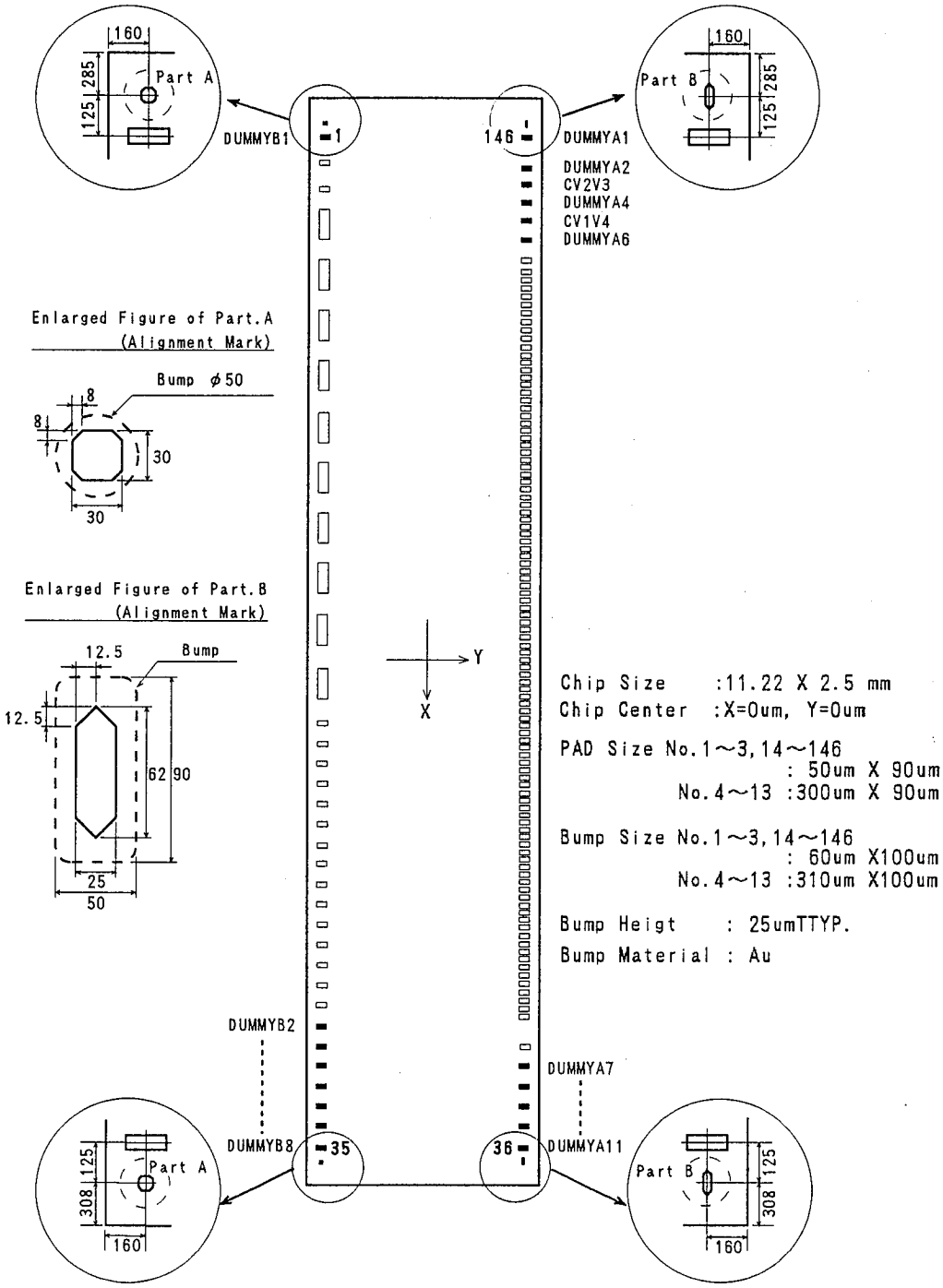


NJU6465CH

■ FEATURES

- 12-character 4-line Dot Matrix LCD Controller Driver
- Maximum 128 Icon Display
- Serial, 4 or 8 Bit parallel Direct Interface with Microprocessor
- Display Data RAM - 48 x 8 bits : Maximum 12-character 4-line Display
- Character Generator ROM - 10,080 bits : 252 Characters for 5 x 7 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 7 Dots)
- Icon Display RAM - 32 x 5 bits : Maximum 128 Icon
- High Voltage LCD Driver : 37-common / 63-segment
- Duty and Bias Ratio : 1/36 duty and 1/7 bias
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Common and Segment driver Location order Select Function(Mode A/Mode B)
- Power On Initialization / Hardware Reset
- Voltage Converter and Bleeder Resistance on-chip
- Voltage regulator on-chip
- Software contrast control
- Oscillation Circuit on-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 3.6 V (Except LCD Driving Voltage)
- Package Outline --- Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



UNIT : um

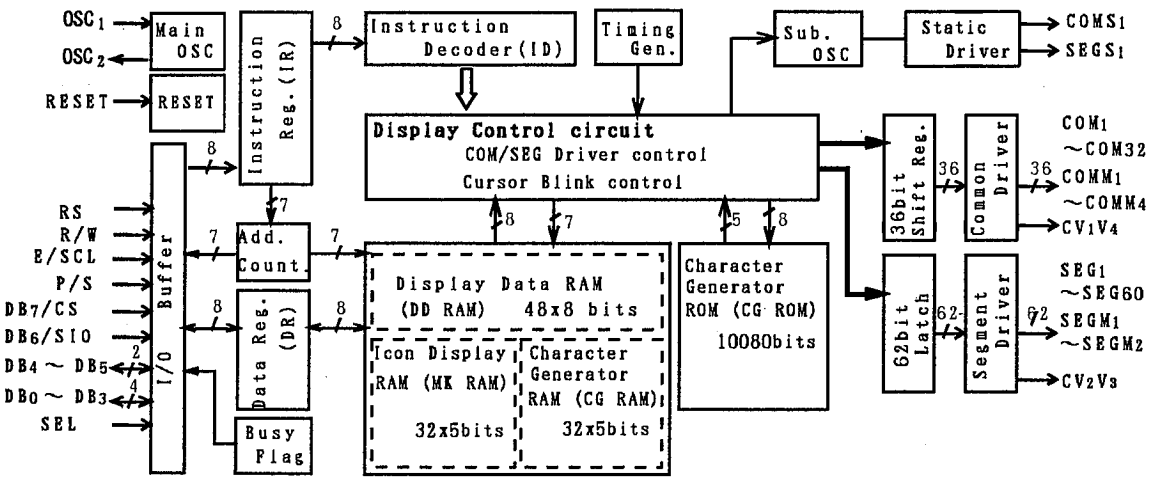
■ PAD COORDINATES

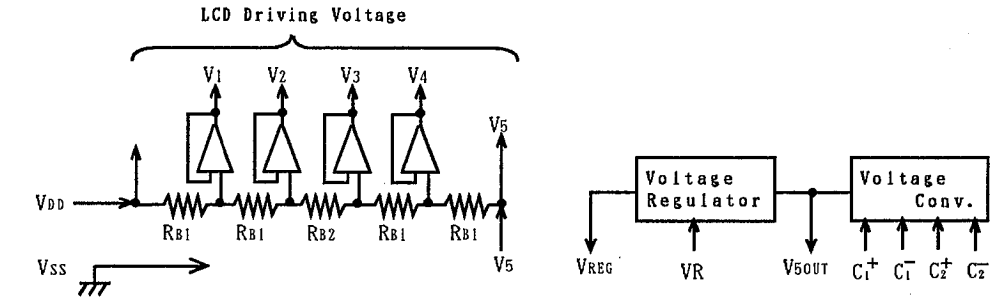
CHIP SIZE 11.22mm x 2.5mm (CHIP CENTER X=0μm, Y=0μm)

PAD No.	PAD NAME		X=(μm)	Y=(μm)	PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B				Mode A	Mode B		
1	$DUMMYB_1$	$DUMMYB_1$	-5200	-1090	51	COM_{26}	COM_{26}	3100	1090
2	OSC_1	OSC_1	-4980	-1090	52	COM_{27}	COM_{27}	3020	1090
3	OSC_2	OSC_2	-4735	-1090	53	COM_{28}	COM_{28}	2940	1090
4	V_5	V_5	-4439	-1090	54	COM_{29}	COM_{29}	2860	1090
5	V_{SS}	V_{SS}	-3939	-1090	55	COM_{30}	COM_{30}	2780	1090
6	V_{5OUT}	V_{5OUT}	-3439	-1090	56	COM_{31}	COM_{31}	2700	1090
7	C_2^-	C_2^-	-2939	-1090	57	COM_{32}	COM_{32}	2620	1090
8	C_2^+	C_2^+	-2439	-1090	58	$SEGM_1$	$SEGM_2$	2540	1090
9	C_1^-	C_1^-	-1939	-1090	59	SEG_1	SEG_{60}	2460	1090
10	C_1^+	C_1^+	-1439	-1090	60	SEG_2	SEG_{59}	2380	1090
11	V_{DD}	V_{DD}	- 939	-1090	61	SEG_3	SEG_{58}	2300	1090
12	VR	VR	- 439	-1090	62	SEG_4	SEG_{57}	2220	1090
13	V_{REG}	V_{REG}	61	-1090	63	SEG_5	SEG_{56}	2140	1090
14	TEST	TEST	509	-1090	64	SEG_6	SEG_{55}	2060	1090
15	SEL	SEL	738	-1090	65	SEG_7	SEG_{54}	1980	1090
16	RESET	RESET	966	-1090	66	SEG_8	SEG_{53}	1900	1090
17	P/S	P/S	1195	-1090	67	SEG_9	SEG_{52}	1820	1090
18	RS	RS	1423	-1090	68	SEG_{10}	SEG_{51}	1740	1090
19	R/W	R/W	1652	-1090	69	SEG_{11}	SEG_{50}	1660	1090
20	E/SCL	E/SCL	1880	-1090	70	SEG_{12}	SEG_{49}	1580	1090
21	DB_0	DB_0	2118	-1090	71	SEG_{13}	SEG_{48}	1500	1090
22	DB_1	DB_1	2355	-1090	72	SEG_{14}	SEG_{47}	1420	1090
23	DB_2	DB_2	2592	-1090	73	SEG_{15}	SEG_{46}	1340	1090
24	DB_3	DB_3	2829	-1090	74	SEG_{16}	SEG_{45}	1260	1090
25	DB_4	DB_4	3066	-1090	75	SEG_{17}	SEG_{44}	1180	1090
26	DB_5	DB_5	3303	-1090	76	SEG_{18}	SEG_{43}	1100	1090
27	DB_6/SIO	DB_6/SIO	3540	-1090	77	SEG_{19}	SEG_{42}	1020	1090
28	DB_7/CS	DB_7/CS	3777	-1090	78	SEG_{20}	SEG_{41}	940	1090
29	$DUMMYB_2$	$DUMMYB_2$	3977	-1090	79	SEG_{21}	SEG_{40}	860	1090
30	$DUMMYB_3$	$DUMMYB_3$	4177	-1090	80	SEG_{22}	SEG_{39}	780	1090
31	$DUMMYB_4$	$DUMMYB_4$	4377	-1090	81	SEG_{23}	SEG_{38}	700	1090
32	$DUMMYB_5$	$DUMMYB_5$	4577	-1090	82	SEG_{24}	SEG_{37}	620	1090
33	$DUMMYB_6$	$DUMMYB_6$	4777	-1090	83	SEG_{25}	SEG_{36}	540	1090
34	$DUMMYB_7$	$DUMMYB_7$	4977	-1090	84	SEG_{26}	SEG_{35}	460	1090
35	$DUMMYB_8$	$DUMMYB_8$	5177	-1090	85	SEG_{27}	SEG_{34}	380	1090
36	$DUMMYA_{11}$	$DUMMYA_{11}$	5177	1090	86	SEG_{28}	SEG_{33}	300	1090
37	$DUMMYA_{10}$	$DUMMYA_{10}$	4977	1090	87	SEG_{29}	SEG_{32}	220	1090
38	$DUMMYA_9$	$DUMMYA_9$	4777	1090	88	SEG_{30}	SEG_{31}	140	1090
39	$DUMMYA_8$	$DUMMYA_8$	4577	1090	89	SEG_{31}	SEG_{30}	60	1090
40	$DUMMYA_7$	$DUMMYA_7$	4400	1090	90	SEG_{32}	SEG_{29}	- 20	1090
41	$SEGS_1$	$SEGS_1$	4200	1090	91	SEG_{33}	SEG_{28}	- 100	1090
42	COM_9	COM_9	3820	1090	92	SEG_{34}	SEG_{27}	- 180	1090
43	COM_{10}	COM_{10}	3740	1090	93	SEG_{35}	SEG_{26}	- 260	1090
44	COM_{11}	COM_{11}	3660	1090	94	SEG_{36}	SEG_{25}	- 340	1090
45	COM_{12}	COM_{12}	3580	1090	95	SEG_{37}	SEG_{24}	- 420	1090
46	COM_{13}	COM_{13}	3500	1090	96	SEG_{38}	SEG_{23}	- 500	1090
47	COM_{14}	COM_{14}	3420	1090	97	SEG_{39}	SEG_{22}	- 580	1090
48	COM_{15}	COM_{15}	3340	1090	98	SEG_{40}	SEG_{21}	- 660	1090
49	COM_{16}	COM_{16}	3260	1090	99	SEG_{41}	SEG_{20}	- 740	1090
50	COM_{25}	COM_{25}	3180	1090	100	SEG_{42}	SEG_{19}	- 820	1090

PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B		
101	SEG_{43}	SEG_{18}	- 900	1090
102	SEG_{44}	SEG_{17}	- 980	1090
103	SEG_{45}	SEG_{16}	-1060	1090
104	SEG_{46}	SEG_{15}	-1140	1090
105	SEG_{47}	SEG_{14}	-1220	1090
106	SEG_{48}	SEG_{13}	-1300	1090
107	SEG_{49}	SEG_{12}	-1380	1090
108	SEG_{50}	SEG_{11}	-1460	1090
109	SEG_{51}	SEG_{10}	-1540	1090
110	SEG_{52}	SEG_{9}	-1620	1090
111	SEG_{53}	SEG_{8}	-1700	1090
112	SEG_{54}	SEG_{7}	-1780	1090
113	SEG_{55}	SEG_{6}	-1860	1090
114	SEG_{56}	SEG_{5}	-1940	1090
115	SEG_{57}	SEG_{4}	-2020	1090
116	SEG_{58}	SEG_{3}	-2100	1090
117	SEG_{59}	SEG_{2}	-2180	1090
118	SEG_{60}	SEG_{1}	-2260	1090
119	$SEGM_{2}$	$SEGM_{1}$	-2340	1090
120	COM_{24}	COM_{24}	-2420	1090
121	COM_{23}	COM_{23}	-2500	1090
122	COM_{22}	COM_{22}	-2580	1090
123	COM_{21}	COM_{21}	-2660	1090
124	COM_{20}	COM_{20}	-2740	1090
125	COM_{19}	COM_{19}	-2820	1090
126	COM_{18}	COM_{18}	-2900	1090
127	COM_{17}	COM_{17}	-2980	1090
128	COM_{9}	COM_{9}	-3060	1090
129	COM_{7}	COM_{7}	-3140	1090
130	COM_{6}	COM_{6}	-3220	1090
131	COM_{5}	COM_{5}	-3300	1090
132	COM_{4}	COM_{4}	-3380	1090
133	COM_{3}	COM_{3}	-3460	1090
134	COM_{2}	COM_{2}	-3540	1090
135	COM_{1}	COM_{1}	-3620	1090
136	$COMM_{4}$	$COMM_{4}$	-3700	1090
137	$COMM_{3}$	$COMM_{3}$	-3780	1090
138	$COMM_{2}$	$COMM_{2}$	-3860	1090
139	$COMM_{1}$	$COMM_{1}$	-3940	1090
140	$COMS_{1}$	$COMS_{1}$	-4045	1090
141	$DUMMYA_{6}$	$DUMMYA_{6}$	-4245	1090
142	CV_1V_4	CV_1V_4	-4445	1090
143	$DUMMYA_{4}$	$DUMMYA_{4}$	-4645	1090
144	CV_2V_3	CV_2V_3	-4845	1090
145	$DUMMYA_{2}$	$DUMMYA_{2}$	-5045	1090
146	$DUMMYA_{1}$	$DUMMYA_{1}$	-5200	1090

■ BLOCK DIAGRAM





■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
11, 5	V_{DD}, V_{SS}		Power Source V_{DD} ; +3V, V_{SS} ; 0V
4	V_6		LCD driving voltage
2	OSC_1	I	System clock input terminal This terminal should be open, for internal clock operation.
3	OSC_2	O	System clock output terminal This terminal can use for clock frequency monitoring.
17	P/S	I	Parallel or serial interface selection terminal "0": Serial interface "1": Parallel interface
18	RS	I	Register selection signal input terminal "0": Instruction register (writing) Busy flag, address counter (reading) "1": Data register (writing / reading)
19	R/W	I	Read / Write selection signal input terminal "0": Write "1": Read
20	E	I	Read / Write activation signal input in parallel mode
	SCL	I	Sift clock input in serial mode
28	DB_7	I/O	3-state data bus for MSB to transfer the Data between MPU and NJU6465 in parallel mode DB_7 is also used for the Busy Flag reading.
	CS	I	Chip select signal input in serial mode
27	DB_6	I/O	3-state data bus for bit 6 to transfer the Data between MPU and NJU6465 in parallel mode
	SIO	I/O	Serial Data I/O in serial mode
25, 26	DB_4, DB_5	I/O	3-state data bus for bit 4 and 5 to transfer the Data between MPU and NJU6465 in parallel mode In serial mode, these terminals are not used and should be open.
21~24	DB_0~DB_3	I/O	3-state data bus for lower 4 bit to transfer the Data between MPU and NJU6465 in parallel mode In serial and 4-bit parallel mode, these terminals are not used and should be open.
142 144	CV_1V_4 CV_2V_3		Capacitor terminals for noise reduction of COM/SEG output voltage. The capacitor connected between CV_1V_4, CV_2V_3 and V_{DD} is required to operate with the LCD panel actually.

No.	SYMBOL	I/O	FUNCTION
42～57 120～135	COM_1～COM_{32}	O	LCD common driving signal output terminals
136～139	$COMM_1$～$COMM_4$	O	Icon common driving signal output terminals
140	$COMS_1$	O	Static driving common signal output terminal When power down mode, V_{DD} or V_{SS} level are output.
59～118	SEG_1～SEG_{60}	O	LCD segment driving signal output terminals
119, 58	$SEGM_1$, $SEGM_2$	O	Icon segment driving signal output terminals
41 7～10	$SEGS_1$ C_1^+, C_1^- C_2^+, C_2^-	O	Static Driving Segment signal output terminal When power down mode, V_{DD} or V_{SS} level are output. Step up voltage capacitor connecting terminals In case of tripler operation, connect the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-. In case of doubler operation, connect the capacitor between C_2^+ and C_2^-, connect C_2^+ to C_1^+, and C_1^- should be open.
6	V_{SOUT}	O	Step up voltage output terminal
13	V_{REG}	O	Voltage regulator output terminal Connect the resistor between this terminal and VR Terminal.
12	VR		Reference voltage for voltage regulator input terminal Connect the resistor between this terminal and V_{DD} terminal.
16	RESET	I	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset (at f_{osc}=212KHz).
15	SEL	I	Common and Segment driver location order select terminal "0": Mode A location (See the PAD COORDINATES) "1": Mode B location (See the PAD COORDINATES)
14	TEST	I	Maker Testing Terminal (Pull down) This terminal should be connected to VSS or open.
29～34 145, 143, 141, 40～37	$DUMMYB_2$～ $DUMMYB_7$ $DUMMYA_2$, $DUMMYA_4$, $DUMMYA_6$, $DUMMYA_7$～ $DUMMYA_{10}$		Dummy terminal These terminals are electrically open.
1 35 146 36	$DUMMYB_1$ $DUMMYB_8$ $DUMMYA_1$ $DUMMYA_{11}$		Dummy terminal These terminals are electrically open and an alignment pattern is placed beside each terminals.

■ FUNCTIONAL DESCRIPTION

(1) Description for each block

(1－1) Register

The NJU6465 incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).

The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.

When the address data for the DD RAM, CG RAM or MK RAM is written into the Register(IR), the addressed data in the DD RAM, CG RAM or MK RAM is transferred to the Register(DR).
By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM, CG RAM or MK RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

5

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter (DB_0～DB_6)
1	0	DR	Write (Register(DR) to DD RAM, CG RAM or MK RAM)
1	1		Read (DD RAM, CG RAM or MK RAM to Register(DR))

(1－2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag (BF) is "1", and any instruction reading is inhibited.

The busy flag (BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.

The next instruction should be written after the busy flag(BF) goes to "0".

(1－3) Address Counter (AC)

The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.

When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.

After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.

The address data in the Counter(AC) is output from DB_6～DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1－4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 48 x 8 bits stores up to 48-character display data represented in 8-bit code.
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.

	←Higher order bit					Lower order bit→	
AC	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
	← Hexadecimal →←			Hexadecimal →			

(Example) DD RAM address " 08 "

0	0	0	1	0	0	0
←— —	O	— —→←— — —		8	— — — →	

· 4-line Display

The relation between DD RAM address and display position on the LCD is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B

← Display Position

← DD RAM Address (Hexadecimal)

Note : The 1st, 2nd, 3rd and 4th line address are defined as $(00)_H$ to $(0B)_H$, $(10)_H$ to $(1B)_H$, $(20)_H$ to $(2B)_H$, and $(30)_H$ to $(3B)_H$. The end of each line address and the beginning of following line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	00
(10) ←	11	12	13	14	15	16	17	18	19	1A	1B	10
(20) ←	21	22	23	24	25	26	27	28	29	2A	2B	20
(30) ←	31	32	33	34	35	36	37	38	39	3A	3B	30

(Right Shift Display)

0B	00	01	02	03	04	05	06	07	08	09	0A	→ (0B)
1B	10	11	12	13	14	15	16	17	18	19	1A	→ (1B)
2B	20	21	22	23	24	25	26	27	28	29	2A	→ (2B)
3B	30	31	32	33	34	35	36	37	38	39	3A	→ (3B)

Note : The left and right shift performes only in same line, the display data do not change to other line.

(1－5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.
The storage capacity is up to 252 kinds of 5 x 7 dots character pattern(available address is $(04)_H$ through $(FF)_H$).
The correspondence between character code and standard character pattern of NJU6465 is shown in Table 2-1.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -02)

Lower 4 bit (Hexadecimal)	Upper 4 bit (Hexadecimal)															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(01)															
5	(02)															
6	(03)															
7	(04)															
8	(01)															
9	(02)															
A	(03)															
B	(04)															
C	(01)															
D	(02)															
E	(03)															
F	(04)															

5

(1 − 6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kind of character in 5 x 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(03)_H$ should be written to the DD RAM as shown in Table 2-1.

Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 (Upper bit ← → Lower bit)	7 6 5 4 3 (Upper bit)	2 1 0 (Lower bit)	4 3 2 1 0 (Upper bit ← → Lower bit)	
0 0 0 0 0 0 0 0	0 1 0 0 0	0 0 0	■ ■ ■ □ □	Character Pattern Example(1)
		0 0 1	□ □ □ □ ■	
		0 1 0	□ □ □ □ ■	
		0 1 1	■ ■ ■ □ □	
		1 0 0	□ □ □ □ □	
		1 0 1	□ □ □ ■ □	
		1 1 0	□ □ □ □ □	
		1 1 1	□ □ □ □ □	←Cursor Position
0 0 0 0 0 0 0 1	0 1 0 0 1	0 0 0	□ □ □ □ ■	Character Pattern Example(2)
		0 0 1	□ ■ □ ■ □	
		0 1 0	■ ■ ■ ■ □	
		0 1 1	□ □ □ □ □	
		1 0 0	■ ■ ■ ■ □	
		1 0 1	□ □ □ □ □	
		1 1 0	□ □ □ □ □	
		1 1 1	□ □ □ □ □	←Cursor Position
		0 0 0		
		0 0 1		
⋮	⋮	⋮	⋮	
0 0 0 0 0 0 1 1	0 1 0 1 1			
		1 0 0		
		1 0 1		
		1 1 0		
		1 1 1		

Notes : 1. Character code bit 0,1 correspond to the CG RAM address bit 3,4(2bits:4 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 2 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1－7) Icon Display RAM (MK RAM)

The NJU6465 can display maximum 128 Icons.
The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.

The relation between MK RAM address and Icon Display position is shown below:

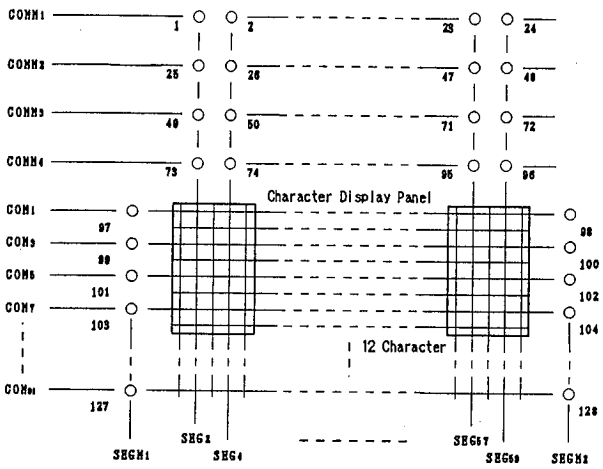


Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address		Bits for Icon Display Position								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0110 0000	60h	*	*	*	1	2	3	4	97	COMM1 Line and Both besides of 1st Line (COM1, 3, 5, 7)
0110 0001	61h	*	*	*	5	6	7	8	98	
:	:	:								
0110 0101	65h	*	*	*	21	22	23	24	102	
0110 0110	66h	*	*	*	*	*	*	*	103	
0110 0111	67h	*	*	*	*	*	*	*	104	
0110 1000	68h	*	*	*	25	26	27	28	105	COMM2 Line and Both besides of 2nd Line (COM9, 11, 13, 15)
0110 1001	69h	*	*	*	29	30	31	32	106	
:	:	:								
0110 1101	6Dh	*	*	*	45	46	47	48	110	
0110 1110	6Eh	*	*	*	*	*	*	*	111	
0110 1111	6Fh	*	*	*	*	*	*	*	112	
0111 0000	70h	*	*	*	49	50	51	52	113	COMM3 Line and Both besides of 3rd Line (COM17, 19, 21, 23)
0111 0001	71h	*	*	*	53	54	55	56	114	
:	:	:								
0111 0101	75h	*	*	*	69	70	71	72	118	
0111 0110	76h	*	*	*	*	*	*	*	119	
0111 0111	77h	*	*	*	*	*	*	*	120	
0111 1000	78h	*	*	*	73	74	75	76	121	COMM4 Line and Both besides of 4th Line (COM25, 27, 29, 31)
0111 1001	79h	*	*	*	77	78	79	80	122	
:	:	:								
0111 1101	7Dh	*	*	*	93	94	95	96	126	
0111 1110	7Eh	*	*	*	*	*	*	*	127	
0111 1111	7Fh	*	*	*	*	*	*	*	128	

(*) Don't care

Notes : 1. When the Icon display function using, the system should be initialized by the software initialization because the MK RAM is not initialized by the power turning on and hardware reset.
2. The cross-points between $SEGM_1$, $SEGM_2$ and some of common $COMM_1$ through $COMM_4$, even common likes as COM_2, COM_4...COM_{32}, are always off because of the corresponding RAM does not exist as shown above.
3. In the table 4, the bits D_5 to D_7 mentioned by * are invalid, therefore both of "0" or "1" can be written but these are no meaning.

(1－8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1－9) LCD Driver

LCD Driver consist of 37-common driver and 63-segment driver.

The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(1－10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(28)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
(AC)	0	1	0	1	0	0	0

4-Line display

	1	2	3	4	5	6	7	8	9	10	11	12
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B

← Display position

← DD RAM address (Hexadecimal)

↑ Cursor position

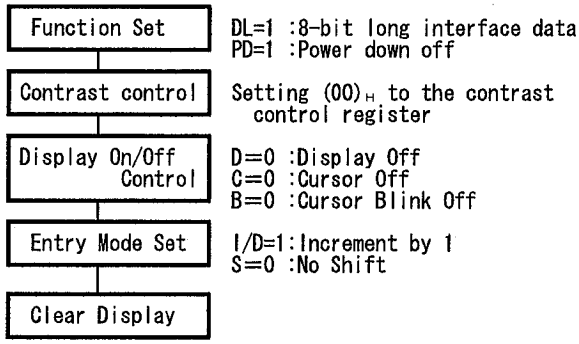
Note : The cursor or blinks also appear when the address counter (AC) selects the CG RAM or the MK RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG or MK RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2－1) Initialization By Internal Reset Circuits

The NJU6465 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 7 ms (f_{osc}=212kHz) after V_{DD} rises to 2.4V.

Initialization flow is shown below:

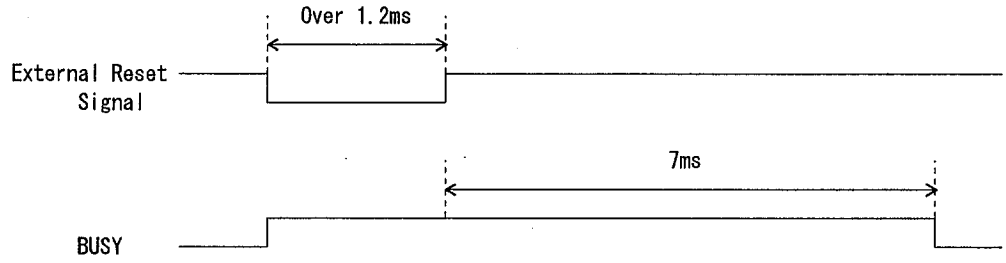


Note
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

(2－2) Initialization By Hardware

The NJU6465 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over 1.2ms to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 7 ms (f_{osc}=212kHz) after $\overline{\text{RESET}}$ terminal goes to "H".

・Timing Chart



(3) Instructions

The NJU6465 incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6465 and MPU or peripheral ICs operating different cycles. The operation of NJU6465 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).
Table 5. shows each instruction and its operating time.

Note : The execution time mentioned in Table 5. based on fcp or fosc=212kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	RS	R/W	C DB7	C DB6	O DB5	O DB4	D DB3	E DB2	DB1	DB0	DESCRIPTION	Execute Time
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	-
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets RAM address $(00)_H$ in AC.	6.87ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets RAM address $(00)_H$ in AC and returns display being shifted original position. RAM contents remain unchanged.	141us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decremen S=1:Accompanies display shift	0us
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	0us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor & shifts display without changing RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	cursor: 141us display: 0us
Function Set	0	0	0	0	1	DL	*	*	*	PD	Sets interface data length(DL) and power down mode(PD).	PD=0:0us PD=1: 200us
Contrast control	0	0	0	1	*	*	←—		C_C	—→	Sets data to Contrast Control Register.	0us
Set RAM Address	0	0	1	←—			A_R			—→	Sets RAM address. After this instruction, the data is transferred to/from RAM.	141us
Read Busy Flag & AC contents	0	1	BF	←—			AC			—→	Reads busy flag and AC content BF=1 : Internally operating BF=0 : Can accept instruction	0us
Write Data to RAM	1	0	←— Write Data (DD RAM) —→								Writes data into RAM.	141us
	1	0	*	*	*	←— (CG RAM) —→						
	1	0	*	*	*	←— (MK RAM) —→						
Read Data from RAM	1	1	←— Read Data (DD RAM) —→								Reads data from RAM.	141us
	1	1	*	*	*	←— (CG RAM) —→						
	1	1	*	*	*	←— (MK RAM) —→						
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM, MK RAM : Icon display RAM, A_R : RAM address (both of DD, CG and MK RAM) AC : Address counter used for both of DD, CG and MK RAM											

* : Don't care

(3－1) Description of each instructions

(a) Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker). Therefore, please avoid all "0" input or no meaning Enable signal input at data "0". (Especially please pay attention the output condition of Enable signal when the power turns on.)

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set increment.

If the cursor or blink are displayed, they are returned to the left end of the 1st line in the LCD.

The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

* = Don't care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the 1st line in the LCD if the cursor or blink are on the display.

The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (−1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shift.

5

(e) Display On/Off Control

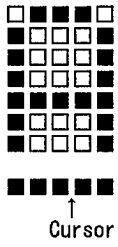
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

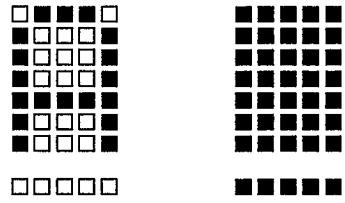
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 439ms at f_{OSC}=212kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. The cursor moves to the 2nd line when it passes the 12th digit of the 1st line.

Notice that the every 1st to 3rd line displays shift at the same time. When the displayed data are shifted repeatedly, each line moves only horizontally.

The 2nd and 3rd line display does not shift into the 1st and 2nd line.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	DL	*	*	*	PD

* = Don't care

Function set instruction which sets the interface data length and powerdown mode, is executed, when the code "1" is written into DB_5 and the code of (DL) and (PD) is written into DB_4(DL) and DB_0(PD), as shown below. In the serial interface operation, the DL is not cared.

When the powerdown mode is set, the display is off automatically (D=0). Afterward, when the powerdown mode is reset, the display is off continuously. The display is appeared by the display on (D="1") instruction.

Note
This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length of 8-bit (using from DB_7 to DB_0) in the parallel operation only
0	Set the interface data length of 4-bit (using from DB_7 to DB_4) in the parallel operation only The data must be sent or received twice in this mode.

PD	Function
1	Power down mode off (Normal operation)
0	Power down mode on (The display goes to off automatically.)

Note: When the Power down mode, it must be not execution except for this instruction.

(h) Contrast Control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	*	C_3	C_2	C_1	C_0	* = Don't care

Contrast Control instruction which adjusts the contrast of the LCD, is executed when the code "1" is written into DB_6 and the codes of C_3 to C_0 are written into DB_3 to DB_0 as shown below.

The contrast of LCD can be adjusted one of 16 voltage stage by setting this 4-bit register. See (5-1) to realize "how to adjust the Contrast of LCD".

Set the binary code "0000" when contrast adjustment is unused.

contrast	C_3	C_2	C_1	C_0
low	0	0	0	0
	:	:	:	:
high	1	1	1	1

(i) Set RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A_6	A_5	A_4	A_3	A_2	A_1	A_0
				←Higher order bit					Lower order bit →	

The RAM address set instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data (DB_6 to DB_0) is written into the address counter (AC) by this instruction. After this instruction execution, the data writing/reading is performed into/from the addressed RAM.

The RAM includes DD RAM, CG RAM and MK RAM, and these RAMs are shared by address as shown below.

RAM Address

DD RAM	1st Line	:	from	$(00)_H$	to	$(0B)_H$
DD RAM	2nd Line	:	from	$(10)_H$	to	$(1B)_H$
DD RAM	3rd Line	:	from	$(20)_H$	to	$(2B)_H$
DD RAM	4th Line	:	from	$(30)_H$	to	$(3B)_H$
CG RAM	4 characters	:	from	$(40)_H$	to	$(5F)_H$
MK RAM	128 icons	:	from	$(60)_H$	to	$(7F)_H$

(j) Read Busy Flag & AC contents

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A_6	A_5	A_4	A_3	A_2	A_1	A_0
				←Higher order bit				Lower order bit→		

This instruction reads out the internal status of the NJU6465. When this instruction is executed, the busy flag (BF) stored in DB_7 and the address counter (AC) contents stored in DB_6 to DB_0 are read out.

The (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(k) Write Data to RAM

Write Data to RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8-bit data (A_7 to A_0) are written into the DD RAM, and the binary 5-bit data (A_4 to A_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

・Write Data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			←Higher order bit						Lower order bit→	

・Write Data to CG or MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	*	*	*	D_4	D_3	D_2	D_1	D_0
						←Higher order bit			Lower order bit →	

(l) Read Data from RAM

Read Data from RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 8-bit data (D_7 to D_0) are read out from the DD RAM, the binary 5-bit data (D_7 to D_0) are read out from the CG or MK RAM. The selection of RAM is determined by previous instruction. Before executing this instruction, RAM address set must be executed, otherwise the read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The RAM address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note: The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the DD RAM, CG RAM or DD RAM. Even if the read instruction is executed after this write instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

・Read Data from DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

←Higher order bit　　Lower order bit→

・Read Data from CG or MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	*	*	*	D_4	D_3	D_2	D_1	D_0

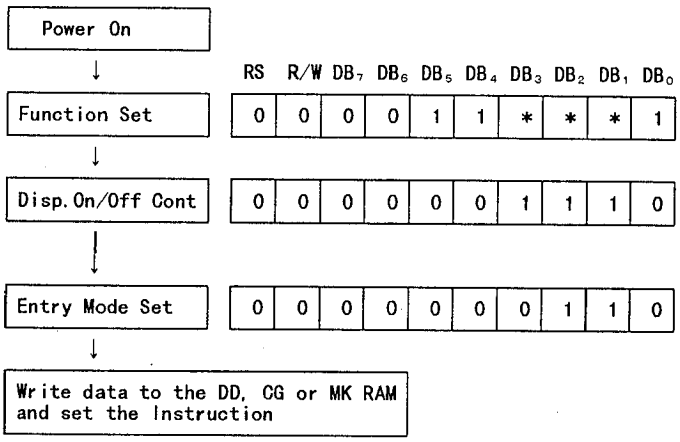
←Higher order bit　　Lower order bit →

5

(3－2) Initialization using the internal reset circuits

(a) 8-bit operation (Using internal reset circuits).

The Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.



Initialized.
No display appears.

Set the 8-bit operation and Powerdown mode off.

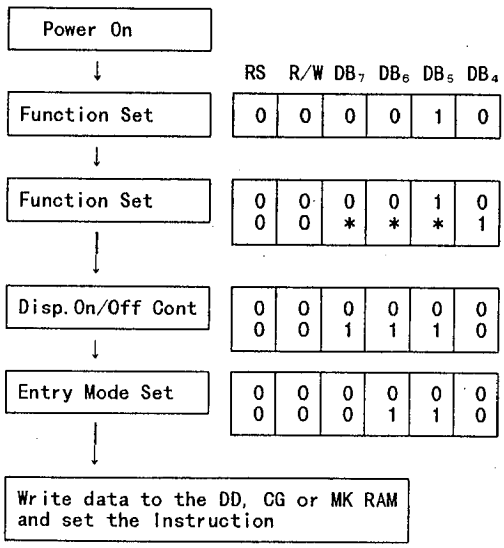
Turns on display and cursor. Entire display is in space mode set by the initialization.

Example for set address increment and cursor right shift when the data write to the DD, CG or MK RAM.

(b) 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.



Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation, Power down mode off, 5 x 7 dots Font.
The 4-bit operation starts from this step.

Turn on display and cursor.
Entire display is in space mode set by the initialization.

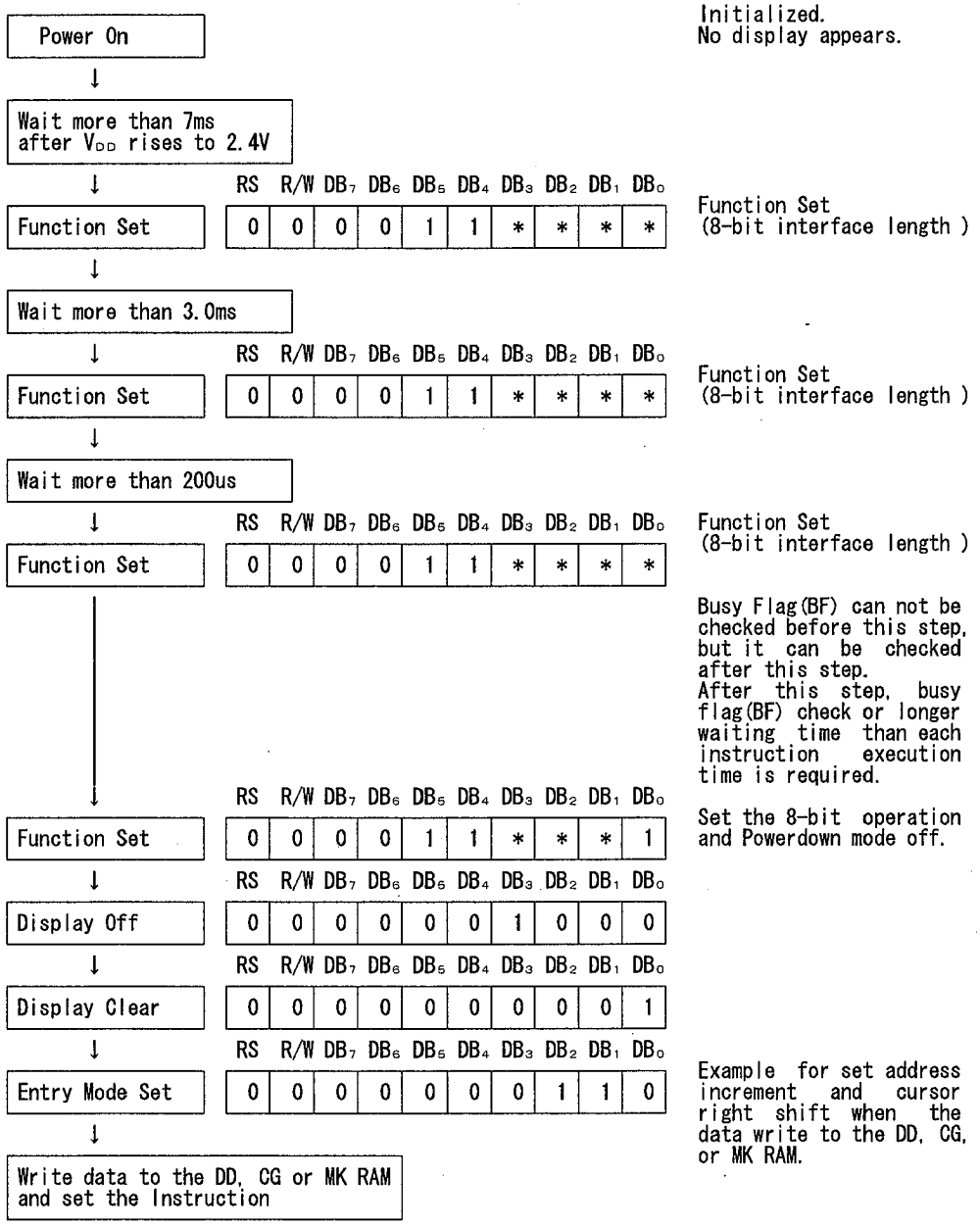
Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

Note: When the Icon display function using, the system should be initialized by software initialization.

(3－3) Initialization by instruction

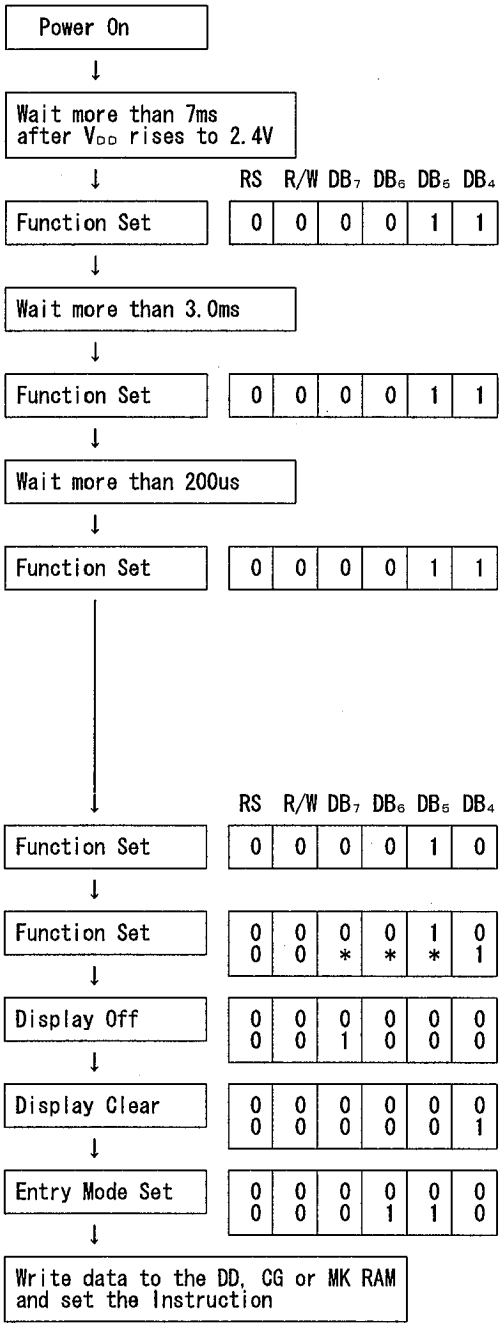
If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6465 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.



Note: When the Icon display function using, the system should be initialized by software initialization.

(b) Initialization by Instruction in 4-bit interface length



Initialized.
No display appears.

Function Set
(8-bit interface length)

Function Set
(8-bit interface length)

Function Set
(8-bit interface length)

Busy Flag (BF) can not be checked before this step, but it can be checked after this step.
After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.

Function Set
Set 4-bit interface length by 8-bit interface length.

Set the 4-bit operation and Powerdown mode off.

Example for set address increment and cursor right shift when the data write to the DD, CG or DD RAM.

Note: When the Icon display function using, the system should be initialized by software initialization.

(4) Powerdown Function

NJU6465 incorporates the powerdown mode to decrease the operating current.
The powerdown mode can be set/reset by the function set instruction.
In the powerdown mode, all the character display (12-character 4-line) and icon display turn off and only the static display area operates automatically.
The status of internal circuits at the powerdown mode is shown below :

- Main oscillator stops operation and sub oscillator for the static display starts operations.
- Voltage converter, voltage regulator and buffer amplifire for the bleeder resistance stop the operation.
- The contents of DD RAM, CG RAM and MK RAM are kept.

(5) LCD display

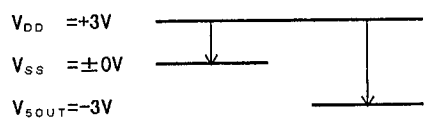
(5－1) Power Supply for LCD Driving

NJU6465 incorporates Voltage converter (tripler or doubler) to generate the LCD driving high voltage, Voltage regulator to adjust the LCD driving voltage, Bleeder resistance and buffer amplifire.

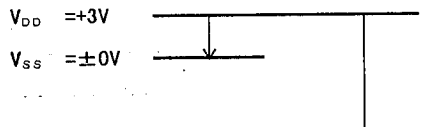
(a) Voltage converter

- Voltage tripler
  By connecting the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-, V_{SS} and V_{5OUT} respectively, two times negative voltage of $V_{DD} - V_{SS}$ output from V_{5OUT}.
- Voltage doubler
  By connecting the capacitor between C_2^+ and C_2^-, V_{SS} and V_{5OUT} respectively, and connecting the C_1^+ terminal to C_2^+ terminal, and C_1^- terminal being open, negative voltage of $V_{DD} - V_{SS}$ output from V_{5OUT}.

The voltage relation for Voltage tripler/doubler



Voltage Doubler

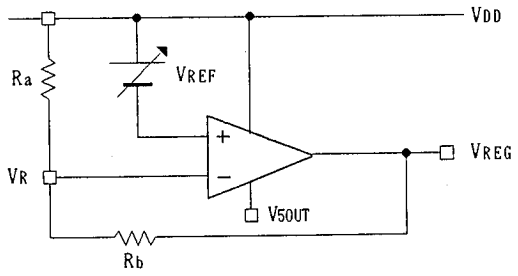


Voltage Tripler

(b) Voltage Regulator

Voltage Regulator incorporates a non-inverting OP-AMP which supplied V_{DD} and V_{5OUT}, and a reference voltage source.
By stetting the VR level by connecting R_a and R_b, the regulator which amplifies V_{REF} output the LCD driving voltage to the V_{REG} terminal.
Therefore, the LCD operating voltage can be output between V_{DD} and V_{REG} by setting V_{REF} and the external resistances R_a and R_b.

$$V_{REG}=(1+R_b/R_a)\cdot V_{REF}$$ where, $V_{DD}=0V$ and $|V_{REG}| < |V_{5OUT}|$

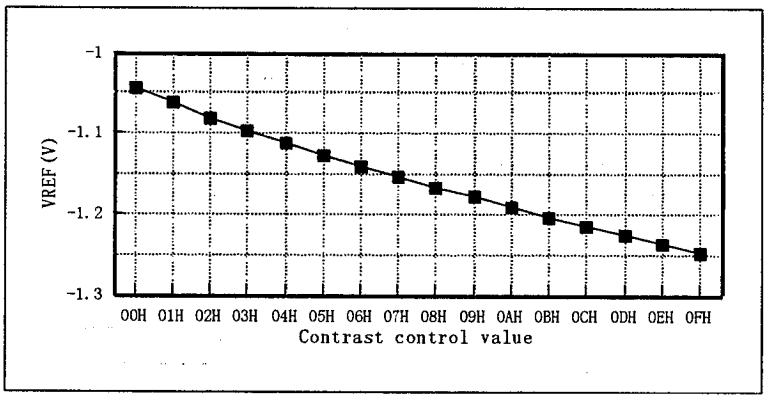


The contrast control function performs V_{REF} value adjustment from 1st step to 16th step by a step setting when the 4-bit data write into the contrast control register by the instruction.

Note : Set the contrast control register to $(00)_H$ when the contrast control function is unused.
Use variable resistances to the external resistances R_a, R_b and a thermister if need due to the voltage reference V_{REF} is changed by the lot and operating temperature.
Take care the Noise input on the V_R terminal because of it designed in high impedance.
Short wiring or sealed wiring are required to avoid the noise input, if necessary.

[The Voltage Reference V_{REF} characteristics]

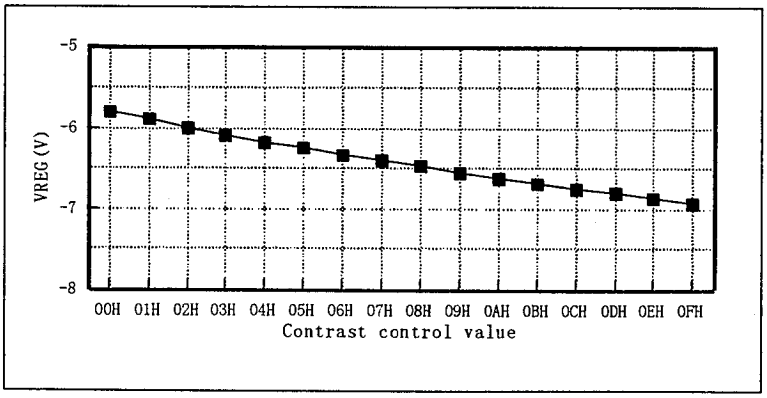
Supply Voltage : V_{DD}= 0V, V_{SS}= -3V Temperature : 25°C



[The LCD Operating Voltage V_{REG} characteristics]

Supply Voltage : V_{DD}= 0V, V_{SS}= -3V Voltage Tripler Output : V_{SOUT}=-9V
External Resistances : Ra = 180KΩ, Rb = 820KΩ Temperature : 25°C

Used Equation : $V_{REG}(xx)_H = (1 + 820k\Omega / 180k\Omega) \cdot V_{REF}(xx)_H$



(c) Bleeder Resistance

Each LCD driving voltage (V_1, V_2, V_3, V_4) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP to get a enough display characteristics with low operating current.

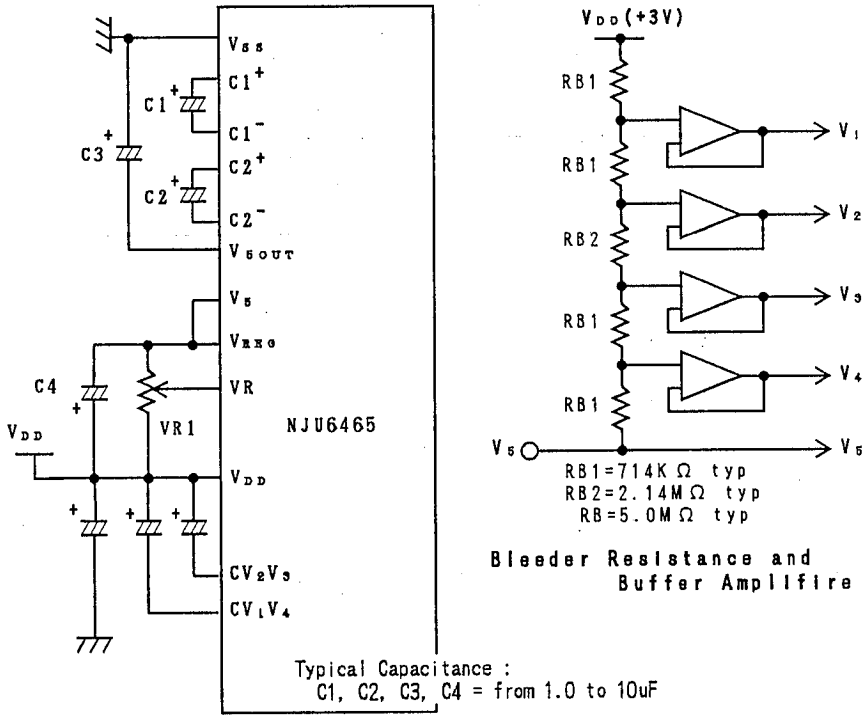
The bleeder resistance is set 1/7 bias suitable for 1/36 duty ratio and 5MΩ resistance in total.

The capacitor connected between V_5 and V_{DD} is needed for stabilizing V_5. The determination of the each capacitance of C_1, C_2 and C_3 generating for LCD operating voltage, is required to operate with the LCD panel actually. The capacitance for the typical application is shown below :

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/36
	Bias	1/7
V_{LCD}		$V_{DD}-V_5$

V_{LCD} is the maximum amplitude for LCD driving voltage.



Typical application
for LCD operating voltage generation

Note 1: Take care the Noise input on the V_R terminal as designed in high impedance. Short wiring or sealed wiring are required to avoid the noise input, if necessary.

Note 2: The capacitor connected CV_1V_4 and CV_2V_3 terminals are required to operate with the LCD panel actually.

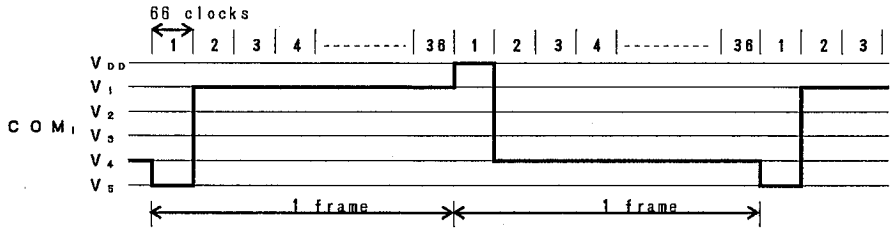
(5－2) Relation between oscillation frequency and LCD frame frequency

As the NJU6465 incorporate oscillation capacitor and resistor for CR oscillation, 192kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 212kHz oscillation.

(1 clock = 4.76us)

1/36 duty ratio



1 frame = 4.76(us) * 66 * 36 = 11.3(ms)

Frame frequency = 1 / 11.3(ms) = 88.5(Hz)

(6) Interface with MPU

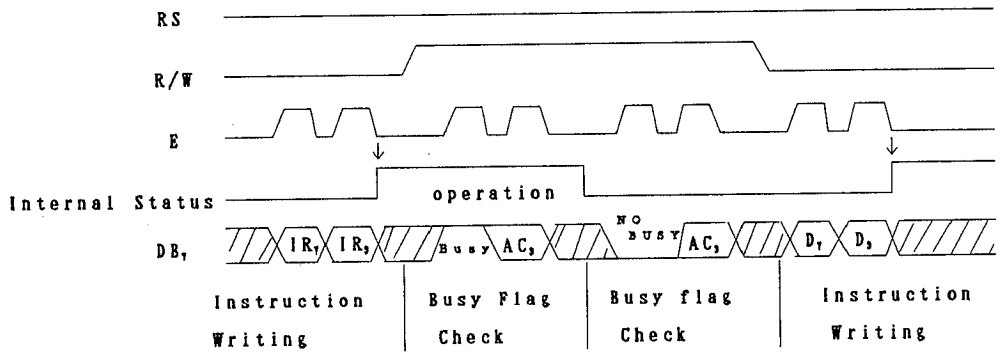
Interface circuits of NJU6465 can be connected to serial or 4/8-bit parallel.
NJU6465 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

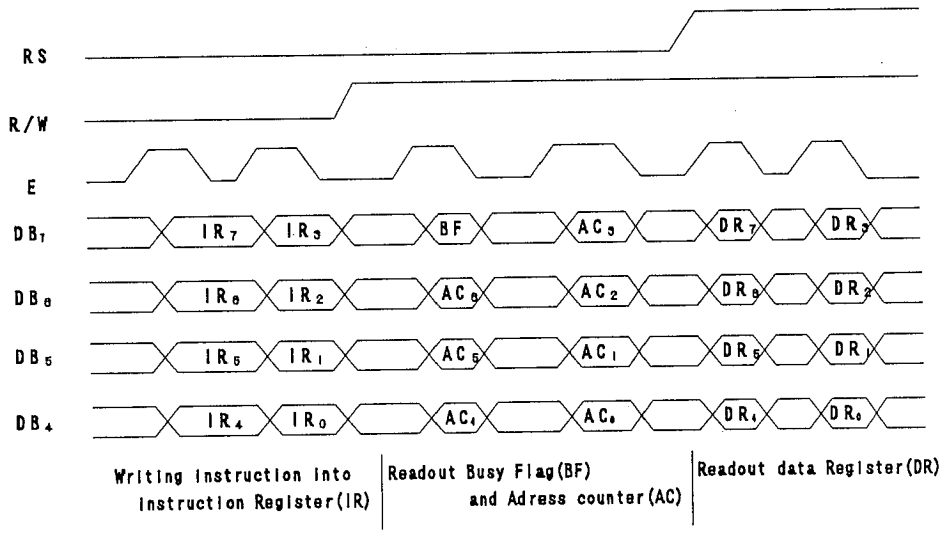
(6－1) 4-bit MPU interface

When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

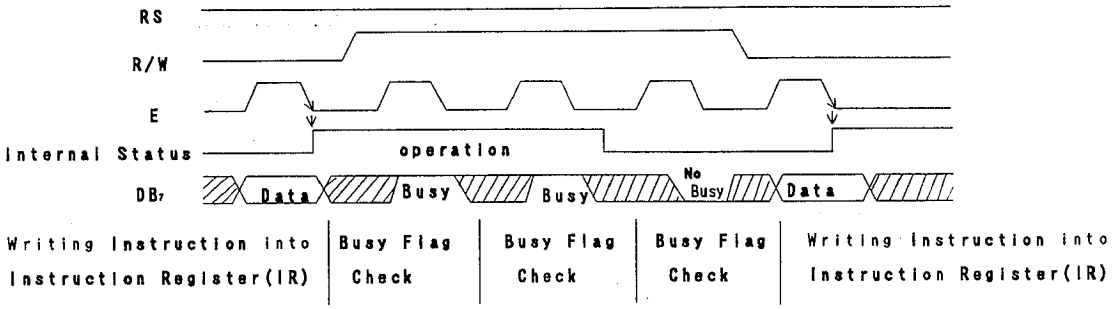
The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check can be executed after two-time 4-bit data transfer (1 instruction execution by two-time transfer). In this case, the data of busy flag and address counter contents are also output twice.





(6－2) 8-bit MPU interface



(6－3) Serial interface

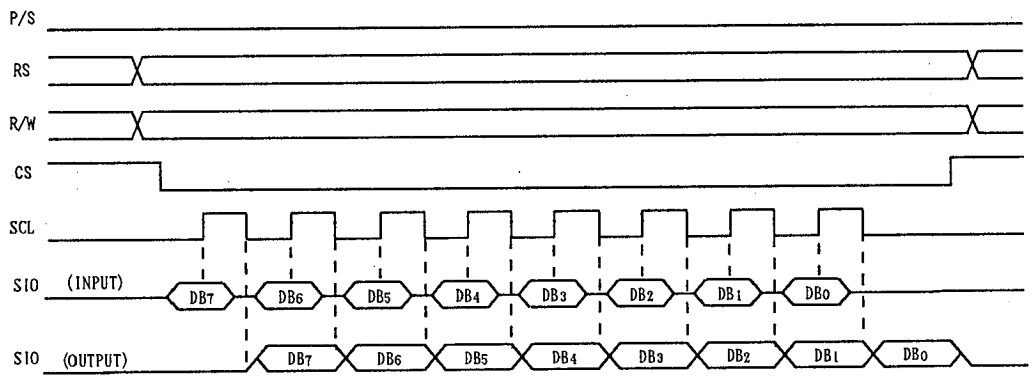
Serial interface circuit is activated when the P/S terminal is set to "L" level then the chip select terminal (CS) goes to "L" level. The data input/output is MSB first like as the order of DB_7, DB_6 ···· DB_0.

The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input. In case of entering over than 8-bit data, valid data is last 8-bit data.

The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	- 0.3 ~ + 7.0	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recomended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.

Note 3) All voltage values are specified as V_{SS} = 0V

Note 4) The relation : $V_{DD} > V_{SS}$, $V_{DD} > V_{SS} \geqq V_{SOUT}$, V_{SS}=0V must be maintained.

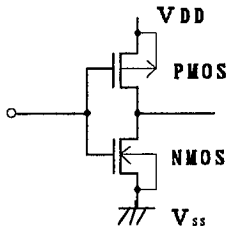
■ **ELECTRICAL CHARACTERISTICS** (V_{DD}=3V±20% , Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	Note
Operationg Voltage		V_{DD}		2.4	3.0	3.6	V	
Input Voltage		V_{IH}		0.8V_{DD}		V_{DD}	V	5
		V_{IL}				0.2V_{DD}	V	5
Output Voltage		V_{OH}	$-I_{OH}$=0.205mA, V_{DD}=3V	2.0			V	6
		V_{OL}	I_{OL}=1.6mA , V_{DD}=3V			0.5	V	6
Driver On-resist. (COM)		R_{COM}	$\pm I_d$=1μA (All com term.)			20	kΩ	9
Driver On-resist. (SEG)		R_{SEG}	$\pm I_d$=1μA (All seg term.)			30	kΩ	9
Input Leakage Current		I_{LI}	V_{IN}=0 or V_{DD}	-1		1	uA	7
Pull-up MOS Current		$-I_P$	V_{DD}=3V (All DB terminals)	10	25	50	uA	
Operating Current		I_{DD1}	V_{DD}=3V, f_{OSC}=Internal Osc. V_5=-5V, during display		180	250	uA	8
		I_{DD2}	V_{DD}=3V, f_{OSC}=Internal Osc. during access, t_{CYCE}=5us			500	uA	8
		I_{DD3}	V_{DD}=3V, f_{OSC}=Internal Osc. during Powerdown mode			20	uA	8
Voltage Converter (Tripler)	Output Voltage	V_{5OUT}	V_{DD}=3V, I_{OUT}=100uA, Ta=25°C	-4.6	-4.8		V	
	Voltage Efficiency	V_{ef}	R_L=∞	90.0	95.0		%	
Voltage Converter (Doubler)	Output Voltage	V_{SOUT}	V_{DD}=3V, I_{OUT}=100uA, Ta=25°C		-1.8		V	
	Voltage Efficiency	V_{ef}	R_L=∞		95.0		%	
Voltage Regulator	Reference Voltage	V_{REF}	Contrast Control=(00)$_H$, Ta=25°C	V_{DD}-0.75	V_{DD}-1.05	V_{DD}-1.35	V	
	Output Voltage	V_{REG}	R_L=∞, V_{5OUT}=-6V, Ta=25°C, R_a=180KΩ, R_b=820KΩ, Contrast Control=(00)$_H$		V_{DD}-5.8			
Bleeder resistance		R_B	V_{DD}-V_5=3V		5		MΩ	
Oscillation Frequency		f_{OSC}	V_{DD}=3V, Ta=25°C	135	212	289	kHz	
LCD Driving Voltage		V_{LCD}	V_{LCD}=V_{DD}-V_5	V_{DD}-3.0		V_{DD}-13.5	V	10

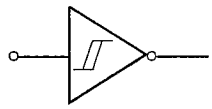
Note 5) Input/Output structure except LCD driver are shown below:

·Input Terminal Structure

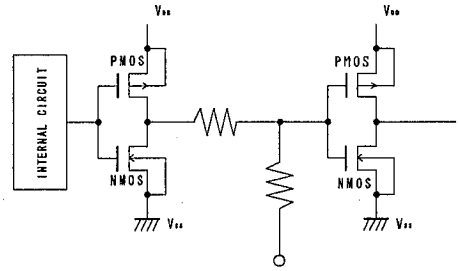
E/SCL, RS, R/W,
P/S, SEL Terminals



$\overline{RESET}$ Terminal

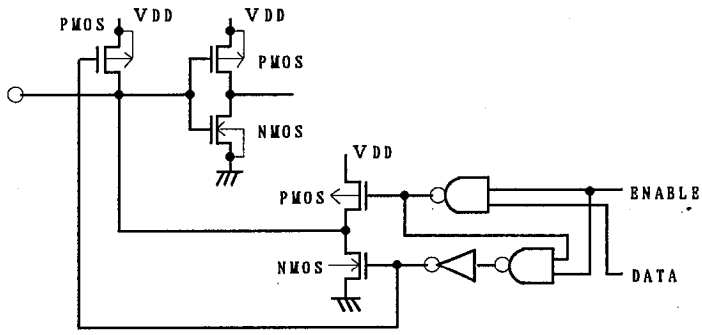


OSC1 Terminal



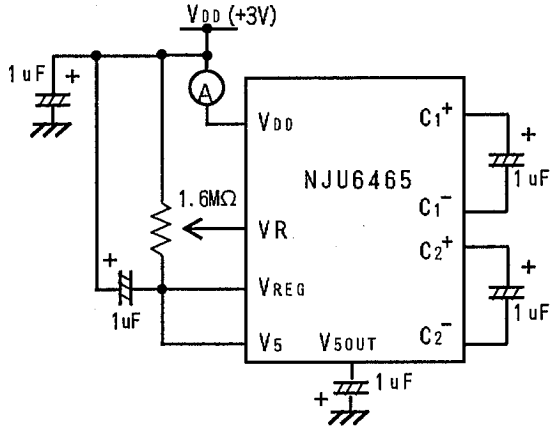
·Input/Output Terminal Structure

DB_0 to DB_7 Terminals



Note 6) Apply to the Output and Input/Output Terminals.
Note 7) Except pull-up resistance current and output driver current.
Note 8) Except Input/output current but including the current flow on bleeder resistance.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

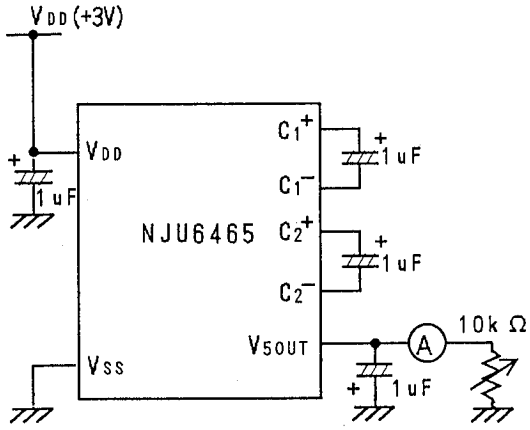
Operating Current Measurement Circuit



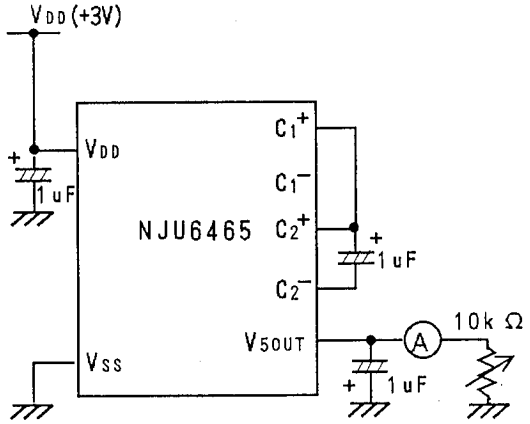
Note 9) R_{COM} and R_{SEG} are the resistance values between power supply terminals (V_{DD}, V_{5OUT}) and each common terminal (COM_1 to COM_{32}, $COMMK_1$ to $COMMK_4$) and suplly voltage (V_{DD}, V_{5OUT}) and each segment terminal (SEG_1 to SEG_{60}, $SEGM_1$ and $SEGM_2$) respectively, and measured when the current I_d is flown on every common and segment terminals at a same time.

Note 10) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_{5OUT}) at no load condition.

Voltage Tripler Measurement Circuit



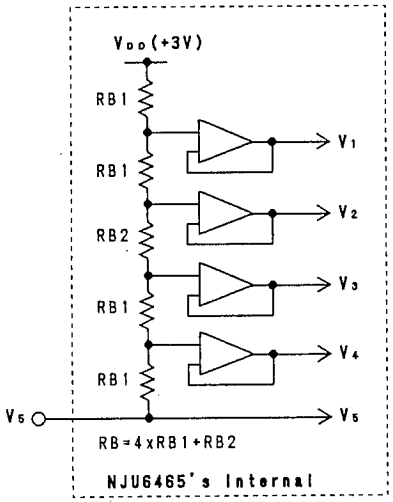
Voltage Doubler Measurement Circuit



5

Voltage Tripler/Doubler
Operation Clock Frequency = 10kHz

Bleeder Resistance and Buffer Amplifire



· **Bus timing characteristics** (V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ~ +75°C)

Write operation (Write from MPU to NJU6465)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1		fig. 1	us
Enable pulse width	"1" level	PW_{EH}	400			ns
Enable rise time, fall time		t_{Er}, t_{Ef}		20		
Set up time	RS, R/W, E	t_{AS}	200			
Address hold time		t_{AH}	200			
Data set up time		t_{DSW}	200			
Data hold Time		t_H	200			

Timing Characteristics (Write operation)

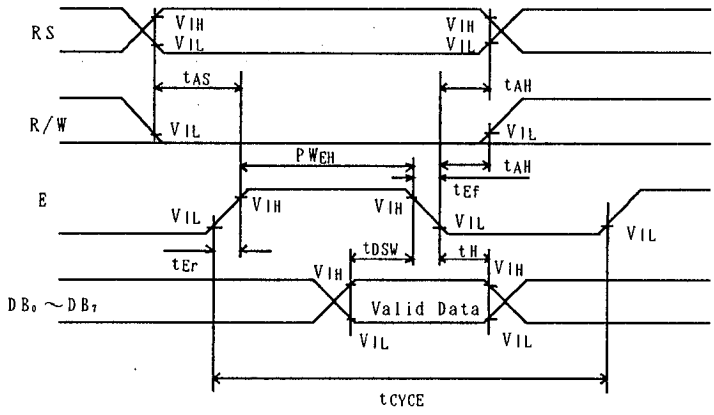


fig. 1

Read operation (Read from NJU6465 to MPU)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1		fig. 2	us
Enable pulse width	"1" level	PW_{EH}	750			ns
Enable rise time, fall time		t_{Er}, t_{Ef}		20		
Set up time	RS, R/W, E	t_{AS}	200			
Address hold time		t_{AH}	200			
Data delay time		t_{DDR}		750		
Data hold time		t_{DHR}	200			

Load Condition of DB0 to DB7 : CL=100pF

Timing Characteristics (Read operation)

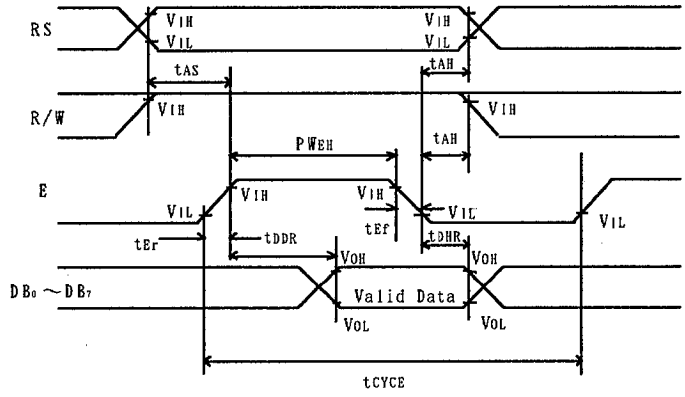


fig. 2

・Serial Interface Sequence

(V_{DD} = 3.0V±20%, V_{SS} = 0V, Ta = -20 ~ +75°C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial clock cycle time		t_{CYCE}	1		fig.3	us
Serial clock width	"1" level	t_{SCH}	300			ns
	"0" level	t_{SCL}	700			ns
Serial clock rise and fall Time		t_{SCr}, t_{SCf}		20		ns
Chip select pulse width		PW_{CS}	500			ns
Chip select set up time		t_{CSU}	200			ns
Chip select hold time		t_{CH}	200			ns
Chip Select rise and fall Time		t_{CSr}, t_{CSf}		20		ns
Set up time	RS, R/W - CS	t_{AS}	200			ns
Address hold time	CS - RS, R/W	t_{AH}	200			ns
Serial input data set up time		t_{SISU}	200			ns
Serial input data hold time		t_{SIH}	200			ns
Serial output data delay time		t_{SOD}		700		ns
Serial output data hold time		t_{SOH}	200			ns

Serial Interface

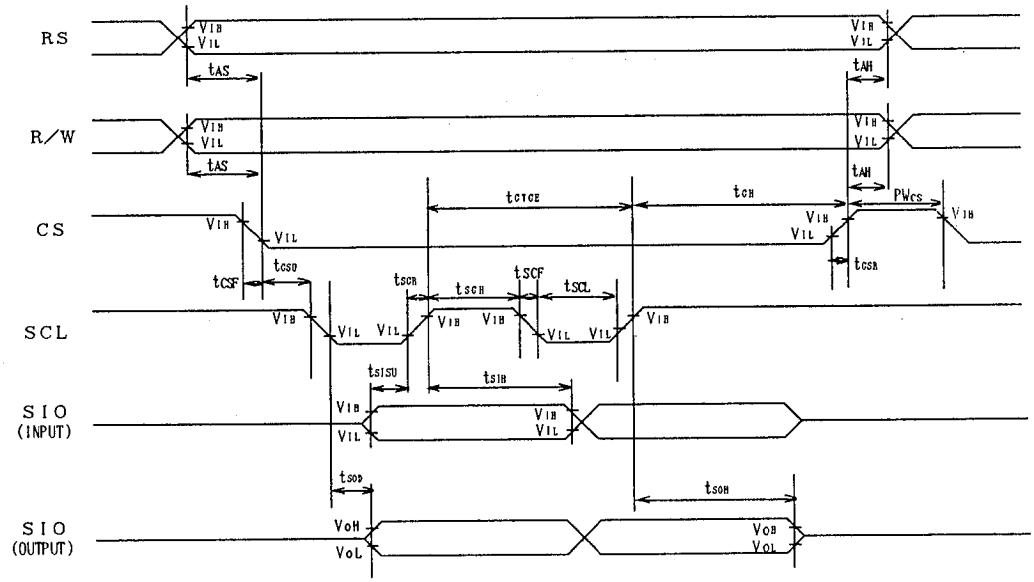
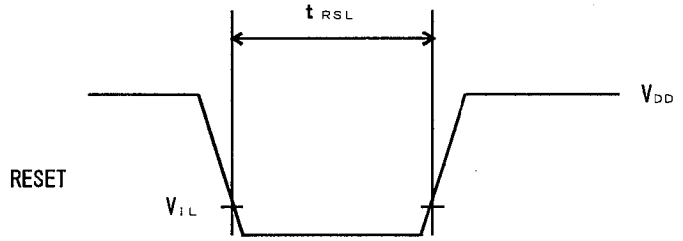


fig. 3

・The Input Condition when using the Hardware Reset Circuit

Input timing

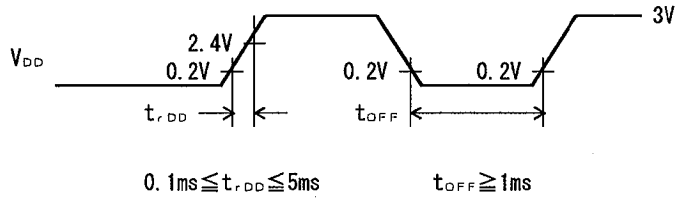


PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset input "0" level width	t_{RSL}	f_{OSC}=212kHz	1.2	-	ms

・Power Supply Condition when using the internal initialization circuit(Ta = -20 ~ +75℃)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power supply rise time	t_{rDD}		0.1	5	ms
Power supply OFF time	t_{OFF}		1		

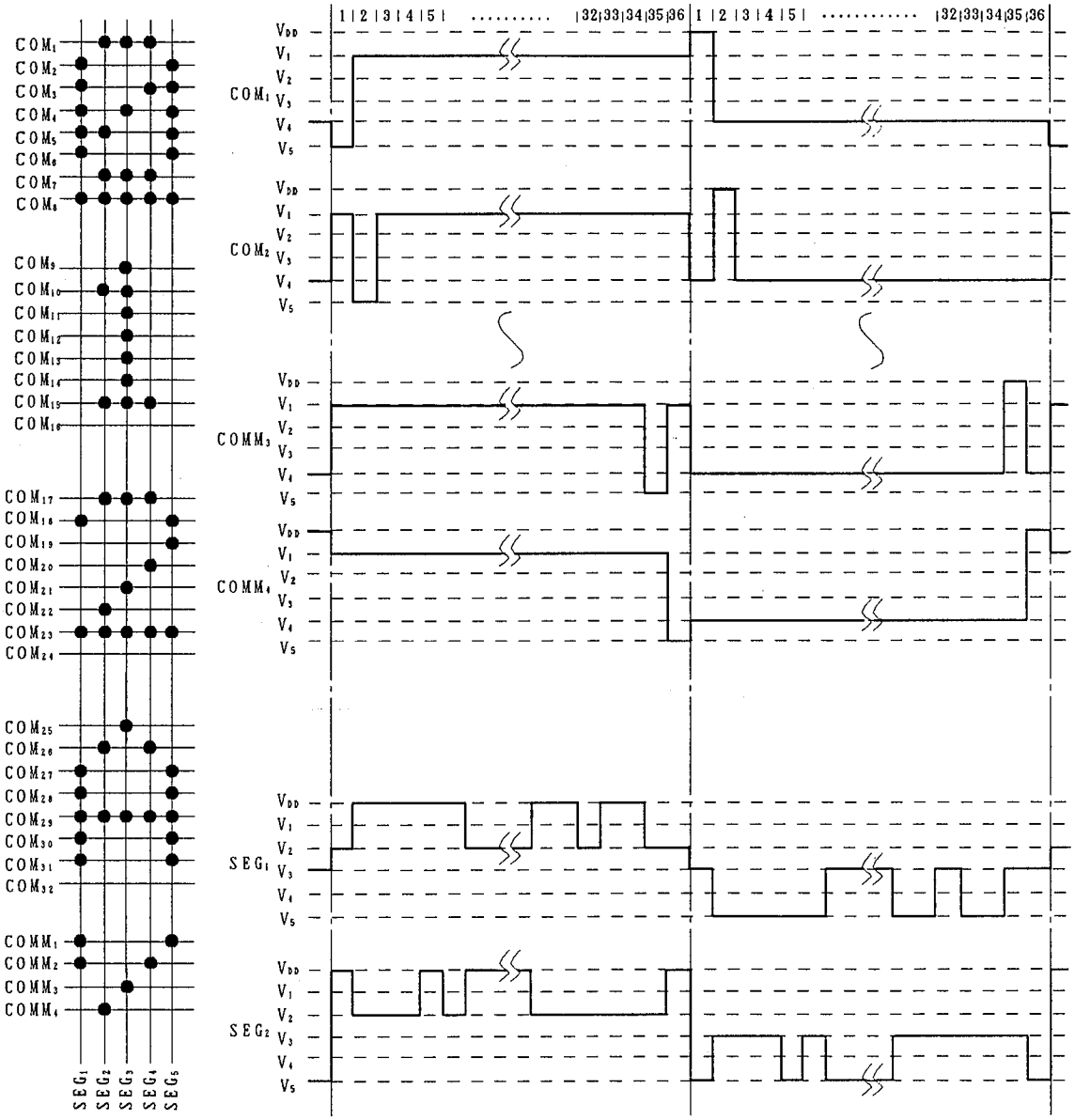
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)



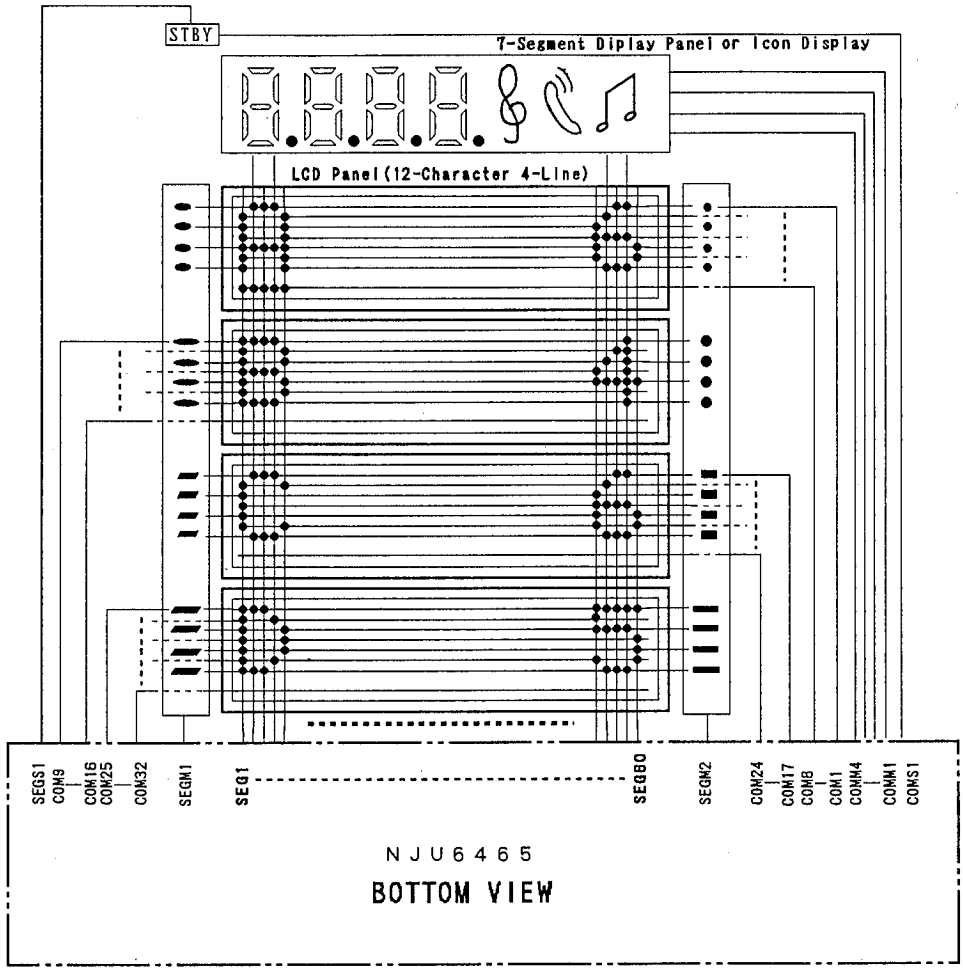
t_{OFF} specifies the power off time in a short period off or cyclical on/off.

■ LCD DRIVING WAVE FORM

1/36 Duty Driving

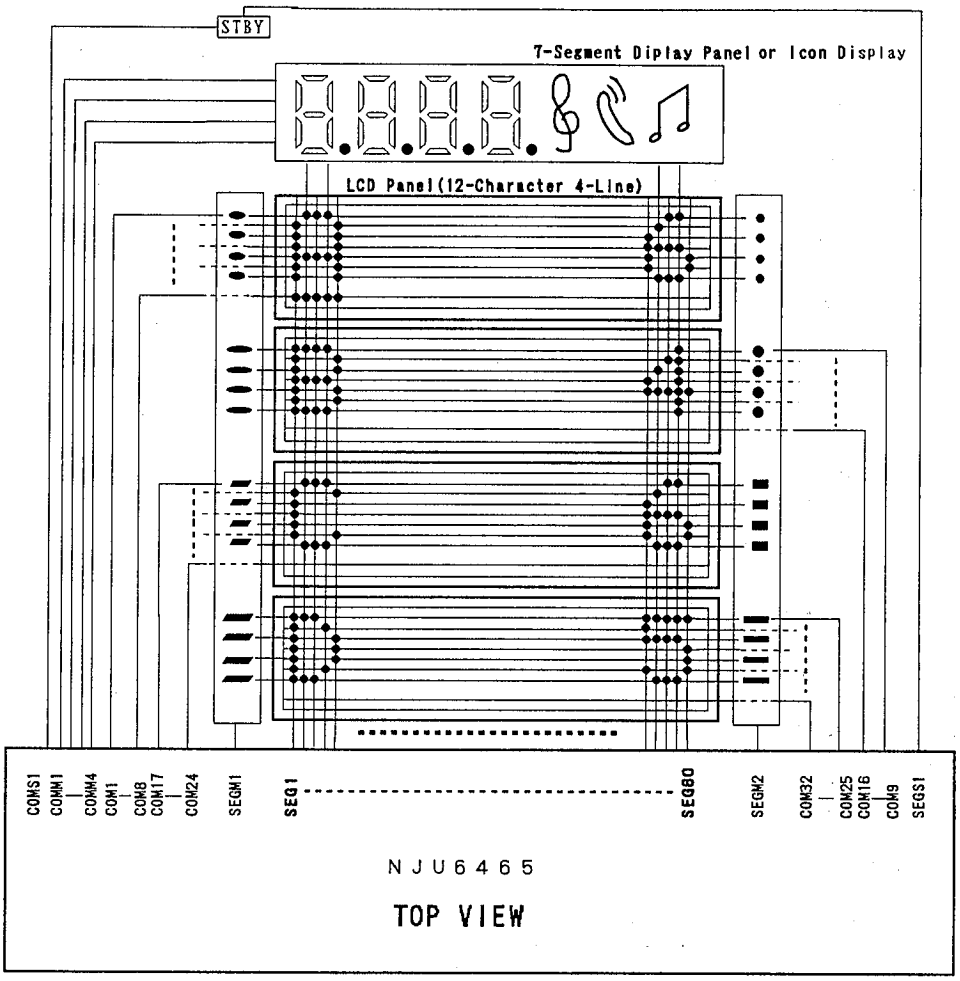


■ APPLICATION CIRCUITS (1)



12-character 4-line Display Example
(The terminal description is "Mode A".)

■ APPLICATION CIRCUITS (2)



12-character 4-line Display Example
(The terminal description is "Mode B".)

MEMO