PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6578 is a bit map LCD driver to display graphics or characters.

It contains 3,366 bits display data RAM, microprocessor interface circuits, instruction decoder, 102-segment and 33-common (1 out of 33-driver is prepared for icon display) drivers.

The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.

33 x 102 dots graphics or 6-character 2-line by 16 x 16 dot character with icon are displayed by NJU6578 itself.

The wide operating voltage from 2.4V to 5.5V and low operating current are useful for small size battery operating items.

The build-in Electrical Variable Resistance is very precision, furthermore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE

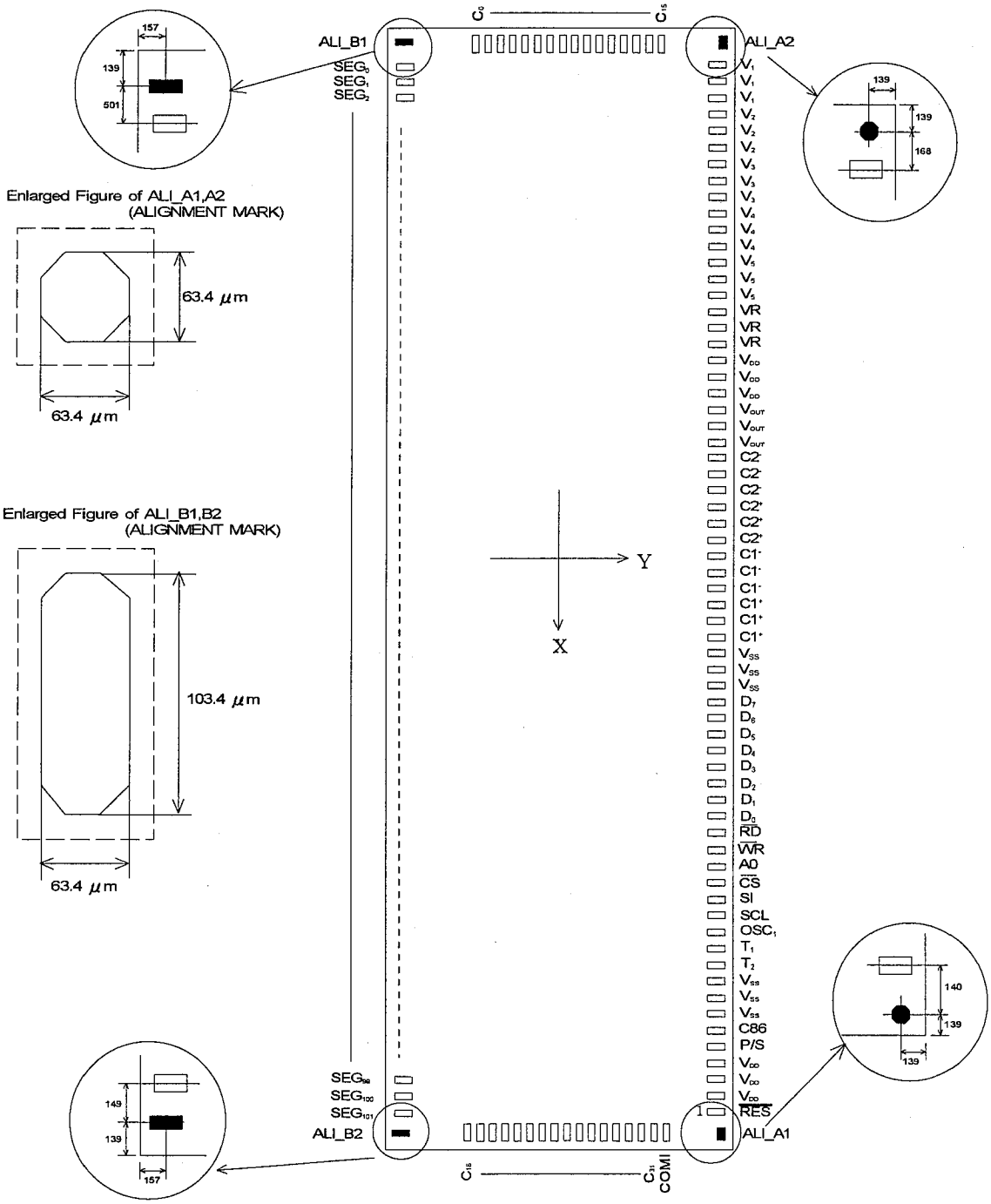
NJU6578CH

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 3,366 bits
- 135 LCD Drivers - 33-common and 102-segment
- Direct Microprocessor for Interface both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 5.5V
- LCD Driving Voltage --- 6.0V to 10V
- Package Outline --- TCP / Bumped Chip
- C-MOS Technology

Feb. 1999
Ver. 1

■ PAD LOCATION



Chip Center	X=0 μ m, Y=0 μ m
Chip Size	X=8.00mm, Y=2.06mm
Chip Thickness	400 μ m ± 30 μ m
Pad Pitch	70 μ m
Bump Size	53 μ m x 83 μ m
Bump Height	25 μ m TYP.
Bump Material	Au

■ : Four PADs illustrated with this mark are the alignment marks for COG.

■ PAD COORDINATES

Chip Size 8.00mm x 2.06mm(Chip Center X=0 μm,Y=0 μm)

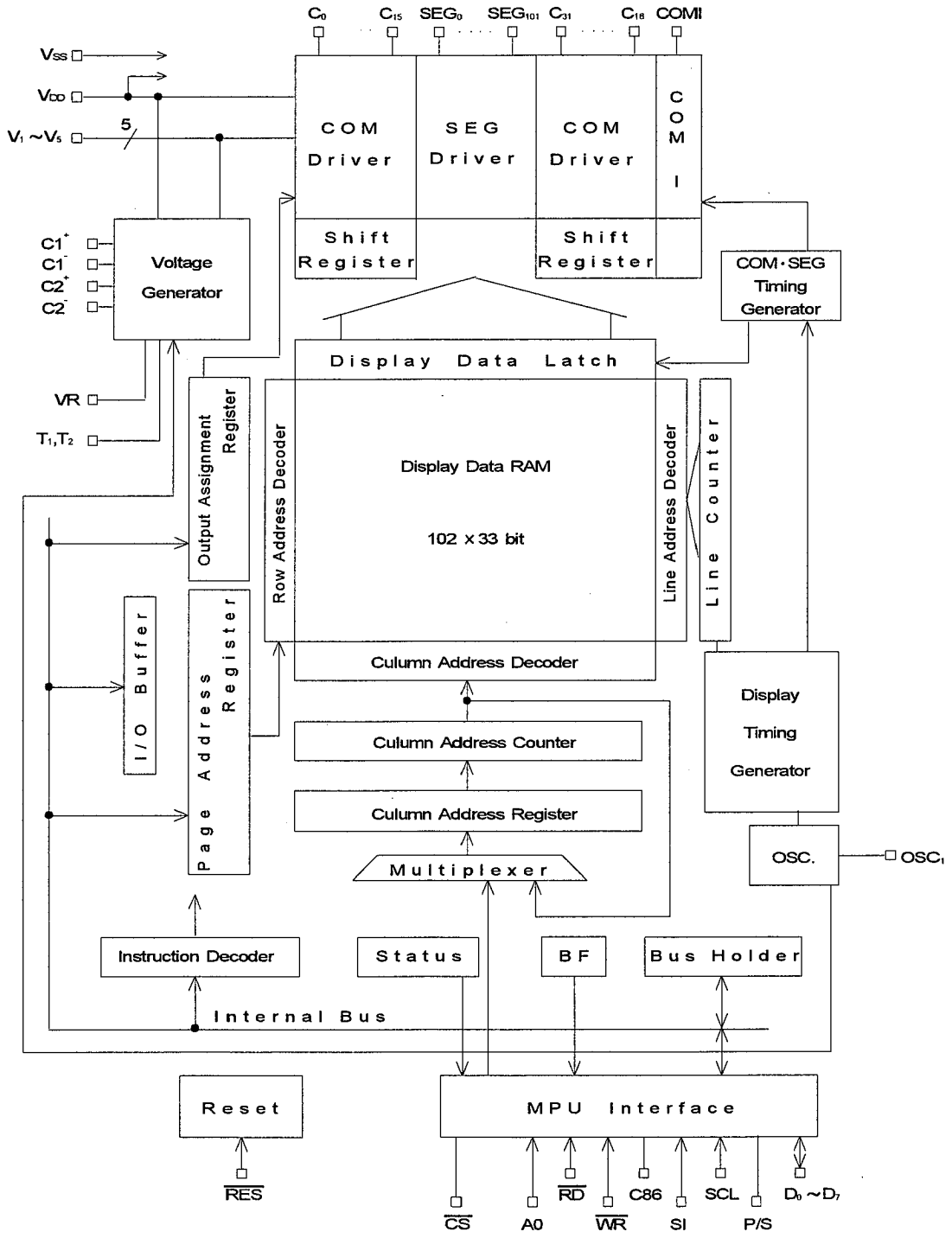
PAD No.	Terminal	X= μm	Y= μm
1	$\overline{RES}$	3721	891
2	V_{DD}	3651	891
3	V_{DD}	3581	891
4	V_{DD}	3511	891
5	P/S	3431	891
6	C86	3361	891
7	V_{SS}	3281	891
8	V_{SS}	3211	891
9	V_{SS}	3141	891
10	T_2	3061	891
11	T_1	2991	891
12	OSC_1	2921	891
13	SCL	2850	891
14	SI	2780	891
15	$\overline{CS}$	2710	891
16	A0	2640	891
17	$\overline{WR}$	2570	891
18	$\overline{RD}$	2500	891
19	D_0	2247	891
20	D_1	1865	891
21	D_2	1483	891
22	D_3	1101	891
23	D_4	719	891
24	D_5	338	891
25	D_6	-45	891
26	D_7	-426	891
27	V_{SS}	-745	891
28	V_{SS}	-815	891
29	V_{SS}	-885	891
30	$C1^+$	-991	891
31	$C1^+$	-1061	891
32	$C1^+$	-1131	891
33	$C1^-$	-1237	891
34	$C1^-$	-1307	891
35	$C1^-$	-1377	891
36	$C2^+$	-1447	891
37	$C2^+$	-1517	891
38	$C2^+$	-1587	891
39	$C2^-$	-1710	891
40	$C2^-$	-1780	891
41	$C2^-$	-1850	891
42	V_{OUT}	-1972	891
43	V_{OUT}	-2042	891
44	V_{OUT}	-2112	891
45	V_{DD}	-2235	891
46	V_{DD}	-2305	891
47	V_{DD}	-2375	891
48	VR	-2455	891
49	VR	-2525	891
50	VR	-2595	891

PAD No.	Terminal	X= μm	Y= μm
51	V_5	-2675	891
52	V_5	-2745	891
53	V_5	-2815	891
54	V_4	-2894	891
55	V_4	-2964	891
56	V_4	-3034	891
57	V_3	-3114	891
58	V_3	-3184	891
59	V_3	-3254	891
60	V_2	-3333	891
61	V_2	-3403	891
62	V_2	-3473	891
63	V_1	-3553	891
64	V_1	-3623	891
65	V_1	-3693	891
66	C_{15}	-3861	573
67	C_{14}	-3861	503
68	C_{13}	-3861	433
69	C_{12}	-3861	363
70	C_{11}	-3861	293
71	C_{10}	-3861	223
72	C_9	-3861	153
73	C_8	-3861	83
74	C_7	-3861	13
75	C_6	-3861	-57
76	C_5	-3861	-127
77	C_4	-3861	-197
78	C_3	-3861	-267
79	C_2	-3861	-337
80	C_1	-3861	-407
81	C_0	-3861	-477
82	SEG_0	-3360	-891
83	SEG_1	-3290	-891
84	SEG_2	-3220	-891
85	SEG_3	-3150	-891
86	SEG_4	-3080	-891
87	SEG_5	-3010	-891
88	SEG_6	-2940	-891
89	SEG_7	-2870	-891
90	SEG_8	-2800	-891
91	SEG_9	-2730	-891
92	SEG_{10}	-2660	-891
93	SEG_{11}	-2590	-891
94	SEG_{12}	-2520	-891
95	SEG_{13}	-2450	-891
96	SEG_{14}	-2380	-891
97	SEG_{15}	-2310	-891
98	SEG_{16}	-2240	-891
99	SEG_{17}	-2170	-891
100	SEG_{18}	-2100	-891

PAD No.	Terminal	X= μm	Y= μm
101	SEG19	-2030	-891
102	SEG20	-1960	-891
103	SEG21	-1890	-891
104	SEG22	-1820	-891
105	SEG23	-1750	-891
106	SEG24	-1679	-891
107	SEG25	-1609	-891
108	SEG26	-1539	-891
109	SEG27	-1469	-891
110	SEG28	-1399	-891
111	SEG29	-1329	-891
112	SEG30	-1259	-891
113	SEG31	-1189	-891
114	SEG32	-1119	-891
115	SEG33	-1049	-891
116	SEG34	-979	-891
117	SEG35	-909	-891
118	SEG36	-839	-891
119	SEG37	-769	-891
120	SEG38	-699	-891
121	SEG39	-629	-891
122	SEG40	-559	-891
123	SEG41	-489	-891
124	SEG42	-419	-891
125	SEG43	-349	-891
126	SEG44	-279	-891
127	SEG45	-209	-891
128	SEG46	-139	-891
129	SEG47	-69	-891
130	SEG48	1	-891
131	SEG49	71	-891
132	SEG50	141	-891
133	SEG51	211	-891
134	SEG52	281	-891
135	SEG53	351	-891
136	SEG54	421	-891
137	SEG55	491	-891
138	SEG56	561	-891
139	SEG57	631	-891
140	SEG58	701	-891
141	SEG59	771	-891
142	SEG60	841	-891
143	SEG61	911	-891
144	SEG62	981	-891
145	SEG63	1051	-891
146	SEG64	1121	-891
147	SEG65	1191	-891
148	SEG66	1261	-891
149	SEG67	1331	-891
150	SEG68	1401	-891
151	SEG69	1471	-891
152	SEG70	1541	-891

PAD No.	Terminal	X= μm	Y= μm
153	SEG71	1611	-891
154	SEG72	1681	-891
155	SEG73	1751	-891
156	SEG74	1822	-891
157	SEG75	1892	-891
158	SEG76	1962	-891
159	SEG77	2032	-891
160	SEG78	2102	-891
161	SEG79	2172	-891
162	SEG80	2242	-891
163	SEG81	2312	-891
164	SEG82	2382	-891
165	SEG83	2452	-891
166	SEG84	2522	-891
167	SEG85	2592	-891
168	SEG86	2662	-891
169	SEG87	2732	-891
170	SEG88	2802	-891
171	SEG89	2872	-891
172	SEG90	2942	-891
173	SEG91	3012	-891
174	SEG92	3082	-891
175	SEG93	3152	-891
176	SEG94	3222	-891
177	SEG95	3292	-891
178	SEG96	3362	-891
179	SEG97	3432	-891
180	SEG98	3502	-891
181	SEG99	3572	-891
182	SEG100	3642	-891
183	SEG101	3712	-891
184	C16	3861	-342
185	C17	3861	-272
186	C18	3861	-202
187	C19	3861	-132
188	C20	3861	-62
189	C21	3861	8
190	C22	3861	78
191	C23	3861	148
192	C24	3861	218
193	C25	3861	288
194	C26	3861	358
195	C27	3861	428
196	C28	3861	498
197	C29	3861	568
198	C30	3861	638
199	C31	3861	708
200	COMI	3861	778
ALIGNMENT	ALI_A1	3861	891
ALIGNMENT	ALI_A2	-3861	891
ALIGNMENT	ALI_B1	-3861	-873
ALIGNMENT	ALI_B2	3861	-873

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>2,3,4,
45,46,47</td><td>V_{DD}</td><td>Power</td><td>V_{DD}=+3V
V_{DD}=+5V. (Less than 3.3V should apply when voltage tripler using.)</td></tr>
<tr><td>7,8,9,
27,28,29</td><td>Vss</td><td>GND</td><td>Vss=0V</td></tr>
<tr><td>63,64,65
60,61,62
57,58,59
54,55,56
51,52,53</td><td>V1
V2
V3
V4
V5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminal. When the internal voltage tripler is not used, supply each level of LCD driving voltage from outside with following relation.
$V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$
When the internal power supply is on, the internal circuits generate supply following LCDbias voltage from V1 to V4 terminals.
<table><tr><td>Terminal</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr><tr><td>Voltage</td><td>V5+6/7VLCD</td><td>V5+5/7VLCD</td><td>V5+2/7VLCD</td><td>V5+1/7VLCD</td></tr></table>(VLCD=VDD-V5)</td></tr>
<tr><td>30,31,32
33,34,35
36,37,38
39,40,41</td><td>C1+
C1-
C2+
C2-</td><td>O</td><td>Step up capacitor connecting terminals.
In case of tripler operation, connect the capacitor between C1+ and C1-, C2+ and C2-.
In case of doubler operation, connect the capacitor between C2+ and C2-, connect C2+ to C1+, and C1- should be open.</td></tr>
<tr><td>42,43,44</td><td>VOUT</td><td>O</td><td>Step up voltage output terminal. Connect the set up capacitor between this terminal and Vss.</td></tr>
<tr><td>48,49,50</td><td>VR</td><td>I</td><td>Voltage adjust terminal. V5 level is adjusted by external bleeder resistance connect between VDD and V5 terminal.</td></tr>
<tr><td>11
10</td><td>T1
T2</td><td>I</td><td>LCD bias voltage control terminals. (※Don't Care)
<table><tr><td>T1</td><td>T2</td><td>Step up Cir.</td><td>Voltage Adj.</td><td>V/F Cir.</td></tr><tr><td>L</td><td>※</td><td>Available</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr></table></td></tr>
<tr><td>19 to 26</td><td>D0 to D7</td><td>I/O</td><td>Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.</td></tr>
<tr><td>16</td><td>A0</td><td>I</td><td>Connect to the Address bus of MPU. The data on the D0 to D7 is distinguished between Display data and Instruction by status of A0.
<table><tr><td>A0</td><td>H</td><td>L</td></tr><tr><td>Distin</td><td>Display Data</td><td>Instruction</td></tr></table></td></tr>
<tr><td>1</td><td>RES</td><td>I</td><td>Reset terminal. When the RES terminal goes to "L", the initialization is performed.
Reset operation is executing during "L" state of RES.</td></tr>
<tr><td>15</td><td>CS</td><td>I</td><td>Chip select terminal. Data Input/Output are available during CS ="L".</td></tr>
<tr><td>18</td><td>RD
(E)</td><td>I</td><td><In case of 80 Type MPU>
RD signal of 80 type MPU input terminal. Active "L".
During this signal is "L", D0 to D7 terminals are output.
<In case of 68 Type MPU>
Enable signal of 68 type MPU input terminal. Active "H".</td></tr>
<tr><td>17</td><td>$\overline{WR}$
(R/W)</td><td>I</td><td><In case of 80 Type MPU>
Connect to the 80 type MPU $\overline{WR}$ signal. Active "L".
The data on the data bus input synchronizing the rise edge of this signal.
<In case of 68 Type MPU>
Read/write control signal of 68 type MPU input terminal.
<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table></td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>6</td><td>C86</td><td>I</td><td>MPU interface type selection terminal.
<table>
<tr><td>C86</td><td>H</td><td>L</td></tr>
<tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>14</td><td>SI</td><td>I</td><td>Serial data input terminal.</td></tr>
<tr><td>13</td><td>SCL</td><td>I</td><td>Serial data clock signal input terminal.
SI data input at the rise edge of SCL in successively. It convert to SCL the parallel data at the 8th SCL clock rise edge.</td></tr>
<tr><td>5</td><td>P/S</td><td>I</td><td>Serial or parallel interface selection terminal.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr>
<tr><td>"H"</td><td>$\overline{CS}$</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
*RAM data and status read operation do not work in mode of the serial interface.
・In case of the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L".
・In case of the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D0 to D7 becomes to the high impedance state.</td></tr>
<tr><td>12</td><td>OSC1</td><td>I</td><td>System clock input terminal for Maker testing.
(This terminal should be open.)</td></tr>
<tr><td>66～81
82～183
184～199</td><td>C15～C0
SEG0
～
SEG101
C31
～
C16</td><td>O</td><td>LCD driving signal output terminals.
Segment output terminals : SEG0 to SEG101
Common output terminals : C0 to C31
・Segment output terminal
The following output voltages are selected by the combination of FR and data in the RAM.
<table>
<tr><td rowspan="2">RAM Data</td><td rowspan="2">FR</td><td colspan="2">Output Voltage</td></tr>
<tr><td>Normal</td><td>Reverse</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
</table>
・Common Output Terminal
The following output voltages are selected by the combination of FR and status of common.
<table>
<tr><td>Scan Data</td><td>FR</td><td>Output Voltage</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>200</td><td>COMI</td><td>O</td><td>Icon common output terminal.
Icon common output when Icon Display instruction execution.
<table>
<tr><td></td><td>Icon Display ON</td><td>Icon Display OFF</td></tr>
<tr><td>State</td><td>COM32</td><td>V1 or V4</td></tr>
</table></td></tr>
</table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

While the internal circuits are operating, the busy flag (BF) is "1", and any instruction excepting for the status read are inhibited .

The busy flag goes to "1" from D_7 terminal when status read instruction is executed.

When enough cycle time over than t_{CYC} indicated in "BUS TIMING CHARACTERISTICS" is ensured, no need to check the busy flag for reduction of the MPU loads.

(1-2) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-3) Column Address Counter

The column address counter is 8-bit pre-settable counter addressing the column address of display data RAM as shown in Fig. 1. It is incremented (+1) up to $(66)_H$ by the Display Data Read/Write instruction execution. It stops the count up operation at $(66)_H$, and it does not count up non existing address area over than $(66)_H$ by the count lock function. This count lock is released by new column address set.

The column address counter is independent of the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM corresponding to the Segment Driver.

(1-4) Page Register

The page register gives a page address of Display Data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required. Page address "4"(D_2="H" and D_1=D_0="L") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM is the bit map RAM consisting of 3,366 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"
When Inverse Display : On="0" , Off="1"

The Display Data RAM outputs 102-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malfunctions to the display.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

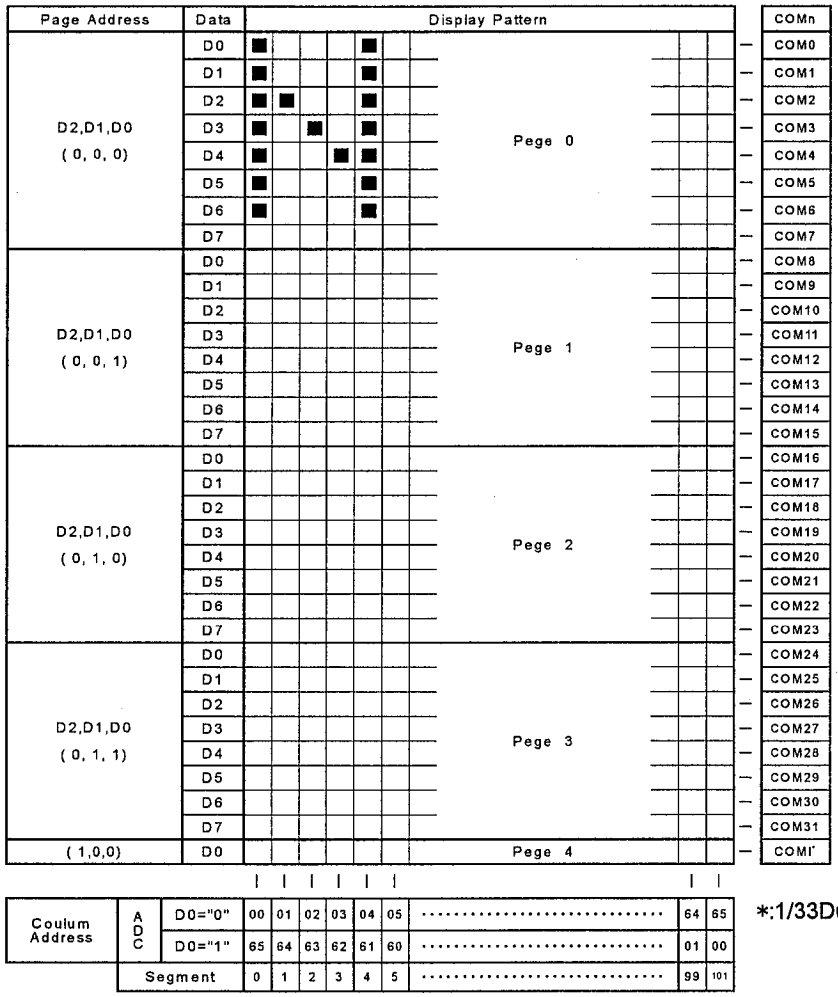


Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/33 duty set.)

(1-6) Common Driver Assignment
The scanning order can be assigned by setting A3 of the Output Assignment Register as shown Table 1.

Register		COM Outputs Terminals			
A3	PAD No.	66	81	184	199
	Pin name	C15	C0	C16	C31
0	→	COM15 ←	COM0	COM16 →	COM31
1	→	COM16 →	COM31	COM15 ←	COM0

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COMI is fixed to COM32 timing regardless the other Common Driver assignment.

(1-7) Reset Circuit
Reset circuit operates the following initializations when the condition of $\overline{RES}$ terminal goes to "L" level.

Initialization
① Display Off
② Normal Display (Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D0="0")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply (Step up) circuits Off .
⑦ Clear the serial interface register
⑧ Set the address (00)H to the Column Address Counter
⑨ Set the page "0" to the Page Address Register
⑩ Select the D3 of the Output Assignment Register to "0"
⑪ Set the EVR register to (00)H

The $\overline{RES}$ terminal should be connected to the Reset terminal of MPU for the initialization at the mean time with MPU as shown "MPU Interface Example". The period of reset signal requires over than 10 μs $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1 μs from the rise edge of RES signal, the operation goes to normal.When the internal LCD power supply is not used, the external LCD power supply into the NJU6578 must be turned on during $\overline{RES}$ = "L". Although the condition of $\overline{RES}$="L" clear each registers and initialize as above, the oscillation circuit and the output terminal conditions (D0 to D7) are not influenced. The initialization must be performed using $\overline{RES}$ terminal at the power on, to prevent hung up or any incorrect operations. The reset Instruction performs the initialization procedures from No.8 to No.11 as shown in above.

NOTE) The noise into the $\overline{RES}$ terminal should be eliminated to avoid error on the application with the careful design.

(1-8) LCD Driving

(a) LCD Driving Circuits

LCD driving circuits are consisted of 135 multiplexers which operate as 102 Segment drivers, 32 Common drivers and 1 Icon common driver. 33 Common drivers with the shift register scan the common display signal. The combination of the Display data, COM scan signal and FR signal forms the LCD driving output voltage. The output wave form is shown in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 102-bit display data temporarily which is output to LCD driver circuits at a common cycle from Display Data RAM addressed by Line Counter. The instructions of Display On/Off, Display inverse On/Off and Static drive On/Off control only the data in Display Data Latch, therefore, the data in the Display Data RAM is not changed.

(c) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock (CL). The line address of Display Data RAM is renewed synchronizing with display clock(CL). 102 bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

Display Timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of the two frame alternative driving method.

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

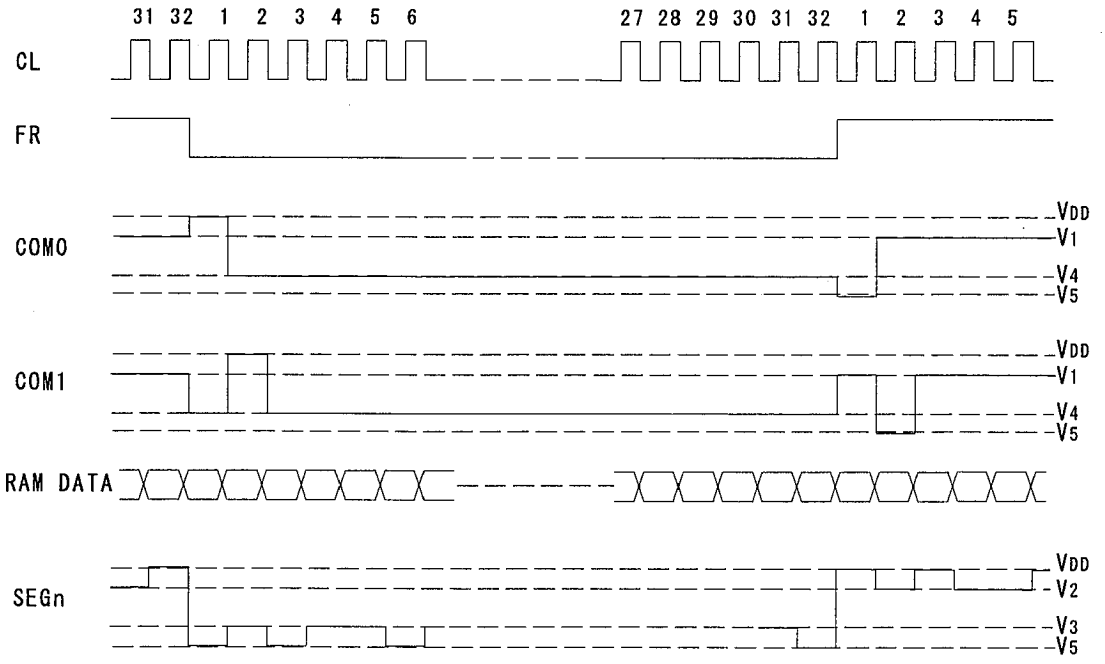


Fig.2 Waveform of Display Timing

(f) Oscillation Circuit

The Oscillation Circuit is a low power CR oscillator incorporating with a Resistor and a Capacitor. It generates clocks for display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuit output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuit

Internal Power Supply Circuit generate the High voltage and Bias voltage for the LCD. The power Supply Circuits consists of Step up (Tripler or Doubler) Circuits, Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application. If the contrast is not good in the large size LCD panel application, please supply the external.

The suitable values of the capacitors connecting to the V_1 to V_5 terminals and the step up circuit, and the feed-back resistors for V_5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluate with actuale LCD module.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

Table.3 (※ : Don't Care)

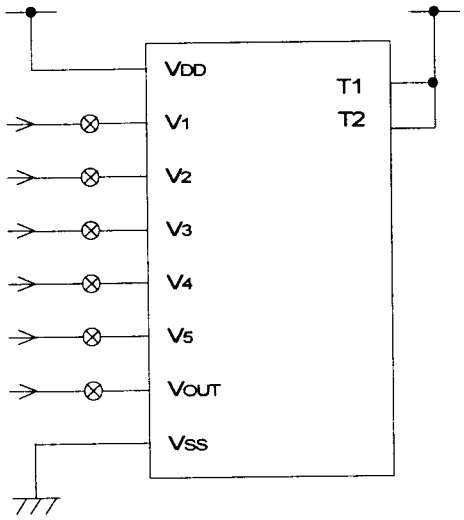
T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Power Supply	$C1^+$,$C1^-$,$C2^+$,$C2^-$	VR Term.
L	※	O	O	O	-		
H	L	X	O	O	V_{OUT}	OPEN	
H	H	X	X	O	V_5, V_{OUT}	OPEN	OPEN

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$ terminals for voltage booster circuits are open because the step up circuits doesn't operate. Therefore the LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

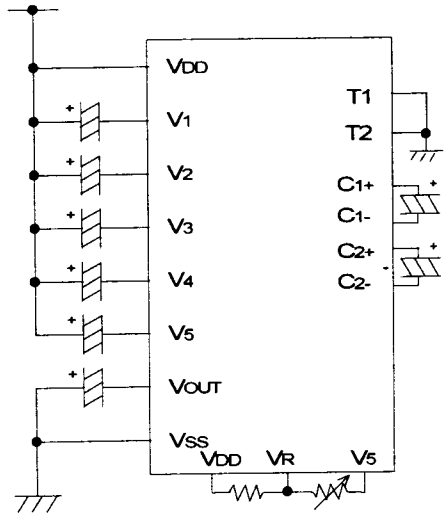
When (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, because the Step up circuits and Voltage adjust circuits do not operate.

○ Power Supply applications

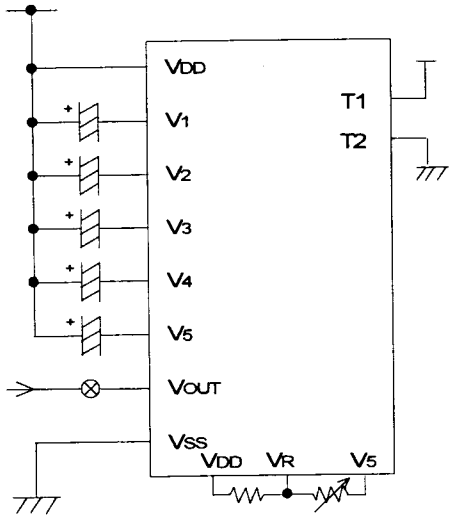
(1) External power supply operation.



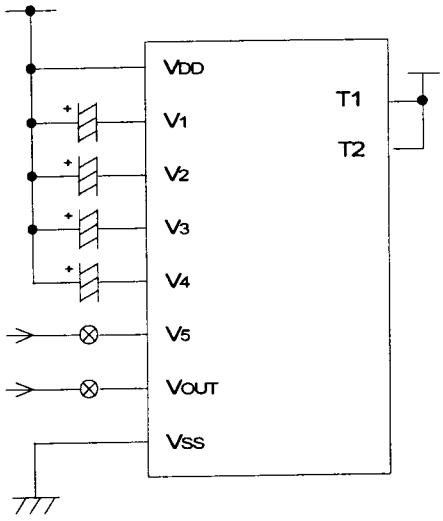
(2)Internal power supply operation.
(Voltage Booster, Voltage Adj., Buffer(V/F))
Internal power supply ON (instruction) (T1,T2)=(L,L)



(3)External power supply operation with
Voltage Adjustment, Buffer(V/F)
Internal power supply ON (Instruction) (T1,T2) = (H,L)



(4)External power supply operation adjusted
Voltage to V5.
Internal power supply ON (Instruction) (T1,T2) =(H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6578 distinguishes the signal on the data bus by combination of A0, $\overline{RD}$ and $\overline{WR}$.
The decode of the instruction and execution are performs only depend on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.
The Table. 4 shows the instruction codes of the NJU6578.

Table 4. Instruction Code

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Address Register
(3)	Column Address Set High Order 3bits	0	1	0	0	0	0	1	0	High Order Column Add.			Set the Higher order 3 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the ON and OFF Display 0:Normal 1:Inverse
(10)	Whole Display ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	Output Assignment Register Set	0	1	0	1	1	0	0	A3	*	*	*	Set the scanning order of common drivers to the Register
(16)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal (external) power supply is turned on
(18)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V_5 output level to the EVR register
(19)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power Save Mode

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off
1:Display On

(b) Page Address Set

When MPU accesses the Display Data RAM, the page address must be selected before the data writing. The access to the Display Data RAM is available by the page and column address set (Refer the Fig. 1.). The page address change does not influence with the display. Page 4 is a Icon display data area which available only for the Do.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	*	A2	A1	A0

(*:Don't care)

A2	A1	A0	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(c) Column Address

When MPU accesses the Display Data RAM, the page address set(refer(b)) and column address set are required before the data writing. The column address set requires twice address set which are higher order 3 bits address set and lower order 4 bits. When the MPU accesses the Display Data RAM sequentially, the column address is increase one by one automatically, therefore, the MPU can access only the data sequentially without address set.

After writing 1page data ,page address setting is required due to page address doesn't increase automatically. The increment of the column address is stopped at the address of (66)H automatically, and the page address is no changed even if the column address increase to (66)H and stop. In this time the page address is not changed.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	0	A6	A5	A4	Higher Order
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower Order

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	1	0	0	1	0	1	65

(d) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0 :Counterclockwise Output (Inverse) Column Address 101-n ⟷ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ⟷ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing by $\overline{RES}$ signal or reset instruction.
0 : -
1 : Initialization Period

(e) Write Display Data

This instruction writes the 8-bit data on the data bus into the Display Data RAM. The column address increases "1" automatically after data writing, therefore, the MPU can write the 8-bit data into the Display Data RAM continuously without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

(f) Read Display Data

This instruction reads out the 8-bit data from Display Data RAM addressed by the column and page address. The column address increase "1" automatically after data reading out, therefore, the MPU can read out the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read must operate after column address set as the explanation in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data is not read out.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D 0 : Clockwise Output (Normal)

1 : Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction changes the condition of display turn on and off as normal or inverse. The contents of Display Data RAM is not changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D 0 : Normal RAM data "1" correspond to "On"

1 : Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction turns on the all pixel independent of the contents of the Display Data RAM. In this time, the contents of Display Data RAM is not change and kept. This instruction takes precedence over the "Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D 0 : Normal Display

1 : Whole Display turn on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits go to the power save mode (refer to the (s) Power Save).

(j) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COMI terminal operate as COM32 and output the icon display data stored in Do of Display Data RAM page 4 (refer to the Fig. 1).

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

D 0 : 1/32 Duty

1 : 1/33 Duty

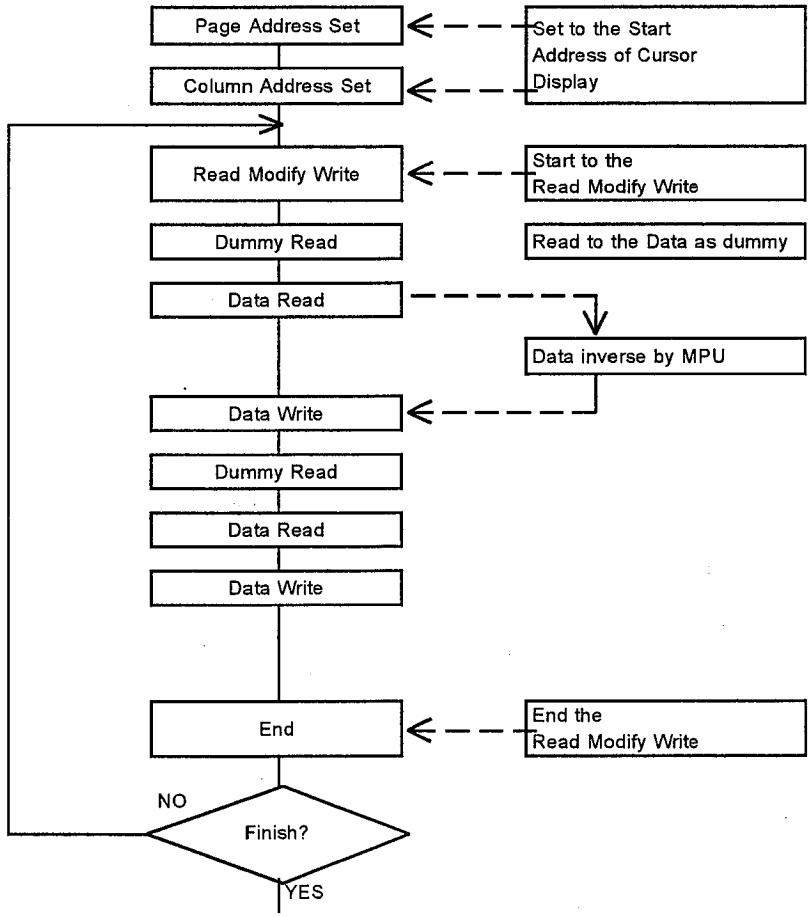
(k) Read Modify Write

This instruction sets the Read Modify Write Mode for the column address increment control. In mode of the Read Modify Mode Write, the column address increases "1" automatically when the Display Data Write Instruction is executed, but the address does not change when the Display Data Read Instruction is executed. This status is continued until End instruction execution. When the End instruction is input.,the column address goes back to the start address before the Read Modify Write instruction input. This function reduces the load of MPU for repeating the display data change in the fixed area (ex. cursor blink).

A0	$\overline{RD}$	R/W $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note) In mode of the Read Modify Write, any instructions except for Column Address Set can execute.

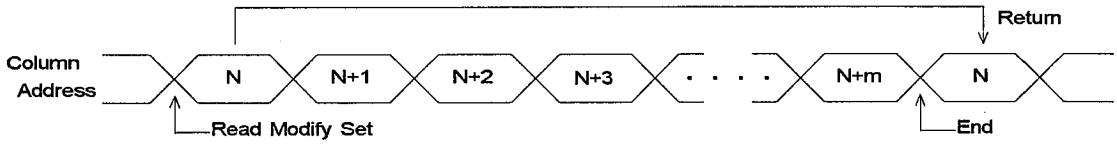
(l) Sequence of cursor blink display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

① Set the Address (00)H into the Column Address Counter.

② Set the page "0" into the Page Address Register.

③ Select the D3 of the Output Assignment Register to "0".

④ Set 0 to the EVR Register to (00)H.

In this time, the Display Data RAM is not influenced.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal (hardware reset) must be input for the power on initialization. Reset Instruction does not perform completely in stead of hardware reset using the $\overline{RES}$ terminal.

(o) Output Assignment Register

This instruction sets the common driver scanning order.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	*	*	*

(*:Don't care)

A3 : Set the scanning order. (Refer to 1-6)

(p) Internal Power Supply

This instruction set the condition of the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Follower are operate at On. To operate the step up circuits, the oscillation circuits must be operating.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	D

D 0 : Internal Power Supply Off

1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q) LCD Driving Voltage Set

This instruction controls LCD driving waveform output through the COM/SEG terminals.

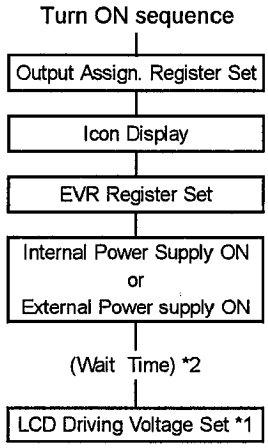
A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

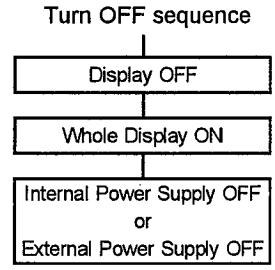
The NJU6578 contains low power LCD driving voltage generator circuit reducing own operation current. Therefore, it requires the following sequence procedures at power on for power source stabilized operation.

● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is turned On/Off.

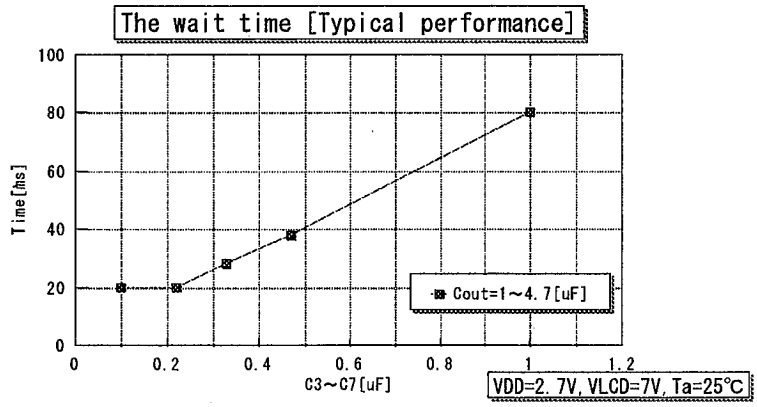
When the power supply is turned on again after the turn off (by the power save instruction), the power save release sequence ((s)Power Save) is required.





*1 This instruction is required in both cases of the internal and external power supply.
Until "LCD driving voltage Set" execution, NJU6578 operating current is higher than usual state and all COM/SEG terminals output VDD level continuously.

*2 The wait time depends on the C3 to C7, COUT capacitors (refer (4) (d)Fig.4), VDD and VLCD voltage.
Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the following graph.)



(r) EVR Register Set

This instruction controls voltage adjustment circuits of internal LCD power supply and changes LCD driving voltage "V5". Finally, it adjusts the contrast of LCD display. By setting a data into EVR register. V_5 output voltage selects one condition out of 16-voltage conditions. The range of V_5 voltage is adjusted by setting external resistors as mentioned in "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	VLCD
0	0	0	0	Low
		:		:
		:		:
1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$
When EVR doesn't use, set the EVR register to (0,0,0,0).

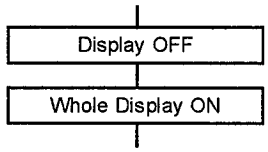
(s) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits go to the power save mode and the operating current is reduced as same as the stand by current.
The internal status in the Power Save Mode is shown in follows;

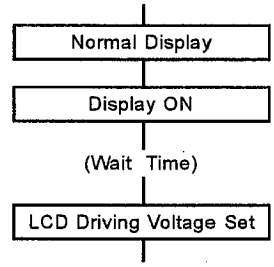
① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Keep the display data and operating mode just before the power save mode.
④ All of LCD driving bias voltage fix to the V_{DD} level.

The power save and its release perform according to the following sequences.

Power Save Sequence



Power Save Release Sequence



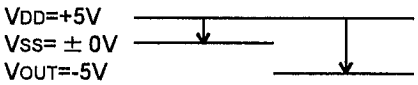
(Whole Display OFF)

*1 In the power save sequence, the power save mode is started after the second instruction "whole Display ON".
*2 In the power save release sequence, the power save mode is released after the Normal Display instruction (Whole display OFF).
The instruction of display ON is input at any timing after the instruction of normal display in power save release sequence.
*3 Until "LCD driving voltage set to ON" execution, NJU6578 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.
*4 In case of the external power supply for LCD driving, it should be turned off and made condition like as disconnection or connection to V_{DD} before the power save mode or at the same time. In this time, V_{OUT} terminal should be made condition like as disconnection or connection to the lowest voltage of the system. (V_5 level from the external power supply.)

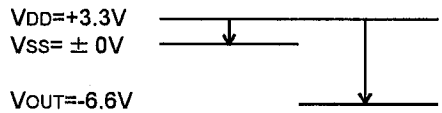
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage (V_{DD} common) of the voltage V_{DD}-V_{SS} is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between $C2^+$ and $C2^-$, V_{SS} and V_{OUT}, then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage of V_{DD} should be less than 3.3V.



Voltage relation in Doubler



Voltage relation in Tripler

(b)Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits for LCD driving. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage is calculated by the following formula.

$$V_{LCD} = V_{DD}-V_5 = (1+Rb/Ra)\cdot V_{REG} \cdots\cdots ①$$

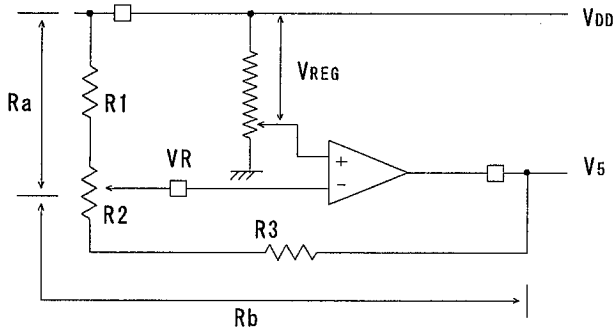


Fig.3

The voltage of V_{REG} is a standard voltage produced from built-in bleeder resistance. And V_{REG} is possible to be fine-adjusted by EVR functions mentioned in (c).

For fine-adjustment of V_5, R_2 as variable resistor, R_1 and R_3 as fixed constant should be connected to V_{DD} terminal, VR and V_5, as shown in Fig3.

[Design example for R1, R2 and R3 / Reference]

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD}-V_5)
- Variable voltage range by the R2. -3V ~ -4.5V ($V_{LCD}=V_{DD}-V_5$ → 6.0V ~ 7.5V)
  (Determined by the LCD electrical characteristics)
- VREG=3V(In case of EVR=(0F)H)
- R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below:
  R1=2.0M Ω , R2=0.5M Ω , R3=2.5M Ω

* If the power supply voltage between V_{DD} and V_{SS} changes, V_5 changes too. Therefore the power supply voltage should be stabilized for V_5 stable operation.

(c) Contrast Adjustment by using the EVR function

The EVR controls voltage of V_{REG} by instruction and changes voltage of V_5.

As result, LCD display contrast is adjusted by V_5. The EVR selects a voltage of V_{REG} in the following 16 conditions by setting 4bits data in to the EVR register.

In case of EVR operation, T_1 terminal and T_2 require to set couples of value as (L,L), (L,H) and (H,L) excepting for (H,H) and the internal power supply must turn on by instruction.

EVR register		V_{REG} [V]	V_{LCD}
$(00)_H$	(0,0,0,0)	(135/150)·(V_{DD}-V_{SS})	Low
$(01)_H$	(0,0,0,1)	(136/150)·(V_{DD}-V_{SS})	:
$(02)_H$	(0,0,1,0)	(137/150)·(V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
$(0D)_H$	(1,1,0,1)	(148/150)·(V_{DD}-V_{SS})	:
$(0E)_H$	(1,1,1,0)	(149/150)·(V_{DD}-V_{SS})	:
$(0F)_H$	(1,1,1,1)	(150/150)·(V_{DD}-V_{SS})	High

● Adjustable range of the LCD driving voltage by EVR function using

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD}=3.0V, V_{SS}=0V

Ra=1M Ω , Rb=1M Ω (Ra:Rb=1:1)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting $(00)_H$ in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)·V_{REG}

= (2/1)·[(135/150)·3.0]

= 5.4V

In case of setting $(0F)_H$ in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)·V_{REG}

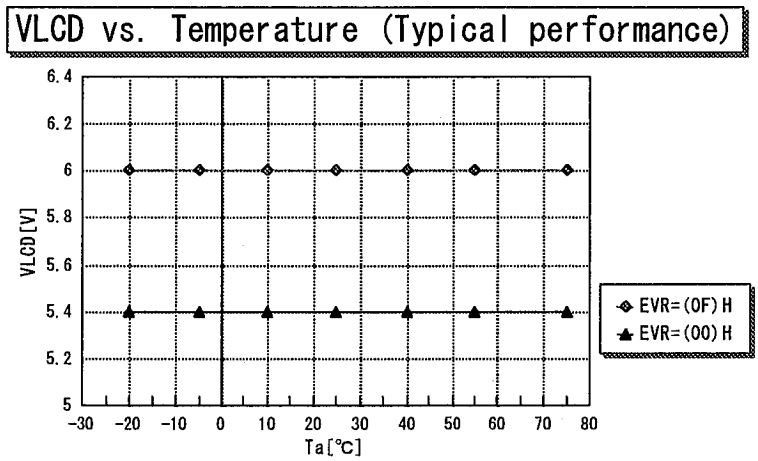
= (2/1)·[(150/150)·3.0]

= 6.0V

	Min.$(00)_H$	Max.$(0F)_H$
Adjustable Range	5.4 · 6.0	[V]
Step Voltage	40	[mV]

*) The V_{LCD} operating temperature. Please refer to the following graphs.

(conditions) V_{DD} = 3V
Ra=1MΩ, Rb=1MΩ (Ra:Rb = 1:1)
Voltage tripler

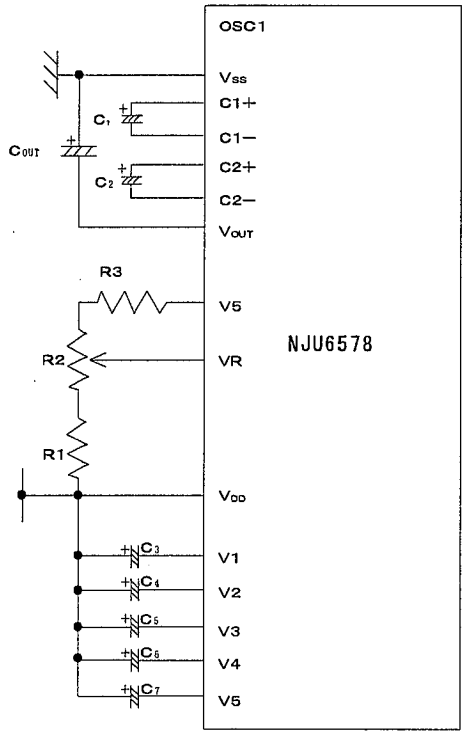


(d) LCD Driving Voltage Generation Circuits

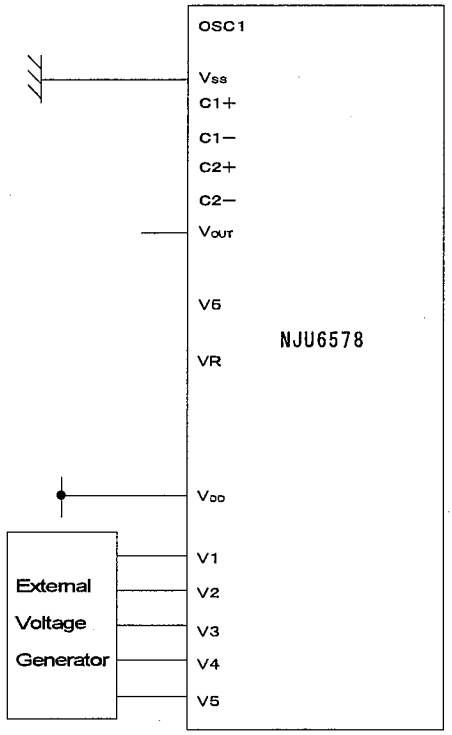
The LCD driving bias voltage of V1,V2,V3,V4 are generated internally by dividing the V5 voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig. 4, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors C3, C4, C5, C6 and C7 are determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

$V_{LCD} = V_{DD} - V_5 \fallingdotseq 6.0 \sim 7.5V$

Item	Value
COUT	4.7 ~ 10 μF
C1,C2	4.7 ~ 10 μF
C3 to C7	0.1 ~ 0.47 μF
R1	2.0M Ω
R2	0.5M Ω
R3	2.5M Ω

Fig. 4

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of VOUT is required when external power supply using.

When Vss > V5 --- VOUT=V5

When Vss ≦ V5 --- VOUT=Vss

(5) MPU Interface

(5-1) Interface type selection

NJU6578 interfaces with MPU by 8-bit bi-directional data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6578 interfaces to 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of C86 terminal connecting to "H" or "L" as shown in table 6.

Table 6

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS}$	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6578 discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal $\overline{CS}$ set to "L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when chip is not selected. The data input from SI terminal is MSB first like as the order of $D_7, D_6, \cdots\cdots D_0$, and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When $\overline{RES}$ terminal becomes "L" or $\overline{CS}$ terminal becomes "H" before 8th serial clock rise edge, NJU6578 recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bits. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface .

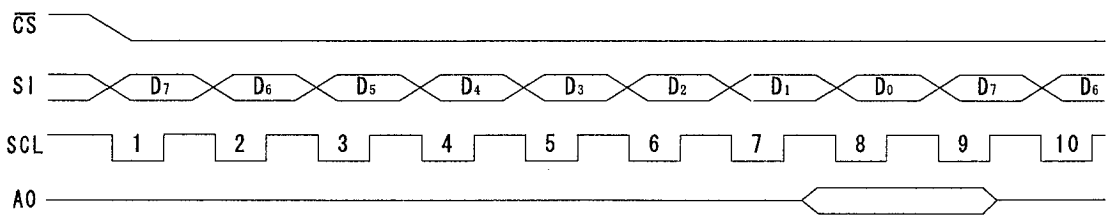


Fig.5

(5-5) Access to the Display Data RAM and Internal Register.

The NJU6578 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle (dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

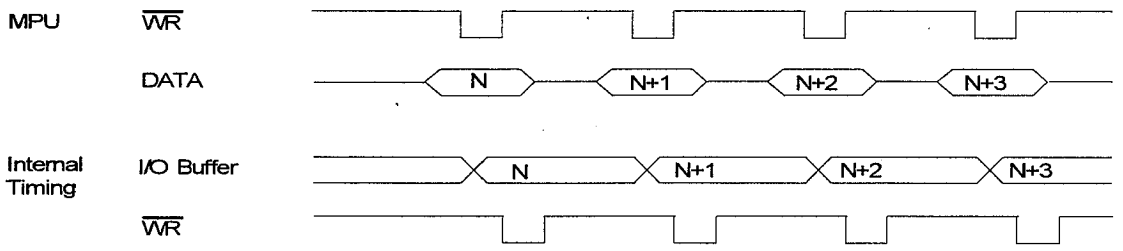
Therefore high speed data transmission between MPU and NJU6578 is available because of it is not limited by the t_{ACC} and t_{DS} as display data RAM access time and is limited by the system cycle time (R) or (W).

If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read the data in the pointed address just after the address set operation, and second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

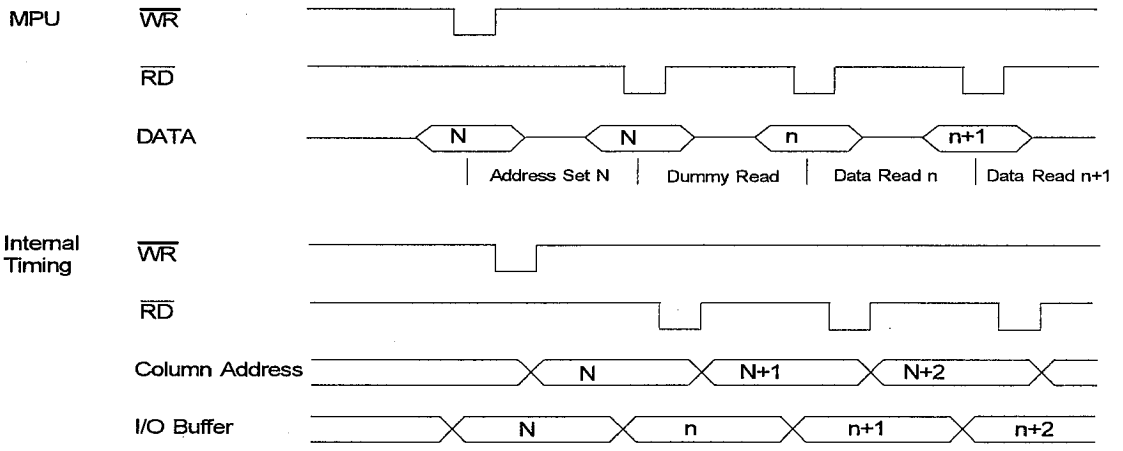


Fig.6

(5-6) Chip Select

$\overline{CS}$ is Chip Select terminal. In case of $\overline{CS}$="L". the interface with MPU is available. In case of $\overline{CS}$="H" ,the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and counter are reset. However, the reset is allways operated in any conditions of CS.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	-0.3～+7.0	V
		-0.3～+3.6(used Tripler)	V
Supply Voltage (2)	V_5	V_{DD}-11.0～V_{DD}+0.3	V
Supply Voltage (3)	V_1～V_4	V_5～V_{DD}+0.3	V
Input Voltag	V_{IN}	-0.3～V_{DD}+0.3	V
Operating Temperatur	T_{opr}	-30～+80	°C
Storage Temperatur	T_{stg}	-55～+125 (Chip)	°C
		-55～+100 (TCP)	

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS}=0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (V_{DD}=5V ± 10%, V_{SS}=0V, Ta=-20 ～ +75°C)

PARAMETE		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	Note
Operating Voltage(1)	Recommend	V_{DD}			4.5	5.0	5.5	V	5
	Available				2.4		5.5		
Operating Voltage(2)	Recommend	V_5			V_{DD}-10.0		V_{DD}-5.0	V	
	Available				V_{DD}-10.0				
	Available	V_1,V_2	V_{LCD}= V_{DD}-V_5		V_{DD}-0.6V_{LCD}		V_{DD}		
	Available	V_3,V_4			V_5		V_{DD}-0.4V_{LCD}		
Input Voltage	High Level	V_{IHC1}	D_0...D_7,A0, $\overline{CS}$,$\overline{RES}$,$\overline{RD}$, $\overline{WR}$,C86,SI, SCL,P/$\overline{S}$ Terminals		0.7V_{DD}		V_{DD}	V	
		V_{IHC2}		V_{DD}=2.7V	0.8V_{DD}		V_{DD}		
	Low Level	V_{ILC1}			V_{SS}		0.3V_{DD}	V	
		V_{ILC2}		V_{DD}=2.7V	V_{SS}		0.2V_{DD}		
Output Voltage	High Level	V_{OHC11}	D_0...D_7 Terminals	I_{OH}=-1mA	0.8V_{DD}		V_{DD}	V	
		V_{OHC12}		I_{OH}=-0.5mA V_{DD}=2.7V	0.8V_{DD}		V_{DD}		
	Low Level	V_{OLC11}		I_{OL}= 1mA	V_{SS}		0.2V_{DD}	V	
		V_{OLC12}		I_{OL}= 0.5mA V_{DD}=2.7V	V_{SS}		0.2V_{DD}		
Input Leakage Current		I_{LI}	All Input terminals		- 1.0		1.0	μA	
		I_{LO}	All I/O Terminals (D_0...D_7)		- 3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=10.0V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Power save Mode			0.05	5.0	μA	
Operating Current		I_{DD12}	Display			28	45	μA	8
		I_{DD14}	V_{LCD}=8.0V	V_{DD}=2.7V		16	25		
		I_{DD21}	Accessing			350	500		9
		I_{DD22}	f_{CYC}=200kHz	V_{DD}=2.7V		170	240		

■ ELECTRICAL CHARACTERISTICS (2) (VDD=5V ± 10%, VSS=0V, Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Input Terminal Capacitance		CIN	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,C86,SI, SCL,P/S,T1,T2,D0...D7 Ta=25°C			10		pF	
Oscillation Frequency		fOSC	Ta=25°C	VDD=5.0V	9	11	13	kHz	
				VDD=2.7V	8	9.75	11.5		
Voltage Tripler	Input Voltage	VDD1	VDD-VSS		2.4		5.5	V	
		VDD2	VDD-VSS, used Tripler		2.4		3.3		10
	Output Volt.	VOUT	VSS-VLCD, used Tripler,VDD=3.3V		- 6.6			V	
	On-resistance	RTRI	VDD=3V;COUT=4.7μF used Tripler			600	1000	Ω	
	Adjustment range of LCD Driving Volt.	VOUT	Tripler Circuit "OFF"		VDD-10.0V		VDD-5.0V	V	11
	Voltage Follower	V5	Voltage Adjustment Circuit "OFF"		VDD-10.0V		VDD-5.0V	V	
	Operating Current	IOUT1	VDD=4.5V, VLCD=8V COM/SEG Terminals Open No Access Display Checkered pattern			58	120	μA	12
		IOUT2				22	45		
		IOUT3				21	43		
	Voltage Reg.	VREG%	VDD=3V,Ta=25°C				3	%	13

Note 5) NJU6578 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of the D0 to D7 terminals.

Note 7) RON is the resistance values between power supply terminals(V1, V2, V3, V4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as IDD1X.

Note 10) Supply voltage (VDD) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V5 can be adjusted within the voltage follower operating range.

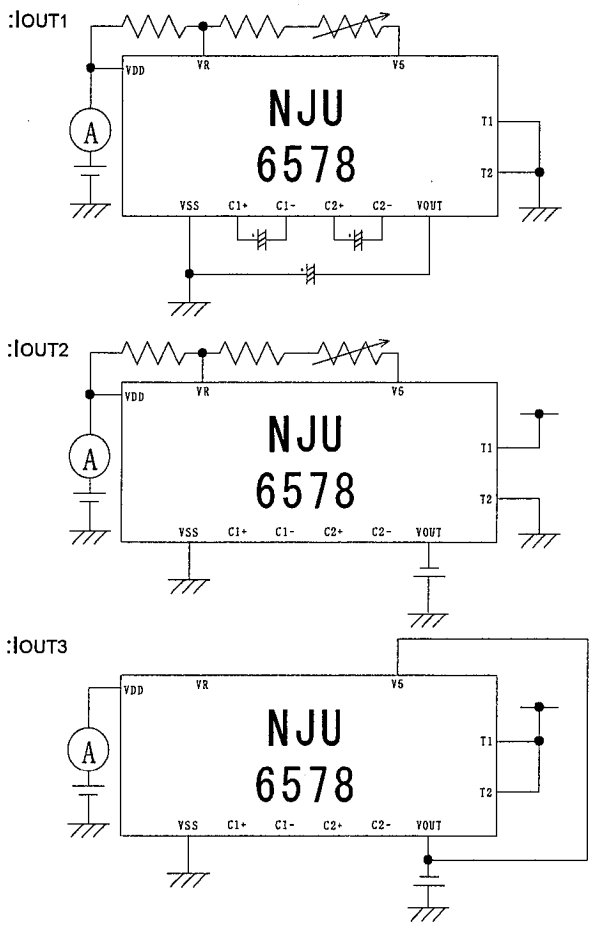
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
IOUT1	L	*	Validity	Validity	Validity	Validity	Unuse
IOUT2	H	L	Validity	Invalidity	Validity	Validity	Use(VOUT)
IOUT3	H	H	Validity	Invalidity	Invalidity	Validity	Use(VOUT,V5)

(* = Don't Care)

Note 13) Apply to the precision of the voltage between VDD and V5 with EVR function.

MEASUREMENT BLOCK DIAGRAM



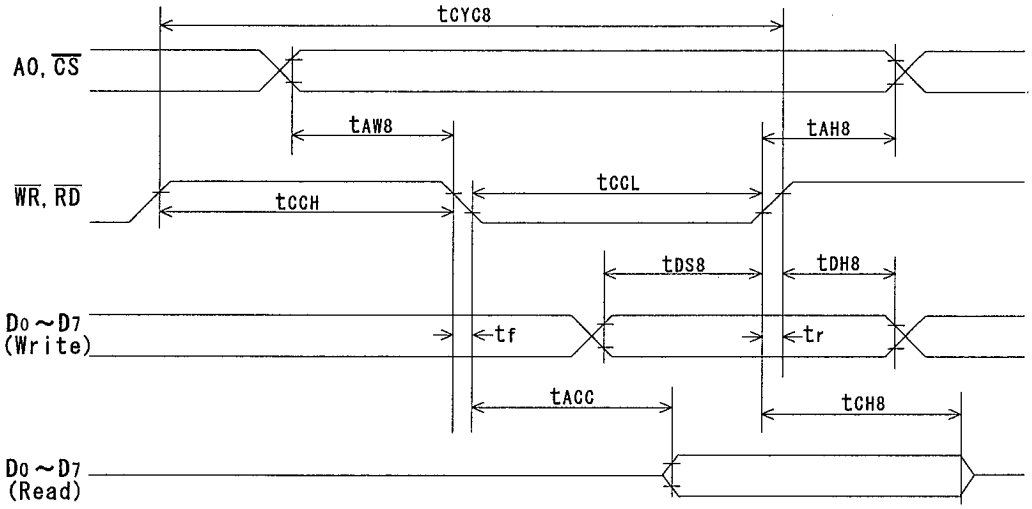
■ ELECTRICAL CHARACTERISTICS (2) (VDD=5V ± 10%, VSS=0V, Ta=-20 ~ +75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	tR	$\overline{RES}$ Terminal	1.0			μs	14
Reset "L" Level Pulse Width	tRW	$\overline{RES}$ Terminal	10			μs	15

Note 14) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 15) Specified minimum pulse width of $\overline{RES}$ signal. Over than tRW "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)



(VDD=5.0V ± 10%,Ta=-20 ~ +75°C)

PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS Terminals	tAH8	10			ns
Address Set Up Time			tAW8	10			ns
System Cycle Time		WR,RD Terminals	tCYC8	180			ns
Control Pulse Width	WR,"L"		tCCL(W)	25			ns
	RD,"L"		tCCL(R)	80			ns
	"H"		tCCH	70			ns
Data Set Up Time		D0~D7 Terminals	tDS8	60			ns
Data Hold Time			tDH8	10			ns
RD Access Time			tACC8		70	CL=100pF	ns
Output Disable Time			tCH8	0	30		ns
Rise Time, Fall Time		CS, WR, RD, A0, D0~D7 Terminals	tr,tf		15		ns

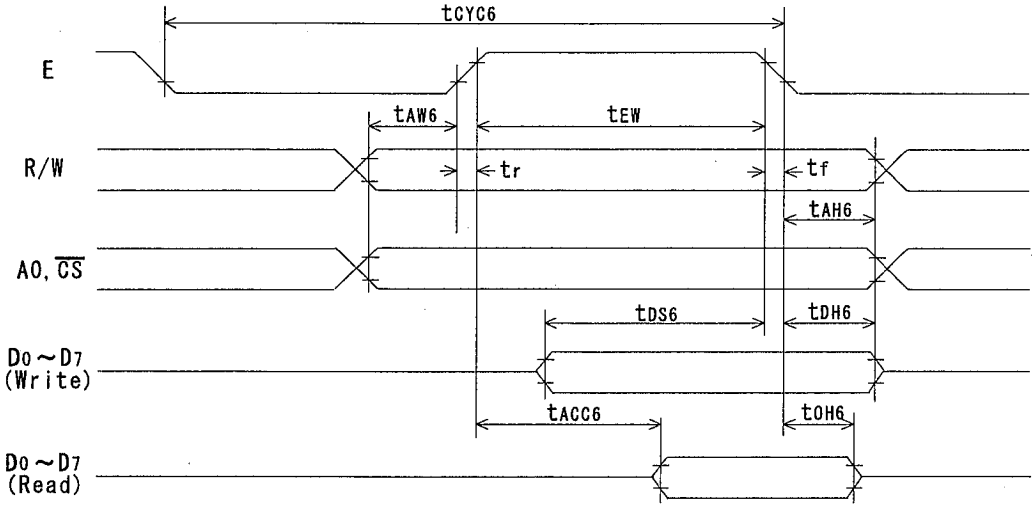
(VDD=2.7 ~ 4.5V,Ta=-20 ~ +75°C)

PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS Terminals	tAH8	25			ns
Address Set Up Time			tAW8	25			ns
System Cycle Time		WR,RD Terminals	tCYC8	450			ns
Control Pulse Width	WR,"L"		tCCL(W)	50			ns
	RD,"L"		tCCL(R)	200			ns
	"H"		tCCH	220			ns
Data Set Up Time		D0~D7 Terminals	tDS8	120			ns
Data Hold Time			tDH8	35			ns
RD Access Time			tACC8		140	CL=100pF	ns
Output Disable Time			tCH8	0	35		ns
Rise Time, Fall Time		CS, WR, RD, A0, D0~D7 Terminals	tr,tf		15		ns

Note 16) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 17) Each timing is specified based on 0.2xVDD and 0.8xVDD.

· Read/Write operation sequence (68 Type MPU)



(V_{DD}=5.0V ± 10%,Ta=-20 ~ +75°C)

PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS,R/W Terminals	tAH6	10			ns
Address Set Up Time			tAW6	10			ns
System Cycle Time			tCYC6	180			ns
Enable Pulse Width	Read	E Terminal	tEW	100			ns
	Write			25			ns
Data Set Up Time		D0~D7 Terminals	tDS6	60			ns
Data Hold Time			tDH6	20			ns
Access Time			tACC6		70	CL=100pF	ns
Output Disable Time			tOH6	0	25		ns
Rise Time, Fall Time		A0, CS, R/W, E, D0~D7 Terminals	tr,tf		15		ns

(V_{DD}=2.7 ~ 4.5V,Ta=-20 ~ +75°C)

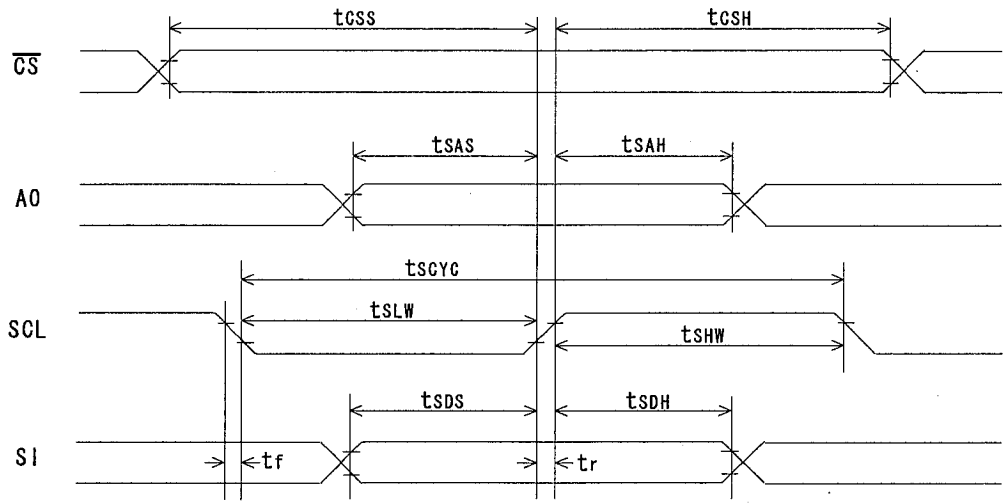
PARAMETER			SYMBOL	MIN.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS,R/W Terminals	tAH6	25			ns
Address Set Up Time			tAW6	25			ns
System Cycle Time			tCYC6	450			ns
Enable Pulse Width	Read	E Terminal	tEW	200			ns
	Write			50			ns
Data Set Up Time		D0~D7 Terminals	tDS6	120			ns
Data Hold Time			tDH6	40			ns
Access Time			tACC6		140	CL=100pF	ns
Output Disable Time			tOH6	0	45		ns
Rise Time, Fall Time		A0, CS, R/W, E, D0~D7 Terminals	tr,tf		15		ns

Note 18) tCYC6 indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 19) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.

Note 20) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

・Write operation sequence (Serial Interface)



(VDD=5.0V ± 10%,Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	500			ns
SCL "H" pulse width		tSHW	150			ns
SCL "L" pulse width		tSLW	150			ns
Address Set Up Time	A0 Terminal	tSAS	120			ns
Address Hold Time		tSAH	200			ns
Data Set Up Time	SI Terminal	tSDS	120			ns
Data Hold Time		tSDH	50			ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS	30			ns
		tCSH	400			ns
Rise Time, Fall Time	SCL, A0, $\overline{CS}$, SI Terminals	tr,tf		15		ns

(VDD=2.7 ~ 4.5V,Ta=-20 ~ +75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	1000			ns
SCL "H" pulse width		tSHW	300			ns
SCL "L" pulse width		tSLW	300			ns
Address Set Up Time	A0 Terminal	tSAS	250			ns
Address Hold Time		tSAH	400			ns
Data Set Up Time	SI Terminal	tSDS	250			ns
Data Hold Time		tSDH	100			ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS	60			ns
		tCSH	800			ns
Rise Time, Fall Time	SCL, A0, $\overline{CS}$, SI Terminals	tr,tf		15		ns

Note 21) Rise time (tr) and fall time (tf) of input signal should be less than 15ns.
Note 22) Each timing is specified based on 0.2xVDD and 0.8xVDD.

■ LCD DRIVING WAVEFORM

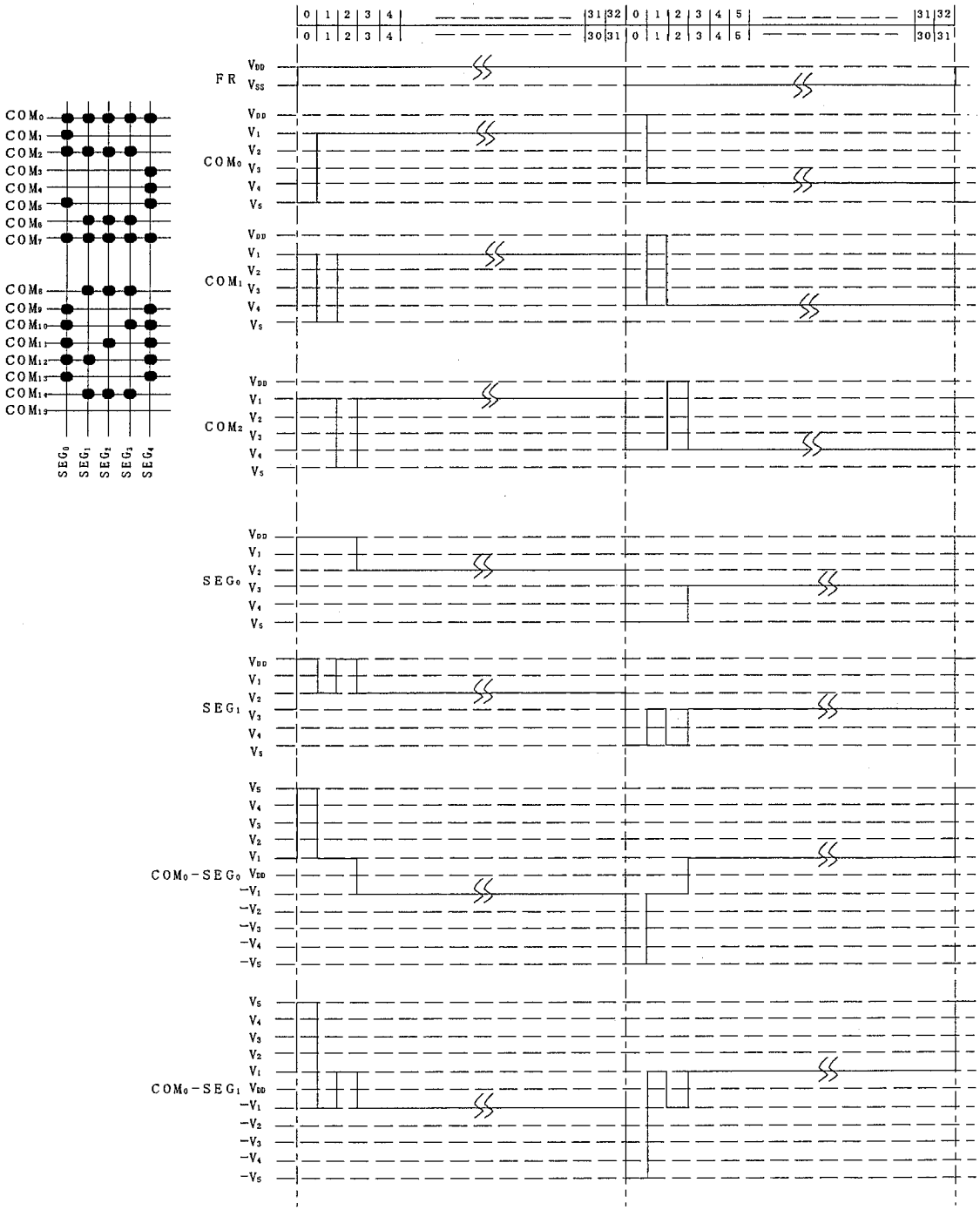


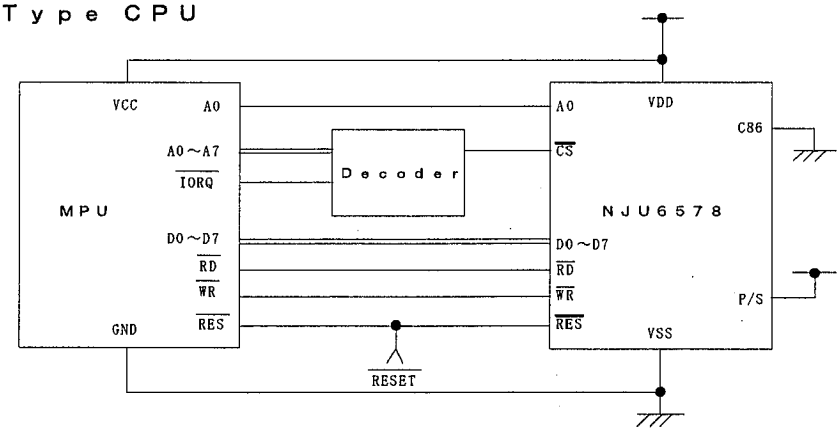
Fig.7

■ APPLICATION CIRCUIT

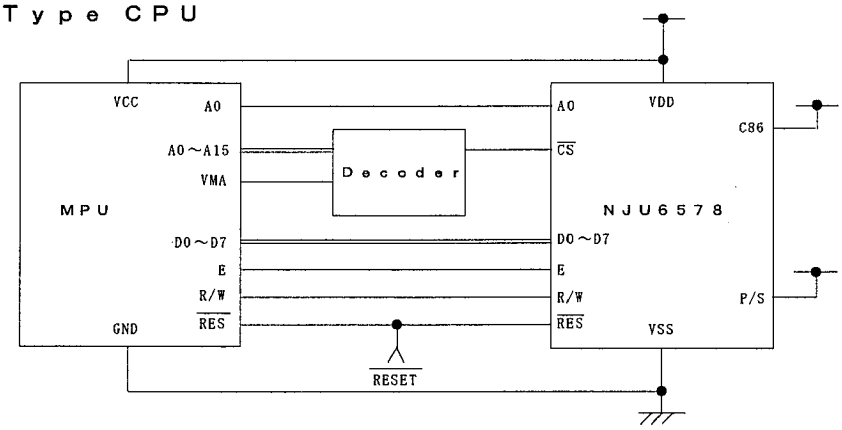
・Microprocessor Interface Example

The NJU6578 can interface with both of 80 type and 68 type MPU by the serial format directly.
Therefore minimum wiring for the MPU interface is available.

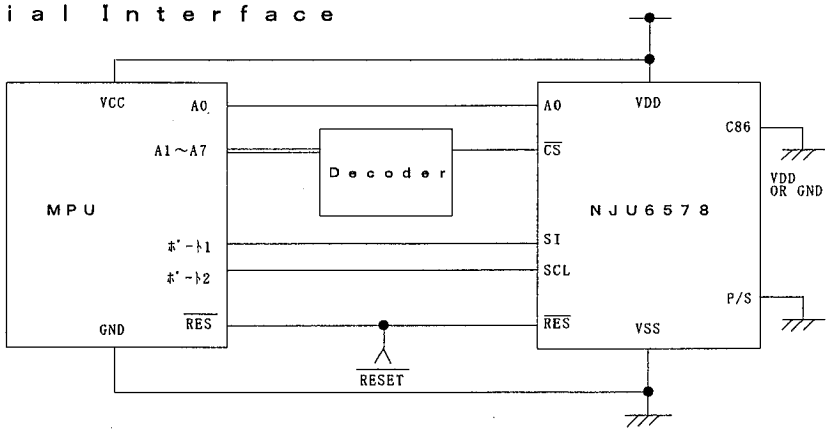
● 8 0 T y p e C P U



● 6 8 T y p e C P U



● S e r i a l I n t e r f a c e



MEMO

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