16-CHARACTER 3-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The **NJU6637** is a 1Chip Dot Matrix LCD controller driver for up to 16-character 3-line display.
It contains microprocessor Interface circuits, Instruction decoder controller, character generator ROM/RAM and common and segment drivers.
The bleeder resistance generates for LCD Bias voltage Internally.
The CR oscillator Incorporates C and R, therefore no external components for oscillation are required.
The microprocessor Interface circuits which operate 1MHz frequency, can be connected directly to serial I/F microprocessor.
The character generator consists of 10,200 bits ROM and 8 x 5 bits RAM. The standard version ROM is coded with 255 characters including capital and small letter fonts.
The 24-common and 80-segment drive up to 16-character 3-line LCD panel which divided two common electrode blocks.
The rectangle outlook is very applicable to COG.

■ PACKAGE OUTLINE

NJU6637CH

■ FEATURES

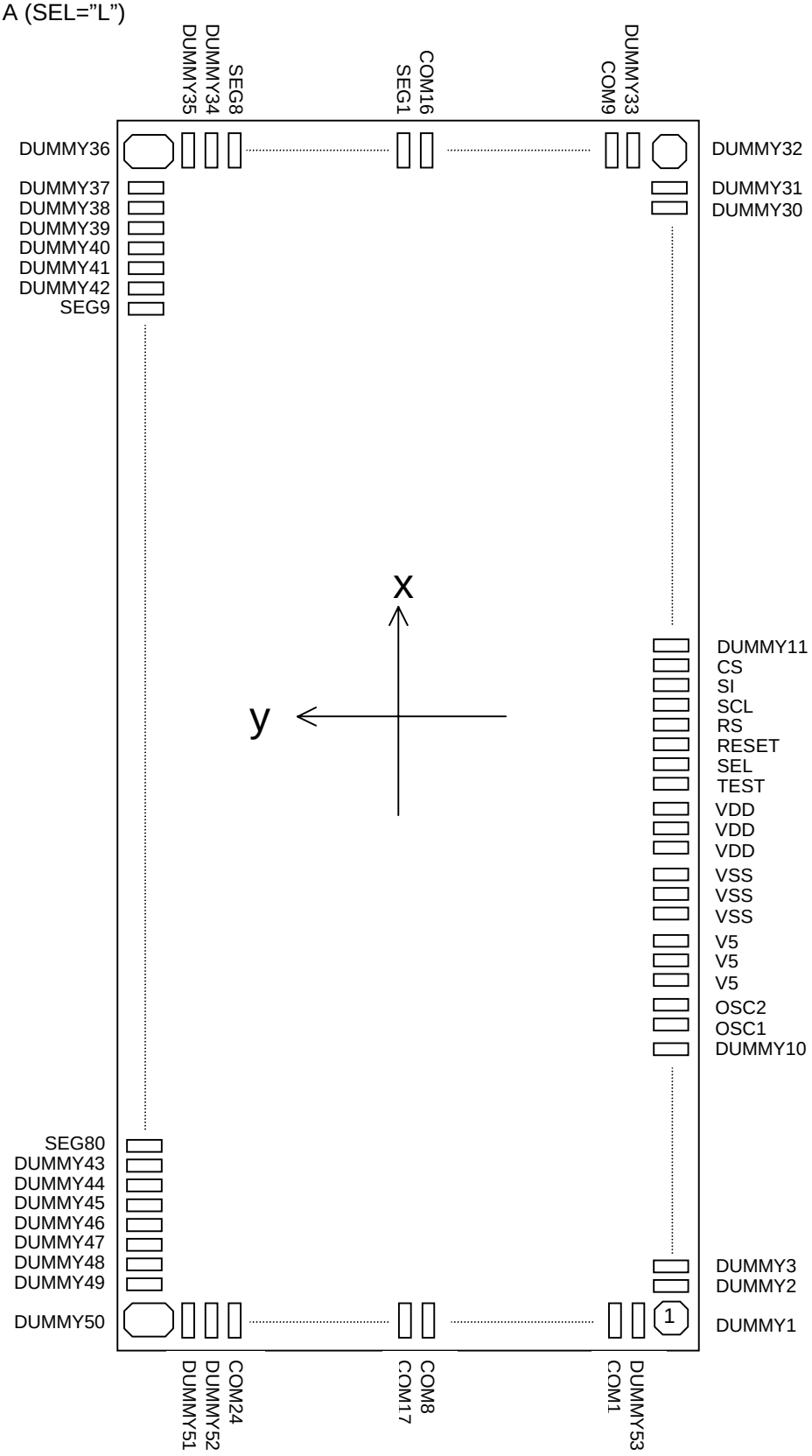
- 16-character 3-line Dot Matrix LCD Controller Driver
- Serial Direct Interface with Microprocessor
- Display Data RAM :48 x 8 bits : Maximum 16-character 3line Display
- Character Generator ROM :10,200 bits ; 255 characters for 5 x 8 dots
- Character Generator RAM :8 x 5 bits ; 1 Patterns(5 x 8 dots)
- Microprocessor direst accessing to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver :24-common / 80-segment
- Duty Ratio :1/24 Duty
- Maximum Display Characters :48 Characters
- Common Driver Order Assignment by mask option

Version	COM1 to COM24 (PAD Name)
NJU6637A	COM1 to COM24
NJU6637B	COM24 to COM1

- Useful Instruction Set
  Clear Display, Returns Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift.
- Power On Reset / Hardware Reset Function
- Oscillation Circuit on chip
- Bleeder Resistance on chip
- Low Power Consumption
- Operating Voltage --- +3V
- Package Outline --- Bumped Chip
- C-MOS Technology

■ PAD LOCATION

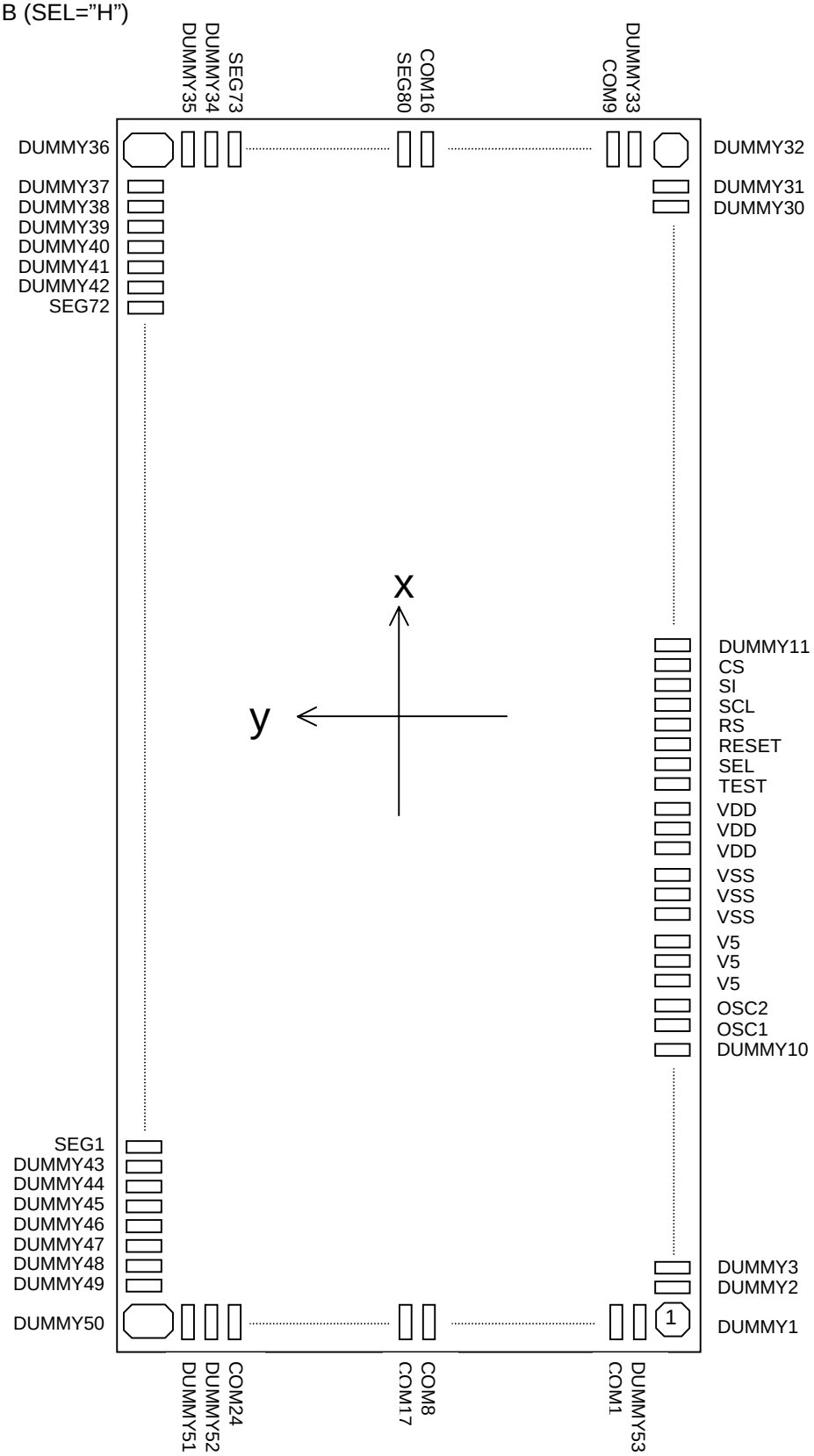
NJU6637A Mode A (SEL="L")



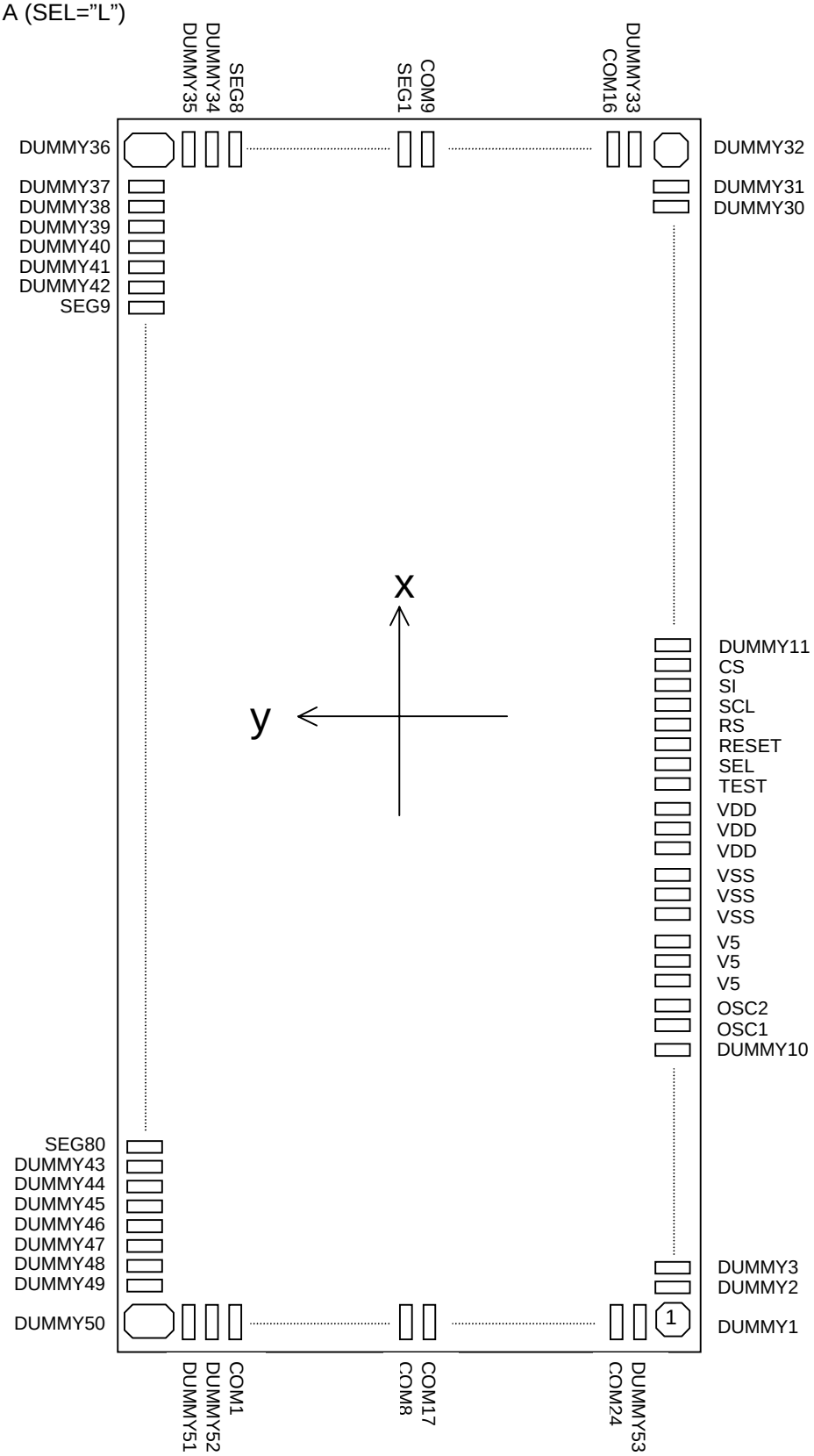
Chip Size : 5.48 x 1.68mm
Chip Size : X=0um, Y=0um
Chip Thickness : 625um±30um

Bump Size : 90 x 45um
Bump Height : 17.5um
Bump Material :Au

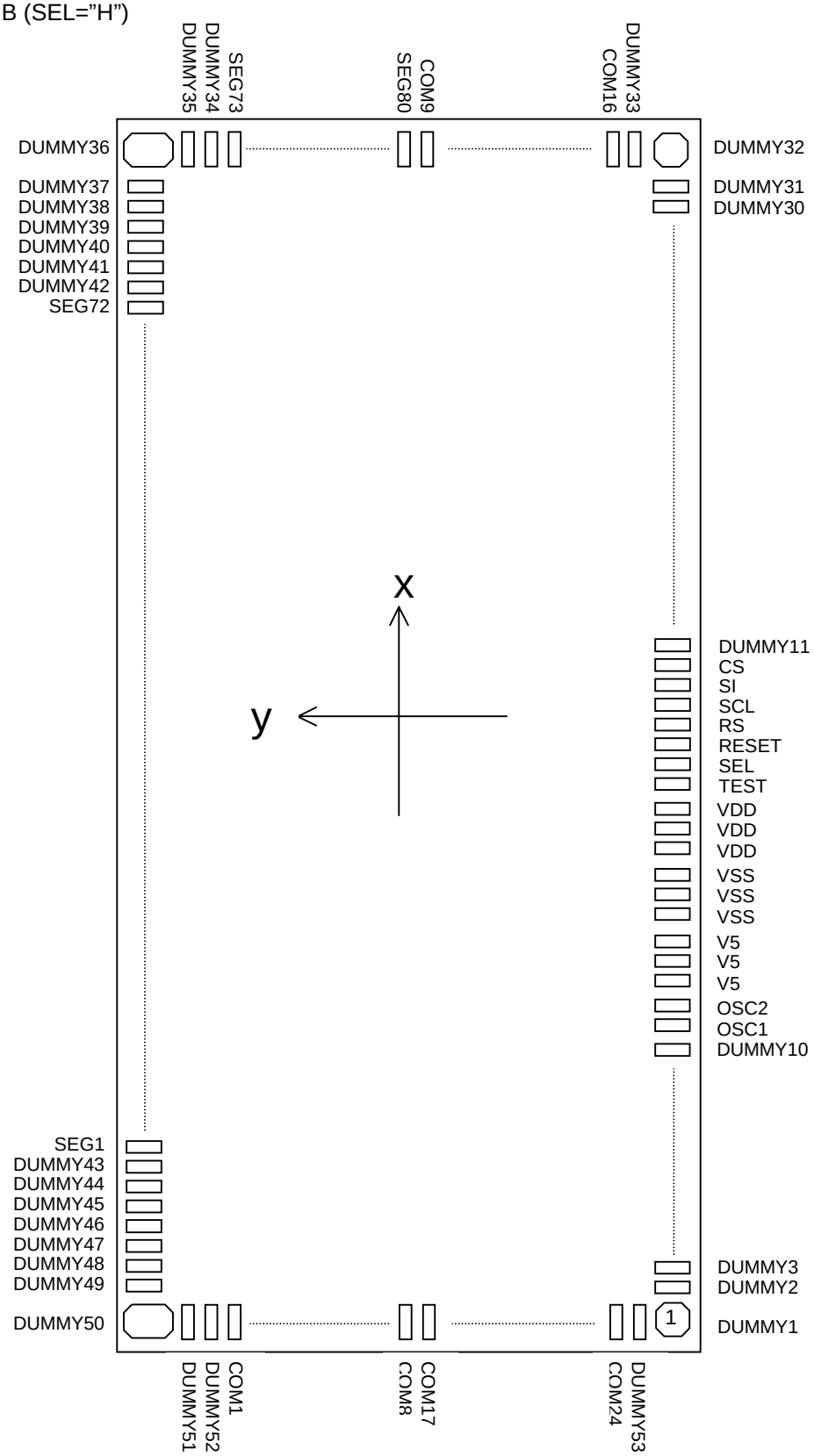
NJU6637A Mode B (SEL="H")



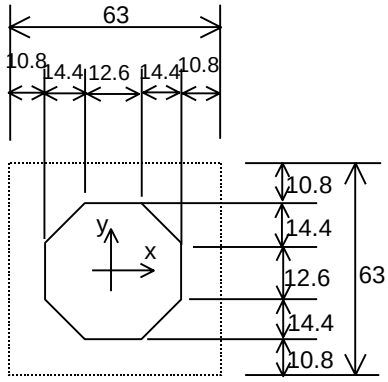
NJU6637B Mode A (SEL="L")



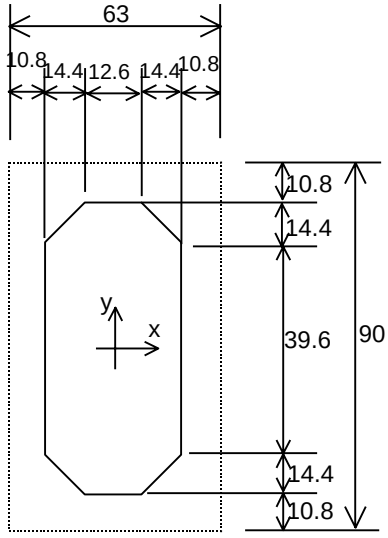
NJU6637B Mode B (SEL="H")



Alignment Mark size



DUMMY1
DUMMY32



DUMMY36
DUMMY50

■ PAD COORDINATES

Chip Size(5.48mm x 1.68mm)

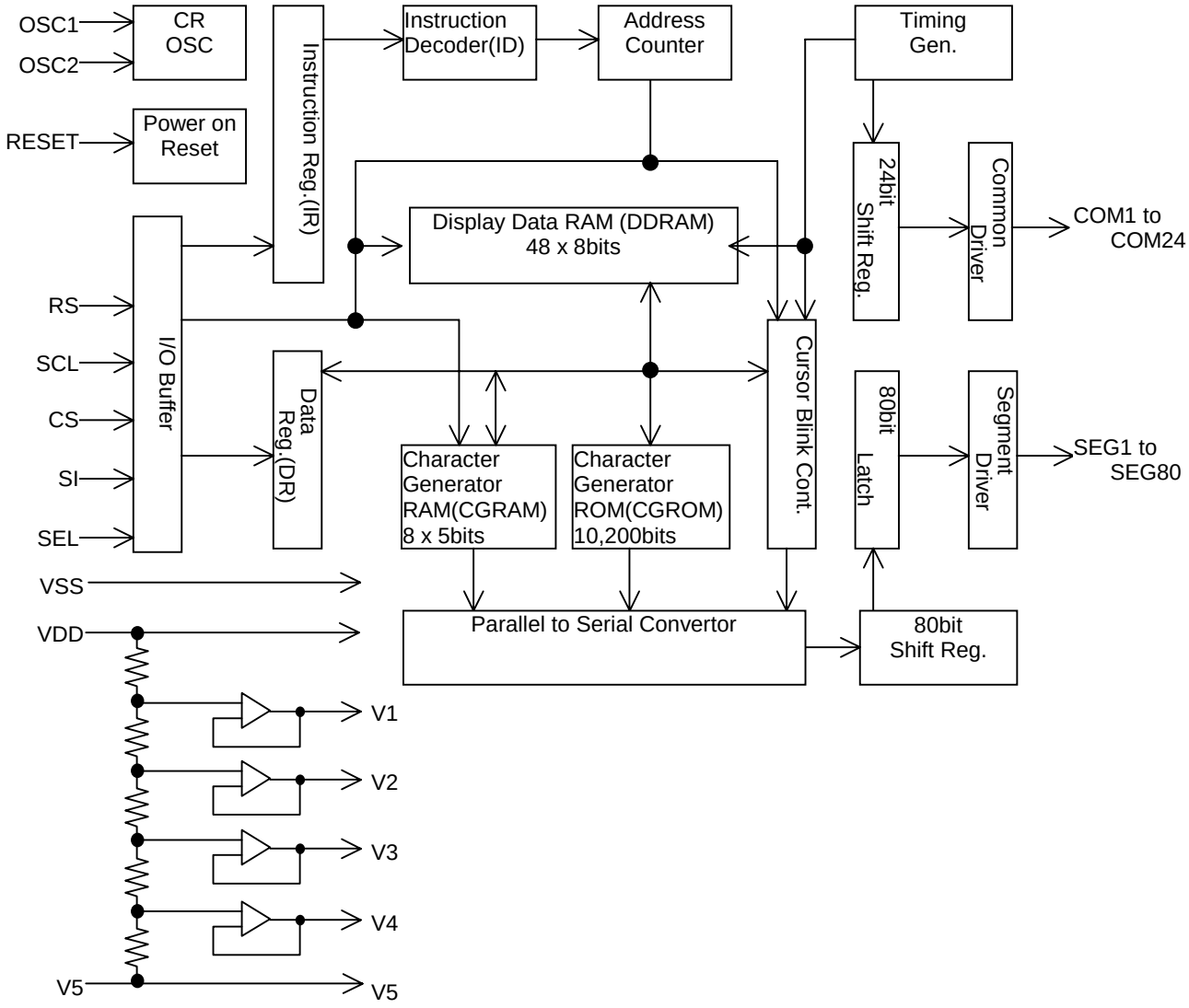
PAD No.	PAD Name		X= µm	Y= µm
	SEL=H	SEL=L		
1	DMY1	DMY1	-2599	-690
2	DMY2	DMY2	-2520	-690
3	DMY3	DMY3	-2460	-690
4	DMY4	DMY4	-2400	-690
5	DMY5	DMY5	-2340	-690
6	DMY6	DMY6	-2280	-690
7	DMY7	DMY7	-2220	-690
8	DMY8	DMY8	-2160	-690
9	DMY9	DMY9	-2100	-690
10	DMY10	DMY10	-2040	-690
11	OSC1	OSC1	-1860	-690
12	OSC2	OSC2	-1620	-690
13	V5	V5	-1440	-690
14	V5	V5	-1380	-690
15	V5	V5	-1320	-690
16	VSS	VSS	-1080	-690
17	VSS	VSS	-1020	-690
18	VSS	VSS	-960	-690
19	VDD	VDD	-900	-690
20	VDD	VDD	-840	-690
21	VDD	VDD	-780	-690
22	TEST	TEST	-540	-690
23	SEL	SEL	-300	-690
24	RESET	RESET	-60	-690
25	RS	RS	180	-690
26	SCL	SCL	420	-690
27	SI	SI	660	-690
28	CS	CS	1140	-690
29	DMY11	DMY11	1320	-690
30	DMY12	DMY12	1380	-690
31	DMY13	DMY13	1440	-690
32	DMY14	DMY14	1500	-690
33	DMY15	DMY15	1560	-690
34	DMY16	DMY16	1620	-690
35	DMY17	DMY17	1680	-690
36	DMY18	DMY18	1740	-690
37	DMY19	DMY19	1800	-690
38	DMY20	DMY20	1860	-690
39	DMY21	DMY21	1920	-690
40	DMY22	DMY22	1980	-690
41	DMY23	DMY23	2040	-690
42	DMY24	DMY24	2100	-690
43	DMY25	DMY25	2160	-690
44	DMY26	DMY26	2220	-690
45	DMY27	DMY27	2280	-690
46	DMY28	DMY28	2340	-690
47	DMY29	DMY29	2400	-690
48	DMY30	DMY30	2460	-690
49	DMY31	DMY31	2520	-690
50	DMY32	DMY32	2599	-690

PAD No.	PAD Name		X= µm	Y= µm
	SEL=H	SEL=L		
51	DMY33	DMY33	2599	-540
52	COM9	COM9	2599	-480
53	COM10	COM10	2599	-420
54	COM11	COM11	2599	-360
55	COM12	COM12	2599	-300
56	COM13	COM13	2599	-240
57	COM14	COM14	2599	-180
58	COM15	COM15	2599	-120
59	COM16	COM16	2599	-60
60	SEG80	SEG1	2599	0
61	SEG79	SEG2	2599	60
62	SEG78	SEG3	2599	120
63	SEG77	SEG4	2599	180
64	SEG76	SEG5	2599	240
65	SEG75	SEG6	2599	300
66	SEG74	SEG7	2599	360
67	SEG73	SEG8	2599	420
68	DMY34	DMY34	2599	480
69	DMY35	DMY35	2599	540
70	DMY36	DMY36	2599	698
71	DMY37	DMY37	2520	698
72	DMY38	DMY38	2460	698
73	DMY39	DMY39	2400	698
74	DMY40	DMY40	2340	698
75	DMY41	DMY41	2280	698
76	DMY42	DMY42	2220	698
77	SEG72	SEG9	2160	698
78	SEG71	SEG10	2100	698
79	SEG70	SEG11	2040	698
80	SEG69	SEG12	1980	698
81	SEG68	SEG13	1920	698
82	SEG67	SEG14	1860	698
83	SEG66	SEG15	1800	698
84	SEG65	SEG16	1740	698
85	SEG64	SEG17	1680	698
86	SEG63	SEG18	1620	698
87	SEG62	SEG19	1560	698
88	SEG61	SEG20	1500	698
89	SEG60	SEG21	1440	698
90	SEG59	SEG22	1380	698
91	SEG58	SEG23	1320	698
92	SEG57	SEG24	1260	698
93	SEG56	SEG25	1200	698
94	SEG55	SEG26	1140	698
95	SEG54	SEG27	1080	698
96	SEG53	SEG28	1020	698
97	SEG52	SEG29	960	698
98	SEG51	SEG30	900	698
99	SEG50	SEG31	840	698
100	SEG49	SEG32	780	698

PAD No.	PAD Name		X= µm	Y= µm
	SEL=H	SEL=L		
101	SEG48	SEG33	720	698
102	SEG47	SEG34	660	698
103	SEG46	SEG35	600	698
104	SEG45	SEG36	540	698
105	SEG44	SEG37	480	698
106	SEG43	SEG38	420	698
107	SEG42	SEG39	360	698
108	SEG41	SEG40	300	698
109	SEG40	SEG41	240	698
110	SEG39	SEG42	180	698
111	SEG38	SEG43	120	698
112	SEG37	SEG44	60	698
113	SEG36	SEG45	0	698
114	SEG35	SEG46	-60	698
115	SEG34	SEG47	-120	698
116	SEG33	SEG48	-180	698
117	SEG32	SEG49	-240	698
118	SEG31	SEG50	-300	698
119	SEG30	SEG51	-360	698
120	SEG29	SEG52	-420	698
121	SEG28	SEG53	-480	698
122	SEG27	SEG54	-540	698
123	SEG26	SEG55	-600	698
124	SEG25	SEG56	-660	698
125	SEG24	SEG57	-720	698
126	SEG23	SEG58	-780	698
127	SEG22	SEG59	-840	698
128	SEG21	SEG60	-900	698
129	SEG20	SEG61	-960	698
130	SEG19	SEG62	-1020	698
131	SEG18	SEG63	-1080	698
132	SEG17	SEG64	-1140	698
133	SEG16	SEG65	-1200	698
134	SEG15	SEG66	-1260	698
135	SEG14	SEG67	-1320	698
136	SEG13	SEG68	-1380	698
137	SEG12	SEG69	-1440	698
138	SEG11	SEG70	-1500	698
139	SEG10	SEG71	-1560	698
140	SEG9	SEG72	-1620	698
141	SEG8	SEG73	-1680	698
142	SEG7	SEG74	-1740	698
143	SEG6	SEG75	-1800	698
144	SEG5	SEG76	-1860	698
145	SEG4	SEG77	-1920	698
146	SEG3	SEG78	-1980	698
147	SEG2	SEG79	-2040	698
148	SEG1	SEG80	-2100	698
149	DMY43	DMY43	-2160	698
150	DMY44	DMY44	-2220	698

PAD No.	PAD Name		X= µm	Y= µm
	SEL=H	SEL=L		
151	DMY45	DMY45	-2280	698
152	DMY46	DMY46	-2340	698
153	DMY47	DMY47	-2400	698
154	DMY48	DMY48	-2460	698
155	DMY49	DMY49	-2520	698
156	DMY50	DMY50	-2599	698
157	DMY51	DMY51	-2599	540
158	DMY52	DMY52	-2599	480
159	COM24	COM24	-2599	420
160	COM23	COM23	-2599	360
161	COM22	COM22	-2599	300
162	COM21	COM21	-2599	240
163	COM20	COM20	-2599	180
164	COM19	COM19	-2599	120
165	COM18	COM18	-2599	60
166	COM17	COM17	-2599	0
167	COM8	COM8	-2599	-60
168	COM7	COM7	-2599	-120
169	COM6	COM6	-2599	-180
170	COM5	COM5	-2599	-240
171	COM4	COM4	-2599	-300
172	COM3	COM3	-2599	-360
173	COM2	COM2	-2599	-420
174	COM1	COM1	-2599	-480
175	DMY53	DMY53	-2599	-540

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD No.	SYMBOL	I/O	FUNCTION
19-21 16-18	V_{DD} V_{SS}	–	Power Source : V_{DD} = +3V, GND : V_{SS} = 0V
13-15	V_5	–	LCD driving Power Source
11	OSC_1	I	Oscillation Frequency Adjustment Terminals. Normally Open. (Oscillation C and R are Incorporated, Osc Freq.=145kHZ)
12	OSC_2	O	Oscillation Frequency Adjustment Terminals. Normally Open. This terminal also operates as the clock frequency monitor.
25	RS	I	Resister selection signal Input "0":Instruction Resister "1":Data Register
26	SCL	I	Shift clock input
28	CS	I	Chip select signal input
27	SI	I	Data input terminal
23	SEL	I	Segment driver location order select terminal "0": Mode A "1": Mode B
52-59 159-174	COM_1 – COM_{24}	O	LCD Common driving signal Terminals
60-67 77-148	SEG_1 – SEG_{80}	O	LCD segment driving signal Terminals
24	RESET	I	Reset Terminal When the “L” level Input over than 1.2ms to this terminal, the system will be reset.(f_{OSC}=145kHz)
22	TEST	I	Maker Test Terminal This terminal should be connected to Vss or open.
1-9 22-51 68-76 149-158 175	$DUMMY_1$ – $DUMMY_{53}$	–	Dummy Terminal These terminals are electrically open.

■ FUNCTIONAL DESCRIPTION

(1)Description for each blocks

(1-1)Register

The **NJU6637** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register (IR) stores Instruction codes such as “Clear Display” and “Return Home”, and address data for Display Data RAM (DD RAM) and Character Generator RAM (CG RAM).

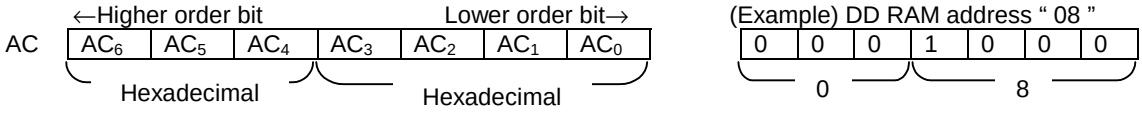
The Register (DR) is a temporary storing register, the data in the Register (DR) is written into the DD RAM or CG RAM.
The data in the Register (DR) written by the MPU is transferred from the Register automatically to the DD RAM or CG RAM by Internal operation.
These two registers are selected by the selection signal RS.

(1-2)Address counter (AC)

The address Counter (AC) addresses the DD RAM and CG RAM.
When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the counter (AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the counter (AC) increments (or decrements) “1” automatically.

(1-3)Display Data RAM (DD RAM)

The display data RAM (DD RAM) consisting of 48 x 8 bits stores up to 48-character display data represented in 8-bit code.
The DD RAM address data set in the address Counter (AC) is represented in hexadecimal.



16-character 2-line Display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAMaddress(Hex.)
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
3rd line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	

The relation between DD RAM address and display position on the LCD shown below.

[Left Shift Display]

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
(10) ←	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10
(20) ←	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	20

[Right Sift Display]

0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	→ (1F)
2F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	→ (2F)

(1-4)Character Generator ROM(CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 255 kinds of 5 x 8 dots character pattern. The correspondence between character code and standard character pattern is shown in Table 2.

User-defined character pattern (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version –02)

Lower 4 bit (Hexadecimal) \ Upper 4 bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-5)Character Generator RAM

The character generator RAM (CG RAM) stores any kinds of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM stores 1 kinds of character in 5 x 8 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 8 dots)

Character Code (DD RAM data)	CG RAM address			Character pattern (CG RAM data)	
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0			4 3 2 1 0	
← →	← →			← →	
Upper bit Lower bit	Upper bit Lower bit			Upperbit Lowerbit	
0 0 0 0 0 0 0 0	0 1 0 0 0	0 0 0		1 1 1 1 0	
		0 0 1		1 0 0 0 1	
		0 1 0		1 0 0 0 1	Character
		0 1 1		1 1 1 1 0	Pattern
		1 0 0		1 0 1 0 0	Example
		1 0 1		1 0 0 1 0	
		1 1 0		1 0 0 0 1	
		1 1 1		0 0 0 0 0	← Cursor Position

Notes: 1. Character code bits 0 and 1 correspond to the CG RAM address 3 and 4.

2. CG RAM address 0, 1 and 2 designate a character pattern line position.
   The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the data of 8th line should be "0".
   If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position corresponding to the CG RAM data bits 0 to 4 are all shown above.
4. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-6)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuit operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be undesirable Influence, such as flickering, in areas other than the display area.

(1-7) LCD Driver

LCD driver consists of 24-common driver and 80-segment driver.

The 80 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-8) Common Driver Assignment

The scanning order can be assigned by mask option as shown as follows:

	COM Outputs Terminals					
PAD No.	174	167	166	159	59	52
Pin name	COM1	COM8	COM17	COM24	COM16	COM9
Ver. A	COM1 →	COM8	COM17 →	COM24	COM16 ←	COM9
Ver. B	COM24 ←	COM17	COM8 ←	COM1	COM9 →	COM16

(1-9) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks. The cursor or blinks appears in the digit position at the DD RAM address set in the address counter(AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	1	0	0	0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
3rd line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F

← Display Position

← DD RAM Address (Hexadecimal)

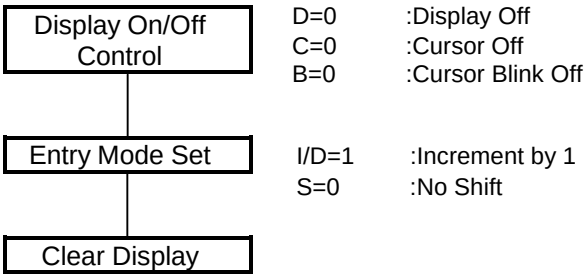
Cursor Position

Note) The cursor or blinks appears when the address counter (AC) selects the CG RAM.
But the displayed cursor and blink are meaningless.
If the AC stores the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2)Power on Initialization by internal circuits

(2-1) Initialization By internal Reset circuits

The **NJU6637** is initialized automatically by the internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.
During the internal power on initialization is kept 4ms after V_{DD} = 2.4V. (fosc=145KHz)
Initialization flow is shown below:

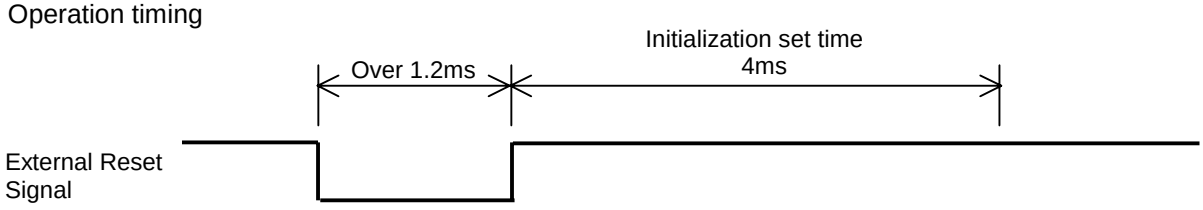


Note) If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power on initialization Circuits will not operate and initialization will not be performed.
In this case, the initialization by MPU software is required.

(2-2) Initialization By Hardware

The **NJU6637** incorporates RESET terminal to initialize the all system. When the “L” level input over than 1.2ms to the RESET terminal, the reset sequence is executed. In this time, the initialization during 4ms after RESET terminal goes to “H”.

- Operation timing



(3)Instructions

The **NJU6637** incorporates two resisters, which are Instruction Register (IR) and a Data Register (DR). These two registers store control information temporarily to allow interface between **NJU6637** and MPU or peripheral ICs operating different cycles. The operation of **NJU6637** is determined by this control signal from MPU. The control information includes register selection signals (RS) and data bus signals (DB_0 to DB_7). Table 5. Shows each instruction and its operating time.

Note) The execution time mentioned in Table 5. is based on fcp or f_{OSC}=145kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 5. Table of Instruction

INSTRUCTION	CODE									DESCRIPTION	EXEC TIME (f_{OSC}=145kHz)*
	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Maker Test	0	0	0	0	0	0	0	0	0	All “0” code is using for maker testing.	–
Clear Display	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	2ms
Return Home	0	0	0	0	0	0	0	1	*	Sets DD RAM address 00H In AC and returns display being shifted to original position. DD RAM contents remain unchanged.	0µs
Entry Mode Set	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and species shift of display are performed In data write. I/D=1:Increment, I/D=D:Decrement, S=1:Accopanies display shift.	0µs
Display ON/OFF Control	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B)	0µs
Cursor or Display Shift	0	0	0	0	1	S/C	R/L	*	*	Move cursor and shifts display without changing DD RAM contents. S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to right R/L=0 : Shift to the left	0µs
Set RAM Address	0	1	RAM address							Sets RAM address. After this instruction, the data is transferred to RAM.	0µs
Write Data to CG or DD RAM	1	Write Data(DD RAM)								Writes data into CG or DD RAM.	55µs
		*	*	*	(CG RAM)						
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM ACG : CG RAM address, ADD : DD RAM address, Corresponds to cursor address AC : Address counter used for both DD and CG RAM										

*:Don't care

(3-1)Description of instruction

a) Maker Test

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0

All “0” code is using device testing mode (only for maker).

b) Clear Display

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code “1” is written into DB_0.
when this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set an increment. If the cursor or blink are displayed, they are returned to the left end of the 1^{st} line on the LCD.
The S of entry mode and CG RAM data does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

c) Return Home

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	*

*=Don’t Care

Return home instruction is executed when the code “1” is written Into DB_1. When this Instruction is executed, the DD RAM address 0 is set to address counter. Display is returned to the original position if shifted, the cursor or blink is returned to the left end of the LCD. If the cursor or blink are on the display, the DD RAM contents are not changed.

d) Entry Mode Set

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets cursor moving direction and display shift On/Off, is executed when the code “1” is written into DB_2 and the codes of (I/D) and (S) are written into DB_1 (I/D) and DB_0 (S) as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	FUNCTION
1	Address increment : The address of the DD RAM increment (+1) when the write, and the cursor or blink moves to the right.
0	Address decrement : The address of the DD or CG RAM decrement (-1) when the write, and the cursor or blink move to the left.

S	FUNCTION
1	Entire display shift. The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated with only the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing into CG RAM.
0	The display does not shifting

e) Display ON/OFF Control

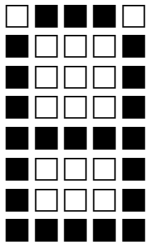
	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code “1” is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB0(B) as shown below.

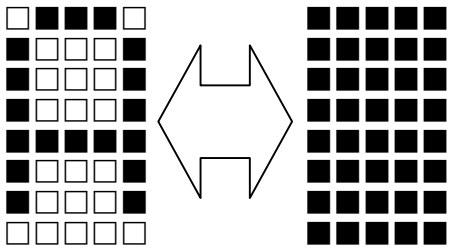
D	FUNCTION
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	FUNCTION
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	FUNCTION
1	The cursor position character is blinking. Blinking rate is 600ms at f_{OSC}=145kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7dots
(1) Cursor display example



Alternating display
(2) Blink display example

f) Cursor Display Shift

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	S/C	R/L	*	*

*=Don’t Care

The Cursor/Display shift instruction shifts the cursor position or display the right or left without writing reading display data. This function is used to correct or search the display. The cursor moves to the 2nd line when it passes the 16th digit of the 1st line. Notice that the every 1st to 3rd line displays shift at the same time. When the displayed data are shifted repeatedly, each line moves only horizontally.
The 2nd and 3rd line display does not shift into the 1st and 2nd line.
The contents of address counter (AC) is not changed by operation of display shift only.
This instruction is executed when the code “1” is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3 (S/C) and DB_2(R/L) as shown below.

S/C	R/L	FUNCTION
0	0	Shifts the cursor position to the left ((AC) is decrement by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

g) Set RAM Address

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	A	A	A	A	A	A	A

←Higher order bit Lower order bit→

The RAM address set instruction is executed when the code "1" is written into DB7 and the address is written into DB6 to DB0 as shown above.
The address data (DB6 to DB0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed RAM.
The RAM includes DD RAM and CG RAM, and these RAMs are shared by address as shown below.

		DD RAM address
DD RAM 1-Line	:	$(00)_H$ – $(0F)_H$
DD RAM 2-Line	:	$(10)_H$ – $(1F)_H$
DD RAM 2-Line	:	$(20)_H$ – $(2F)_H$
CG RAM 1character	:	$(40)_H$ – $(47)_H$

h) Write Data to CG or DD RAM

- Write data to DD RAM

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	D	D	D	D	D	D	D	D

←Higher order bit Lower order bit→

- Write data to CG RAM

	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	*	*	*	D	D	D	D	D

←Higher order bit Lower order bit→ *=Don't Care

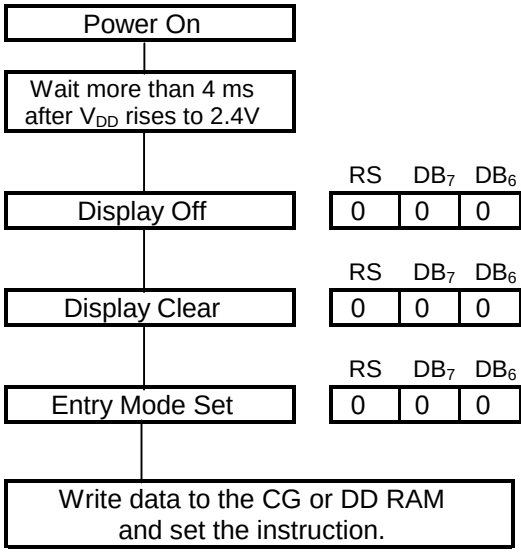
Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 5-bit data "DDDDD" are written into the CG RAM, and the binary 8-bit data "DDDDDDDD" are written into the DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(3-2) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not method, the **NJU6637** must be initialized by the instruction.



	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Display Off	0	0	0	0	0	1	0	0	0
Display Clear	0	0	0	0	0	0	0	0	1
Entry Mode Set	0	0	0	0	0	0	1	1	0

Initialized.
No display appears.

Example for set address increment and cursor right shift when the data write to the DD RAM.

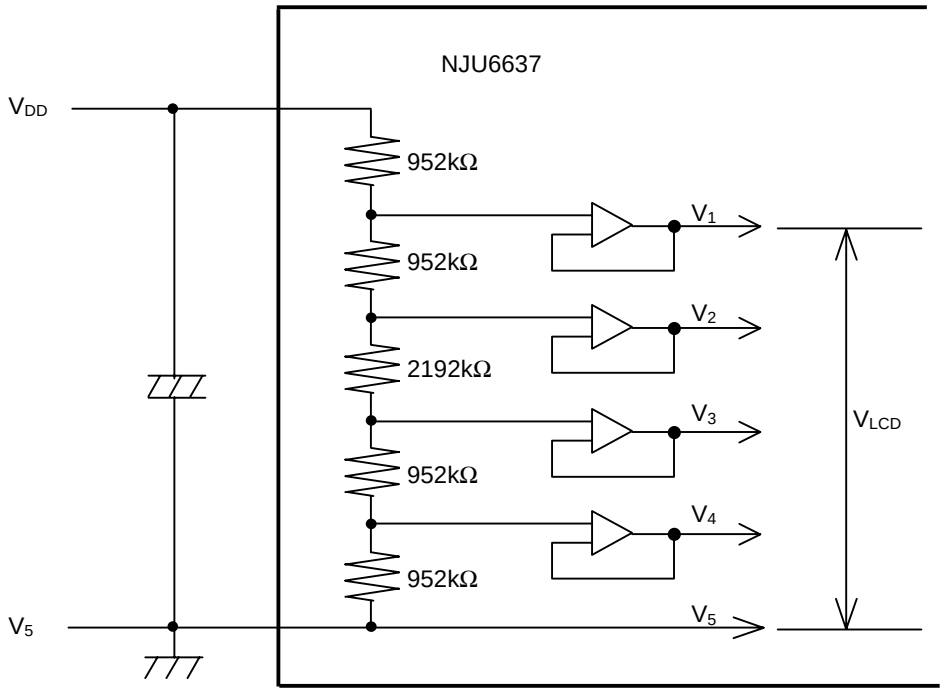
(4) Bleeder Resistance

Each LCD driving voltage (V1, V2, V3, V4) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP to get a enough display characteristics with low operating current. The bleeder resistance is set 1/6.3 bias suitable for 1/24 duty ratio and 5MΩ resistance in total. The capacitor connected between V5 and VDD is needed for stabilizing V5. The determination of the each capacitance of C1, C2 and C3 generating for LCD operating voltage, is required to operate with the LCD panel actually. The capacitance for the typical application is shown below :

LCD Driving Voltage vs. Duty Ratio

Power Supply	Duty Ratio	1/24
	Bias	1/6.3
V_5		V_{DD}-V_{LCD}

∗ The V_{LCD} is maximum swing of LCD waveform.



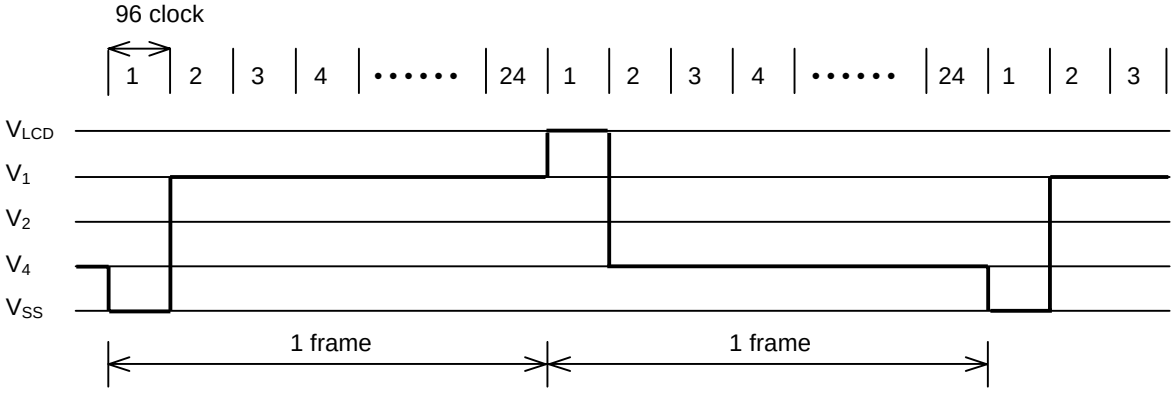
LCD Driving Voltage example

(5) Relation between oscillation frequency and LCD frame frequency.

As the **NJU6637** incorporate oscillation capacitor and resistor for CR oscillation, 145kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 145kHz oscillation.(1clock =6.875μs)

- 1/24 duty



1 frame = 6.875 (μs) x 96 x 24 = 15.84 (ms)
Frame frequency = 1 / 15.84 (ms) = 63.1 (Hz)

(6) Interface with MPU

Serial interface circuit is activated when the chip select terminal (CS) goes to "L" level. The data input is MSB first like as the order of DB7, DB6 ---- DB0.

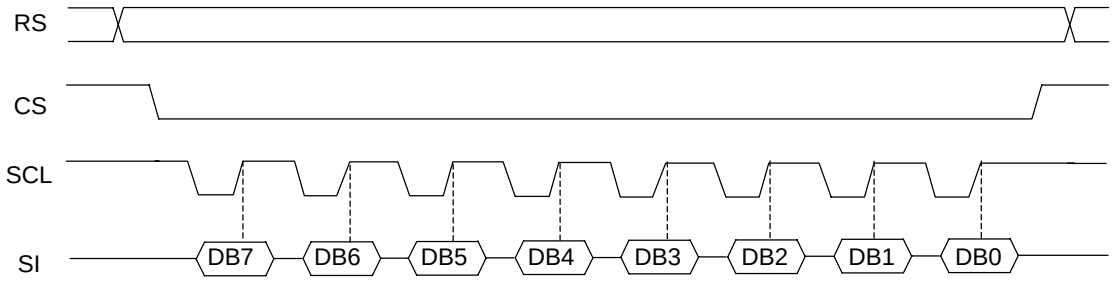
The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL.

The shift register converted to parallel data at the CS rise edge input.

In case of entering over than 8-bit data, valid data is last 8-bit data.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS terminals should be set before CS terminal goes to "L" level.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage (1)	V_{DD}	-0.3 – +7.0	V	
Supply Voltage (2)	V_{LCD}	VDD-7.0 – VDD+0.3	V	V5 Terminal
Input Voltage	V_{IN}	-0.3 – V_{DD}+0.3	V	
Operating Temperature	T_{opr}	-30 – +80	°C	
Storage Temperature	T_{stg}	-55 – +125	°C	

Note 1.) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2.) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.
Note 3.) All voltage values are specified as V_{SS} =0V
Note 4.) The relation $V_{DD}>V_5\geq V_{SS}$, V_{SS}=0V must be maintained.

■ ELECTRICAL CHARACTERISTICS

(VDD=2.4 – 3.6V, VSS=0V, Ta=25°C)

PARAMETER	SYMBOL	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Operating Volt.	V_{DD}	V_{DD}	2.4	3.0	3.6	V	
Input Voltage 1	V_{IH1}	All Input / Output Terminals except OSC1 Terminals	0.8 V_{DD}	–	V_{DD}	V	
	V_{IL1}		V_{SS}	–	0.2 V_{DD}	V	
Input Voltage 2	V_{IH2}	OSC1 Terminal	V_{DD}-0.5	–	V_{DD}	V	
	V_{IL2}		V_{SS}	–	0.5	V	
Output Voltage	V_{OH}	$-I_{OH}$=0.205mA, V_{DD}=3V	2.0	–	–	V	5
	V_{OL}	I_{OL}=1.6mA, V_{DD}=3V	–	–	0.5	V	
Driver On-resist.(COM)	R_{COM1}	$\pm I_d$=1µA, Vo= V_{DD},V5	–	–	20	kΩ	
Driver On-resist.(SEG)	R_{SEG1}	$\pm I_d$=1µA, Vo= V_{DD},V5	–	–	30	kΩ	
Driver On-resist.(COM)	R_{COM2}	$\pm I_d$=1µA, Vo= V1,V4	–	–	40	kΩ	
Driver On-resist.(SEG)	R_{SEG2}	$\pm I_d$=1µA, Vo= V2,V3	–	–	50	kΩ	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{DD}	-1	–	1	µA	6
Operating Current	I_{DD1}	VDD=3V fOSC=Internal Osc. V5=2V,during display		T.B.D.		µA	7
	I_{DD2}	VDD=3V fOSC=Internal Osc. during access, TCYCE=5us		T.B.D.		µA	
LCD Driving Voltage	V_1	V_{DD}=3V, Ta=25°C, V5=2V	2.08	2.21	2.34	V	
	V_2		1.28	1.41	1.54		
	V_3		-0.54	-0.41	-0.28		
	V_4		-1.34	-1.21	-1.08		
Oscillation Frequency	f_{OSC}	V_{DD}=3V, Ta=25°C	110	145	180	kHz	
LCD Driving Voltage	V_{LCD}	V_{DD}=3V, V_5 Terminal	V_{DD}-3	–	V_{DD}-6	V	
V5 Terminal Current	I5	V_{DD}=3V, V5=2V		200		µA	

Note 5.) Apply to the OSC2 Terminals.
Note 6.) Except pull-down resistance current. (All input terminal except OSC terminal)
Note 7.) Except Input / Output current but including the current flow on bleeder resistance.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to “H” or “L”.

■ Bus timing characteristics

(V_{DD}=2.4 – 3.6V, V_{SS}=0V, Ta=25°C)

• Serial Interface Sequence

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Serial clock cycle time		t_{CYCE}	1	–	µs	Fig.1
Serial clock width	"High" level	t_{SCH}	300	–	ns	
	Low" level	t_{SCL}	700	–	ns	
Serial clock rise and fall Time		t_{SCr}, t_{SCf}	–	20	ns	
Chip select pulse width		PW_{CS}	500	–	ns	
Chip select set up time		t_{CSU}	200	–	ns	
Chip select hold time		t_{CH}	200	–	ns	
Chip Select rise and fall Time		t_{CSr}, t_{CSf}	–	20	ns	
Address set up time		t_{AS}	200	–	ns	
Address hold time		t_{AH}	200	–	ns	
Serial input data set up time		t_{SISU}	200	–	ns	
Serial input data hold time		t_{SIH}	200	–	ns	

Serial Interface timing

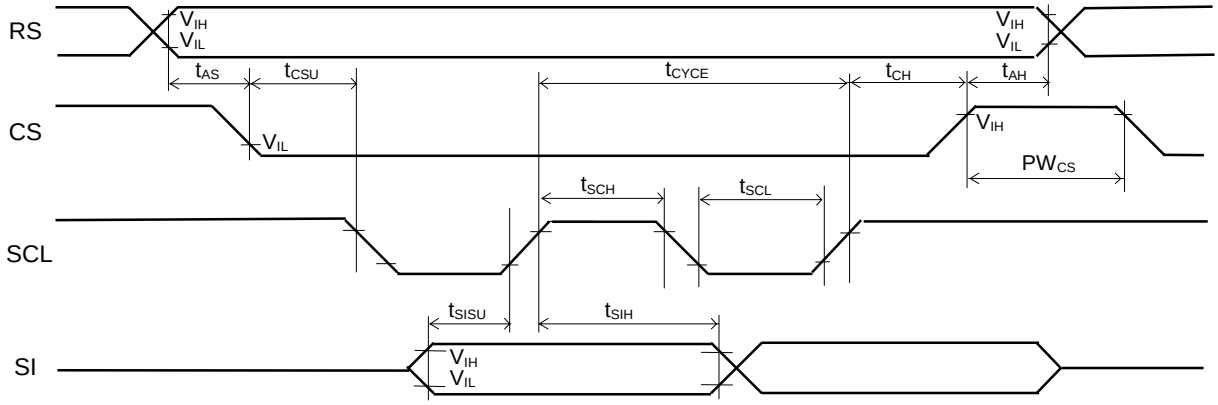
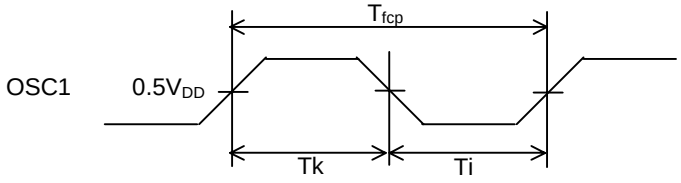


Fig.1

• External clock input

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
External clock operation Frequency	f_{CP}	110	180	KHz	Fig.2
External clock Duty	Duty	45	55	%	
External clock rise Time	t_{CPr}	–	0.2	µs	
External clock fall Time	t_{CPf}	–	0.2	µs	



$$Duty = \frac{Tk}{Tk+Ti}$$

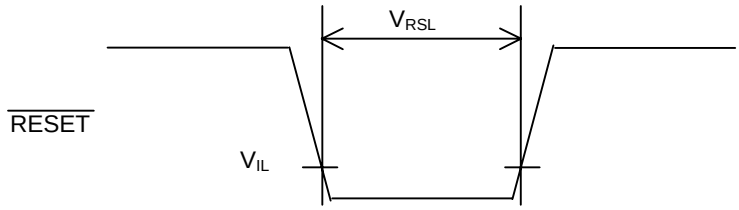
$$Tfcp = 1/fcp$$

Fig.2

• The Input Condition when using the Hardware Reset Circuit

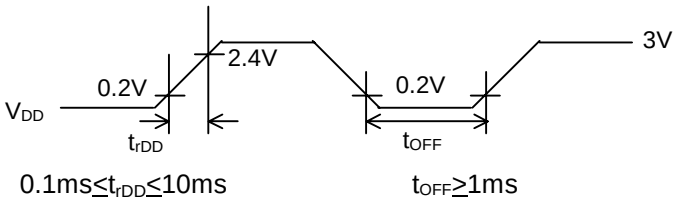
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
RESET input "Low" level width	t_{RSL}	f_{OSC} =145kHz	1.2	–	–	ms

Input timing



• Power supply condition when using the internal initialization circuit

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{rDD}	–	0.1	–	5	ms
Power supply OFF time	t_{OFF}	–	1	–	–	ms



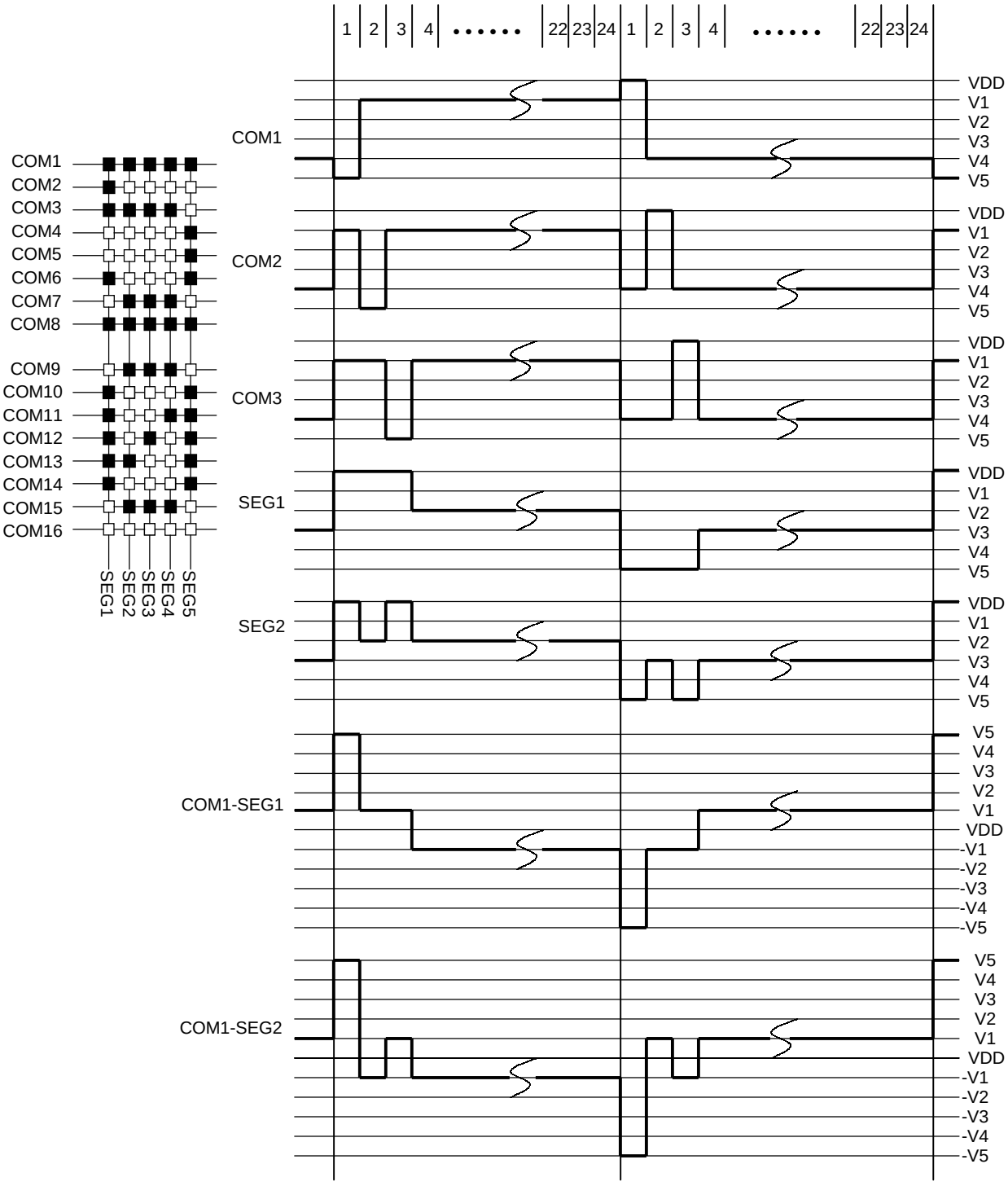
0.1ms≤t_{rDD}≤10ms t_{OFF}≥1ms

*t_{OFF} specifies the power OFF time in a short period OFF or cyclical ON/OFF

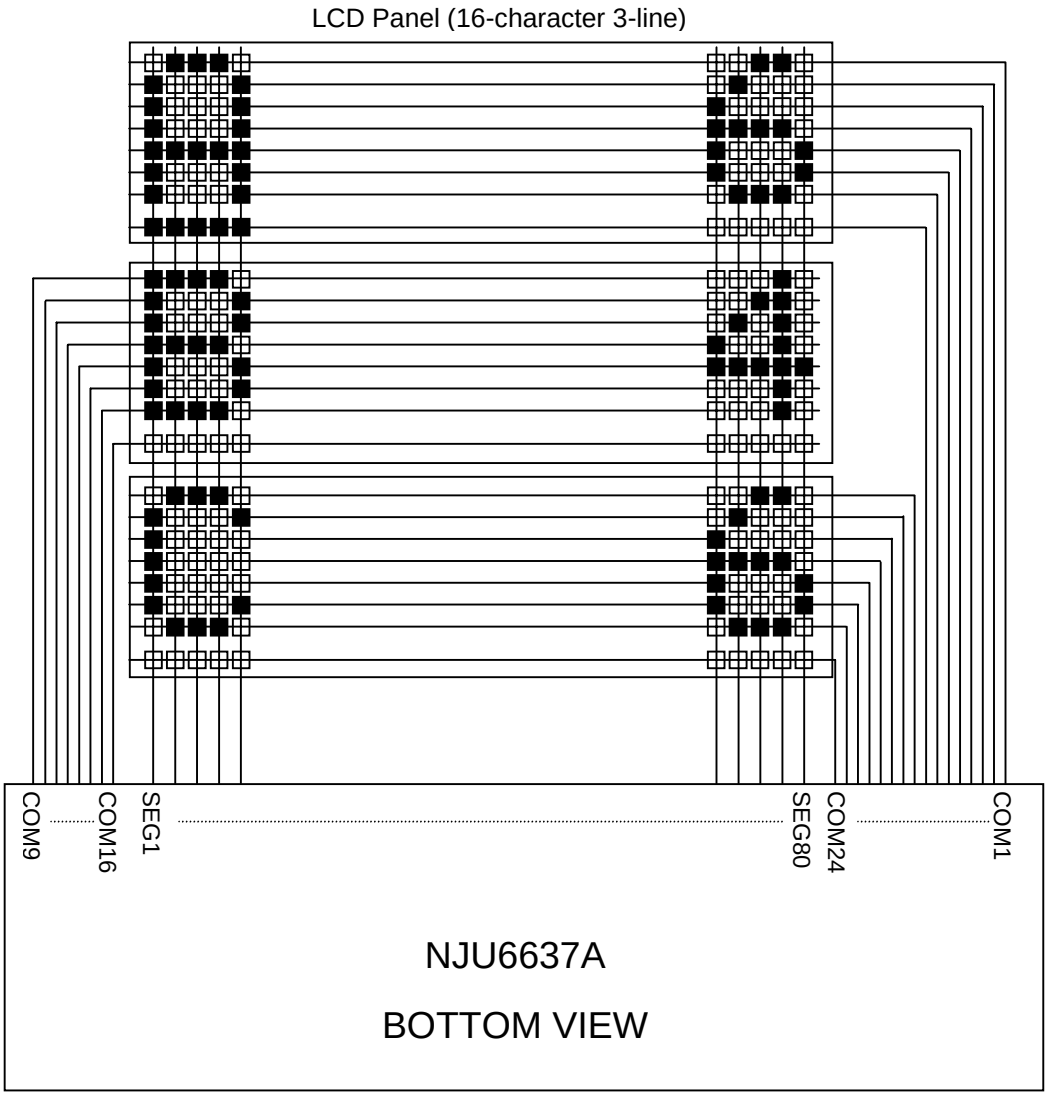
Note.) Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction(Refer to initialization by the instruction).

■ LCD DRIVING WAVE FROM

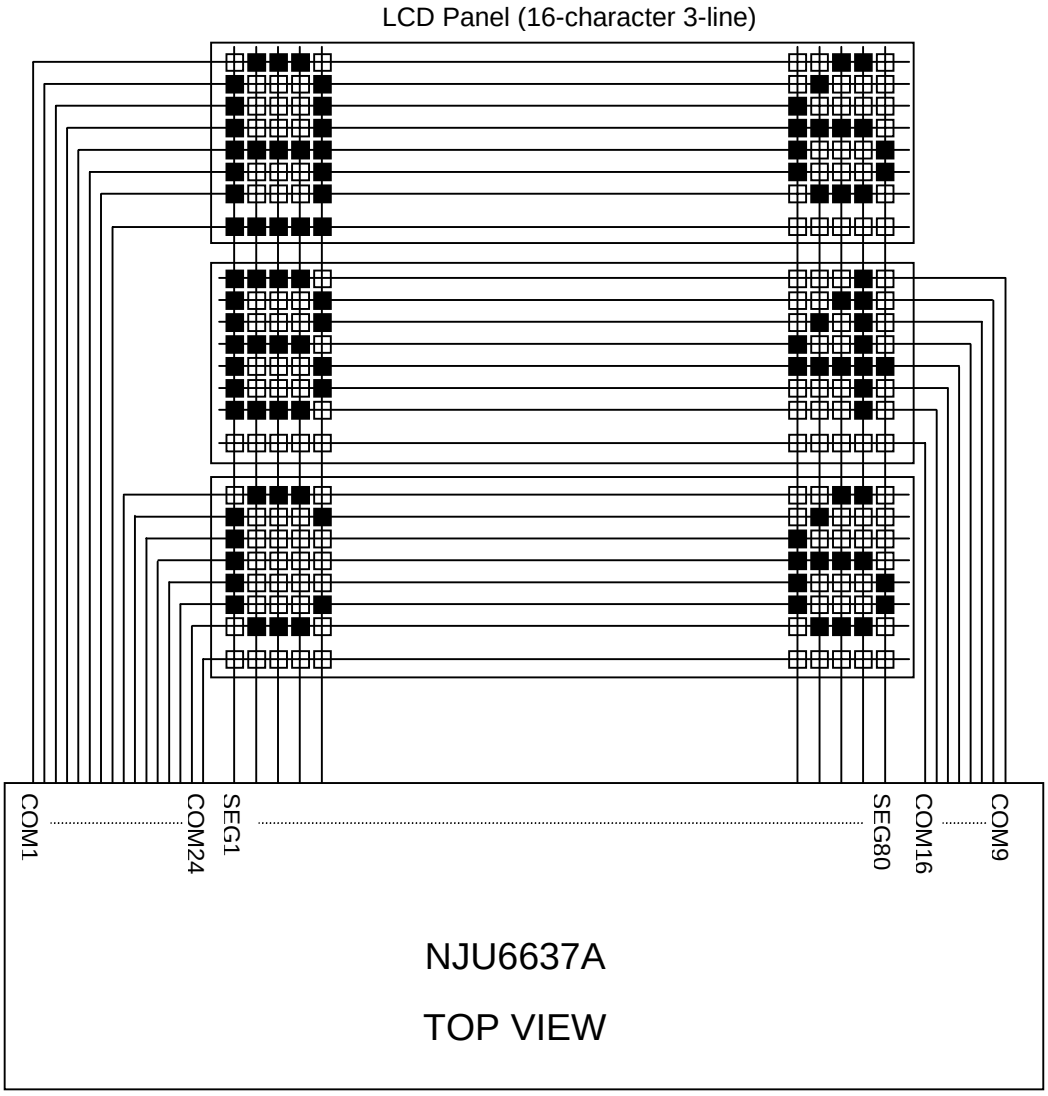
NJU6637 1/24 Duty driving



■ APPLICATION CIRCUITS



16-character 3-line Display Example
(The terminal description is “Mode A”.)



16-character 3-line Display Example
(The terminal description is “Mode B”.)

MEMO

[CAUTION]
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