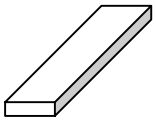
Preliminary

88-common x 272-segment Bitmap LCD Driver

■ GENERAL DESCRIPTION

The **NJU6657** is a bitmap LCD driver to display graphics or characters.
It contains 23,936 bits display data RAM, microprocessor interface circuits, instruction decoder, 88-common and 272-segment drivers.
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.
88 x 272 dots graphics or 17-character 5-line by 16 x 16 dots character with icon are displayed by **NJU6657** itself.
The NJU6657 contains a built-in OSC circuit for reducing external components.
The wide operating voltage from 2.7 to 5.5V and low operating current are suitable for battery-powered applications.

■ PACKAGE OUTLINE

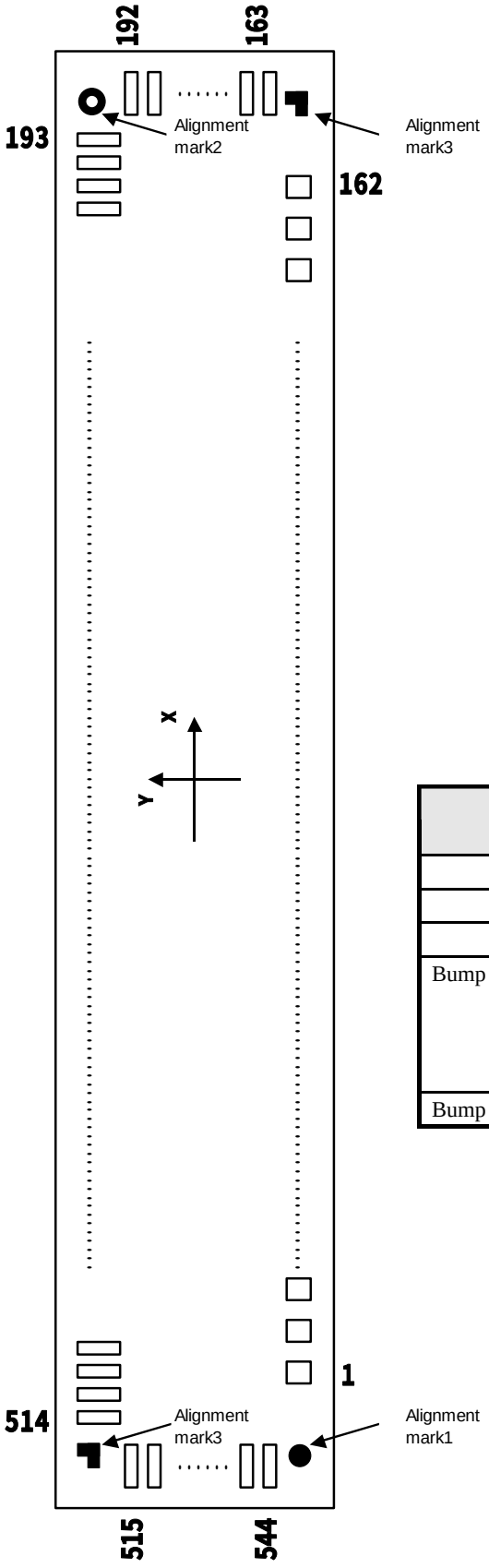


NJU6657CJ

■ FEATURES

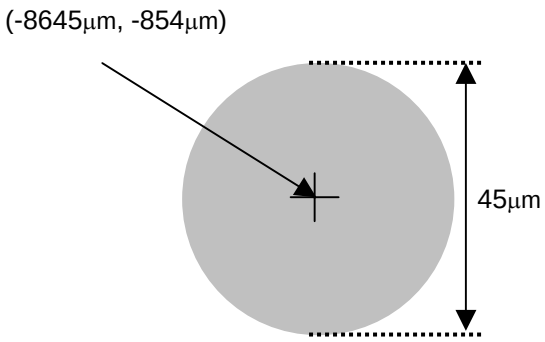
- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM – 23,936 bits
- 225 LCD Drivers – 88-common and 272-segment
- Direct Microprocessor Interface for both of 68 and 80 type MPU
- Serial Interface (SDA, SCL, A0, CSB)
- Programmable Bias selection : 1/5,1/7,1/8,1/9,1/10 bias
- Useful Instruction Set
  Display On/Off Cont, Initial Display Line Set, Page Address Set, Column Address Set, Status Read, Display Data Read/Write, ADC Select, Common Direction Register Set, Inverse Display, Entire Display On/Off, Partial Select, n-line Inverse Drive Register Set, Dummy Period Set, Read Modify Write, End, Internal Oscillation Circuit ON/OFF, Oscillation Frequency Set, Bias Select, Power Control set, EVR Register Set, Voltage Booster Circuits Multiple Select, Voltage Booster Circuits Clock Select, Temperture Sensor ON/OFF, Soft Reset, Power Save.
- Power Supply Circuits for LCD Incorporated
  Voltage Booster Circuits (12-time Maximum),
  Voltage Adjust Circuits, Voltage Follower x 4
- High Precision Voltage Regulator Incorporated (V_{REF}=±3%, Ta=25^{O}C)
- Precision Electrical Variable Resistance (400-step)
- V_{LCD} Temperature Coefficient :-0.00 to –0.15%/^{O}C
- Low Power Consumption 130uA(Typ.).
- Operating Voltage (All the voltages are based on V_{SS}=0V.)
  - Logic Operating Voltage : V_{DD}=2.7V to 5.5V
  - Voltage Booster Operating Voltage : V_{EE}=V_{DD} to 5.5V
  - LCD Driving Voltage : V_{LCD}= 4.8 to 28.8V(External Voltage: 36.0V)
- Rectangle outlook for COG
- Package Outline : Bump-chip
- C-MOS Technology (Substrate : P)

■ **PAD LOCATION**

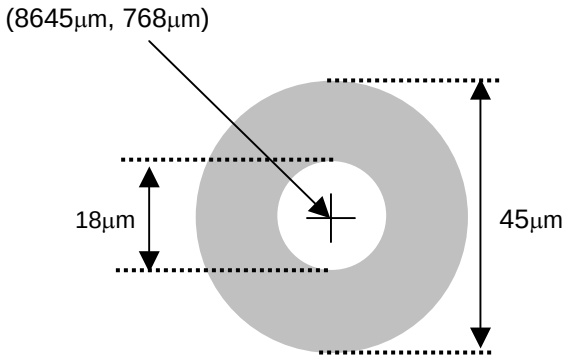


ITEM		SIZE		UNIT
		X	Y	
Chip Size		17.76	1.97	mm
Chip Tchickness		625±30		um
Bump Pich		50(min)		um
Bump Size	No. 1 to 162	79	86	um
	No. 163 to 192	122	30	um
	No. 193 to 514	30	122	um
	No. 515 to 544	122	30	um
Bump Height		17.5		um

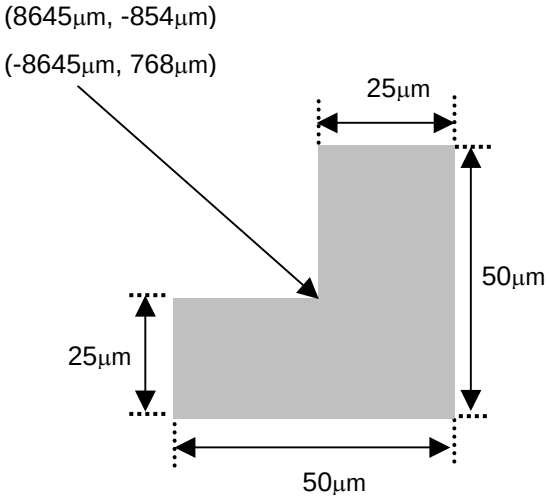
Alignment Mark 1



Alignment Mark 2



Alignment Mark 3



■ PAD COORDINATES

Chip Size 17.76 x 1.97mm(Chip Center X=0um, Y=0um)

PAD No.	Terminal	X=µm	Y=µm
1	DUMMY0	-8050	-853.8
2	DUMMY1	-7950	-853.8
3	DUMMY2	-7850	-853.8
4	DUMMY3	-7750	-853.8
5	DUMMY4	-7650	-853.8
6	DUMMY5	-7550	-853.8
7	DUMMY6	-7450	-853.8
8	BUSY	-7350	-853.8
9	DUMMY7	-7250	-853.8
10	OSC1	-7150	-853.8
11	DUMMY8	-7050	-853.8
12	DUMMY9	-6950	-853.8
13	CSB	-6850	-853.8
14	RSTB	-6750	-853.8
15	A0	-6650	-853.8
16	VPDN	-6550	-853.8
17	WRB	-6450	-853.8
18	RDB	-6350	-853.8
19	VPUP	-6250	-853.8
20	D7/SDA	-6150	-853.8
21	D6/SCL	-6050	-853.8
22	D0	-5950	-853.8
23	D1	-5850	-853.8
24	D2	-5750	-853.8
25	D3	-5650	-853.8
26	D4	-5550	-853.8
27	D5	-5450	-853.8
28	D6/SCL	-5350	-853.8
29	D7/SDA	-5250	-853.8
30	VPDN	-5150	-853.8
31	CLS	-5050	-853.8
32	VPUP	-4950	-853.8
33	CSEL	-4850	-853.8
34	VPDN	-4750	-853.8
35	SEL68	-4650	-853.8
36	VPUP	-4550	-853.8
37	PS	-4450	-853.8
38	VPDN	-4350	-853.8
39	VSS	-4250	-853.8
40	VSS	-4150	-853.8
41	VSS	-4050	-853.8
42	VSS	-3950	-853.8
43	VSS	-3850	-853.8
44	VSS	-3750	-853.8
45	VSS	-3650	-853.8
46	VSS	-3550	-853.8
47	VSSE	-3450	-853.8
48	VSSE	-3350	-853.8
49	VSSE	-3250	-853.8
50	VSSE	-3150	-853.8

PAD No.	Terminal	X=µm	Y=µm
51	VSSE	-3050	-853.8
52	VSSE	-2950	-853.8
53	VSSE	-2850	-853.8
54	VSSE	-2750	-853.8
55	VSSA	-2650	-853.8
56	VSSA	-2550	-853.8
57	VSSA	-2450	-853.8
58	VSSA	-2350	-853.8
59	VSSA	-2250	-853.8
60	VSSA	-2150	-853.8
61	VDD	-2050	-853.8
62	VDD	-1950	-853.8
63	VDD	-1850	-853.8
64	VDD	-1750	-853.8
65	VDD	-1650	-853.8
66	VDD	-1550	-853.8
67	VDD	-1450	-853.8
68	VDD	-1350	-853.8
69	VEE	-1250	-853.8
70	VEE	-1150	-853.8
71	VEE	-1050	-853.8
72	VEE	-950	-853.8
73	VEE	-850	-853.8
74	VEE	-750	-853.8
75	VEE	-650	-853.8
76	VEE	-550	-853.8
77	VST1	-450	-853.8
78	C1P	-350	-853.8
79	C1P	-250	-853.8
80	C1P	-150	-853.8
81	C1P	-50	-853.8
82	C1P	50	-853.8
83	C1P	150	-853.8
84	C1N	250	-853.8
85	C1N	350	-853.8
86	C1N	450	-853.8
87	C1N	550	-853.8
88	C1N	650	-853.8
89	C1N	750	-853.8
90	VST1	850	-853.8
91	VST1	950	-853.8
92	VST1	1050	-853.8
93	VST1	1150	-853.8
94	VST1R	1250	-853.8
95	VST1R	1350	-853.8
96	VST1R	1450	-853.8
97	VST1R	1550	-853.8
98	VDCIN	1650	-853.8
99	VDCIN	1750	-853.8
100	VDCIN	1850	-853.8

PAD No.	Terminal	X=µm	Y=µm
101	VDCIN	1950	-853.8
102	VDCOUT	2050	-853.8
103	VDCOUT	2150	-853.8
104	VDCOUT	2250	-853.8
105	VDCOUT	2350	-853.8
106	C2P	2450	-853.8
107	C2P	2550	-853.8
108	C2P	2650	-853.8
109	C2N	2750	-853.8
110	C2N	2850	-853.8
111	C2N	2950	-853.8
112	C4P	3050	-853.8
113	C4P	3150	-853.8
114	C4P	3250	-853.8
115	C6P	3350	-853.8
116	C6P	3450	-853.8
117	C6P	3550	-853.8
118	DUMMY10	3650	-853.8
119	C5P	3750	-853.8
120	C5P	3850	-853.8
121	C5P	3950	-853.8
122	C3N	4050	-853.8
123	C3N	4150	-853.8
124	C3N	4250	-853.8
125	C3P	4350	-853.8
126	C3P	4450	-853.8
127	C3P	4550	-853.8
128	VDCOUT	4650	-853.8
129	VDCOUT	4750	-853.8
130	VDCIN	4850	-853.8
131	VDCIN	4950	-853.8
132	VLCD	5050	-853.8
133	VLCD	5150	-853.8
134	VLCD	5250	-853.8
135	V1	5350	-853.8
136	V1	5450	-853.8
137	V1	5550	-853.8
138	V2	5650	-853.8
139	V2	5750	-853.8
140	V2	5850	-853.8
141	V3	5950	-853.8
142	V3	6050	-853.8
143	V3	6150	-853.8
144	V4	6250	-853.8
145	V4	6350	-853.8
146	V4	6450	-853.8
147	VSSA	6550	-853.8
148	VSSA	6650	-853.8
149	VSS	6750	-853.8
150	VSS	6850	-853.8

PAD No.	Terminal	X=µm	Y=µm
151	TEST2	6950	-853.8
152	TEST1	7050	-853.8
153	TSV	7150	-853.8
154	TEST3	7250	-853.8
155	TEST4	7350	-853.8
156	DUMMY11	7450	-853.8
157	DUMMY12	7550	-853.8
158	DUMMY13	7650	-853.8
159	DUMMY14	7750	-853.8
160	DUMMY15	7850	-853.8
161	DUMMY16	7950	-853.8
162	DUMMY17	8050	-853.8
163	DUMMY18	8596.1	-768.8
164	DUMMY19	8596.1	-718.8
165	COM43	8596.1	-668.8
166	COM42	8596.1	-618.8
167	COM41	8596.1	-568.8
168	COM40	8596.1	-518.8
169	COM39	8596.1	-468.8
170	COM38	8596.1	-418.8
171	COM37	8596.1	-368.8
172	COM36	8596.1	-318.8
173	COM35	8596.1	-268.8
174	COM34	8596.1	-218.8
175	COM33	8596.1	-168.8
176	COM32	8596.1	-118.8
177	COM31	8596.1	-68.8
178	COM30	8596.1	-18.8
179	COM29	8596.1	31.2
180	COM28	8596.1	81.2
181	COM27	8596.1	131.2
182	COM26	8596.1	181.2
183	COM25	8596.1	231.2
184	COM24	8596.1	281.2
185	COM23	8596.1	331.2
186	COM22	8596.1	381.2
187	COM21	8596.1	431.2
188	COM20	8596.1	481.2
189	COM19	8596.1	531.2
190	DUMMY20	8596.1	581.2
191	DUMMY21	8596.1	631.2
192	DUMMY22	8596.1	681.2
193	DUMMY23	8025	702.3
194	DUMMY24	7975	702.3
195	DUMMY25	7925	702.3
196	DUMMY26	7875	702.3
197	COM18	7825	702.3
198	COM17	7775	702.3
199	COM16	7725	702.3
200	COM15	7675	702.3

PAD No.	Terminal	X=µm	Y=µm
201	COM14	7625	702.3
202	COM13	7575	702.3
203	COM12	7525	702.3
204	COM11	7475	702.3
205	COM10	7425	702.3
206	COM9	7375	702.3
207	COM8	7325	702.3
208	COM7	7275	702.3
209	COM6	7225	702.3
210	COM5	7175	702.3
211	COM4	7125	702.3
212	COM3	7075	702.3
213	COM2	7025	702.3
214	COM1	6975	702.3
215	COM0	6925	702.3
216	SEG0	6875	702.3
217	SEG1	6825	702.3
218	SEG2	6775	702.3
219	SEG3	6725	702.3
220	SEG4	6675	702.3
221	SEG5	6625	702.3
222	SEG6	6575	702.3
223	SEG7	6525	702.3
224	SEG8	6475	702.3
225	SEG9	6425	702.3
226	SEG10	6375	702.3
227	SEG11	6325	702.3
228	SEG12	6275	702.3
229	SEG13	6225	702.3
230	SEG14	6175	702.3
231	SEG15	6125	702.3
232	SEG16	6075	702.3
233	SEG17	6025	702.3
234	SEG18	5975	702.3
235	SEG19	5925	702.3
236	SEG20	5875	702.3
237	SEG21	5825	702.3
238	SEG22	5775	702.3
239	SEG23	5725	702.3
240	SEG24	5675	702.3
241	SEG25	5625	702.3
242	SEG26	5575	702.3
243	SEG27	5525	702.3
244	SEG28	5475	702.3
245	SEG29	5425	702.3
246	SEG30	5375	702.3
247	SEG31	5325	702.3
248	SEG32	5275	702.3
249	SEG33	5225	702.3
250	SEG34	5175	702.3

PAD No.	Terminal	X=µm	Y=µm
251	SEG35	5125	702.3
252	SEG36	5075	702.3
253	SEG37	5025	702.3
254	SEG38	4975	702.3
255	SEG39	4925	702.3
256	SEG40	4875	702.3
257	SEG41	4825	702.3
258	SEG42	4775	702.3
259	SEG43	4725	702.3
260	SEG44	4675	702.3
261	SEG45	4625	702.3
262	SEG46	4575	702.3
263	SEG47	4525	702.3
264	SEG48	4475	702.3
265	SEG49	4425	702.3
266	SEG50	4375	702.3
267	SEG51	4325	702.3
268	SEG52	4275	702.3
269	SEG53	4225	702.3
270	SEG54	4175	702.3
271	SEG55	4125	702.3
272	SEG56	4075	702.3
273	SEG57	4025	702.3
274	SEG58	3975	702.3
275	SEG59	3925	702.3
276	SEG60	3875	702.3
277	SEG61	3825	702.3
278	SEG62	3775	702.3
279	SEG63	3725	702.3
280	SEG64	3675	702.3
281	SEG65	3625	702.3
282	SEG66	3575	702.3
283	SEG67	3525	702.3
284	SEG68	3475	702.3
285	SEG69	3425	702.3
286	SEG70	3375	702.3
287	SEG71	3325	702.3
288	SEG72	3275	702.3
289	SEG73	3225	702.3
290	SEG74	3175	702.3
291	SEG75	3125	702.3
292	SEG76	3075	702.3
293	SEG77	3025	702.3
294	SEG78	2975	702.3
295	SEG79	2925	702.3
296	SEG80	2875	702.3
297	SEG81	2825	702.3
298	SEG82	2775	702.3
299	SEG83	2725	702.3
300	SEG84	2675	702.3

PAD No.	Terminal	X=µm	Y=µm
301	SEG85	2625	702.3
302	SEG86	2575	702.3
303	SEG87	2525	702.3
304	SEG88	2475	702.3
305	SEG89	2425	702.3
306	SEG90	2375	702.3
307	SEG91	2325	702.3
308	SEG92	2275	702.3
309	SEG93	2225	702.3
310	SEG94	2175	702.3
311	SEG95	2125	702.3
312	SEG96	2075	702.3
313	SEG97	2025	702.3
314	SEG98	1975	702.3
315	SEG99	1925	702.3
316	SEG100	1875	702.3
317	SEG101	1825	702.3
318	SEG102	1775	702.3
319	SEG103	1725	702.3
320	SEG104	1675	702.3
321	SEG105	1625	702.3
322	SEG106	1575	702.3
323	SEG107	1525	702.3
324	SEG108	1475	702.3
325	SEG109	1425	702.3
326	SEG110	1375	702.3
327	SEG111	1325	702.3
328	SEG112	1275	702.3
329	SEG113	1225	702.3
330	SEG114	1175	702.3
331	SEG115	1125	702.3
332	SEG116	1075	702.3
333	SEG117	1025	702.3
334	SEG118	975	702.3
335	SEG119	925	702.3
336	SEG120	875	702.3
337	SEG121	825	702.3
338	SEG122	775	702.3
339	SEG123	725	702.3
340	SEG124	675	702.3
341	SEG125	625	702.3
342	SEG126	575	702.3
343	SEG127	525	702.3
344	SEG128	475	702.3
345	SEG129	425	702.3
346	SEG130	375	702.3
347	SEG131	325	702.3
348	SEG132	275	702.3
349	SEG133	225	702.3
350	SEG134	175	702.3

PAD No.	Terminal	X=µm	Y=µm
351	SEG135	125	702.3
352	DUMMY27	75	702.3
353	DUMMY28	25	702.3
354	DUMMY29	-25	702.3
355	DUMMY30	-75	702.3
356	SEG136	-125	702.3
357	SEG137	-175	702.3
358	SEG138	-225	702.3
359	SEG139	-275	702.3
360	SEG140	-325	702.3
361	SEG141	-375	702.3
362	SEG142	-425	702.3
363	SEG143	-475	702.3
364	SEG144	-525	702.3
365	SEG145	-575	702.3
366	SEG146	-625	702.3
367	SEG147	-675	702.3
368	SEG148	-725	702.3
369	SEG149	-775	702.3
370	SEG150	-825	702.3
371	SEG151	-875	702.3
372	SEG152	-925	702.3
373	SEG153	-975	702.3
374	SEG154	-1025	702.3
375	SEG155	-1075	702.3
376	SEG156	-1125	702.3
377	SEG157	-1175	702.3
378	SEG158	-1225	702.3
379	SEG159	-1275	702.3
380	SEG160	-1325	702.3
381	SEG161	-1375	702.3
382	SEG162	-1425	702.3
383	SEG163	-1475	702.3
384	SEG164	-1525	702.3
385	SEG165	-1575	702.3
386	SEG166	-1625	702.3
387	SEG167	-1675	702.3
388	SEG168	-1725	702.3
389	SEG169	-1775	702.3
390	SEG170	-1825	702.3
391	SEG171	-1875	702.3
392	SEG172	-1925	702.3
393	SEG173	-1975	702.3
394	SEG174	-2025	702.3
395	SEG175	-2075	702.3
396	SEG176	-2125	702.3
397	SEG177	-2175	702.3
398	SEG178	-2225	702.3
399	SEG179	-2275	702.3
400	SEG180	-2325	702.3

PAD No.	Terminal	X=µm	Y=µm
401	SEG181	-2375	702.3
402	SEG182	-2425	702.3
403	SEG183	-2475	702.3
404	SEG184	-2525	702.3
405	SEG185	-2575	702.3
406	SEG186	-2625	702.3
407	SEG187	-2675	702.3
408	SEG188	-2725	702.3
409	SEG189	-2775	702.3
410	SEG190	-2825	702.3
411	SEG191	-2875	702.3
412	SEG192	-2925	702.3
413	SEG193	-2975	702.3
414	SEG194	-3025	702.3
415	SEG195	-3075	702.3
416	SEG196	-3125	702.3
417	SEG197	-3175	702.3
418	SEG198	-3225	702.3
419	SEG199	-3275	702.3
420	SEG200	-3325	702.3
421	SEG201	-3375	702.3
422	SEG202	-3425	702.3
423	SEG203	-3475	702.3
424	SEG204	-3525	702.3
425	SEG205	-3575	702.3
426	SEG206	-3625	702.3
427	SEG207	-3675	702.3
428	SEG208	-3725	702.3
429	SEG209	-3775	702.3
430	SEG210	-3825	702.3
431	SEG211	-3875	702.3
432	SEG212	-3925	702.3
433	SEG213	-3975	702.3
434	SEG214	-4025	702.3
435	SEG215	-4075	702.3
436	SEG216	-4125	702.3
437	SEG217	-4175	702.3
438	SEG218	-4225	702.3
439	SEG219	-4275	702.3
440	SEG220	-4325	702.3
441	SEG221	-4375	702.3
442	SEG222	-4425	702.3
443	SEG223	-4475	702.3
444	SEG224	-4525	702.3
445	SEG225	-4575	702.3
446	SEG226	-4625	702.3
447	SEG227	-4675	702.3
448	SEG228	-4725	702.3
449	SEG229	-4775	702.3
450	SEG230	-4825	702.3

PAD No.	Terminal	X=µm	Y=µm
451	SEG231	-4875	702.3
452	SEG232	-4925	702.3
453	SEG233	-4975	702.3
454	SEG234	-5025	702.3
455	SEG235	-5075	702.3
456	SEG236	-5125	702.3
457	SEG237	-5175	702.3
458	SEG238	-5225	702.3
459	SEG239	-5275	702.3
460	SEG240	-5325	702.3
461	SEG241	-5375	702.3
462	SEG242	-5425	702.3
463	SEG243	-5475	702.3
464	SEG244	-5525	702.3
465	SEG245	-5575	702.3
466	SEG246	-5625	702.3
467	SEG247	-5675	702.3
468	SEG248	-5725	702.3
469	SEG249	-5775	702.3
470	SEG250	-5825	702.3
471	SEG251	-5875	702.3
472	SEG252	-5925	702.3
473	SEG253	-5975	702.3
474	SEG254	-6025	702.3
475	SEG255	-6075	702.3
476	SEG256	-6125	702.3
477	SEG257	-6175	702.3
478	SEG258	-6225	702.3
479	SEG259	-6275	702.3
480	SEG260	-6325	702.3
481	SEG261	-6375	702.3
482	SEG262	-6425	702.3
483	SEG263	-6475	702.3
484	SEG264	-6525	702.3
485	SEG265	-6575	702.3
486	SEG266	-6625	702.3
487	SEG267	-6675	702.3
488	SEG268	-6725	702.3
489	SEG269	-6775	702.3
490	SEG270	-6825	702.3
491	SEG271	-6875	702.3
492	COM44	-6925	702.3
493	COM45	-6975	702.3
494	COM46	-7025	702.3
495	COM47	-7075	702.3
496	COM48	-7125	702.3
497	COM49	-7175	702.3
498	COM50	-7225	702.3
499	COM51	-7275	702.3
500	COM52	-7325	702.3

PAD No.	Terminal	X=µm	Y=µm
501	COM53	-7375	702.3
502	COM54	-7425	702.3
503	COM55	-7475	702.3
504	COM56	-7525	702.3
505	COM57	-7575	702.3
506	COM58	-7625	702.3
507	COM59	-7675	702.3
508	COM60	-7725	702.3
509	COM61	-7775	702.3
510	COM62	-7825	702.3
511	DUMMY31	-7875	702.3
512	DUMMY32	-7925	702.3
513	DUMMY33	-7975	702.3
514	DUMMY34	-8025	702.3
515	DUMMY35	-8596.1	681.2
516	DUMMY36	-8596.1	631.2
517	DUMMY37	-8596.1	581.2
518	COM63	-8596.1	531.2
519	COM64	-8596.1	481.2
520	COM65	-8596.1	431.2
521	COM66	-8596.1	381.2
522	COM67	-8596.1	331.2
523	COM68	-8596.1	281.2
524	COM69	-8596.1	231.2
525	COM70	-8596.1	181.2
526	COM71	-8596.1	131.2
527	COM72	-8596.1	81.2
528	COM73	-8596.1	31.2
529	COM74	-8596.1	-18.8
530	COM75	-8596.1	-68.8
531	COM76	-8596.1	-118.8
532	COM77	-8596.1	-168.8
533	COM78	-8596.1	-218.8
534	COM79	-8596.1	-268.8
535	COM80	-8596.1	-318.8
536	COM81	-8596.1	-368.8
537	COM82	-8596.1	-418.8
538	COM83	-8596.1	-468.8
539	COM84	-8596.1	-518.8
540	COM85	-8596.1	-568.8
541	COM86	-8596.1	-618.8
542	COM87	-8596.1	-668.8
543	DUMMY38	-8596.1	-718.8
544	DUMMY39	-8596.1	-768.8
545			
546			
547			
548			
549			
550			

PAD No.	Terminal	X=µm	Y=µm
551			
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562			
563			
564			
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566			
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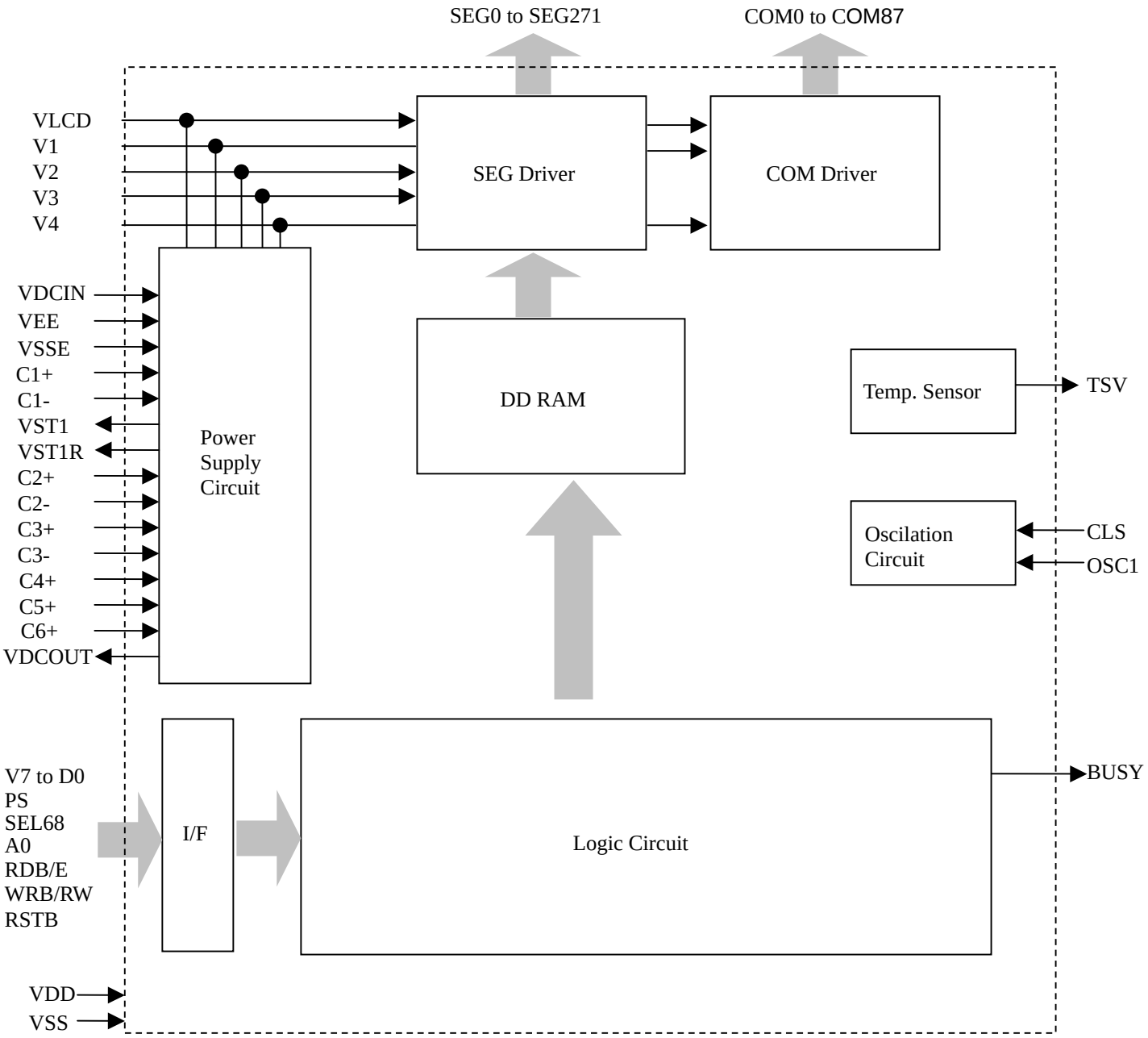
■ BLOCK DIAGRAM



■ TERMINAL DISCRIPTION(Power Supply)

No.	Symbol	I/O	FUNCTION
61 to 68	VDD	Power	Power supply Terminal
39 to 46 149, 150	VSS	GND	GND Terminal
69 to 76	VEE	Power	Voltage booster input ・When the internal voltage booster is not used, This terminal connected VDD.
47 to 54	VSSE	Power	Voltage booster input This terminal is internally connected to the VSS level.
102 to 105, 128, 129	VDCOUT	Power	2nd voltage booster output. This terminal must be connected VDCIN. When the internal voltage booster used, the capacitor between VSS terminal must be connected. Note: It recommends using 102 to 105 terminals, when the external power supply used.
98 to 101, 130,131	VDCIN	Power	Voltage booster input, This terminal connected VDCIN Note: It recommends using 98 to 101 terminals, when the external power supply used.
132 to 134	VLCD	Power/ Out	LCD driving voltage • When the internal voltage booster is not used, external LCD driving voltages (V1 to V4, VSSA and VLCD) should be supplied onto these terminals. The external voltages should be maintained with the following relationship. VDCIN≥V0≥V1≥V2≥V3≥V4≥VSSA • When the internal voltage booster is used, the capacitors between these terminals (VLCD and V1 to V4) and VSS terminal must be connected.
135 to 137	V1		
138 to 140	V2		
141 to 143	V3		
144 to 146	V4		
55 to 60, 147,148	VSSA		
78 to 83	C1P	Out	Capacitor connection terminal for the 1st voltage booster
84 to 89	C1N		
77, 90 to 93	VST1	Power/ Out	1st voltage booster output for high voltage circuits The capacitor between VSS terminal must be connected. 1st voltage booster used, 2nd voltage booster is not used: VST1=VST1R=VDCOUT=VDCIN 1st voltage booster is not used, 2nd voltage booster used: OPEN or VST1R=VST1 1st voltage booster is not used, In the case of use by a voltage regulating function of a 2nd voltage booster circuit: Please supply an external power supply from this terminal. Note: It recommends using 90 to 93 terminals, when the external power supply used. 1st and 2nd booster are not used: OPEN
94 to 97	VST1R	Power/ Out	2nd voltage booster output for high voltage circuits OPEN or The capacitor between VSS terminal must be connected. 1st voltage booster used, 2nd voltage booster is not used: VST1=VST1R=VDCOUT=VDCIN 1st voltage booster is not used, 2nd voltage booster used: Please supply an external power supply from this terminal. 1st voltage booster is not used, In the case of use by a voltage regulating function of a 2nd voltage booster circuit: The capacitor between VSS terminal must be used. 1st and 2nd booster are not used: The capacitor between VSS terminal must be connected or OPEN.

No.	Symbol	I/O	FUNCTION
106～108	C2P	O	2nd voltage boostor capacitor connection terminal
109～111	C2N		
125～127	C3P		
122～124	C3N		
112～114	C4P		
119～121	C5P		
115～117	C6P		

■ TERMINAL DESCRIPTION(FIX)

No.	Symbol	I/O	FUNCTION
19,32,36	VPUP	Power/ O	This terminal is internally connected to VDD level. ・This terminal is used to fix the VDD level. When the not used normally open.
16,30,34, 38	VPDN	Power/ O	This terminal is internally connected to VSS level. ・Thisterminal is used to fix the VSS level. When the not used normally open.

■ TERMINAL DESCRIPTION(INTERFACE)

No.	Symbol	I/O	FUNCTION
20,29	D7/SDA	I/O	Data I/O terminal In the parallel interface mode (P/S="H") D7 to D0: 8-bit bi-directional bus In the serial interface mode (P/S="L") D7: Serial data bi-directional bus(SDA) D6: Serial clk input terminal(SCL) D0 to D5: Hi-Z When CSB="H" status, the D5 to D0 terminals are in the high impedance status therefore those terminals should be fixed to VDD or VSS.
21,28	D6/SCL		
27	D5		
26	D4		
25	D3		
24	D2		
23	D1		
22	D0		
37	PS	I	Parallel / Serial interface mode select P/S ="L": Serial interface P/S ="H": Parallel interface In the serial interface mode (P/S="L") RAM Data and status read operation do not work in mode of serial intrerface.
35	SEL68	I	MPU interface type select This teminal must be fixed VDD or VSS. SEL68 =L: 80 series parallel / 3 wire-serial H:68 series parallel / 5wire-serial
13	CSB	I	Chip select Active "0" Data Input/Output are avaibal during CSB="L"
15	A0	I	Resister select ・The data on the D_0 to D_7 is distinguished between Display data and Instruction data by status of A0. A0 L: Instruction command H: Display data
18	RDB (E)	I	<In case of 80 Type MPU> (PS="H",SEL68="L") RDb signal of 80 type MPU input terminal. Active "L" During this signal is "L", D0 to D7 terminals output. <In case of 68 Type MPU> (PS="H",SEL68="H") Enable signal of 68 type MPU input terminal. Active "H"
17	WRB (R/W)	I	<In case of 80Type MPU> (PS="H",SEL68="L") Connect to the 80 type MPU WRb signal. Active "L" The data on the data bus input synchronizing the rise edge of this signal. <In case of 68 Type MPU>(PS="H",SEL68="H") The read/write control signal of 68 type MPU input terminal. RW L: Write H: Read
14	RESB	I	Reset terminal. When the RESB terminal goes to "L", the initialization is performed.

■ TERMINAL DISCRIPTION(LCD DRIVER)

<table>
<tr><th>No.</th><th>SYMBOL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>165～189,
197～215,
492～510,
518～542</td><td>C0~C87</td><td>O</td><td>LCD driving signal output terminals(Common)
Common output terminals
The following output voltages are selected by the combination of alternating (FR) signal and Common scanning data.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VLCD</td></tr>
<tr><td>L</td><td>VSS</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>216～351,
356～491</td><td>S0~S271</td><td>O</td><td>LCD driving signal output terminals(Segment)
Segment output terminals
The following output voltages are selected by the combination of alternating (FR) signal and display data in the RAM.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VLCD</td><td>V2</td></tr>
<tr><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VLCD</td></tr>
<tr><td>L</td><td>V3</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>1～7,
9,11,12,
118,
156～164,
190～196,
352～355,
511～517,
543,544</td><td>DUMMYx</td><td>-</td><td>Dummy Terminals.
Normally Open.</td></tr>
</table>

■ TERMINAL DISCRIPTION(OTHER TERMINAL)

No.	SYMBOL	I/O	FUNCTION
10	OSC1	I	External clock input terminal In internal oscillation operation, this terminal must connect to VDD or VSS.
31	CLS	I	Terminal to select whether or enable or disable the display clock internal oscillation circuit. CLS="H" : Internal oscillation circuit is enable. CLS="L" : Internal oscillation circuit is disabled. (requires external clock) When CLS="L", input the display clock through the OSC1 terminal.
33	CSEL	I	Common driver output select terminal "L" : Both sides wiring mode "H": Comb wiring mode
153	TSV	O	Thermo sensor analog voltage output terminal In case of not used, this terminal is open.
8	BUSY	O	Busy flag terminal
152	TEST1	O	TEST terminal Normaly open
151	TEST2	O	TEST terminal Normaly open
154	TEST3	I	TEST terminal Normaly open
155	TEST4	I	TEST terminal Normaly open

■ FUNCTIONAL DESCRIPTION

(1) Discription for each blocks

(1-1) Selection of Parallel or Serial interface

NJU6657 interfaces with MPU by 8-bit bi-directional data bus (D7 to D0) or serial interface(SDA, SCL).
The 8-bit parallel or serial interface is determined by a condition of the PS terminal connecting to "H" or "L" level.
The PS terminal is used to select parallel or serial interface mode as shown in the following table. In the parallel interface mode, the SEL terminal is used to select 68- or 80-type MPU interface type.
In the serial interface mode, the SEL terminal used to select 5 wire serial or 3 wire serial interfase type.
In case of the serial interface, status and RAM data read out operation is impossible.

PS	SEL	MPU type	CSB	A0	RDB	WRB	D7	D6	D5 to D0
H	H	68 type MPU	CSB	A0	E	WR	Data		
	L	80 type MPU	CSB	A0	RDB	WRB	Data		
L	H	5 wire serial	CSB	A0	-	WR	SDA	SCL	Note 1
	L	3 wire serial	CSB	-	-	-	SDA	SCL	Note 1

Note 1) "-": Fix to "VDD" or "VSS".

(1-2) Data recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the A0, RDB, and WRB(R/W) signals.

A0	68 type	80 type		Function
	RW	RDB	WRB	
L	1	0	1	Status read
L	0	1	0	Write into the Register(Instruction)
H	1	0	1	Read Display Data
H	0	1	0	Write Display Data

(1-3) Parallel interface

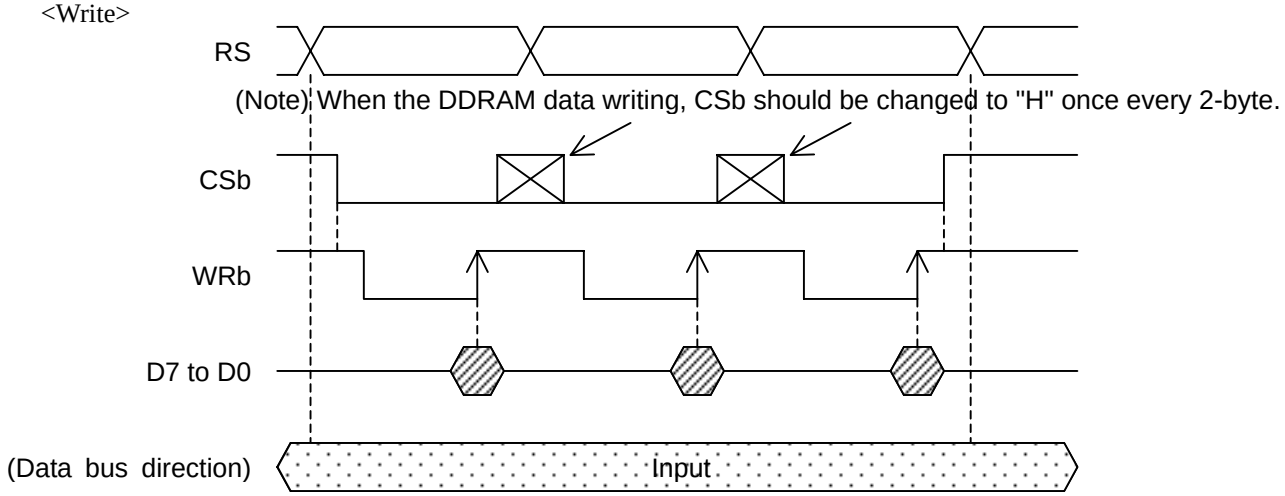
While the chip select is active (CSB="L"), the data from MPU can be written into the DDRAM or the instruction register. When the A0 is "L", the data is interpreted as display data whitch is stored in the DDRAM. The display data is latched at the rising edge of the WRB signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

A0	Data
H	Display RAM data
L	Internal command register

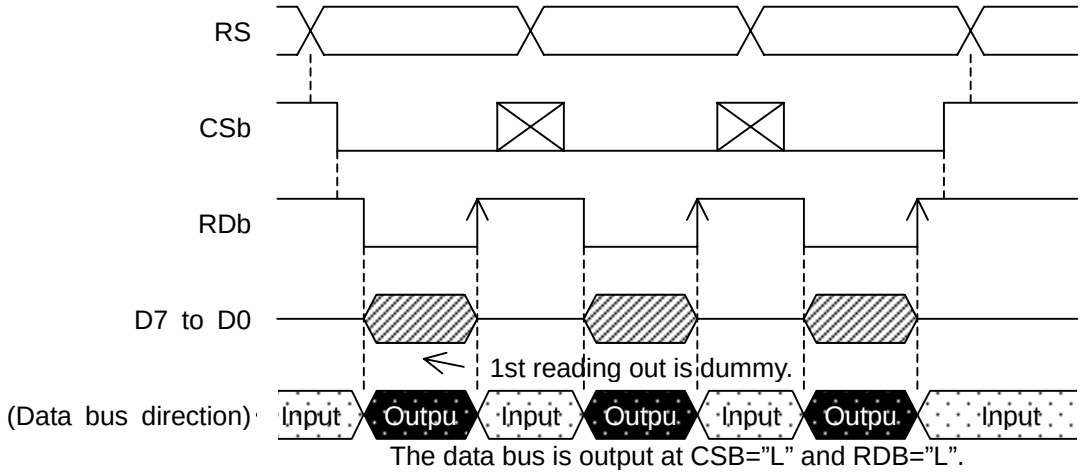
In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial inter face.

80-series parallel data transmission (PS="H", SEL68="L")

<Write>



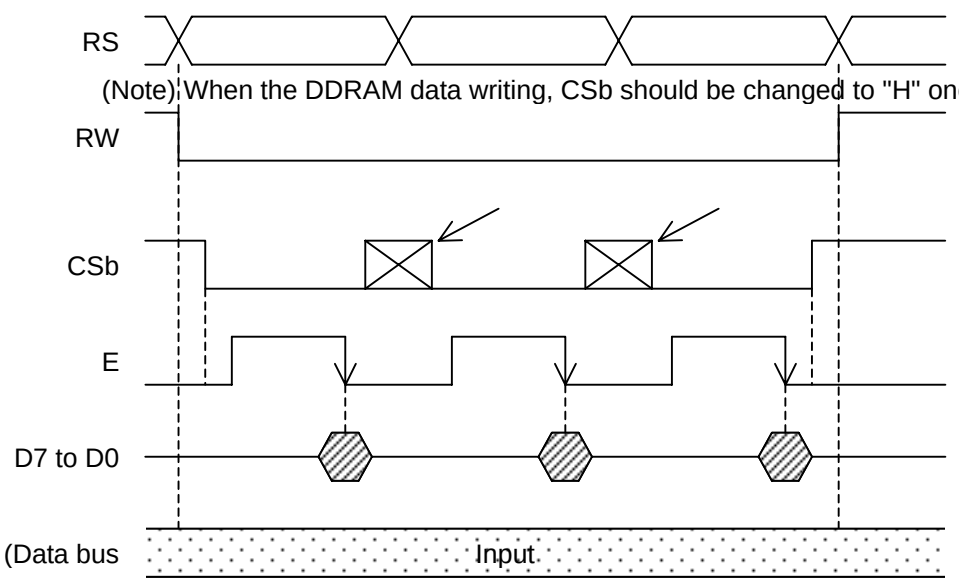
<Read>



The data bus is output at CSB="L" and RDB="L".

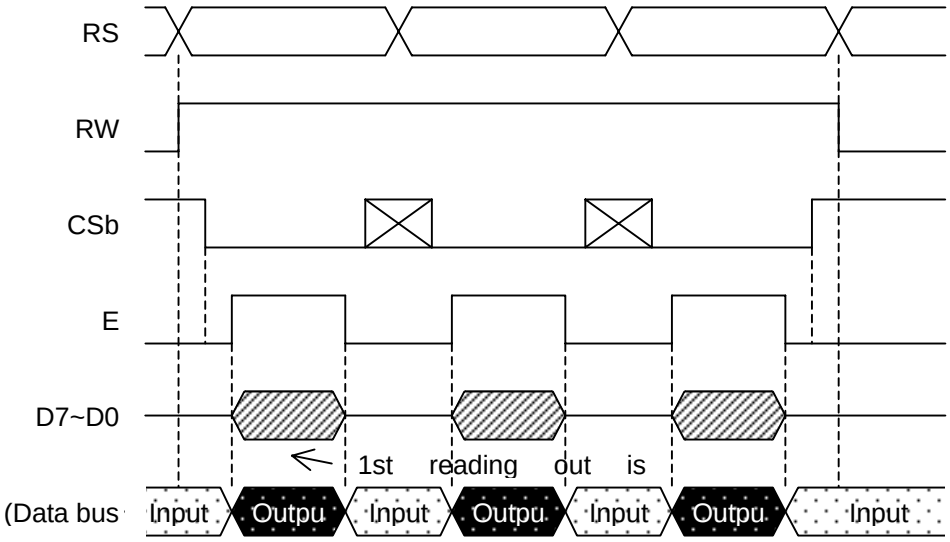
68-series parallel data transmission (PS=”H”, SEL68=”H”)

<Write>



(Note) When the DDRAM data writing, CSb should be changed to "H" once every 2-byte.

<Read>



The data bus is output at RW=”H”, CSb=”L” and E=”H”.

(1-4) 5 wire serial Interface

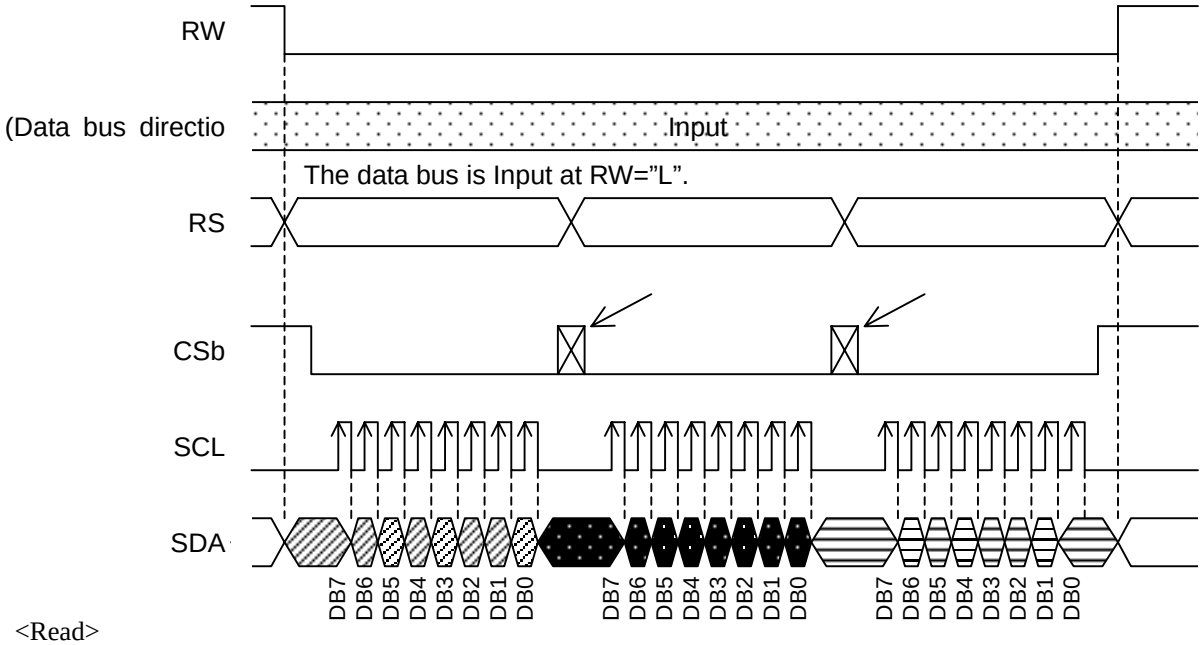
While the chip select is active (CSB="L"), the SDA and SCL are enabled. While the chip select is inactive (CSB="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initilized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D7, D6, …, and D0, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data instruction according to the A0.

A0	Data
H	Display RAM data
L	Internal command register

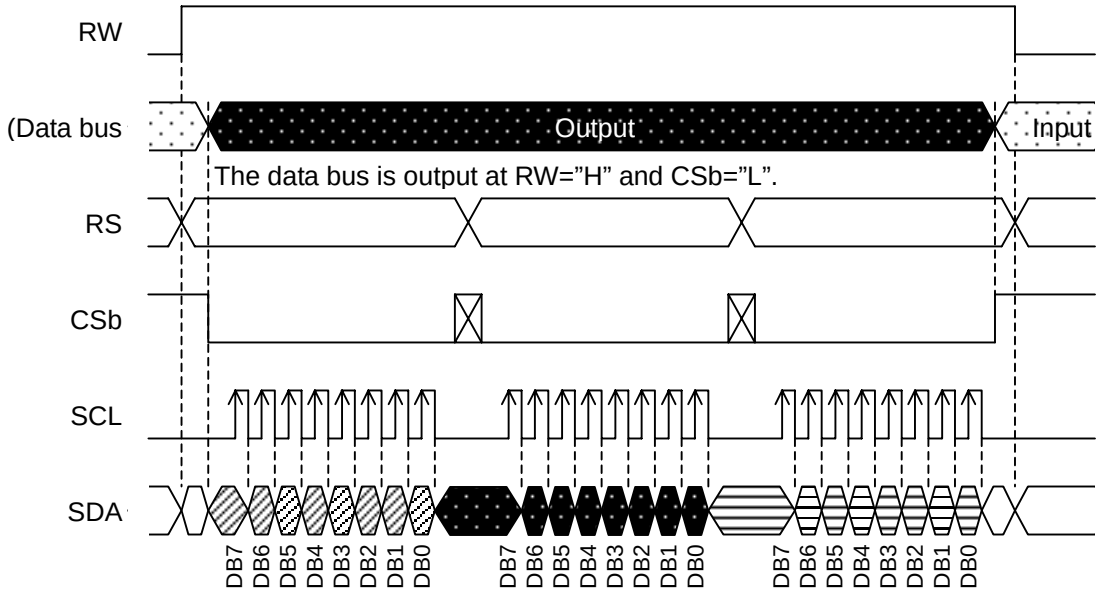
Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip select (CSB="H") temporary whenever 8-bit data transmission is completed.

Serial data transmission (PS="L", SEL="L")

<Write>



<Read>

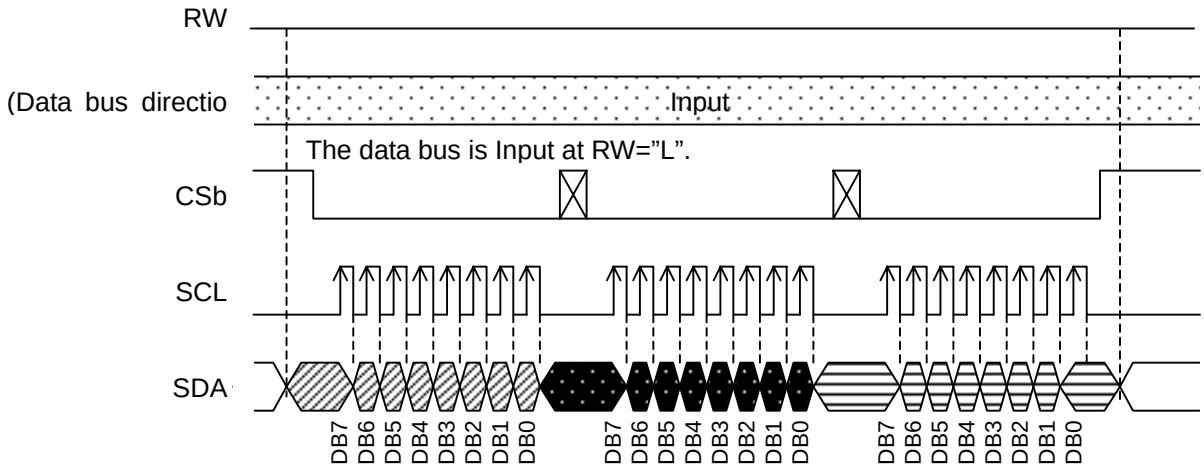


(1-5) 3 wire serial Interface

While the chip select is active (CSB=”L”), the SDA and SCL are enabled. While the chip select is not active (CSB=”H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is lached at the rising edge of the SCL signal in order of A0, D7, D6, … , and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the A0 bit status.

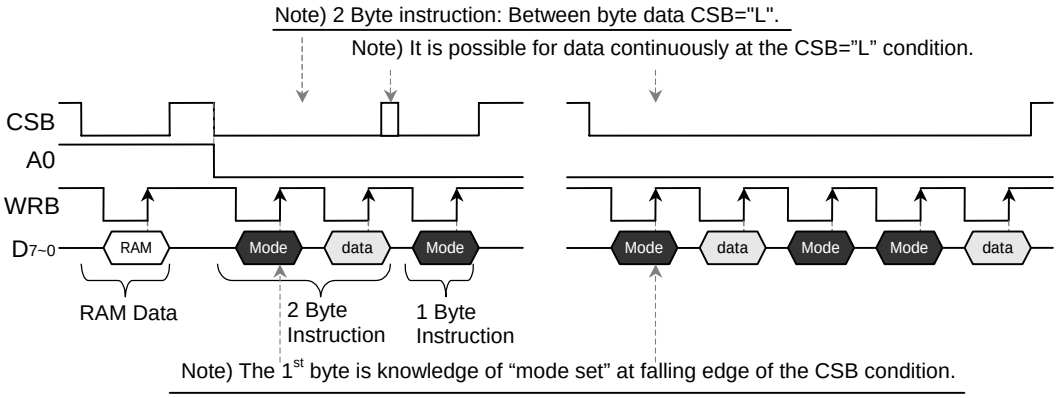
Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSB=”H”) temporary whwnever 9-bit data transmission is completed.

3wire Serial data transmission (PS=”L”, SEL=”H”)



(1-6) Write to Internal Register

The writing internal register, therre are two byte and 1byte instruction.
In two byte instruction, 1st byte specifies “Mode Set”. The relation of CSB and Data is shown in below.
And then Moreover, it is also possible to write in the instruction of plurality with CSB=L continuously, in order to judge automatically distinction of a 1-byte instruction or a 2-byte instruction inside.



(1-7) Busy Flag (BF)

While the internal circuits are operating, the busy flag(BF) is “1”, and any instruction excepting for the status read are inhibited.

The busy flag goes to “1” from D7 terminal when status read instruction is executed.

When enough cycle time over than Tcyc indicated in “AC CHARACTERISTICS” is ensured, no need to check the busy flag for reduction of the MPU loads.

(1-8) Initial display line register

The initial display line register assigns a DDRAM line address, which corresponds to COM0 by “initial display line set” instruction. It is used for not only normal display but also vertical display scrolling and page swiching without changing the contents of the DDRAM.

(1-9) Line counter

The line counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-10) Column address counter

The coulumn address counter is 8-bit pre-settable counter addressing the column address of display data RAM as shown in Fig. 1. It is incremented (+1) by the display data read / write instruction execution.

The column address counter is independent of the page register.

By the address inverse instruction, the column address decoder inverse the column address of display data RAM corresponding to the segment driver.

(1-11) Page register

The page register gives a page address of display data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required.

Page address “8”(D4 to D0 = “0100”) is Icon RAM area, the data only for the D0 is valid.

(1-12) Display data RAM

Display data RAM is the bit map RAM consisting of 23,936 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the display data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When normal display : On=”1”, Off=”0”

When inverse display : On=”0”, Off=”1”

The display data RAM outputs 272-bit parallel data in the area addressed by the line counter, and these data are set into the display data latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled to operate independently that the data rewriting does not influence with any malufunctions to the display.

Page Address	Data	Line Address	Common Driver
P3,P2,P1,P0 (0,0,0,0)	D0	00H	C80
	D1	01H	C81
	D2	02H	C82
	D3	03H	C83
	D4	04H	C84
	D5	05H	C85
	D6	06H	C86
	D7	07H	C87
P3,P2,P1,P0 (0,0,0,1)	D0	08H	C0
	D1	09H	C1
	D2	0AH	C2
	D3	0BH	C3
	D4	0CH	C4
	D5	0DH	C5
	D6	0EH	C6
	D7	0FH	C7
P3,P2,P1,P0 (0,0,1,0)	D0	10H	C8
	D1	11H	C9
	D2	12H	C10
	D3	13H	C11
	D4	14H	C12
	D5	15H	C13
	D6	16H	C14
	D7	17H	C15
	D0	18H	C16
	D1	19H	C17
		1AH	C18
		4DH	C69
	D6	4EH	C70
	D7	4FH	C71
P3,P2,P1,P0 (1,0,1,0)	D0	50H	C72
	D1	51H	C73
	D2	52H	C74
	D3	53H	C75
	D4	54H	C76
	D5	55H	C77
	D6	56H	C78
	D7	57H	C79

Column Address	ADC										
		D0="0"	000	001	002	003	004	005	006	→	10E	10F
		D0="1"	10F	10E	10D	10C	10B	10A	109	←	001	000
	Segment Drivers		0	1	2	3	4	5	6		270	271

For example the Initial display is 08H.

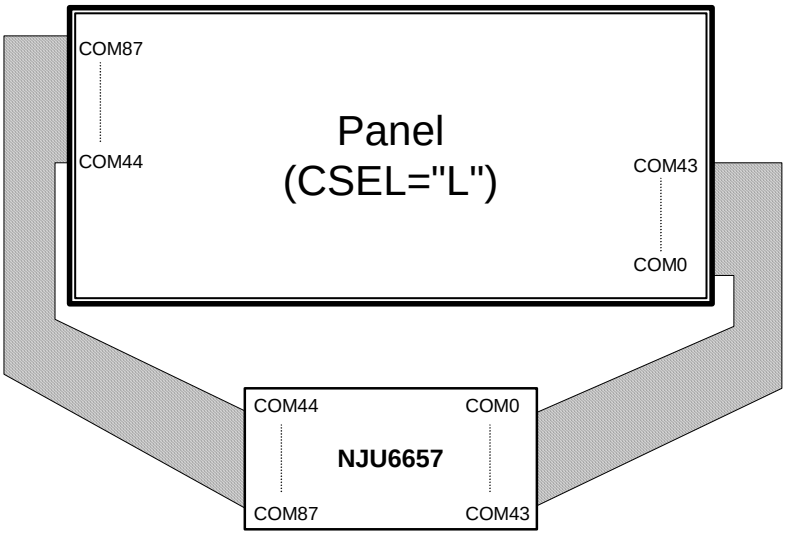
Fig.1 Display data RAM (DDRAM) Map

(1-13) COMMON DRIVER OUTPUT SWITCHING

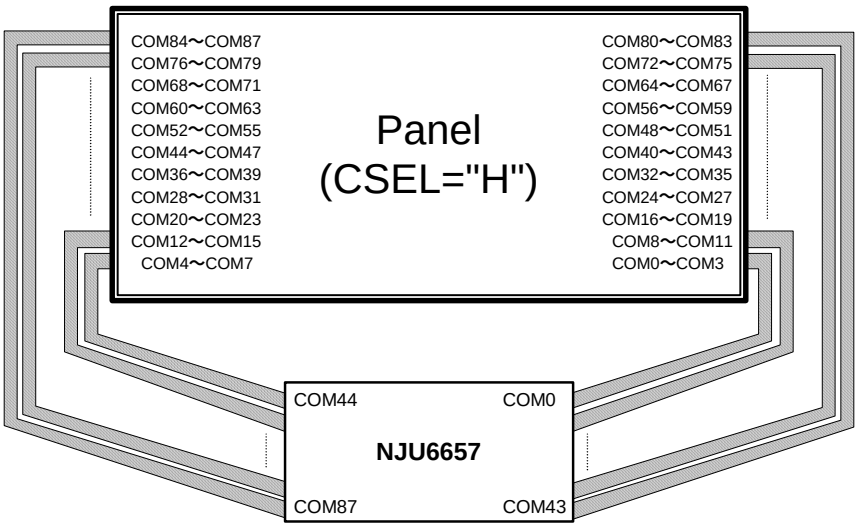
The common output order of NJU6657 is selected by CSEL terminal (Both sides wiring or Comb wiring). When the CSEL="L", the COM0 to 43 connects on the lower half of the panel and the COM44 to 87 connects on the upper half. When the CSEL="H", the COM is divided by 4, that is connected to the panel by the comb pattern.

< Wiring image >

(i) CSEL="L" Both sides wiring mode



(ii) CSEL="H" Comb wiring mode



The common direction register is selected by the "Common direction register set" is shown in Table.

Table. Common direction

INV	Status	Common direction
0	Normal	COM0 -> COM87
1	Inverse	COM87 -> COM0

(1-14)Display scroll function

NJU6657 is executed to the vertical smooth scroll display of 1-dot.

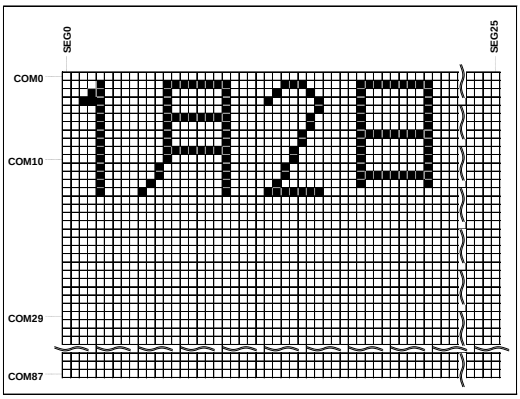
The Start line display set the line address shown Fig 1.

(1-15) Partial display function

The partial display is executed by Partial select instruction.

This function reduces the LCD driving voltage and the power consumption when the duty set low like the clock display of stand-by.

Initialize Status: 1/88 Duty



Page Address	data	Line Address
page0	D0	00h
	D1	01h
	D2	02h
	D3	03h
	D4	04h
	D5	05h
	D6	06h
	D7	07h
page1	D0	08h
	D1	09h
	D2	0Ah
	D3	0Bh
	D4	0Ch
	D5	0Dh
	D6	0Eh
	D7	0Fh
page2	D0	10h
	D1	11h
	D2	12h
	D3	13h
	D4	14h
	D5	15h
	D6	16h
	D7	17h
page3	D0	18h
	D1	19h
	D2	1Ah
	D3	1Bh
	D4	1Ch
	D5	1Dh
	D6	1Eh
	D7	1Fh
	D0	20h
	D1	21h
	·	·
	·	·
	·	·
	·	·
	D6	4Eh
	D7	4Fh
page10	D0	50h
	D1	51h
	D2	52h
	D3	53h
	D4	54h
	D5	55h
	D6	56h
	D7	57h

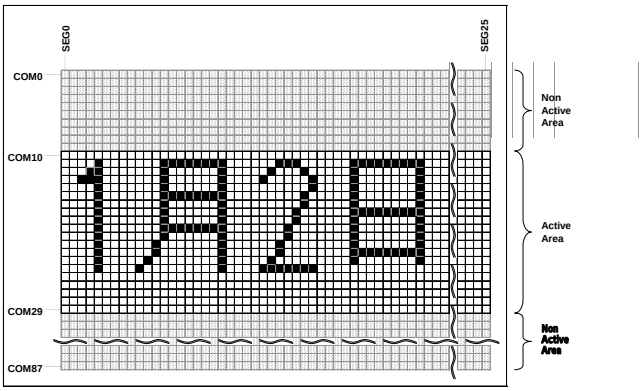
COM Start	COM Out
00h	COM0
01h	COM1
02h	COM2
03h	COM3
04h	COM4
05h	COM5
06h	COM6
07h	COM7
08h	COM8
09h	COM9
0Ah	COM10
0Bh	COM11
0Ch	COM12
0Dh	COM13
0Eh	COM14
0Fh	COM15
10h	COM16
11h	COM17
12h	COM18
13h	COM19
14h	COM20
15h	COM21
16h	COM22
17h	COM23
18h	COM24
19h	COM25
1Ah	COM26
1Bh	COM27
1Ch	COM28
1Dh	COM29
1Eh	COM30
1Fh	COM31
20h	COM32
21h	COM33
·	·
·	·
·	·
·	·
4Eh	COM78
4Fh	COM79
50h	COM80
51h	COM81
52h	COM82
53h	COM83
54h	COM84
55h	COM85
56h	COM86
57h	COM87

1/88 Duty Display

Display Area

(Example 1) Partial Select Command (Display line count="04H", COM Start position ="AH")

Partial Select Command
Display line: 04H(20-line)
COM start position 0AH(COM10) Setting.



Page Address	data	Line Address
page0	D0	00h
	D1	01h
	D2	02h
	D3	03h
	D4	04h
	D5	05h
	D6	06h
	D7	07h
page1	D0	08h
	D1	09h
	D2	0Ah
	D3	0Bh
	D4	0Ch
	D5	0Dh
	D6	0Eh
	D7	0Fh
page2	D0	10h
	D1	11h
	D2	12h
	D3	13h
	D4	14h
	D5	15h
	D6	16h
	D7	17h
page3	D0	18h
	D1	19h
	D2	1Ah
	D3	1Bh
	D4	1Ch
	D5	1Dh
	D6	1Eh
	D7	1Fh
	D0	20h
	D1	21h
	·	·
	·	·
	·	·
	·	·
	D6	4Eh
	D7	4Fh
page10	D0	50h
	D1	51h
	D2	52h
	D3	53h
	D4	54h
	D5	55h
	D6	56h
	D7	57h

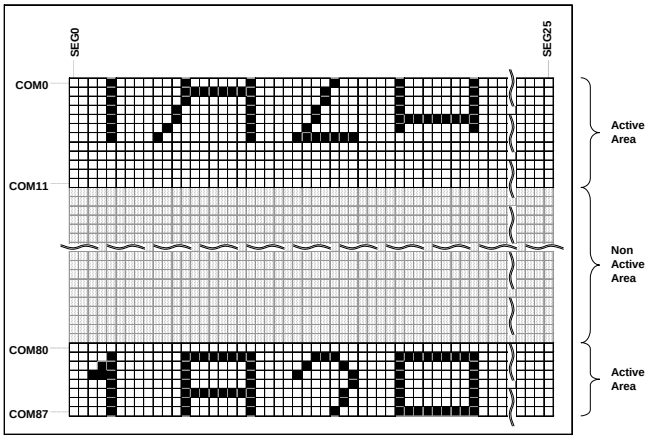
COM Start Address	COM Out
00h	COM0
01h	COM1
02h	COM2
03h	COM3
04h	COM4
05h	COM5
06h	COM6
07h	COM7
08h	COM8
09h	COM9
0Ah	COM10
0Bh	COM11
0Ch	COM12
0Dh	COM13
0Eh	COM14
0Fh	COM15
10h	COM16
11h	COM17
12h	COM18
13h	COM19
14h	COM20
15h	COM21
16h	COM22
17h	COM23
18h	COM24
19h	COM25
1Ah	COM26
1Bh	COM27
1Ch	COM28
1Dh	COM29
1Eh	COM30
1Fh	COM31
20h	COM32
21h	COM33
·	·
·	·
·	·
·	·
4Eh	COM78
4Fh	COM79
50h	COM80
51h	COM81
52h	COM82
53h	COM83
54h	COM84
55h	COM85
56h	COM86
57h	COM87

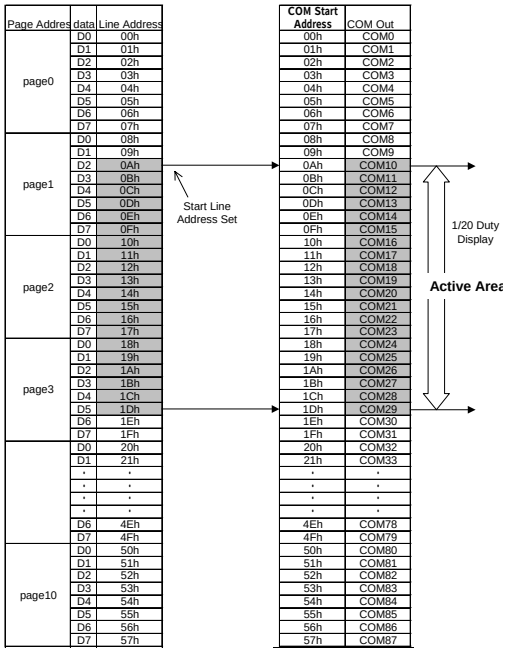
1/20 Duty Display

Active Area

(Example 2) When both of Partial Select and Initial Display line set instruction are executed, the smmoth scroll for vertical direction in partial display area.

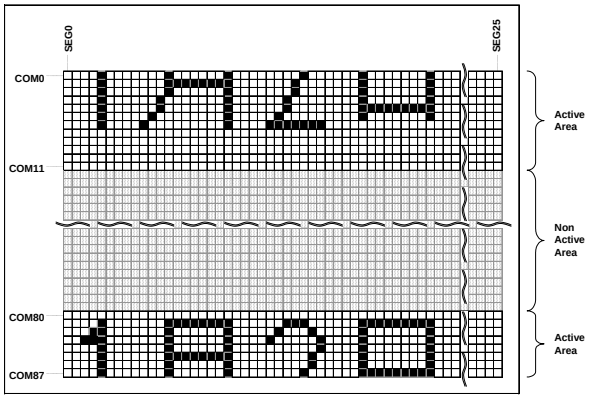
Partial Select Command
Display line: 04H(20-line)
COM start position 0AH(COM10)
Initial Display Start Line Command
Line Address: 0AH
Setting.

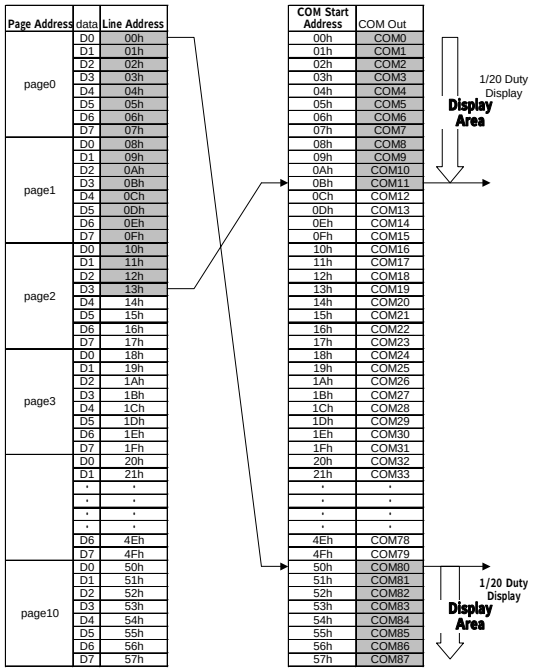




(Example 3) Partial Select Command (Display line count=”50H”, COM Start position=”AH”)

Partial Select Command
Display line: 04H(20-line)
COM start position 50H(COM80)
Initial Display Start Line Command
Line Address: 0AH
Setting.





* Duty is changed automatically when Partial Display execution, but LCD Driving Voltage , Bias ratio, EVR register are not changed. The optimum conditions should fix refering the result of actual display.

* The Dummy period Insertion position of Partial Display executed.
(Example 1) <display line count: 20-line, COM Start Position: COM10>

COM10→COM29→Dummy Time

(The dummy period is inserted in front of a COM display starting position.)

* The Dummy period Insertion position of when the overlap display and Partial Display executed.
(Example 2) <Display line count: 20-line, COM start Position: COM80>

COM80→COM87→COM0→COM11→Dummy Time

(When straddling the end of display position, the Dummy period is inserted in front of a COM display starting position.)

(1-16) Reset circuit

The reset circuit initializes the LSI to the following status by using of the reset signal into the RESB terminal.

-Reset status using the RESB terminal:

	PARAMETER	Register name	RESET status	Int. No.
1	Display ON/OFF: OFF	D	0	(1)
2	Start display line set: Set to COM0	SL6 to 0	00H	(2)
3	Page address set: Set to 0 page	PA3 to 0	0H	(3)
4	Culumn address set: Set to	AC7 to 0	00H	(4)
5	ADC select: Normal	ADC	0	(8)
6	Common direction: Normal	SCAN	0	(9)
7	Display normal/inverse: normal	REV	0	(10)
8	All display ON/OFF: OFF	ALLON	0	(11)
9	Partial select	DN6 to 0 DST6 to 0	48H 00H	(12)
10	N-line inverse ON/OFF: OFF	NLS	0	(13)
11	N-line inverse register set	MIX NL6 to 0	0 00H	(14)
12	Dummy time set	ST, DUM	0,0	(15)
13	Read modyfy write: OFF			(16)
14	Oscilator ON/OFF : ON	INTCK	1	(18)
15	Internal oscillator frequency set: 43.1kHz	SH1 to 0 OS4 to 0	10 10000	(19)
16	Bias ratio set: 1/10	BS2 to 0	000	(20)
17	Temperature coefficient: 0%/^{O}C	TC2 to 0	000	(21)
18	Power controll: DC/DC, VREG, VF	DC1 to 0 VRG VF	00 0 0	(22)
19	E.V.R set : Min.	ER8 to 0	000H	(23)(24)
20	Boost. Voltage controll function set	VU2 to 0	0H	(27)
21	Boost. Clock set	DCC2 to 0	101	(28)
22	Temp. sensor ON/OFF : OFF	TSON	0	(29)
23	Discharge ON/OFF : OFF	DIS	0	(30)
24	Power save : OFF			(33)

The RESB terminal should be connected to MPU's reset terminal, and the reset operation should be executed at the same timing of the MPU reset. As described in the "BUS TIMING CHARACTERISTICS", it is necessary to input 1.0us(min.) or over "L" level signal into the RES terminal in order to carry out the reset operation. The LSI will return to normal operation after about 1.5us(max.) from the rising edge of the reset signal.

The reset operation by RESb="L" initializes each register setting as above reset status, but the internal oscillation circuit and output terminals (D_0 to D_7) are not affected.

The reset operation is necessary to avoid malfunctions.

Note 1) The "Reset" instruction in Table.4 can't be substituted for the reset operation by using of the RESBterminal. It executes above-mentioned only 11 to 20 items.

Note 2) The reset terminal is susceptible to external noise, so design PCB layout in consideration for the noise.

Note 3) In case of using external power supply for LCD driving voltage, the RESb terminal is required to be being "L" level when the external power supply is turned-on.

(1-17) LCD driving circuits

LCD drivers consist of 88-common drivers, 272-segment divers.

As shown in "□ LCD driving waveform", LCD driving waveforms are generated by the combination of display data, common timing signal and internal FR timing signal.

(1-18) Display data latch circuit

The display data latch circuit temporally stores 272-bit display data transferred from the DDRAM in the synchronization with the common timing signal, and then it transfers these stored data to the segment drivers.

"Display on/off", "inverse display on/off" and "entire display on/off" instructions control only the contents of this latch circuit, they can't change the contents of the DDRAM.

In addition, the LCD display isn't affected by the DDRAM accuses during its displaying because the data read-out timing from this latch circuit to the segment drivers is independent of accessing timing to the DDRAM.

(1-19) Line counter and latch signal or latch Circuits

The clock line counter and latch signal to the latch circuits are generated from the internal display clock (CL). The line address of display data RAM is renewed synchronizing with display clock (CL).

272bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(1-20) Display timing generator

The display timing generates the timing signal for the display system by combination of the master clock CL and driving signal FR (refer to Fig.2) The frame signal FR and LCD alternative signal generate LCD driving waveform on the 2-frame alternative driving method or the n-line inverse driving method.

(1-21) Dummy selection period

Immediately after COM88 has been selected, the selection period equivalent to Display 1 line is provided as dummy.

Therefore, The relation between Display Lline count and Display Duty by setting of Partial Display.

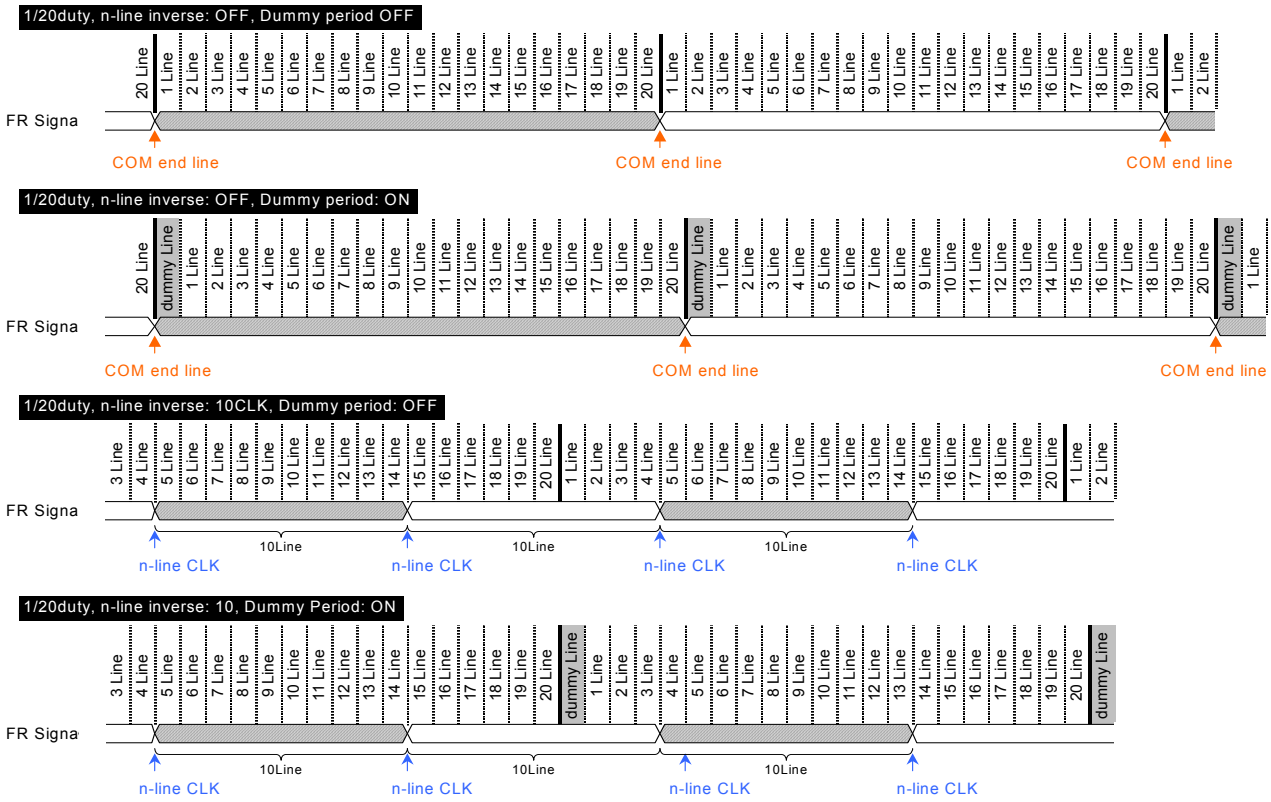
The formula is shown below.

$$Duty = \frac{1}{(CL+Dummy)} = \frac{1}{(CL+1)}$$

CL: Display line unit

(1-22) n-line inversion

NJU6657 sets the number of inversion line of the alternating signal for LCD to the optional values from 2 to 88.
The relation of the alternating signal, n-line inversion and dummy period are shown in below.



(1-23) Common timing generation

The common timing is generated by display clock CL (refer to Fig.2)

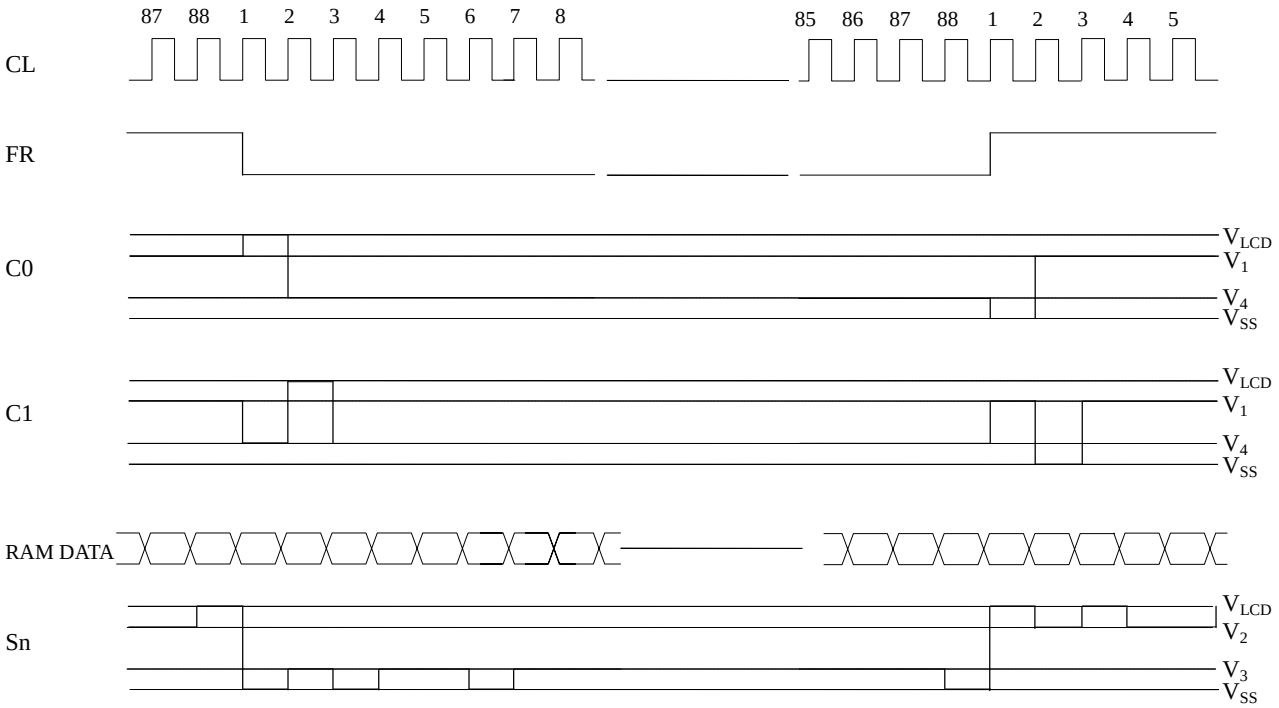


Fig.2-1 2-frame alternating drive mode(N-line inverse set OFF)

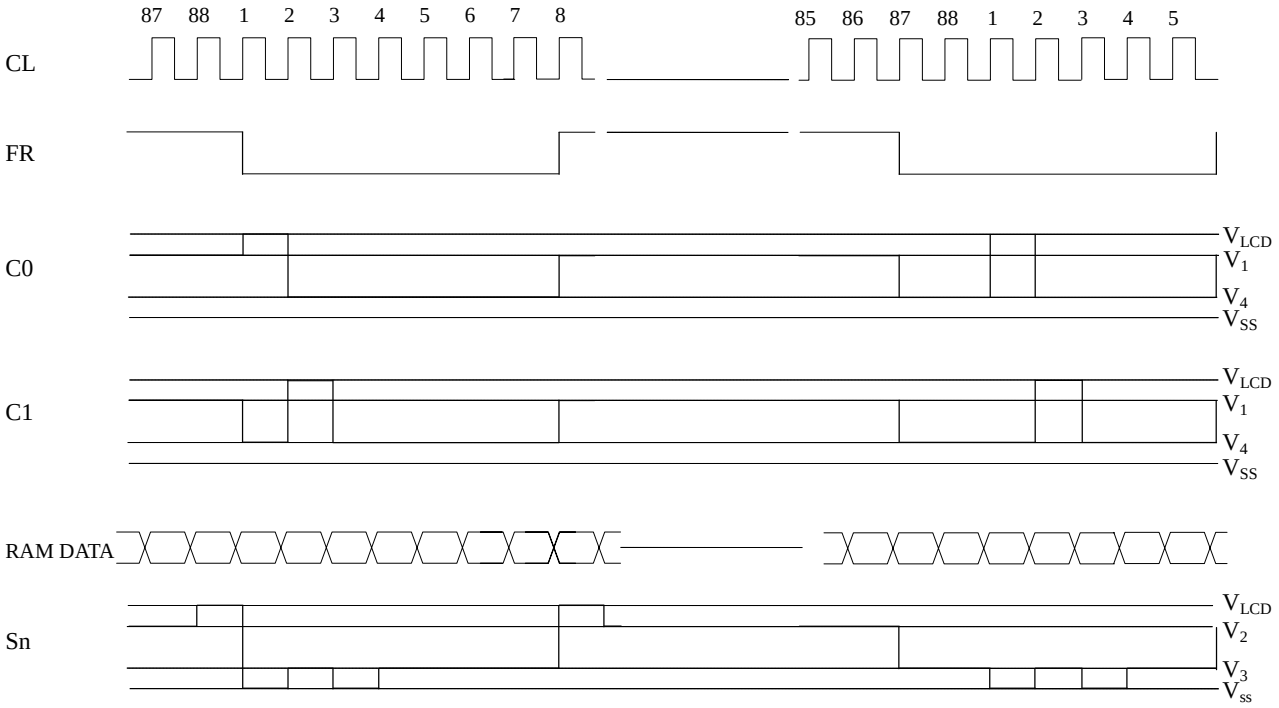


Fig.2-2 n-line inverse drive mode (n=7, line inverting register set to 6)

(1-24) OSCILLATION CIRCUIT

NJU6657 is equipped with the CR oscllation circuit, and generates internal clocks used for the display timing. The generating method of the clock selects by the internal oscillation or external clock. When the internal oscillation circuit is used, Oscillator starts after input of the Internal Oscillator ON/OFF command input. (INTCK="H")

In addition, oscillation frequency can be selected by programming the "Internal oscillation frequency control" instruction So that is possible to optimize the Display duty.

When CLS="L", oscillation stops, and display clock is input from the OSC1 terminal.

When external oscillation circuit is operating by setting CLS terminal gives priority more than the operation of the internal oscillation circuit.

CLS Terminal	INTCK	Ext. Input Status	Internal Oscillator
L	0	Available	Inactive
L	1	Available (Priority)	Active
H	0	Not available	Inactive
H	1	Not available	Active

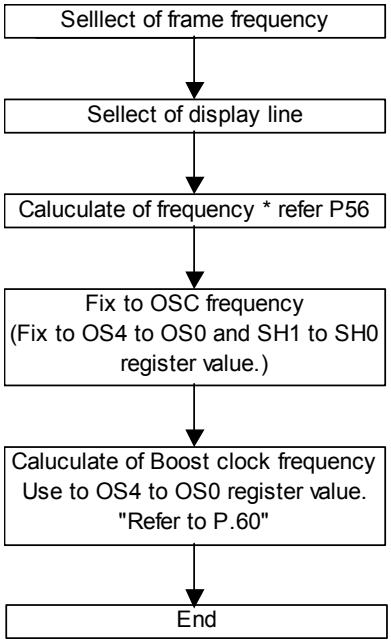
When external clock input, the divide value is reflection setting by "Interanal oscillation circuit frequency set" instruction. The divide set is normally using select by the 1 divide ("SH1 to 0 = "00")

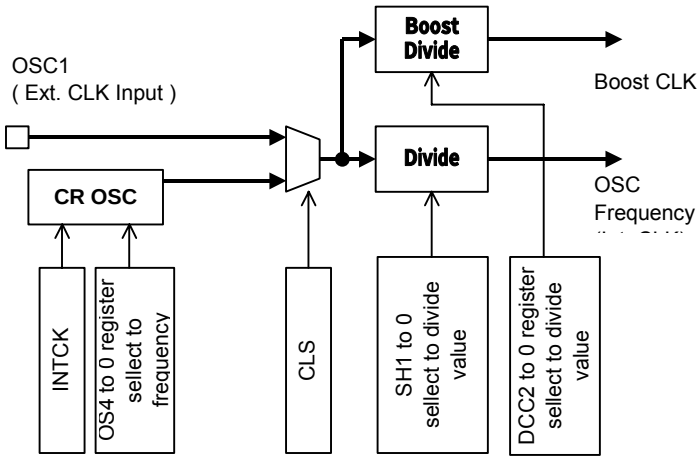
When partial display function used, the divide value changing by divide set instruction.

When frame frequency changes by partial display etc by external clock used.

You shuld be changing external clock frequency and also possible to have you change or to change oscillating frequency using a divide setup.

The set to each of frequency value is shown in below. (also in case of External CLK operation.)





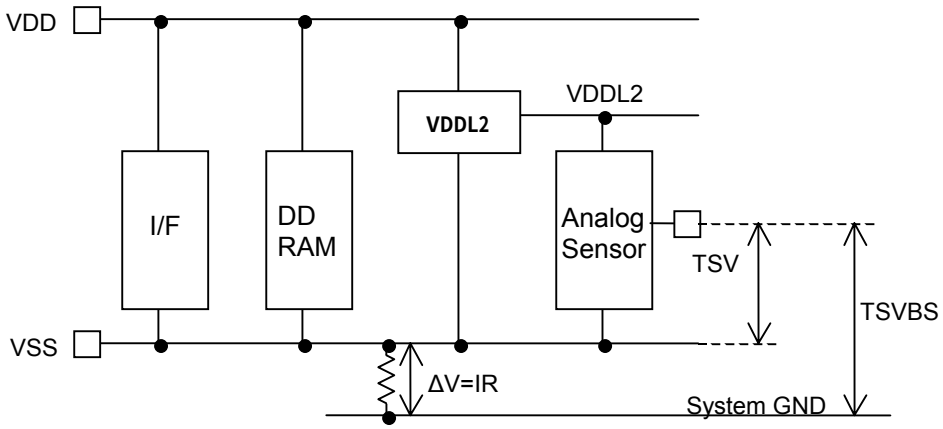
BLOCK DIAGRAM

(1-25) Thermal Sensor Circuit

The NJU6657 has the built-in thermal sensor circuit equipped with the pin to output the analog voltage, which represents the –4.19[mV/℃](typ) temprature gradient. When the TSON="1" ,from Thermal Sensor command ON/OFF.
The suitable tone LCD display is enabled in a wide temprature range by inputting the electronic control resister value sent from the MPU for the thermal sensor output value to control the LCD drive voltage.

* Note

When the resistance component R exists between the system GND and the IC's VSS terminal, the IC's substrate potential VSS viewed from the system GND drops as follows:
⊿V=IR (I: Supply Current by the NJU6657)



(1-26)Power supply circuit

The internal power circuits are composed of boost voltage converter, adjust voltage circuit and voltage followers. Each portion of the internal power circuits is controlled by "Power Control Set" instruction as shown in Table below. In addition, the combination of power supply circuits is described as shown in Table.

When the External power supply used, the bias voltage of V1 to V4 and VLCD for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, $C4^+$, $C5^+$ and $C6^+$ should be open.

When the Internal power supply used, the stabilize capacitor of V1 to V4 and VLCD should be connection.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	1	0	0	1	0	1	Mode Set
			*	*	*	*	DC1	DC0	VRG	VF	Internal Power Cont.

Power supply combinations

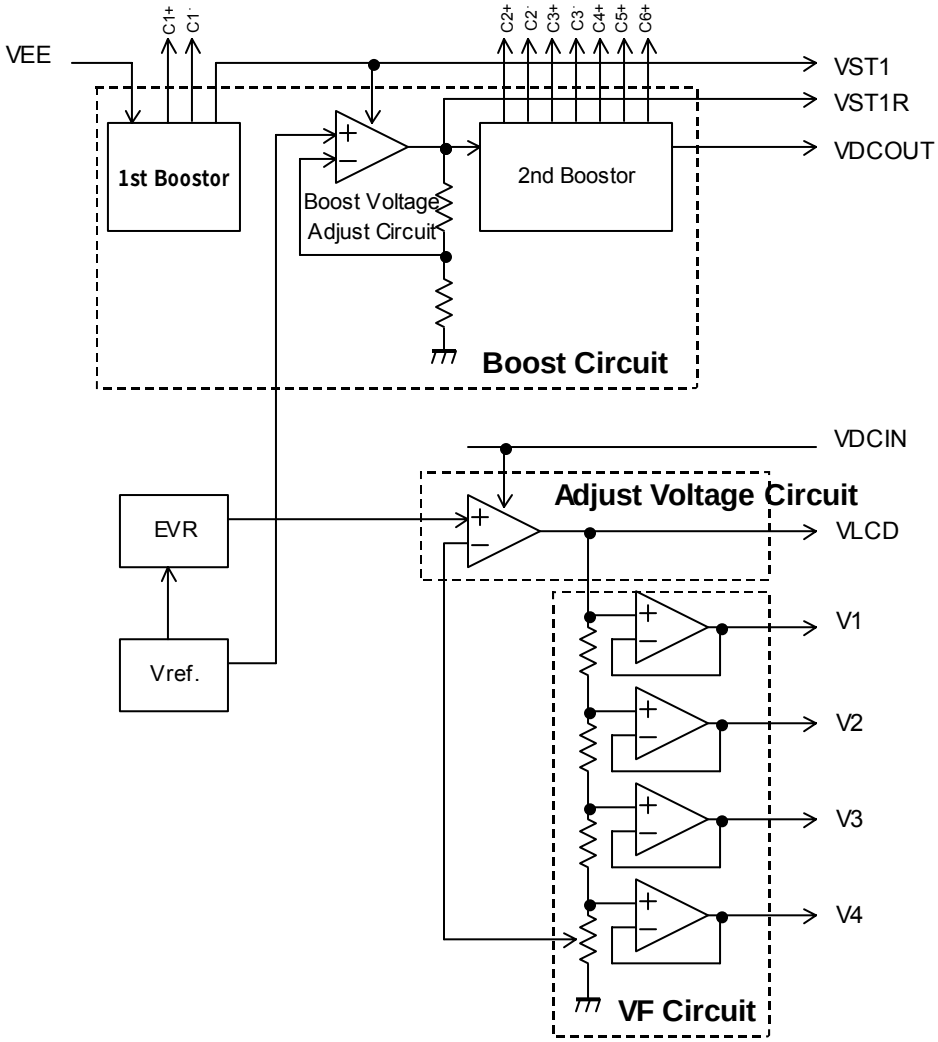
Status	DC1	DC0	VRG	VF	2^{nd} Boost	1^{st} Boost	Adjust V	VF	Ext. Power
1) All internal power supply circuit	1	1	1	1	ON	ON	ON	ON	V_{EE}
2) 1^{st} Boostor, Adjust voltage circuit and Voltage followers only	0	1	1	1	OFF	ON	ON	ON	V_{EE}
3) 2^{nd} Boostor , Adjust voltage circuit and Voltage followers only	1	0	1	1	ON	OFF	ON	ON	V_{ST1R}
4) Voltage Reg. and Voltage followers only	0	0	1	1	OFF	OFF	ON	ON	V_{DCIN}
5) Voltage followers only	0	0	0	1	OFF	OFF	OFF	OFF	V_{LCD}
6) External power supply only	0	0	0	0	OFF	OFF	OFF	OFF	V_{LCD} to V_4

* Capacitor input terminals: $C1^+$,$C1^-$,$C2^+$,$C2^-$,$C3^+$,$C3^-$,$C4^+$,$C5^+$,$C6^+$
* Do not use other combinations except examples in table Power supply combinations.

The internal LCD power supply is designed to drive small LCD panels. Thus, if the IC is used to drive a large panel, make sure whether it works with the internal power supply or needs an external power supply.

The selections of external components for the LCD bias circuit, the voltage booster and the feedback loop depend on panel sizes, so make sure what are the best values in the particular application.

■BLOCK DIAGRAM (Power Supply)



(1-27-1) Voltage Regulator Circuit

VLCD voltage genetator produces the VDCIN voltage.

The **NJU6657** has consist of voltage regulator and EVR circuit. The EVR, variable with 400-step, is used to fine-tune the LCD driving voltage (VLCD) by setting the "EVR Control Instruction".

(a) EVR

The "EVR Control Instruction" sets 9-bit data into the EVR register to determine the output voltage.

The relation of EVR register and EVR value is shown in table.

ER8	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EVR	V_{LCD}
0	0	0	0	0	0	0	0	0	0	Min.(4.8[V]) (Default)
0	0	0	0	0	0	0	0	1	1	:
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	0	0	400	Max.(28.8[V])

$$VLCD = Va + (EVR \times \Delta Vb)$$

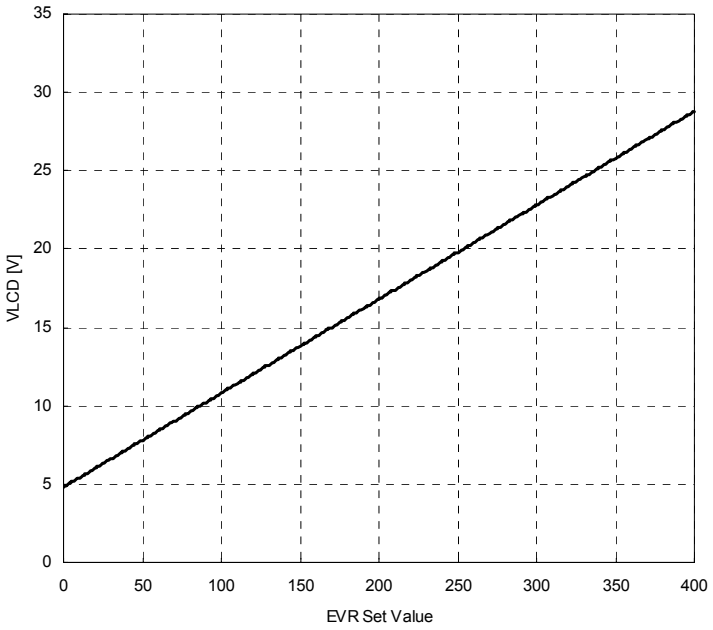
Va = 4.8[V] Default

ΔVb = 60[mV] EVR Step

* Example: EVR=250

$$VLCD = 4.8 + (250 \times 0.06) = 19.8[V]$$

The relation of EVR value and LCD driving voltage is shown in graph.



Note1) When using voltage follower circuit, you should be bigger than set to EVR=20(ER="000010100",VLCD=6[V])

(b) Temperature Gradient Selection Circuit

The circuit is used for selecting the temperature gradient characteristics of the LCD driving voltage.
The set "Temperature Gradient Slect" instruction allows selection of temperature gradient characteristics from 6 stetes.
The Teprature gradient value is refer to shown in table.
Selecting temperature gradient characteristics matching temperature characteristics to be used enables you to configure the system without an external add-on device for correcting temperature characteristics.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command
0	1	0	0	1	0	0	1	1	1	0	Mode Set
			*	*	*	*	*	TC2	TC1	TC0	Temprature Gradient Select

TC2	TC1	TC0	Temperature Gradient Value [%/℃]
0	0	0	-0.000 (Default)
0	0	1	-0.050
0	1	0	-0.075
0	1	1	-0.100
1	0	0	-0.125
1	0	1	-0.150

When using this function, you should be reviced LCD driving voltage at Ta=25^{O}C.

* Example) EVR=250, Ta=25^{O}C, Temperature Gradient Value=0,0,0
In case of changing temperature to +40^{O}C.

$$VLCD = [Va+(EVR \times \Delta Vb)] \times [1+(temp-25) \times (incline/100)]$$
$$= [4.8+(250 \times 0.06)] \times [1+(40-25) \times (-0.1/100)]$$
$$= 19.503 \text{ [V]}$$

(1-27-2) Voltage Follower Circuit

Each LCD driving voltage (V1, V2, V3, V4) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP. The bias voltage is selected by the instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Command
0	1	0	1	0	1	0	0	0	1	0	Mode Set
			*	*	*	*	*	BS2	BS1	BS0	Bias Ratio Set

BS2	BS1	BS0	Bias Ratio
0	0	0	1/10 (Default)
0	0	1	1/9
0	1	0	1/8
0	1	1	1/7
1	0	0	1/6
1	0	1	1/5
1	1	0	1/4

The external capacitor connected each of bias terminals needed for stabilizing bias voltage.
And the value of capactors are determined depending on the actual LCD panel display evaluation.

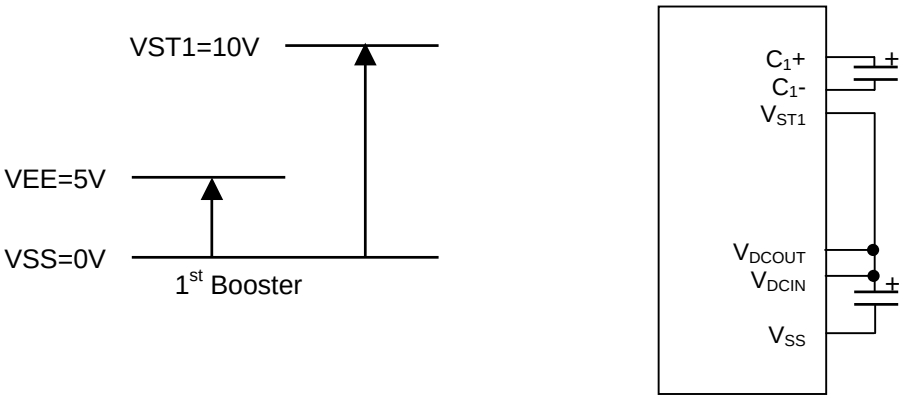
(1-27-3) Voltage boost Circuit

(a) 1st Boost Circuit (2-time Boost)

The 1st Boost circuit outputs the positive Voltage(VSS Common) boosted 2 times of VEE-VSS from the VST1 terminal with connecting the two capacitors between C1+ and C1-, VST1 and VSS.

The purpose of 1st Boost circuit is two reason, 1st is input voltage less than 5V or Using 2nd Boost circuit depends on voltage shortage. The 1st Boost circuit only used, the VST1 terminal with connecting VDCOUT and VDCIN outside.

-External Capacitor Connection of 1st Voltage Booster

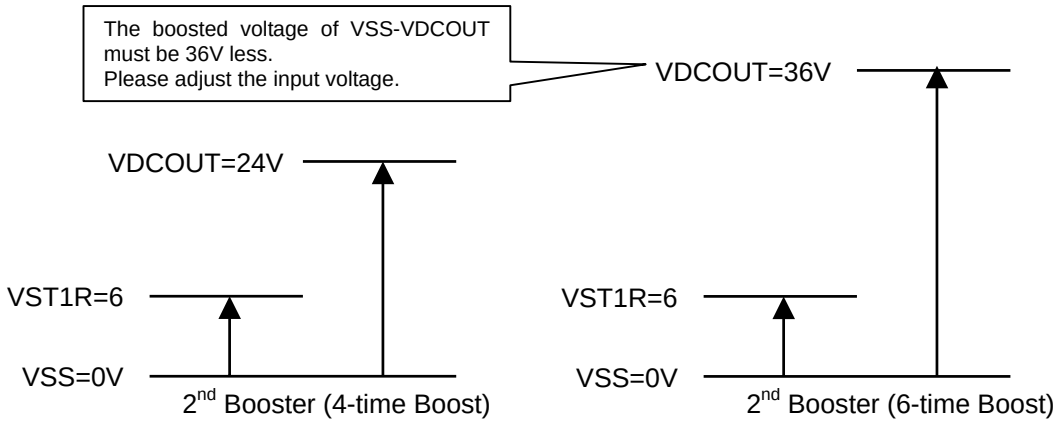


(b) 2nd Booster Circuit (6-time Boost)

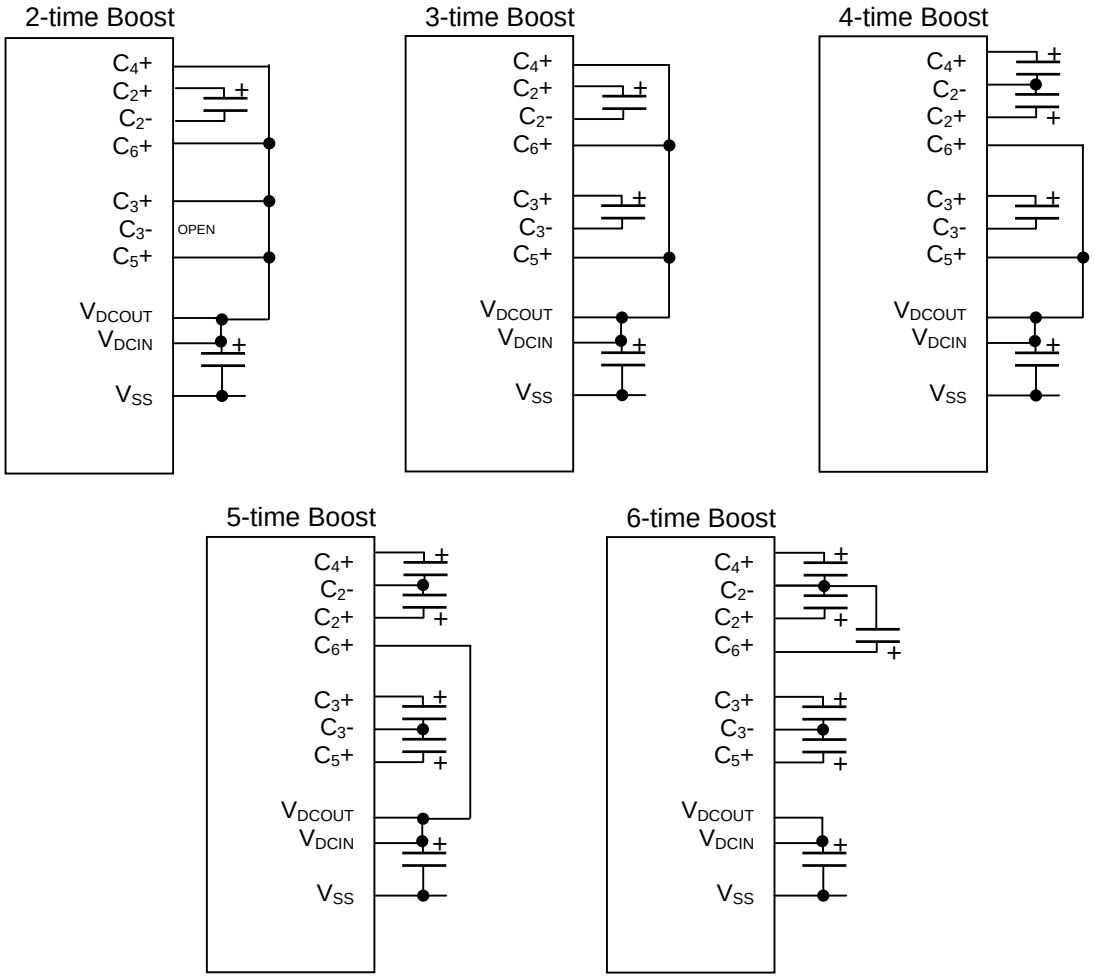
The 2nd Boost circuit outputs the positive Voltage(VSS Common) boosted 6 times of VST1-VSS from the VDCOUT terminal with connecting the six capacitors between C2+ and C2-, C3+ and C3-, C4+ and C2-, C5+ and C3-, C6+ and C2-, and VSS and VDCOUT. The boosting time is selected out of 2 times to 6 by changing the external capacitors connection.

The VDCOUT and VDCIN terminal should be connecting outside.

When the input voltage of voltage boost circuit is over than 5.5V, the 2nd boost circuit should be using only.



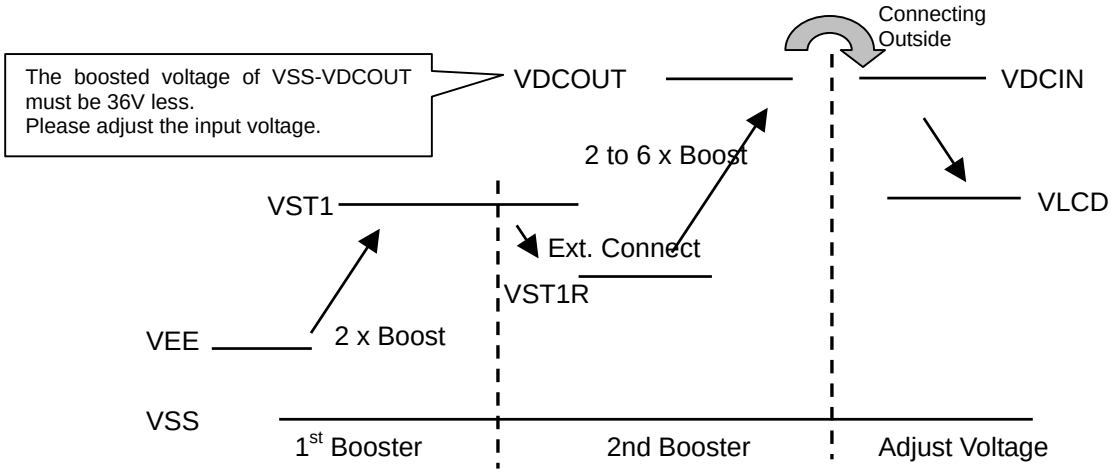
- External Capacitor Connection of 2nd Voltage Booster (Power Supply = VST1R)



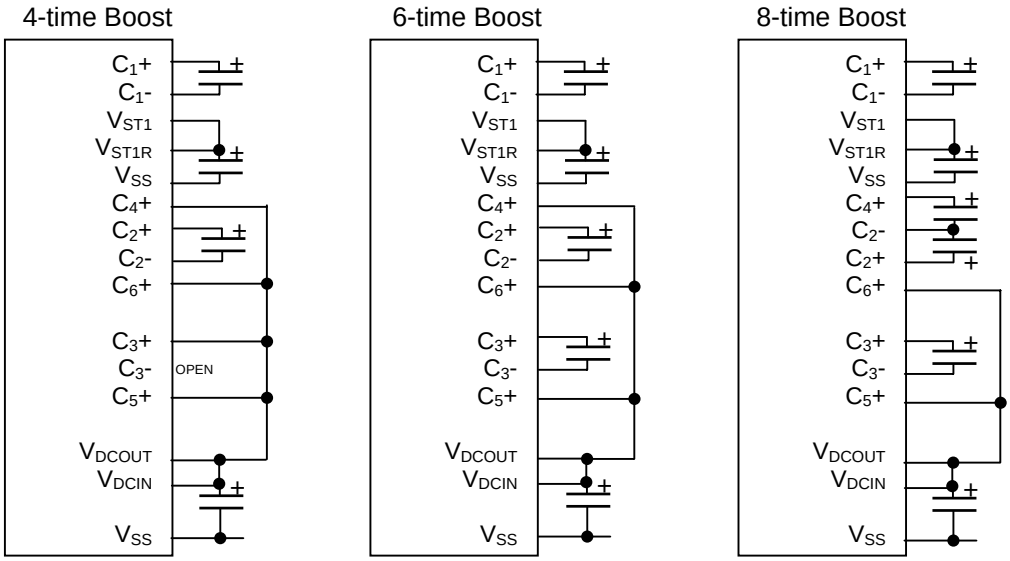
(c) Combination using of 1st boost and 2nd boost circuit

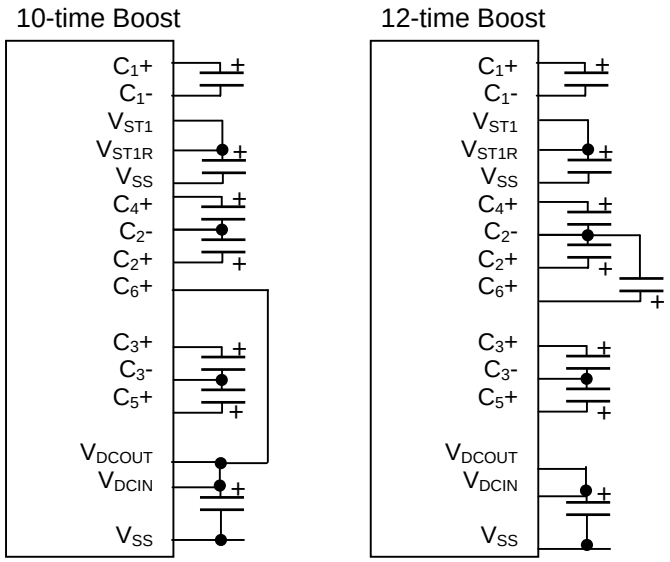
The combination of 1st boost and 2nd boost circuits the positive voltage(VSS common) boosted 4 to 12 times of VEE-VSS from the VDCOUT terminal with connecting outside the VST1 and VST1R , VDCOUT and VDCIN terminals.

The relation of 1st boost circuit, 2nd boost circuit and Voltage adjust circuit is shown in below.



-External Capacitor Connection of Voltage Booster





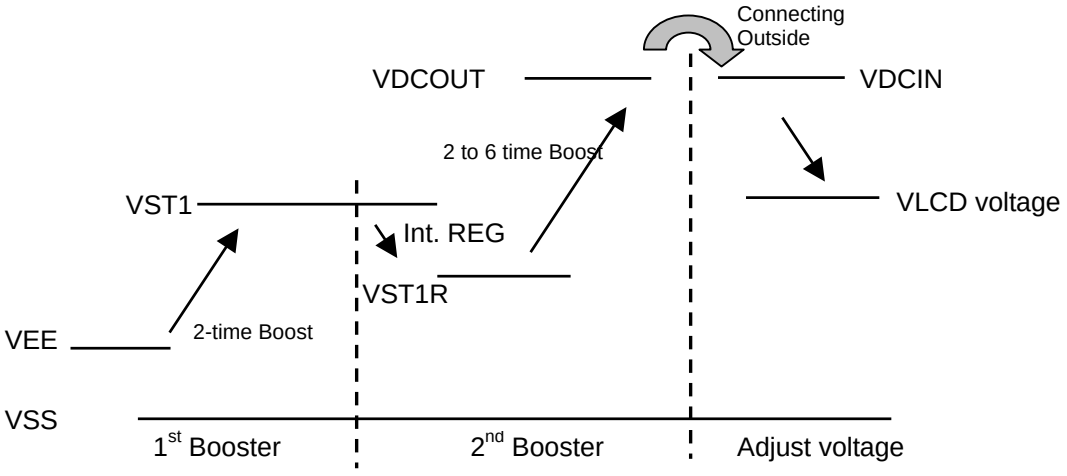
(d) Adjust voltage boost function

The Adjust voltage boost circuit generates VST1R voltage by Adjust voltage boost set instruction.
Register value(VU2 to VU0) should be setting of according to use 2nd Booster condition.
When the this function used, using of 2nd Boost circuit and combination of 1st and 2nd Boost circuits.
The combination of the auto control function can't used.
In using 2nd boost circuit only, the input voltage input to VST1 terminal. In using combination of 1st boost and 2nd boost circuit used, the input voltage input to VEE terminal. In this time , each of the connect to capacitor between VST1, VST1R and VSS terminals.
This function controls 2nd booster output voltage less than Maxmum voltage (36V)
If this function is used, it can set up VEE and VST1 voltage without considering Maxmum voltage.
This function is control by set to command "Adjust voltage boost instruction".
The register value (VU2 to 0) set are before starting of 2nd boost circuit.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Instruction
0	1	0	1	0	0	0	1	1	0	1	Mode Set
			*	*	*	*	*	VU2	VU1	VU0	Adjust Boost Voltage

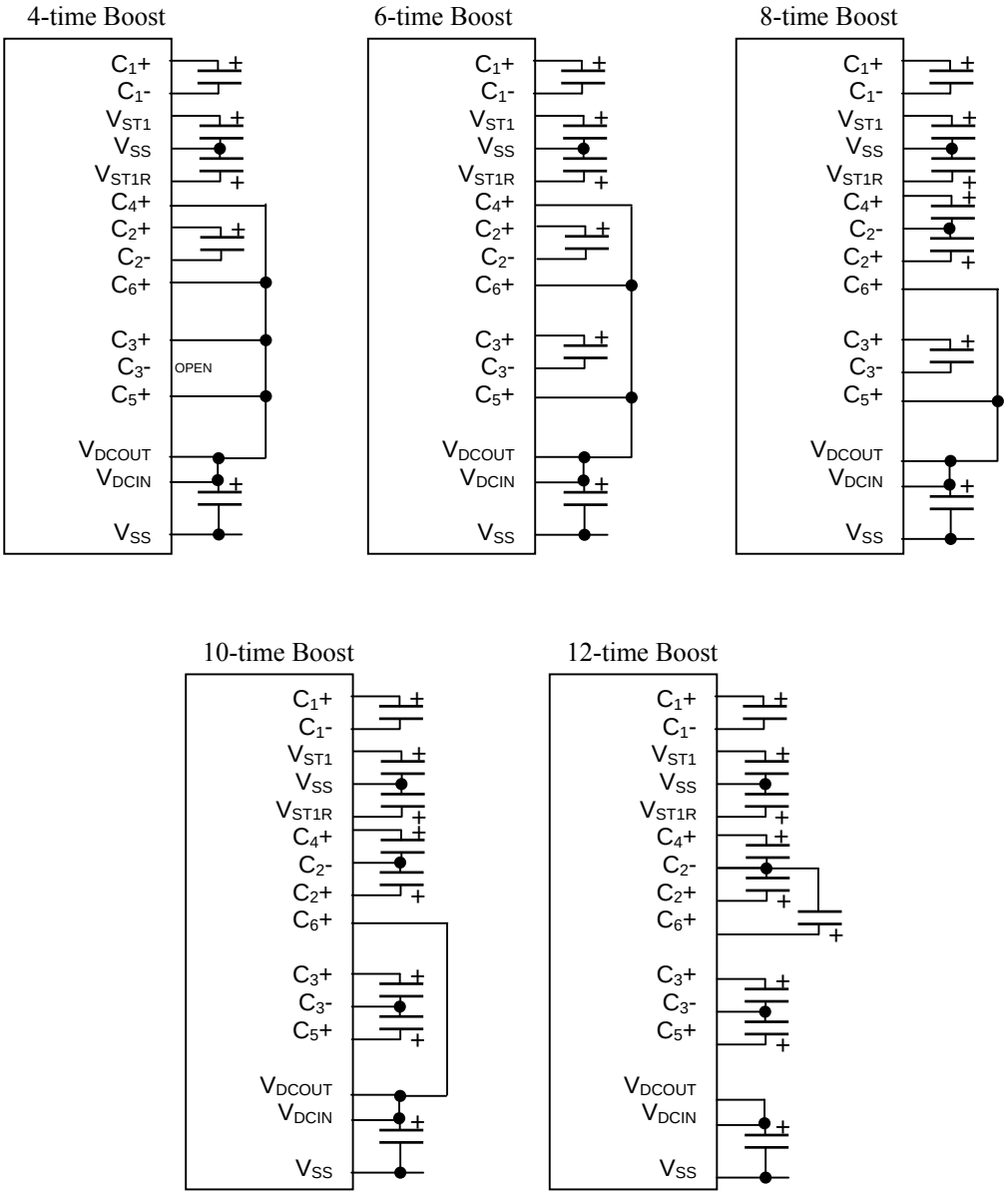
VU2	VU1	VU0	2nd Booster
0	0	0	OFF (Default)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time

The relation of 1st boost circuit, 2nd boost circuit and Voltage adjust circuit is shown in below.



The output voltage of a VST1R terminal generates voltage according to the number of stages of 2nd-Boost circuit.
The 2nd-Boost circuit controls less than maximum voltage. Therefore, in case of VEE=5.5V or VST1=15V condition, VDCOUT voltage is less than 36V.

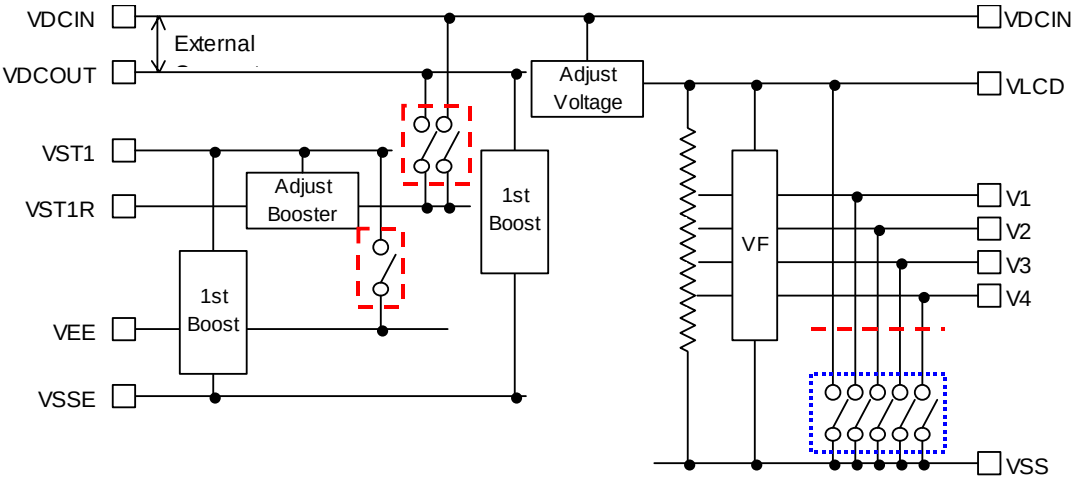
- External Capacitor Connection of Voltage Booster



(1-27-4)Discharge circuit

The **NJU6657** incorporates a discharge circuit.

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the VDCOUT, VDCIN, VLCD, V1 to V4, VST1 and VST1R. This instruction prevents the unknown display at the power supply off. (refer to shown below)



(1-27-5)Attention of Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply.

(**i**) Power ON/OFF in using external LCD supply

• Power ON

First “VDD and VDDL ON”, next “Reset by RESb”, then “External LCD power supply ON”. When using only internal voltage converter, first “VDD and VDDL ON”, next “Reset”, then “VDCIN ON”.

• Power OFF

First “Reset by RESb” or “Power save” instruction” to isolate external LCD bias voltage, next “VDD OFF”. For more safety, placing a resistor in series on the VLCD or VDCIN line are recommended. That resistance is usually between 50Ω
and 100Ω.

The value of resistance is fixed with the result of actual LCD display evaluation.

(**ii**) Power ON/OFF in using internal LCD supply

• Power ON

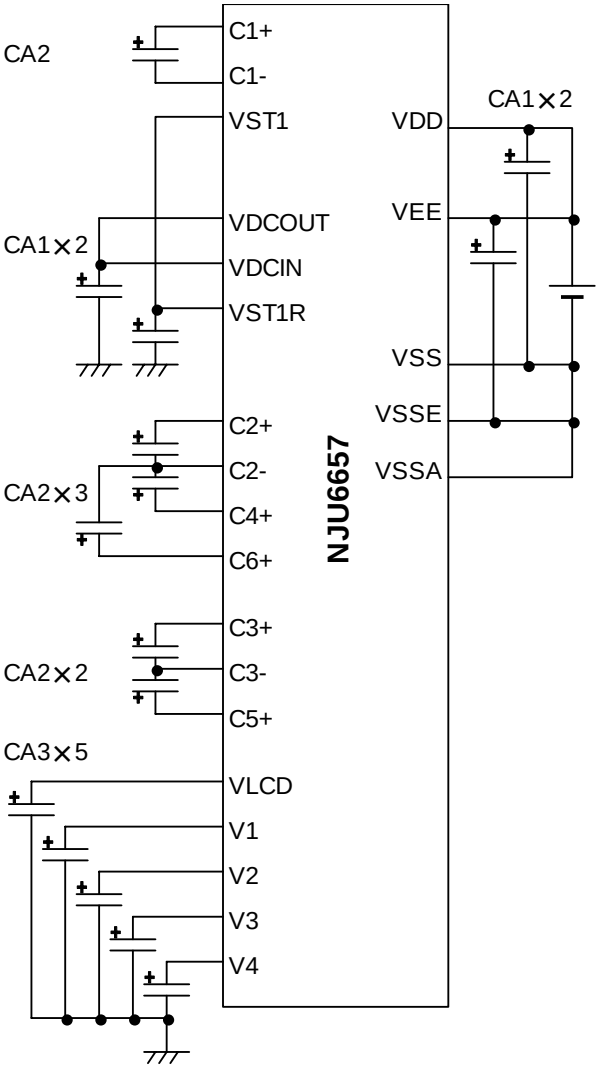
First “VDD, VDDL and VEE ON”, next “Reset by RESb”, then “Internal LCD Power supply ON”. Be sure to excute the “Display ON” instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

• Power OFF

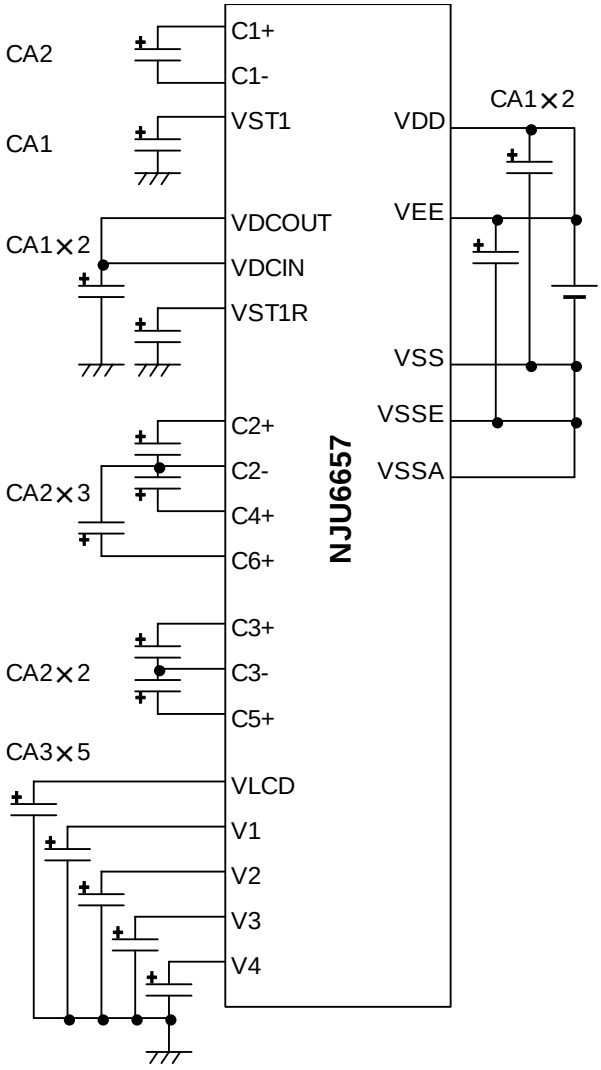
First “Reset by RESb or “Power save” instruction, next “Dispcharge ON” next “VEE OFF” then “VDD OFF”. If using different power sources for the VDD and the VEE individually, the VEE must be turned off after that, the VDD can be turned off, waiting until the LCD bias voltgae (VLCD, V1, V2, V3 and V4) drop below the threshold level of LCD pixels.

-External Components for LCD Power Supply -

1) Using Only Internal LCD Power Supply
(VEE=VDD, 12-time Boost)



2) Using Only Internal LCD Power Supply
(VEE=VDD, 12-time Boost, Adjust Boost circuit.)



Reference Values

CA1	1.0 ~ 4.7μF
CA2	1.0 ~ 4.7μF
CA3	0.47 ~ 1μF

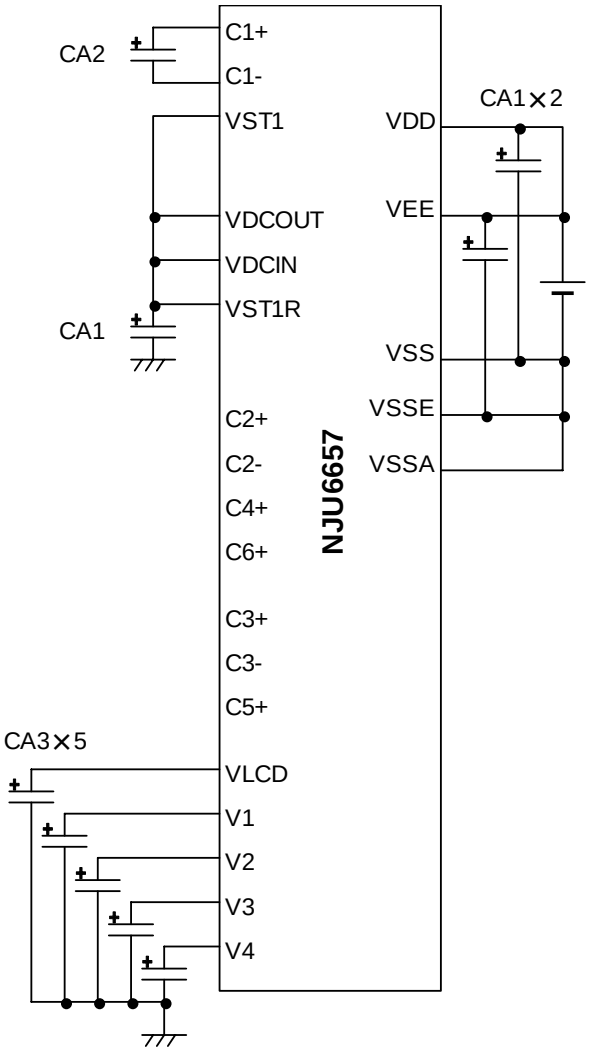
Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VSS, VDD, VSSE, VEE, VDCIN, VLCD, V1 to V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality.

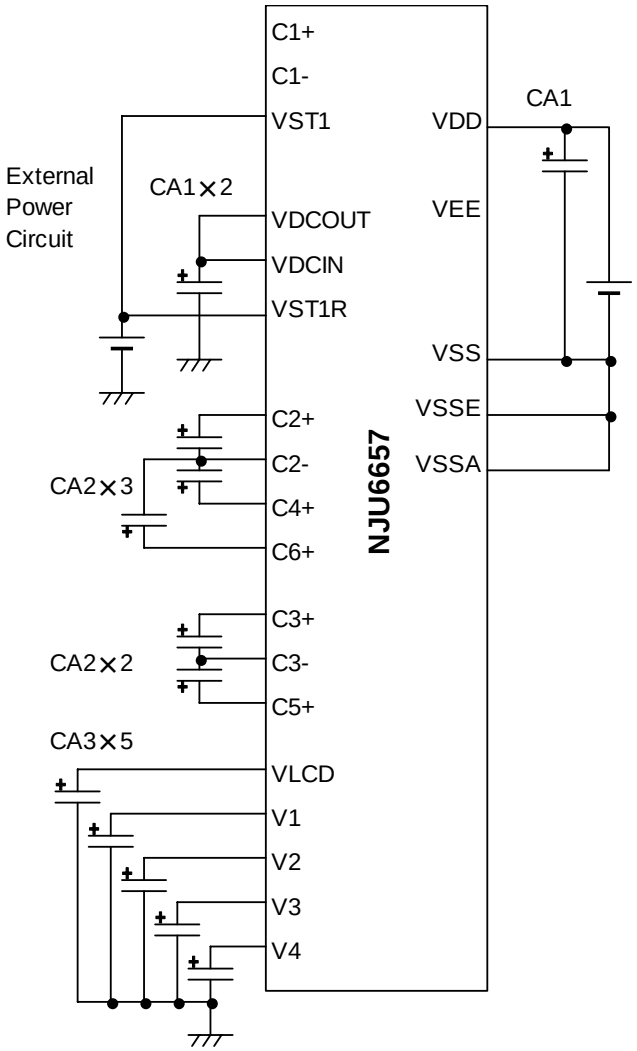
Note 3) When using 1st and 2nd boost circuits, the capactor value (connect between C1+/C1- and VST1 terminals) should be bigger than capacitor value of 2nd boost circuit. (Recommendation is 3-times.)

-External Components for LCD Power Supply

3) Using Internal LCD Power Supply within 1st Boost, Adjust Voltage Circuit, VF Circuit (VEE=VDD)



4) Using Internal LCD Power Supply within 2nd Boost, Adjust Voltage Circuit, VF Circuit. (6-time Boost)



Reference Values

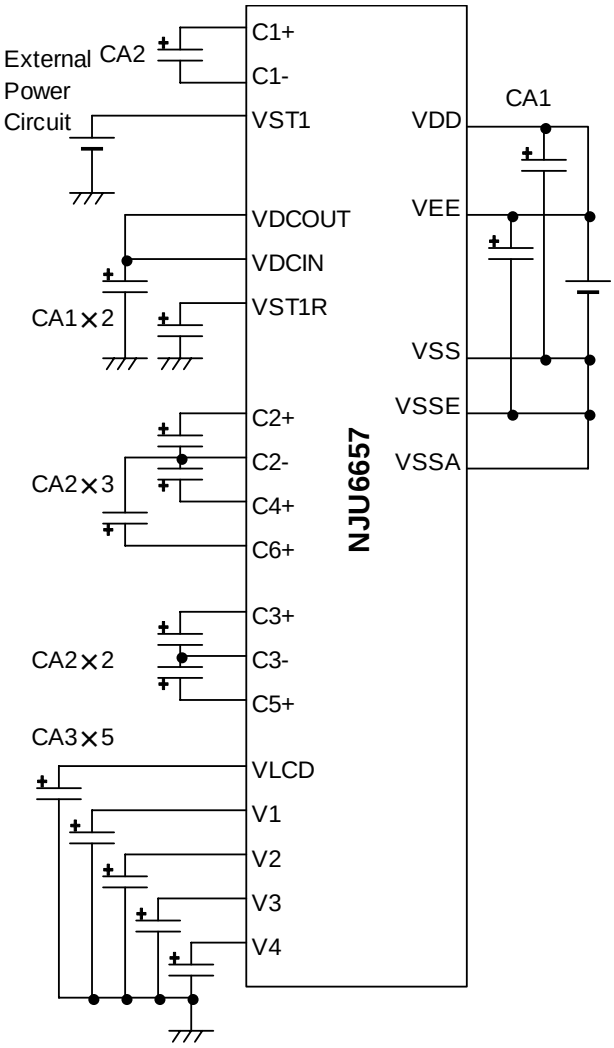
CA1	1.0 ~ 4.7μF
CA2	1.0 ~ 4.7μF
CA3	0.47 ~ 1μF

Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

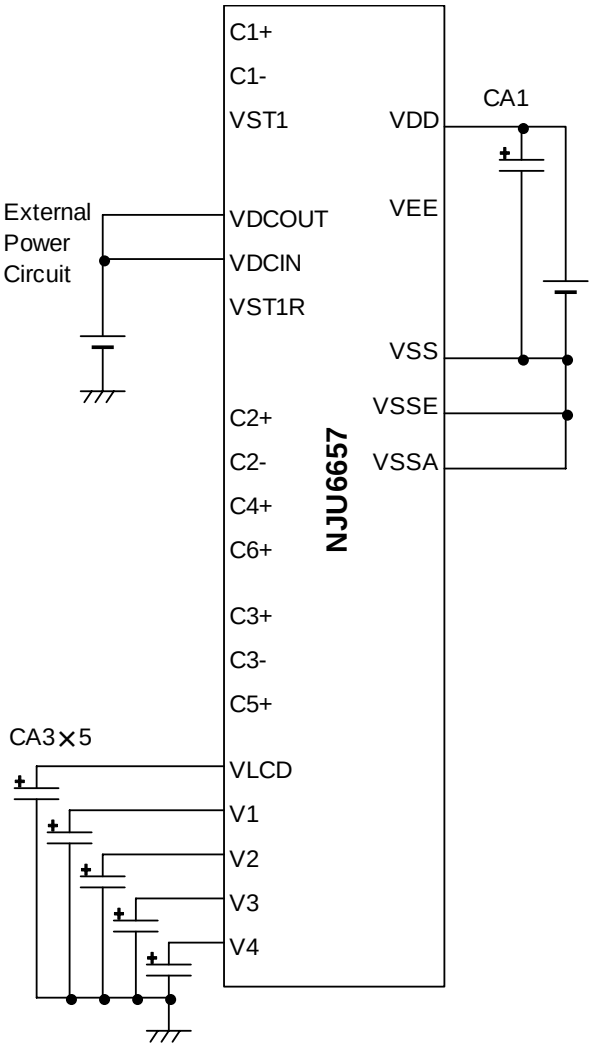
Note 2) Parasitic resistance on the power supply lines (VSS, VDD, VSSE, VEE, VDCIN, VLCD, V1 to V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality.

-External Components for LCD Power Supply

5) Using Internal LCD Power Supply within 2nd Boost, Adjust Voltage Circuit, VF Circuit (6-time Boost, Adjust Boost Voltage circuit)



6) Using Internal LCD Power Supply within Adjust Voltagae Circuit, VF Circuit (VDCIN Ext. Input)



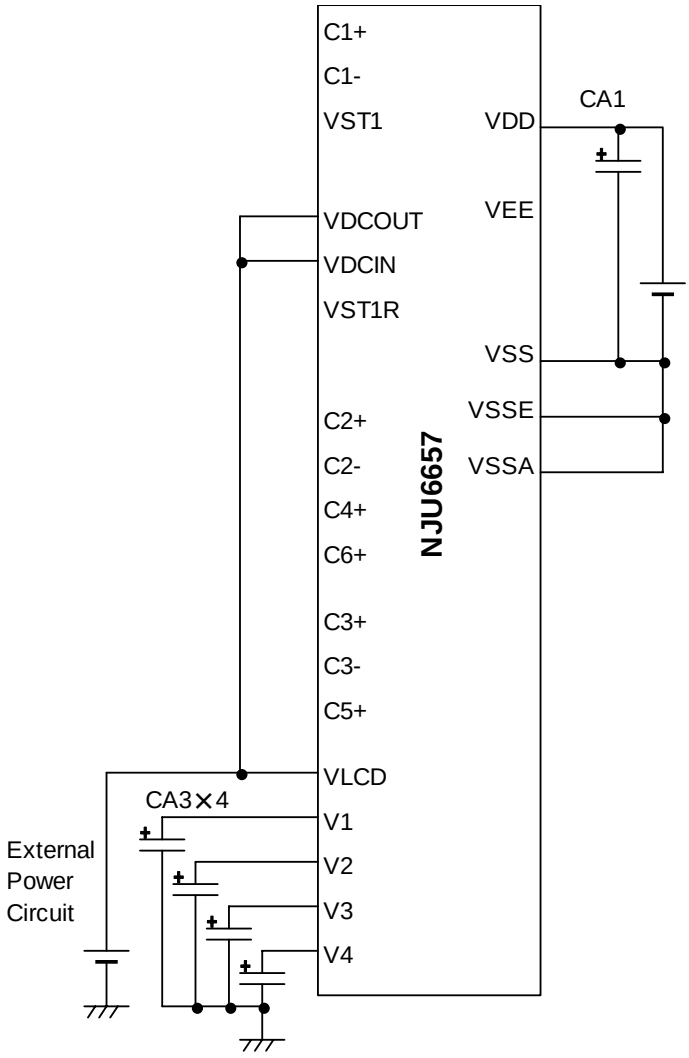
Reference Values

CA1	1.0 ~ 4.7μF
CA2	1.0 ~ 4.7μF
CA3	0.47 ~ 1μF

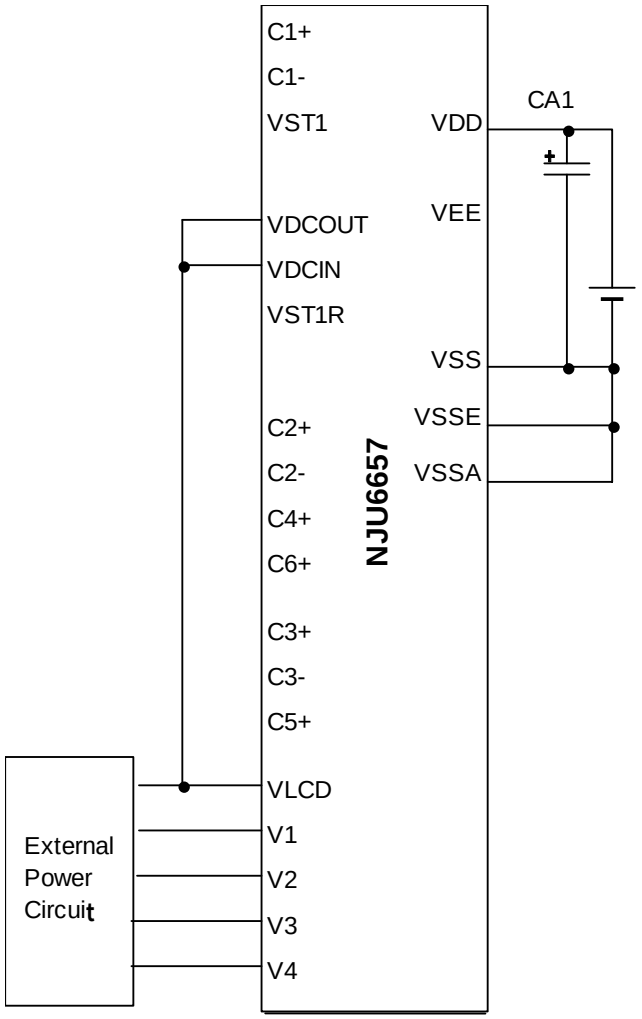
Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VSS, VDD, VSSE, VEE, VDCIN, VLCD, V1 to V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality.

7. Using Only Internal Voltage follower Circuit.



8. Using Only External LCD Power Supply



Reference Values

CA1	1.0 ~ 4.7μF
CA2	1.0 ~ 4.7μF
CA3	0.47 ~ 1μF

Note 1) B grade capacitor is recommended for CA1 to CA3. Make sure what is the best capacitor value in the particular application.

Note 2) Parasitic resistance on the power supply lines (VSS, VDD, VSSE, VEE, VDCIN, VLCD, V1 to V4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality.

(1) Instruction Set-

The **NJU6657** distinguishes the signal on the data bus D0 to D7 as an instruction by combination of A0, RDB and WRB(R/W). The decode of the instruction and execution performs with only high speed Internal timing without relation to the external clock. In case of serial interface, the data input as MSB(D7) first serially. The Table. 4-1, 4-2 shows the instruction codes of the **NJU6657**.

Table. 4-1 Instruction table (1/2) (*: Don't Care)

Instruction		A0	RDb	WRb	Instruction code								Defoult	Description
					D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	0	D0=0:OFF, D0=1:ON
(2)	Initial Display Line Set	0	1	0	1 *	0 SL6	0 SL5	0 SL4	1 SL3	0 SL2	1 SL1	0 SL0	00H	SL6 to 0: Initial Display Line Address
(3)	Page Address Set	0	1	0	1 *	0 *	1 *	1 *	0 PA3	0 PA2	0 PA1	1 PA0	0H	PA3 to 0: Page Address of DDRAM
(4)	Column Address Set	0	1	0	0 *	0 *	0 *	1 *	0 CA3	0 CA2	1 CA1	1 CA0	00H	CA8 to 0: Column Address of DDRAM
		0	1	0	0 *	0 *	0 *	1 CA8	0 CA7	1 CA6	0 CA5	0 CA4	00H	
(5)	Status Read	0	0	1	Status								-	
(6)	Write Display Data	1	0	0	Write Data								-	Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								-	Read the data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	ADC	0	ADC: Set the DDRAM vs Segment
(9)	Common Direction Select	0	1	0	1	1	0	0	0	0	0	INV	000	INV: Common Direction
(10)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	REV	0	REV: Inverse the ON and OFF Display
(11)	**Whole Display ON/OFF**	0	1	0	1	0	1	0	0	1	0	ALL ON	0	ALLON: Whole Display Turns ON
(12)	LCD Duty Ratio Set	0	1	0	1 *	0 DN6	1 DN5	1 DN4	1 DN3	1 DN2	0 DN1	1 DN0	48H	Partial Select Function DN5 to 0: LCD Duty Ratio DS5 to 0: COM Start Position
	Common Start Position Set	0	1	0	1 *	0 DS6	1 DS5	1 DS4	1 DS3	1 DS2	1 DS1	0 DS0	00H	
(13)	n-line Inverse Drive Set	0	1	0	1	1	1	0	0	1	0	NLS	0	NLS: n-line Inverse Drive Set
(14)	n-line Inverse Drive Register Set	0	1	0	0 MIX	0 NL6	1 NL5	1 NL4	0 NL3	1 NL2	1 NL1	0 NL0	-	NL6 to 0: Set the number of inverse drive line. MIX: n-line inverse + 2-frame
(15)	Dummiy width Set				0	0	1	1	0	0	ST	DUM	00	DUM: Dummy Width ON/OFF ST: Segment Output Status
(16)	Read Modify Write Set	0	1	0	1	1	1	0	0	0	0	0	-	Read Modify Write Set
(17)	End	0	1	0	1	1	1	0	1	1	1	0	-	Read Modify Write Reset

table. 4-2 Instruction table (2/2) (*: Don't Care)

Instruction		A0	RDb	WRb	Instruction Code								Default	Description
					D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
(18)	Internal Oscillation Circuit On/Off	0	1	0	1	0	1	0	1	0	1	INTCK	1	INTCK: Oscillation Circuit ON/OFF
(19)	Oscillation Circuit Frequency Set	0	1	0	0 *	1 SH1	0 SH0	1 OS4	1 OS3	1 OS2	1 OS1	1 OS0	101000 0	SH1 to 0: Divide Set OS3 to 0: Oscillation Circuit Frequency ON/OFF
(20)	LCD Bias Ratio Set	0	1	0	1 *	0 *	1 *	0 *	0 *	0 BS2	1 BS1	0 BS0	000	BS2 to 0: LCD Bias Ratio Set
(21)	Temprature Gradient Set	0	1	0	0 *	1 *	0 *	0 *	1 *	1 TC2	1 TC1	0 TC0	000	TC2 to 0: Temprature Gradient of LCD Drive Voltgae
(22)	Power Control Set	0	1	0	0 *	0 *	1 *	0 *	0 DC1	1 DC0	0 VRG	1 VF	0000	DC1 to 0: Boost ON/OFF VRG: Adjust Voltage ON/OFF VF: VF ON/OFF
(23)	EVR Register Set (Upper Bit)	0	1	0	1 *	0 *	0 *	0 ER8	0 ER7	0 ER6	0 ER5	1 ER4	00h	ER8 to 4: EVR Register Set (Upper-4bit)
(24)	EVR Register Set (Lower Bit)	0	1	0	1 *	0 *	0 *	0 *	0 ER3	0 ER2	1 ER1	0 ER0	0H	ER3 to 0: EVR Register Set (Lower-4bit)
(25)	EVR Step Up	0	1	0	1	0	0	0	0	0	1	1	-	EVR Step Up
(26)	EVR Step Down	0	1	0	1	0	0	0	0	1	0	0	-	EVR Step Down
(27)	Boost Voltage Control Set				1 *	0 *	0 *	0 *	1 *	1 VU2	0 VU1	1 VU0	0h	VU2 to 0: 2nd Boost Set
(28)	Boost Clock Set	0	1	0	1 *	0 *	0 *	0 *	0 *	1 DCC2	1 DCC1	0 DCC0	101	DCC2 to 0: Boost Clock Set
(29)	Thermo Sensor ON/OFF	0	1	0	0	0	1	0	1	0	0	TSON	0	TSON: Thermo Sensor ON/OFF
(30)	Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	DIS	0	DIS: Discharge ON/OFF
(31)	Address Home	0	1	0	1	1	1	0	0	0	1	0	-	Initialize of PA and CA value
(32)	Power Save	0	1	0	1	1	1	1	1	0	0	0	-	Set to Power Save
(33)	Power Save Reset	0	1	0	1	1	1	1	0	0	0	1	-	Power Save Reset
(34)	Low Voltage Operation Mode	0	1	0	0 *	1 *	1 *	0 *	0 *	1 *	1 *	0 LVM	0	LVM: Set to Low Voltage Operation

(1-1) Explanation of Instruction Code

1. Display ON/OFF

This instruction selects display turn-on or turn-off regardless of the contents of the DDRAM.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	1	1	1	D	Display ON/OFF

D 0: Display OFF
1: Display ON

2. Initial Display Line Set (refer to ■FUNCTIONAL DESCRIPTION Fig.1 Display data RAM (DDRAM) Map)

This instruction specifies the DDRAM line address which correponds to the COM0 position.
By means of repeating this instruction, the initial display line address will be dynamically changed; it means smooth display scrolling will be enabled.
In this time, DDRAM data are unchanged.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	1	0	1	0	Mode Set
			*	SL6	SL5	SL4	SL3	SL2	SL1	SL0	Initial Display Line Set

SL6	SL5	SL4	SL3	SL2	SL1	SL0	Line Address (HEX)
0	0	0	0	0	0	0	00H (Default)
1	0	0	0	0	0	1	01H
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	1	0	1	1	1	57H

3. Page Address Set (refer to ■FUNCTIONAL DESCRIPTION Fig.1 Display data RAM (DDRAM) Map)

In order to access to the DDRAM for writing or reading display data, both “page address set” and “column address set” instructions are required before accessing.
The change of page address is not affected to the display.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	1	0	0	0	1	Mode Set
			*	*	*	*	P3	P2	P1	P0	Page Address Set

P3	P2	P1	P0	Page
0	0	0	0	0 (Default)
0	0	0	1	1
:	:	:	:	:
:	:	:	:	:
1	0	1	0	10

4. Column Address Set (refer to ■FUNCTIONAL DESCRIPTION Fig.1 Display data RAM (DDRAM) Map)

As abobe-mentioned, in order to access to the DDRAM for writing or reading display data, it is necessary to execute both “page address set” and “column address set” before accessing.

Once the column address is set, it will automatically increment (+1) whenever the DDRAM will be accessed, so that the DDRAM will be able to be continuously accessed without “column address set” instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	0	1	0	0	1	1	Mode Set
			*	*	*	*	CA3	CA2	CA1	CA0	Column Address Set 1

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	0	1	0	1	0	0	Mode Set
			*	*	*	CA8	CA7	CA6	CA5	CA4	Column Address Set 2

CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Column Address (HEX)
0	0	0	0	0	0	0	0	0	00H (Default)
0	0	0	0	0	0	0	0	1	01H
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	1	1	1	1	10FH

5. Status Read

This instruction reads out the internal status regarding “busy flag”, “ADC select”, “Display on/off”, “Power save” “2nd Booster on/off”, “1st Booster on/off.”, “Voltage regulator on/off” and “Voltage follower on/off”

< Status Read Command >

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	0	1	BF	ADC	D	PO	DC1	DC0	VRG	VF	Status Read

BF 0: The instruction can be input.
1: operating status

ADC 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

D 0: Display OFF
1: Display ON

PO 0: Normal
1: Power Seve

DC1 0: 2nd Boost Circuit OFF
1: 2nd Boost Circuit ON

DC0 0: 1st Boost Circuit OFF
1: 1st Boost Circuit ON

VRG 0: Adjust Voltage Circuit OFF
1: Adjust Voltage Circuit ON

VF 0: VF Circuit OFF
1: VF Circuit ON

6. Display Data Write

This instruction writes display data into the selected column address on the DDRAM.
The column address automatically increments (+1) whenever the display data is written by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
1	1	0	Write Data								Display Data Write

7. Display Data Read

This instruction reads out the display data stored in the selected column address on the DDRAM.
The column address automatically increments (+1) whenever the display data is read out by this instruction, so that this instruction can be continuously issued without “column address set” instruction.
After the “column address set” instruction, adummy read will be required, please refer to the (*-*).
In case of using serial interface mode, this instruction can’t be used.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
1	0	1	Read Data								Display Data Read

8. ADC Select

This instruction selects segment driver direction.
The correspondence between the column address and segment driver direction is shown in Fig.1.
This function reduces the restrictions on the IC position of an LCD module.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	0	0	0	ADC	ADC select

ADC 0: Clockwise Output (Normal) Segment Driver S0 to S271 (Default)
1: Counterclockwise Output (Inverse) Segment Driver S271 to S0

9. Common Driver Direction Select

This instruction selects common driver direction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	0	0	0	0	0	INV	Common Driver Direction

INV 0: Normal Common driver direction C0 to C88 (Default)
1: Inverse Common driver direction C88 to C0

10. Inverse Display ON/OFF

This instruction inverses the status of turn-on or turn-off of entire LCD pixels. It doesn't change the contents of the DDRAM.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	0	1	1	REV	Normal / Inverse

REV 0: Normal RAM data "1" correspond to "ON" (Default)
1: Inverse RAM data "0" correspond to "ON"

11. Whole Display ON/OFF

This instruction turns on entire LCD pixels regardless the contents of the DDRAM. It doesn't change the contents of DDRAM.
This instruction should be performed prior to the "Inverse display ON/OFF" instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	0	1	0	ALL ON	Whole Display ON/OFF

ALLON 0: Normal Display (Whole Display OFF) (Default)
1: Whole Display Turns ON (Whole Display ON)

12. Partial Select

The partial display is executed by combining the Display Duty Ratio with the Display Start Position instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	1	1	1	0	1	Mode Set
			*	DN6	DN5	DN4	DN3	DN2	DN1	DN0	Duty Ratio

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	1	1	1	1	0	Mode Set
			*	DS6	DS5	DS4	DS3	DS2	DS1	DS0	COM Start Potision

DN6	DN5	DN4	DN3	DN2	DN1	DN0	Duty Ratio
0	0	0	0	0	0	0	1/16
0	0	0	0	0	0	1	1/17
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	0	1	0	0	0	1/88 (Default)

DS6	DS5	DS4	DS3	DS2	DS1	DS0	COM Start Position
0	0	0	0	0	0	0	COM0(COM87) (Default)
0	0	0	0	0	0	1	COM1(COM86)
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	1	0	1	1	1	COM87(COM0)

( ): INV="1" set by "Common Direction Select" instruction
Duty is changed automatically when Partial Display execution. But VLCD voltage and frame frequency are not changed. The optimum conditions should fix refering the result of actual display.

13. n-line Inverse ON/OFF

This instruction sets n-line inversion.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	0	0	1	0	NLS	n-line Inverse ON/OFF

NLS 0: 2-frame alternating drive mode. (Default)
1: N-line inverse drive mode.

14. n-line Inverse Drive Register Set

This instruction specifies the number of n-line. The line count to be set is 2 to 88.
In case of Mix="1", the driving wave form is Mixed. (n-line Inverse + 2-frame alternating drive mode.)

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	1	1	0	1	1	0	Mode Set
			0	NL6	NL5	NL4	NL3	NL2	NL1	NL0	n-line Inverse Register Set

NL6	NL5	NL4	NL3	NL2	NL1	NL0	Inverse Lines
0	0	0	0	0	0	0	2 (Default)
0	0	0	0	0	0	1	3
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	1	0	1	0	1	87
1	0	1	0	1	1	0	88

15. Dummy period

This instruction specifies the insert position of dummy period.
In addition, SEG outputs of dummy period are made by ST register

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	1	1	0	0	ST	DUM	Dummy Period Set

DUM 0: 1/CL Duty (Default)
1: 1/ (CL+1dummy) Duty

ST 0: All segment drivers output non-active.. (Default)
1: All segment drivers output active.

CL: Display line count

16. Read Modify Write

This instruction controls column address increment.

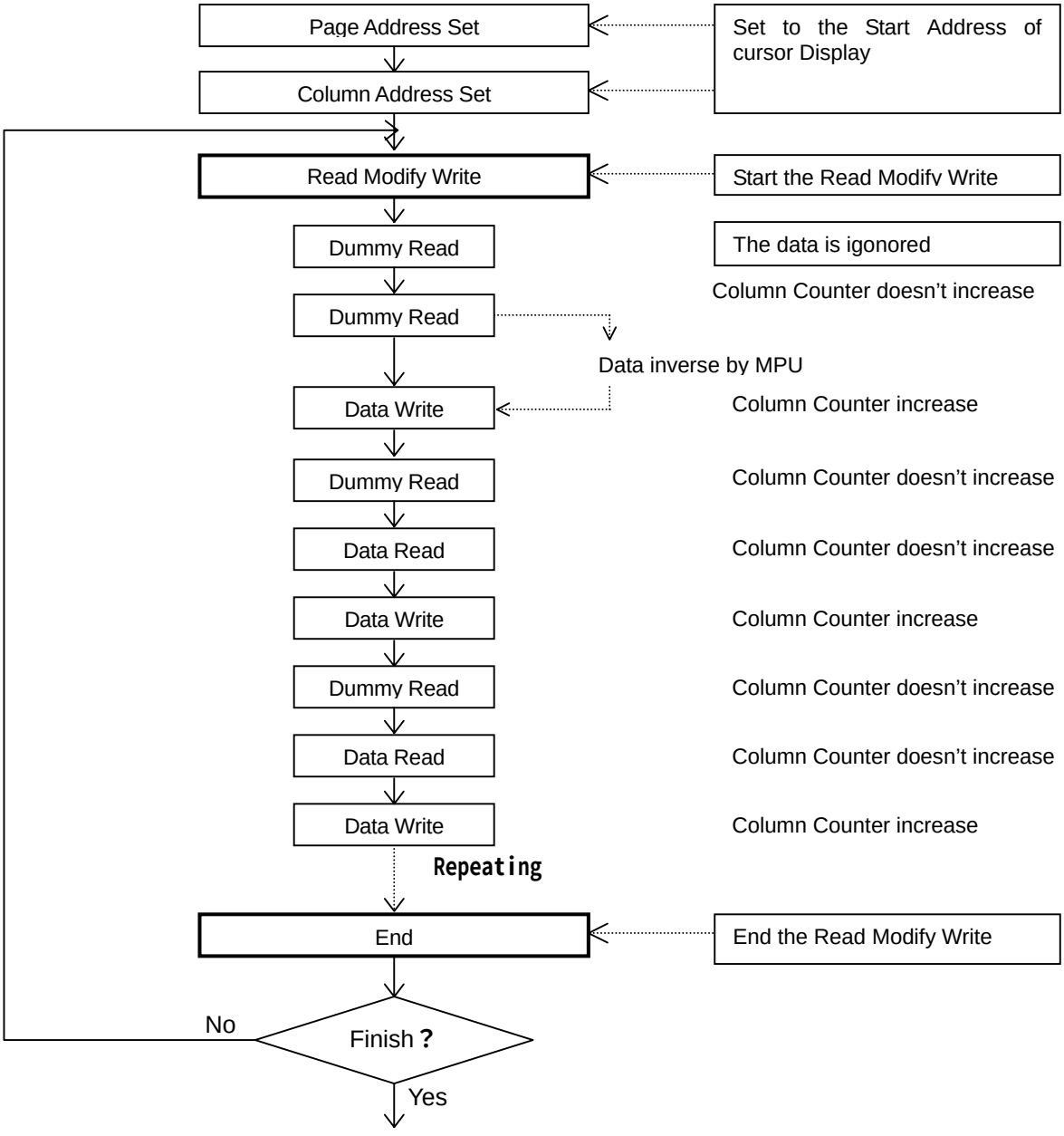
By using of this instruction, the column address can't increment when read operation but it can increment when write operation. This status will be continued until the below-mentioned "end" instruction will be issued.

This instruction can reduce the load of MPU, during the display data in specific DDRAM area is repeatedly changed for cursor blink or others.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	0	0	0	0	0	Read Modify Write

Note) In this "Read Modify Write" mode, out of display data "Read" / "Write", any instructions except "Column Address Set" can be executed

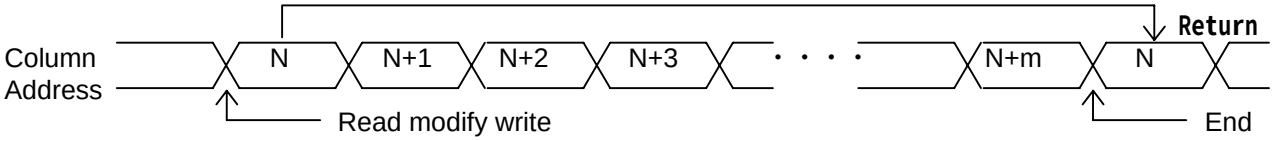
- The Sequence of Cursor Blink Display



17. End

The “end” instruction cancels the read modify write mode and makes the coulumn address return to the initial value just before “read modify write” is atarted

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	0	1	1	1	0	End



18. Internal Oscillator Circuit ON/OFF

This command starts the internal oscillator circuit operation. (INTCLK = “1”)
This setting is effective when CLS=”1”.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	1	0	1	INT CLK	Oscillator Control

INTCLK 0: Internal OSC OFF (Default)
1: Internal OSC ON

19. Internal Oscillator Circuit Frequency Select

This instruction sets the internal oscillator circuit frequency.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	1	0	1	1	1	1	1	Mode Set
			*	SH1	SH0	OS4	OS3	OS2	OS1	OS0	OSC Frequency Control

SH1	SH0	Divide Frequency Select
0	0	f_{OSC}
0	1	$f_{OSC}/2$
1	0	$f_{OSC}/4$ (Default)
1	1	$f_{OSC}/8$

OS4	OS3	OS2	OS1	OS0	OS4~0 (HEX)	Internal Frequency f_{OSC} [kHz]			
						f_{OSC}	$f_{OSC}/2$	$f_{OSC}/4$	$f_{OSC}/8$
0	0	0	0	0	0h	82.4	41.2	20.6	10.3
0	0	0	0	1	1h	88.0	44.0	22.0	11.0
0	0	0	1	0	2h	93.4	46.7	23.4	11.7
0	0	0	1	1	3h	99.2	49.6	24.8	12.4
0	0	1	0	0	4h	104.7	52.4	26.2	13.1
0	0	1	0	1	5h	110.3	55.1	27.6	13.8
0	0	1	1	0	6h	115.2	57.6	28.8	14.4
0	0	1	1	1	7h	120.8	60.4	30.2	15.1
0	1	0	0	0	8h	126.0	63.0	31.5	15.8
0	1	0	0	1	9h	131.6	65.8	32.9	16.4
0	1	0	1	0	Ah	137.0	68.5	34.2	17.1
0	1	0	1	1	Bh	142.3	71.2	35.6	17.8
0	1	1	0	0	Ch	147.5	73.8	36.9	18.4
0	1	1	0	1	Dh	153.1	76.5	38.3	19.1
0	1	1	1	0	Eh	158.5	79.2	39.6	19.8
0	1	1	1	1	Fh	163.9	81.9	41.0	20.5
1	0	0	0	0	10h	169.0	84.5	42.2 (Default)	21.1
1	0	0	0	1	11h	174.4	87.2	43.6	21.8
1	0	0	1	0	12h	179.4	89.7	44.9	22.4
1	0	0	1	1	13h	184.9	92.4	46.2	23.1

* The table above showns the values at 25^{O}C and without of manufacturing variations in the internal oscillation circuit frequency.
* The frame frequency changed automatically when Partial Display execution. The optimum conditions should be select refer to formula is shown below.

◆ Formula of OSC Frequency

When using internal OSC Circuit.

Dummy Period Set: DUM='0'

$$\text{OSC frequency} \quad f_{OSC} = f_{FR} \times (CL \times 6)$$

f_{FR}: frame frequency
CL: Display line count

Dummy Period Set: DUM='1'

$$\text{OSC Frequency} \quad f_{OSC} = f_{FR} \times \{ (CL+1dummy) \times 6 \}$$

f_{FR}: frame frequency
CL: Display line count

In External clock operation, the external clock input to OSC1 terminal.
The formula is shown below.
Condition: DUM='0'

External clock frequency f_{OSC} = n × f_{FR} × (CL × 6)

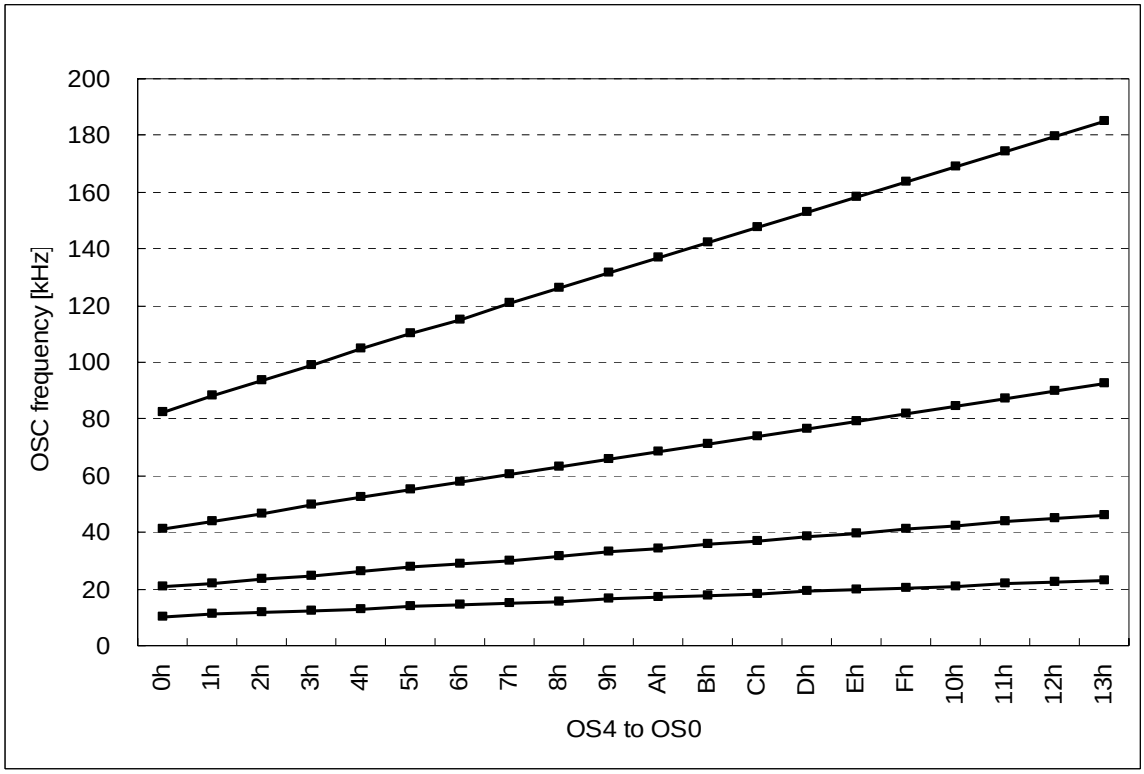
n: Divide count
f_{FR}: Frame frequency
CL: Display line

Condition: External clock Input, DUM="1"

External Clock Frequency f_{OSC} = n × f_{FR} × { (CL+1dummy) × 6 }

n: Divide count
f_{FR}: Frame frequency
CL: Display line

The relationship between OSC register (OS4 to OS0) and OSC frequency are shownbelow.



20. Bias Select

This instruction selects LCD bias value.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	1	0	0	0	1	0	Mode Set
			*	*	*	*	*	BS2	BS1	BS0	Bias Select

NL2	NL1	NL0	Bias Ratio
0	0	0	1/10 (Default)
0	0	1	1/9
0	1	0	1/8
0	1	1	1/7
1	0	0	1/6
1	0	1	1/5
1	1	0	1/4

21. Temperature Gradient Set

This instruction is used to set the temperature gradient characteristics of the VLCD voltage output from the internal power supply circuit.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	1	0	0	1	1	1	0	Mode Set
			*	*	*	*	*	TC2	TC1	TC0	Temperature Gradient Set

TC2	TC1	TC0	Temperature Gradient [%/**°C**]
0	0	0	-0.000 (Default)
0	0	1	-0.050
0	1	0	-0.075
0	1	1	-0.100
1	0	0	-0.125
1	0	1	-0.150

22. Power Control Set

This instruction controls the status of internal power circuits. Please refer to the (1-24) internal power circuit more detail.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	1	0	0	1	0	1	Mode Set
			*	*	*	*	DC1	DC0	VRG	VF	Internal Power Supply Control

DC1 0: 2nd Boost OFF (Default)
1: 2nd Boost ON

DC0 0: 1st Boost OFF (Default)
1: 1st Boost ON

VRG 0: Adjust Voltage Circuit OFF (Default)
1: Adjust Voltage Circuit ON

VF 0: V/F Circuit OFF (Default)
1: V/F Circuit ON

The internal power supply must be Off when external power supply using.

*The wait time depends on the C4 to C8, COUT capacitors, and VDD and VLCD Voltage.
Therefore it requires the actual evaluation using the LCD module to get the correct time.

23. EVR Register Set (Upper bit)

The EVR values is controled in 400 steps by setting the combination of “EVR register set” instruction..

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	0	0	0	1	Mode Set
			*	*	*	ER8	ER7	ER6	ER5	ER4	EVR Register Set 2

24. EVR Register Set (Lower bit)

The EVR values is controled in 400 steps by setting the combination of “EVR register set” instruction..

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	0	0	0	1	Mode Set
			*	*	*	*	ER3	ER2	ER1	ER0	EVR Register Set 1

The combination of EVR register at shown in below.

ER8	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EVR	V_{LCD}
0	0	0	0	0	0	0	0	0	0	Min. (Default)
0	0	0	0	0	0	0	0	1	1	:
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	0	0	400	Max.

25. EVR register Step Up

The “EVR register Step Up” instruction controls +1 step of EVR register value.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	0	0	1	1	EVR Register Step Up

26. EVR register Step Down

The “EVR Register Step Down” instruction controls – 1 step of EVR register value

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	0	1	0	0	EVR Register Step Down

27. Adjust Boost Voltage Set

The “Adjust Boost Voltage Set” instruction controls 2nd Voltage Booster at Vlcd = 36(V).

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	1	1	0	1	Mode Set
			*	*	*	*	*	VU2	VU1	VU0	Adjust Boost Voltage Set

VU2	VU1	VU0	2nd Boost Circuit
0	0	0	OFF (Default)
0	0	1	2-Time
0	1	0	3-Time
0	1	1	4-Time
1	0	0	5-Time
1	0	1	6-Time

28. Boost Clock Set

The "Boost Clock Set" instruction controls Boost Clock Frequency of 1st Vand 2nd Voltage Booster.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	0	0	0	0	1	1	0	Mode Set
			*	*	*	*	*	DCC 2	DCC 1	DCC 0	Boost CLK Set

DCC2	DCC1	DCC0	Boost CLK	
0	0	0	2 Divide	84.5[kHz]
0	0	1	4 Divide	42.2[kHz]
0	1	0	8 Divide	21.1[kHz]
0	1	1	16 Divide	10.6[kHz]
1	0	0	32 Divide	5.28[kHz]
1	0	1	64 Divide	2.64[kHz] (Default)
1	1	0	128 Divide	1.33[kHz]
1	1	1	256 Divide	0.66[kHz]

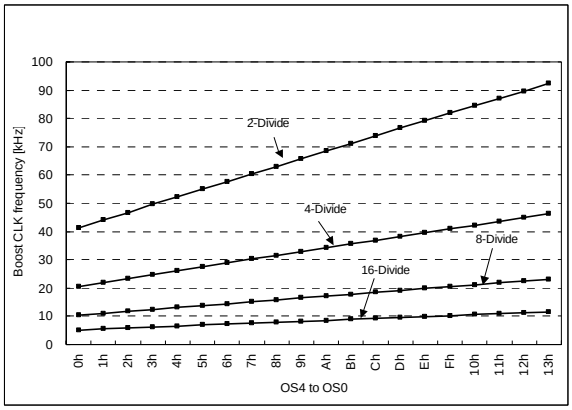
* The Boost clock frequency is changes by register (OS4 to 0) of Internal Oscillator frequency select instruction. Upper table value is Boost clock when set to reset condition. (OS4 to 0 ='10000)
When fix to Internal Frequency, the boost clock frequency caluculate is shown in below.

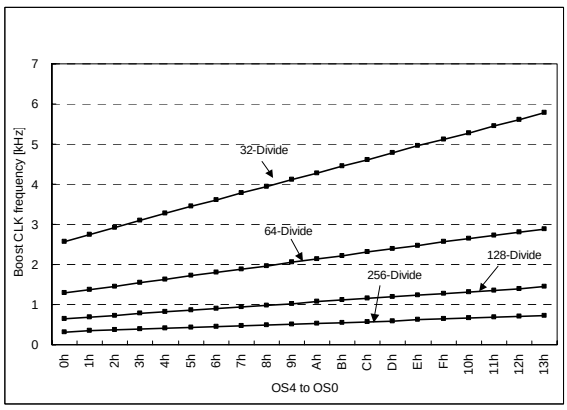
Boost Clock Frequency: fDCC = fDOSC / n

n: Fix to divide
fDOSC: Basis Frequency (Internal Oscillator :)

* In case of using external clock, Basis frequency interchange External clock frequency.

OS 4	OS 3	OS 2	OS 1	OS 0	OS4~ 0(HEX)	Boost CLK
0	0	0	0	0	0h	82.4
0	0	0	0	1	1h	88.0
0	0	0	1	0	2h	93.4
0	0	0	1	1	3h	99.2
0	0	1	0	0	4h	104.7
0	0	1	0	1	5h	110.3
0	0	1	1	0	6h	115.2
0	0	1	1	1	7h	120.8
0	1	0	0	0	8h	126.0
0	1	0	0	1	9h	131.6
0	1	0	1	0	Ah	137.0
0	1	0	1	1	Bh	142.3
0	1	1	0	0	Ch	147.5
0	1	1	0	1	Dh	153.1
0	1	1	1	0	Eh	158.5
0	1	1	1	1	Fh	163.9
1	0	0	0	0	10h	169.0 (Default)
1	0	0	0	1	11h	174.4
1	0	0	1	0	12h	179.4
1	0	0	1	1	13h	184.9





Fundamental frequency (it corresponds to OS4 to 0 of a built-in oscillating frequency setting command)

29. Thermal Sensor ON/OFF

The ON/OFF of the thermal sensor is set by this instruction.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	0	1	0	1	0	0	TSON	Thermal Sensor ON/OFF

TSON 0: Thermal Sensor OFF (Default)
1: Thermal Sensor ON

30. Discharge ON/OFF

Discharge circuits is used discharge out the stabilizing capacitors placed on the VLCD, V1, V2, V3, V4 and VSS.. This instruction prevents the unknown display at the power supply OFF.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	0	1	0	1	DIS	Discharge ON/OFF

DIS 0: Discharge OFF (Default)
1: Discharge ON

31. Address Home

This instruction sets the initialization of Page Address and Coulumn Address.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	0	0	0	1	0	Address Home

- Initialize Status

	PARAMETER	Resistor	Default
1	Page Address: Set to “0” page.	PA3～0	0H
2	Coulumn Address: St to “0”.	AC7～0	00H

32. Power Save

This instruction sets the LSI into the power save mode. This instruction is reducing operating current.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	1	1	0	0	0	Power Save

<Power Save Status>

PARAMETER	Status
Internal Oscillator	Stop
Adjust Voltage Circuit	Stop
VF Circuit	Stop
Voltage Boost Circuit	Stop
Thermo Sensor	Stop
All COM/SEG output terminals	VSS

* When the external clock operation, it can not be accessed.
* The DDRAM can be accessed during the power save mode.

33. Power Save Reset

This instruction releases the power save mode.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	1	1	1	1	0	0	0	1	Power Save Reset

34. Low Voltage Operation Mode

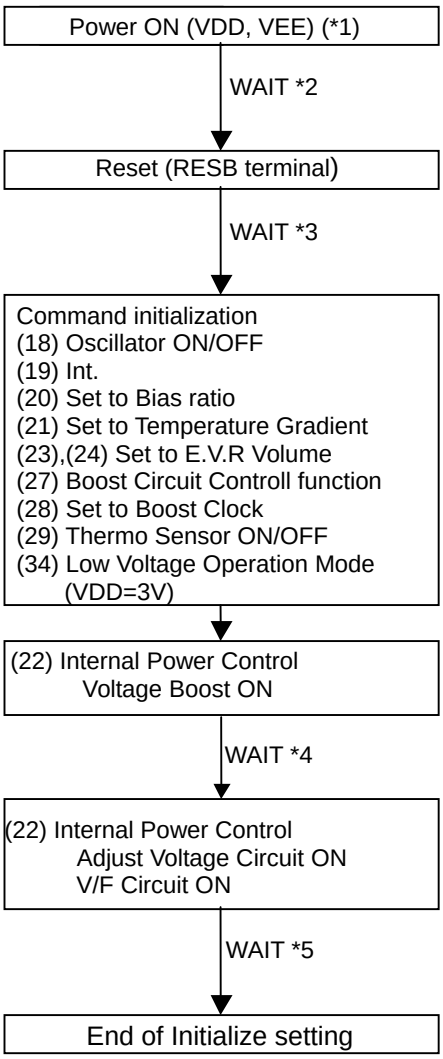
When using to the Low VDD condition (VDD=2.7 to 3.3V), Please set up to “Low Voltage Operation Mode ON”.

A0	RDB	WRE	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	COMMAND
0	1	0	0	1	1	0	0	1	1	0	Low Voltage Operation Mode
			*	*	*	*	*	*	*	LVM	

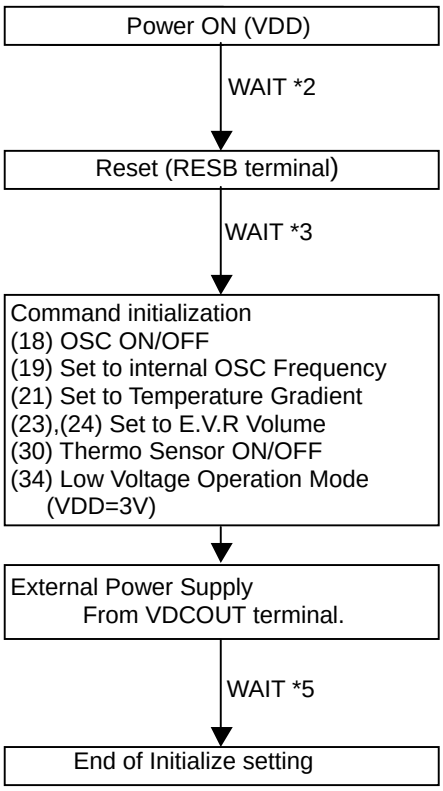
LVM 0: Low Voltage Operation Mode OFF (Default)
1: Low Voltage Operation Mode ON

TYPICAL INSTRUCTION SEDUENCE

Initialization Sequence in Using Internal LCD Power Supply



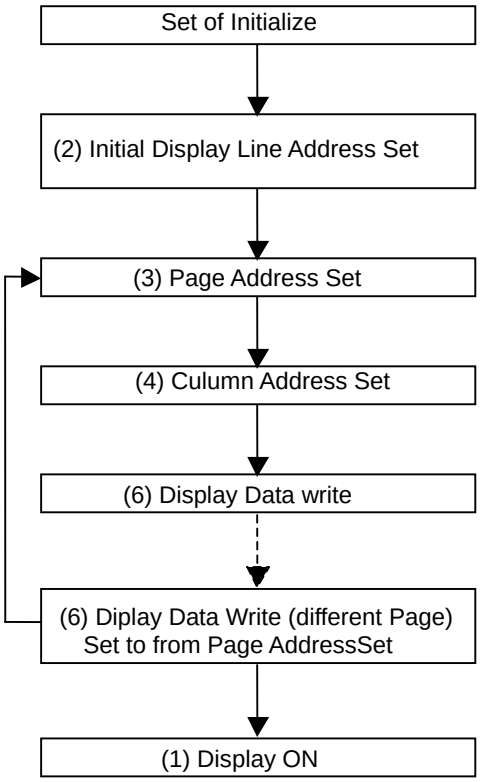
Initialization Sequence in Using Ext. LCD Power Supply



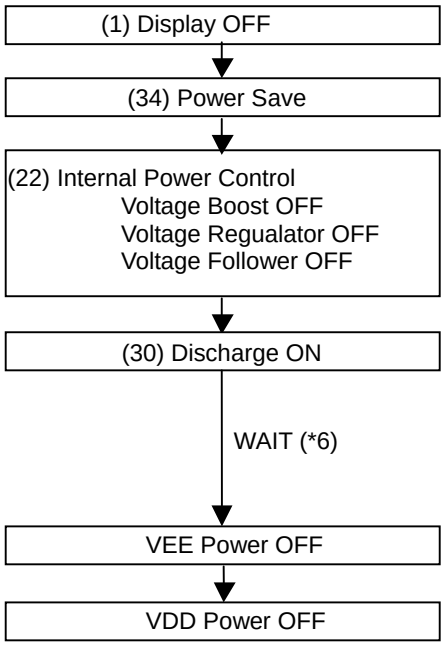
*1 If different power sources are applied to the VDD and the VEE, turn ON the VDD first.
*2 Wait until the VDD and VEE are stabilized
*3 Reset wait time. (Over than 2mS)
*4 Wait until the VDCOUT and VDCIN are stabilized
*5 Wait until the VLCD and V1 to V4 are stabilized

Note) Wait time for stabilizing internal power supply differs by external components, VDD, and VLCD.
Make sure what is the eait time in the particular application.

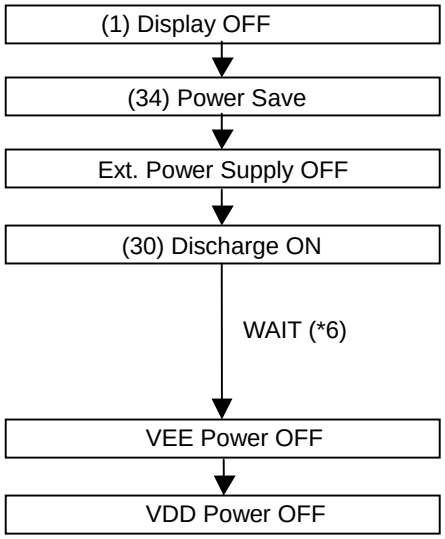
Example for Display Data Write Sequence



Example for Power OFF Sequence in using Internal Power Supply.



Example for Power OFF Sequence in using Ext. Power Supply



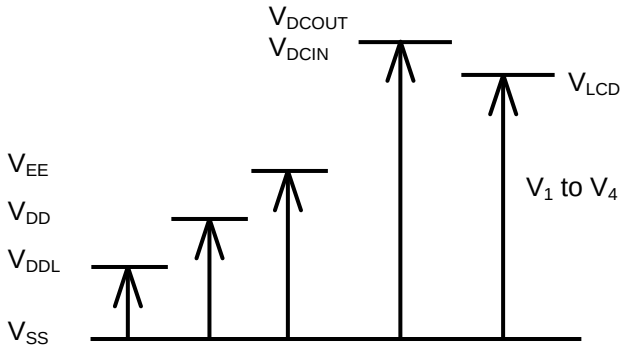
*6 Wait until the discharge stabilized .

Wait time for End of discharge differs by external components, VDD, and VLCD.Make sure what is the eait time in the particular application.

■ ABSOLUTE MAXIMUMN RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD}	-0.3 to +6.0	V
Supply Voltage (2)	V_{EE}	-0.3 to +6.0	V
Supply Voltagae (3)	V_{ST1},V_{ST1R} V_{DCOUT},V_{DCIN},V_{LCD}	-0.3 to +40.0	V
Supply Voltage (4)	V_1,V_2,V_3,V_4	-0.3 to V_{LCD}	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Output Voltgae	V_{OUT}	-0.3 to V_{DD} + 0.3	V
Operation Temperature	T_{opr}	-40 to +105	℃
Storage Temperature (Chip)	T_{stg}	-55 to +125	℃



Note 1) V_{DD}, V_{LCD} to V_4, V_{DCOUT}, V_{DCIN} voltage values are specified as V_{SS} = 0V.

Note 2) The relation of $V_{DCOUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{ss}$; $V_{OUT} > V_{DD} \geq V_{SS}$ must be maintained.
In case of inputting external LCD driving voltage, LCD drive voltage should start supplying to **NJU6657** at the mean time of turning on V_{DD} power supply or after turned on V_{DD}.
In use of the voltage boost circuit, the condition that the supply voltage : 40V $\geq V_{OUT} - V_{SS}$ is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ DC Electrical Characteristics

(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	単位	NOTE
Power Supply (1)	V_{DD}			2.7	-	5.5	V	5
Power Supply (2)	V_{EE}	1st Boost Input Voltage		2.7		5.5	V	
Power Supply (3)	V_{ST1} V_{ST1R}			V_{DD}		15	V	6
Power Supply (4)	V_{DCOUT}			V_{EE}	-	36	V	6
	V_{DCIN}			6	-	36		
	V_{LCD}			6	-	36		
	V_1,V_2			$0.4V_{LCD}$	-	V_{LCD}		
	V_3,V_4			V_{SS}	-	$0.6V_{LCD}$		
"H" Level Input Voltage	V_{IHC1}	V_{DD}=2.7 to 5.5V		$0.8V_{DD}$	-	V_{DD}	V	7
"L" Level Input Voltage	V_{ILC1}			V_{SS}	-	$0.2V_{DD}$	V	
"H" Level Output Voltage	V_{OHC1}	V_{DD}=2.7 to 5.5V	I_{OH}=-25uA	$0.8V_{DD}$	-	V_{DD}	V	8
"L" Level Output Voltage	V_{OLC1}		I_{OL}= 25uA	V_{SS}	-	$0.2V_{DD}$	V	
Leakage Current	I_{LI}	VIN=VDD or VSS		-1.0	-	1.0	uA	9
	I_{LO}			-3.0	-	3.0	uA	10
Driver On-resistance	R_{ON1}	Ta=25℃	V_{LCD}=20V	-	1	1.7	kΩ	11
	R_{ON2}		V_{LCD}=10V	-	2.5	4.2	kΩ	
Stand-by Current	I_{DDQ}	V_{DD}=3V,Ta=25℃		-	0.3	5	uA	
	I_{EEQ}	V_{EE}=3V, Ta=25℃		-	0.3	5		
	I_{LCDQ}	V_{LCD}=20V, Ta=25℃		-	2	10		
Oscillation Frequency	f_{OSC}	Ta=25℃, Initialize Status		38.0	42.2	46.5	kHz	12
External Clock Frequency	f_{CL}			-	42.2	200	kHz	

Note 5) Although the **NJU6657** can operate in wide range of the operating voltage, it shall not be guaranteed in a suddeen voltage flucuation during the access with MPU.
Note 6) Apply to using of external power supply.
Note 7) Apply to A0,D_0 to D_7, RDB, WRB, CSB, RESB, CEL68, PS, VDLS, CLS terminals.
Note 8) Apply to D_0 to D_7, BUSY terminals.
Note 9) Aplly to All Input terminals.
Note 10) Apply to D_0 to D_7, All output terminals.
Note 11) R_{ON} is the resistance values in supplying 0.1V voltage-difference between power supply terminals (V1, V2, V3, V4) and each output terminals (common/segment) of 1/7 bias setting.
Note 12) Internal osillation frequency when the reset status.
SH1～0 = '10'
OS4～0 = '10000'
Note 13) The divide of internal oscillation frequency.
SH1 to 0 = '00'

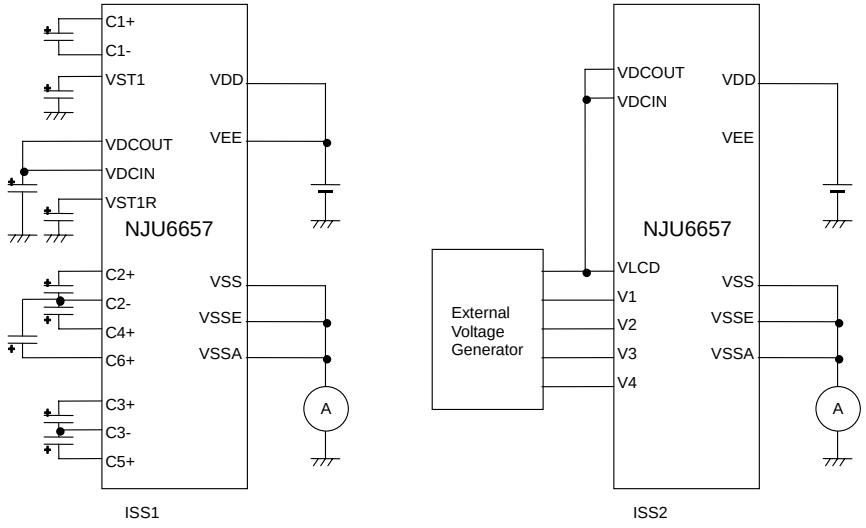
(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
1st Boost Input Voltgae	V_{EE}	4-times boost	2.7		5.5	V	14
		6-times boost	2.7		5.5		
		8-times boost	2.7		5.0		
		10-times boost	2.7		4.0		
		12-times boost	2.7		3.3		
2nd Boost Input Voltage	V_{ST1R}	2-times boost	V_{DD}	-	15.0	V	
		3-times boost	V_{DD}	-	13.3		
		4-times boost	V_{DD}	-	10.0		
		5-times boost	V_{DD}	-	8.0		
		6-times boost	V_{DD}	-	6.6		
1st Boost output Voltgae	V_{ST1}	V_{SS} common	-	-	11.0	V	
2nd Boost output Voltage	V_{DOUT}	V_{SS} common	-	-	36	V	
Adjustment Range LCD Driving Voltage	V_{LCD}	Voltage boost operation off External power supply	6	-	36	V	15
Voltage Follower Operating Voltage	V_{LCD}		6	-	36	V	
Operating current	I_{SSQ1}	Power save mode		1	40	uA	
	I_{SS1}	V_{DD}=3V, V_{LCD}=20V, All COM/SEG open, without MPU access, checker flag display		1.7	3	mA	16
	I_{SS2}			220	500	uA	

Note 14) Applies to the condition when using the internal voltage booster, VST1 and VST1R terminals are connected. The adjust boost voltage and boost autocontroled function are not used.
Note 15) The voltage adjustment circuit controls V_{LCD} within the range of the E.V.R circuit.
Note 16) Each operating current shall be defined as being measured in the following condition.
(fFR=80[Hz], 1/10Bias, 1/88Duty, Low voltage operation mode, Driver terminals are open)

SYMBOL	Power Control				Operating Condition				External Voltage Supply (Input Terminal)
	DCC1	DCC0	VRG	VF	1st Booster	2nd Booster	Voltage regulator	Voltage followers	
I_{SS1}	1	1	1	1	On	On	On	On	12-Time Boost
I_{SS2}	0	0	0	0	Off	Off	Off	Off	V_{DCIN}, V_{LCD}~V_4

ISS 1,2 measurement circuit:



■ Temperature Sensor Characteristics

(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Operating Temperature Range	Ta		-40	-	105	℃	
Temperature Gradient	T	Ta=-40 to 105℃	-5.0	-	5.0	℃	
Output Voltage	T_{SV}	Ta=-40℃	1.412	1.433	1.454	V	
		Ta=25℃	1.144	1.165	1.186		
		Ta=105℃	0.807	0.828	0.849		
Output Voltage Temperature gradient	V_{INC}		-	-4.19	-	mV/℃	
Temperature sensor Setup time	T_{TSV}		20	-	-	ms	18
Operating Current	I_{TS}		-	20	50	uA	

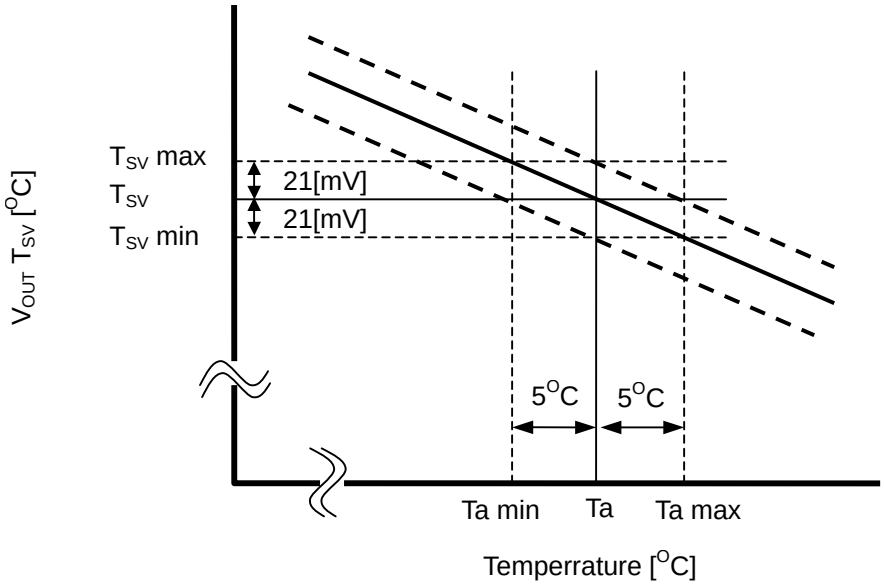
Note 17) The typ. Value of the sensor analog output voltage TSV when ambient temperature is Ta [^{O}C] is approximated by the following expression.

$$V_{TSV} = -0.0006 \times Ta^2 - 4.1386 \times Ta + 1269mV \text{ [mV]}$$

The sensor analog output voltage is output with accuracy of $\pm$ 5^{O}C.
The output voltage temperature gradient VINC.
Since it is -4.19 [mV/OC], variation voltage [of TSV] ΔT_{SV} is denoted by the following formula.

$$\Delta V_{TSV} = \pm(4.19 \times 5^{O}C) = 21 \text{ [mV]}$$

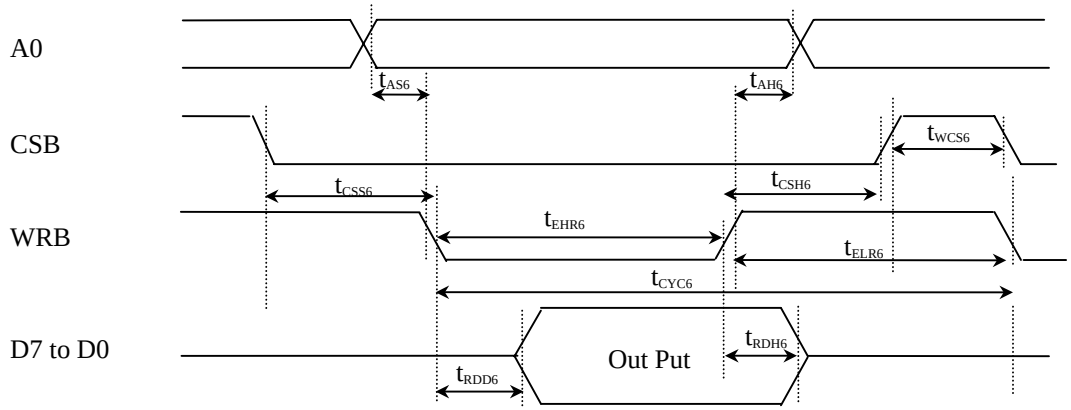
The relationship of between VOUT and Temperature as shown in below.

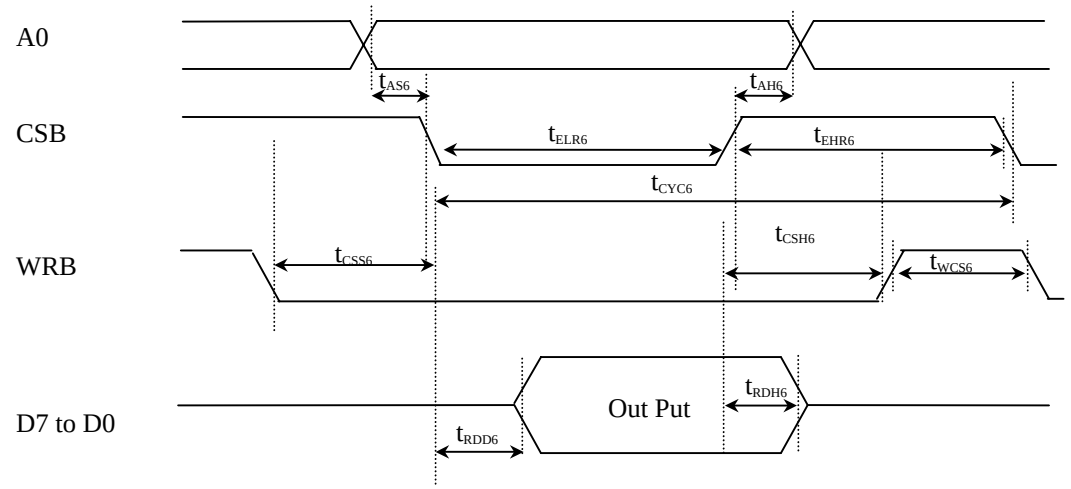


Note 18) The setup time is possible of Read-out from after input a temperature sensor ON/OFF instruction. The TSV terminal is OPEN.

■ BUS TIMING CHARACTERISTICS

- Read and Write characteristics (80 type MPU)



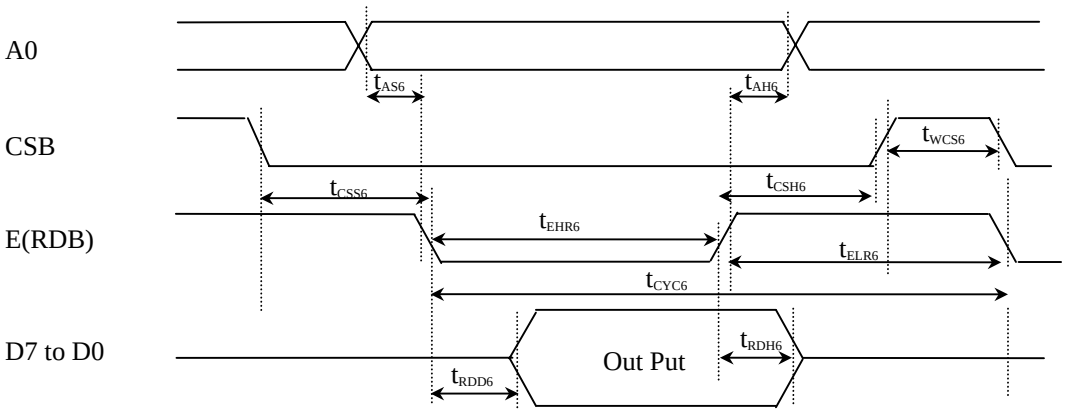


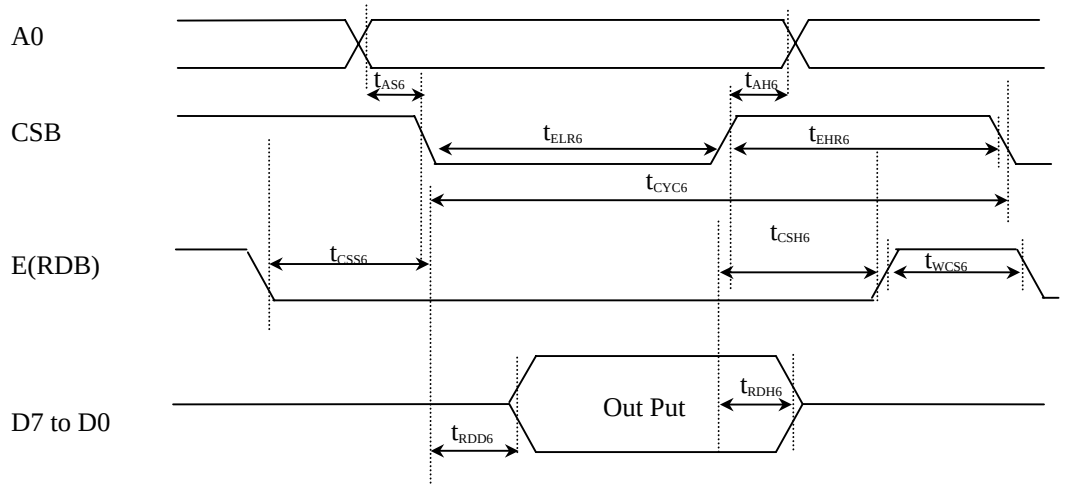
(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
A0 Hold Time	t_{AS8}		50	-	ns	A0
A0 Set Up Time	t_{AH8}		0		ns	
CSB Hold Time	t_{CSH8}		100	-	ns	CSB
CSB Set Up Time	t_{CSS8}		100		ns	
CSB "H" Level Width	t_{WCS8}		500		ns	
System Cycle Time	t_{CYC8}		1350	-	ns	WRB
Write "L" Pulse Time	t_{WRLW8}		550		ns	
Write "H" Pulse Time	t_{WRHW8}		700		ns	
Data Set Up Time	t_{DS8}		250	-	ns	D7 to D0
Data Hold Time	t_{DH8}		300		ns	

Note) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.
* : (1) Accessed by WRb and RDb signal when CS_1b="L". (2) Accessed by CS_1b signal when WRb and RDb ="L".

- System bus read timing (80 type MPU)



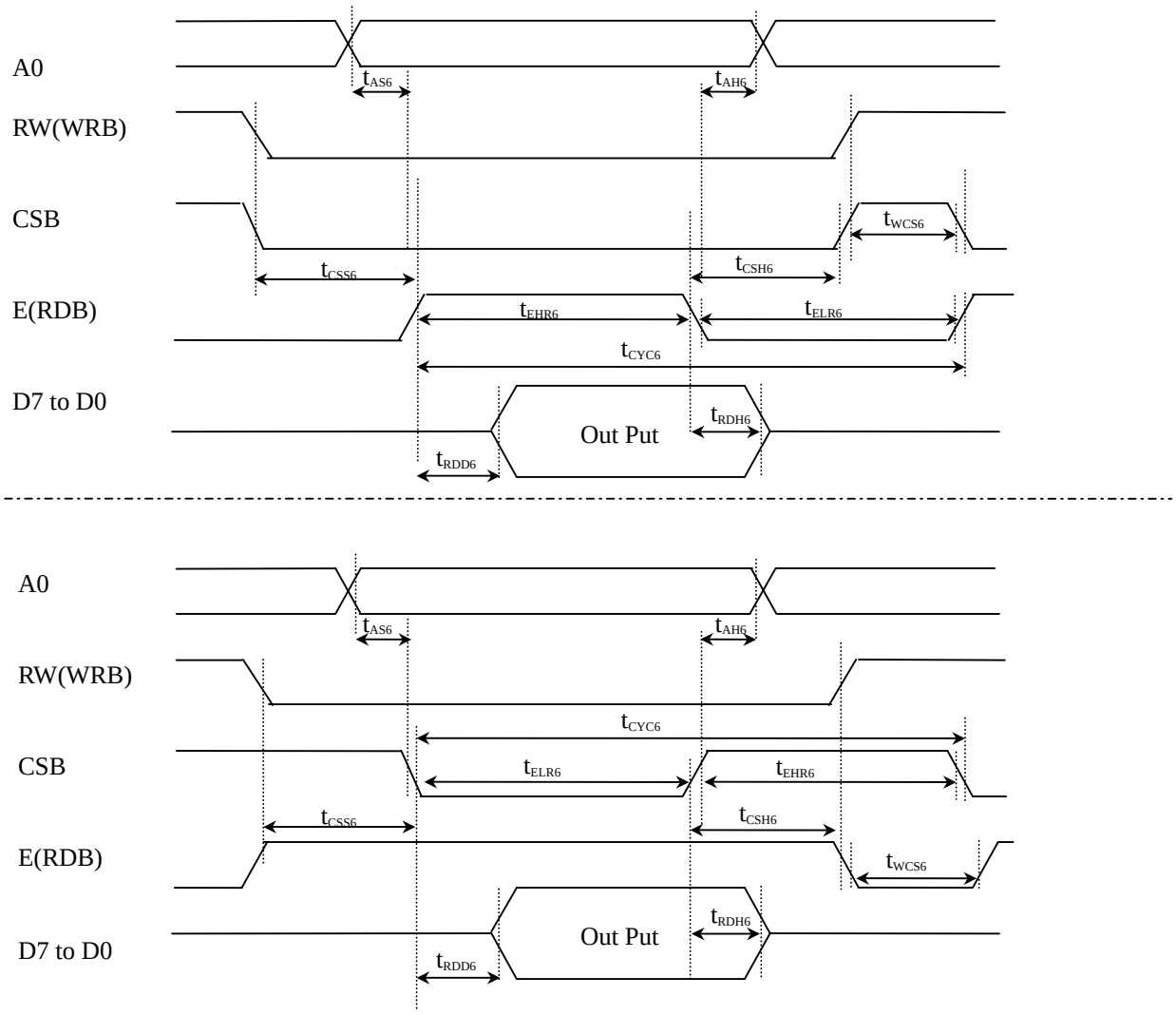


(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
A0 Hold Time	t_{AS8}		50	-	ns	A0
A0 Set Up Time	t_{AH8}		0		ns	
CSB Hold Time	t_{CSH8}		100	-	ns	CSB
CSB Set Up Time	t_{CSS8}		100		ns	
CSB "H" Level Width	t_{WCS8}		500		ns	
System Cycle Time	t_{CYC8}		2100	-	ns	RDB
Read "L" Pulse Width	t_{WRLR8}		1150		ns	
Read "H" Pulse Width	t_{WRHR8}		700		ns	
Read Data Out Delay Time	t_{RDD8}	CL=100pF		1150	ns	D7 to D0
Read Data Hold Time	t_{RDH8}		0		ns	

Note) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.
* : (1) Accessed by WRb and RDb signal when CS_1b="L". (2) Accessed by CS_1b signal when WRb and RDb ="L".

- System bus write timing (68 type MPU)



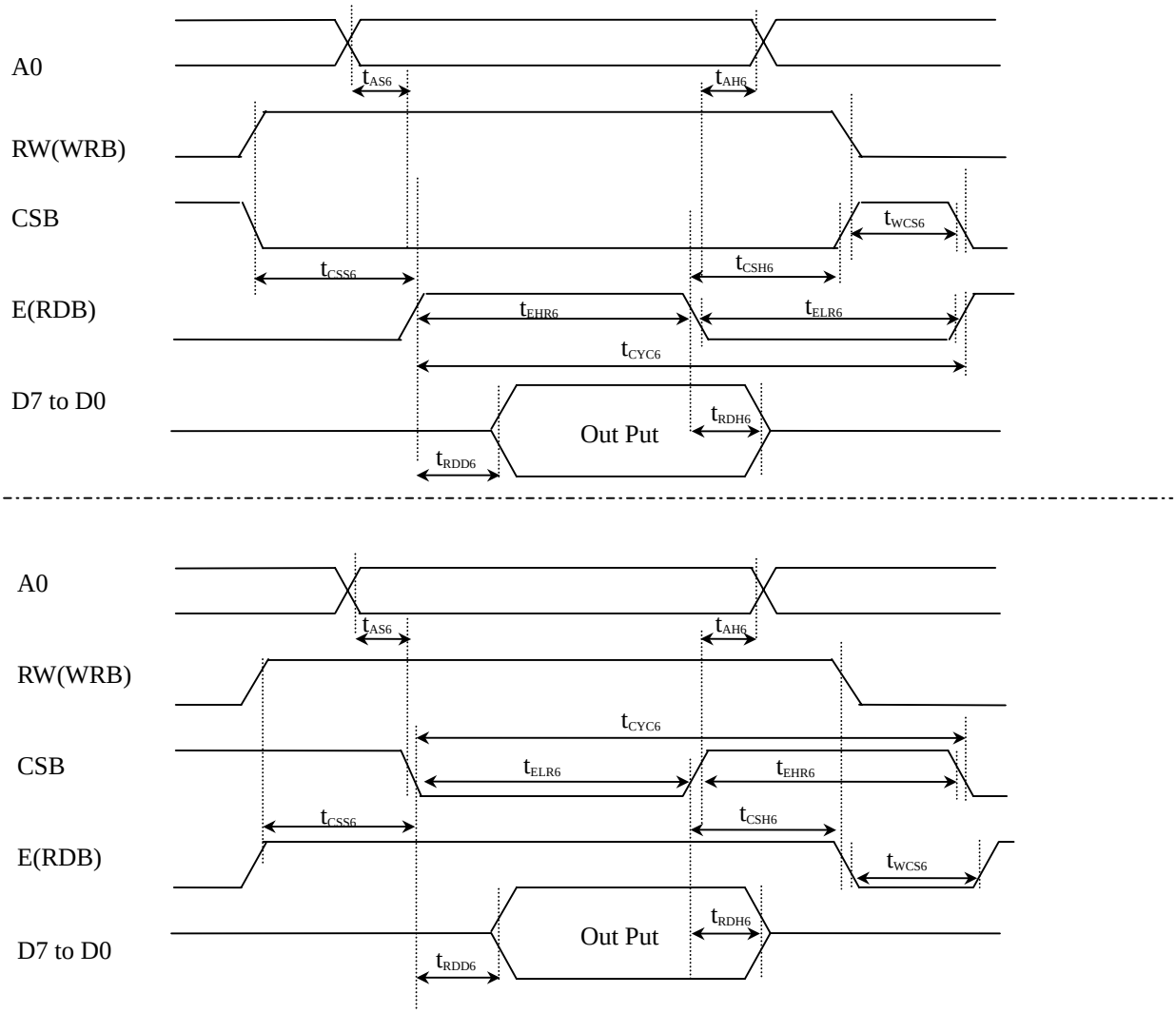
(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
A0 Hold Time	t_{AS6}		50	-	ns	A0
A0 Set Up Time	t_{AH6}		0		ns	
CSB Hold Time	t_{CSH6}		100	-	ns	CSB
CSB Set Up Time	t_{CSS6}		100		ns	
CSB "H" Level Pulse Width	t_{WCS6}		500		ns	
System Cycle Time	t_{CYC6}		1350	-	ns	E
Enable "L" Pulse Time	t_{ELW6}		700		ns	
Enable "H" Pulse Time	t_{EHW6}		550		ns	
Data Set Up Time	t_{DS6}		250	-	ns	D7 to D0
Data Hold Time	t_{DH6}		300		ns	

Note) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.

* : (1) Accessed by WRb and RDb signal when CS_1b="L". (2) Accessed by CS_1b signal when WRb and RDb ="L".

- System bus read timing (68 Type MPU)

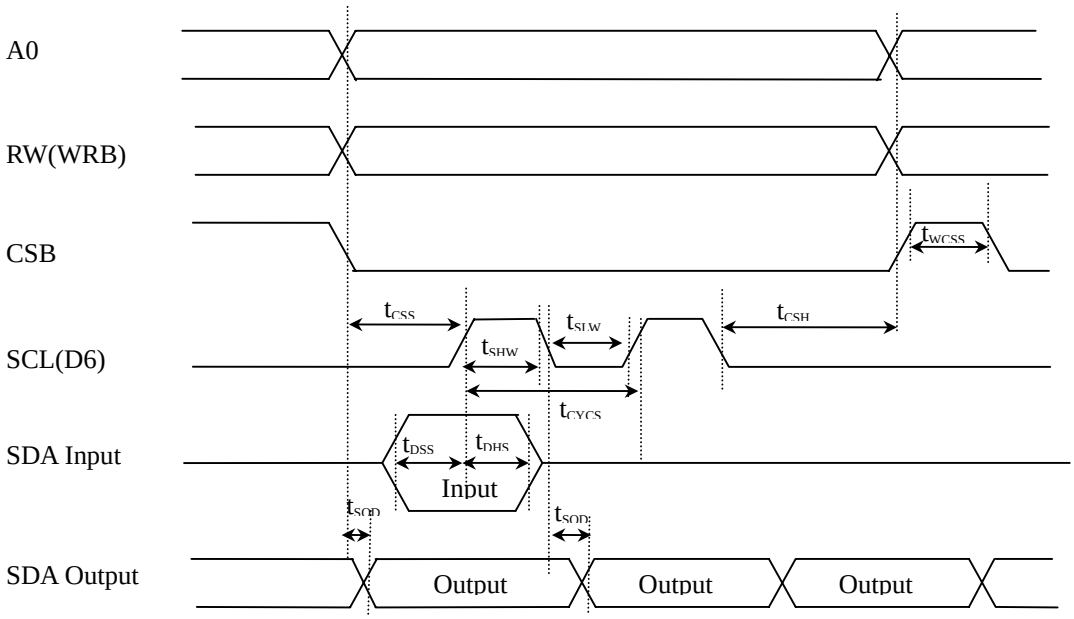


(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
A0 Hold Time	t_{AS6}		50	-	ns	A0
A0 Set Up Time	t_{AH6}		0		ns	
CSB Hold Time	t_{CSH6}		100	-	ns	CSB
CSB Set Up Time	t_{CSS6}		100		ns	
CSB "H" Level Pulse Width	t_{WCS6}		500		ns	
System Cycle Time	t_{CYC6}		2100	-	ns	E
Enable "L" Pulse Width	t_{ELR6}		700		ns	
Enable "H" Pulse Width	t_{EHR6}		1150		ns	
Read Data Out Daley Time	t_{RDD6}	CL=100pF		1150	ns	D7 to D0
Read Data Hold Time	t_{RDH6}		0		ns	

Note) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.
* : (1) Accessed by WRb and RDb signal when CS_1b="L". (2) Accessed by CS_1b signal when WRb and RDb ="L".

- Serial interface timing (5-wire/3-wire)

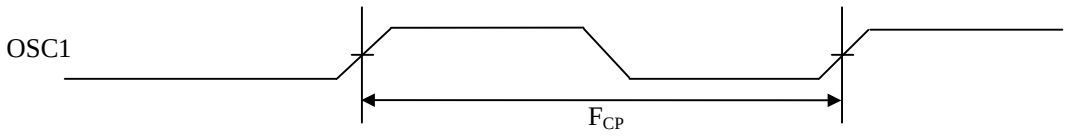


(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial Clock Cycle	t_{CYCS}		650		ns	
SCL “H” Pulse Width	t_{SHW}		300	-	ns	SCL
SCL ”L” Pulse Width	t_{SLW}		300		ns	
Data Set Up Time	t_{DSS}		200	-	ns	SDA
Data Hold Time	t_{DHS}		200		ns	
Serial Data Output Delay Time	t_{SOD}	CL=50pF	-	250	ns	SDA
CSB – SCL Time	t_{CSS}		400		ns	
CSB Hold Time	t_{CSH}		200	-	ns	CSB
CSB "H” Level Pulse Width	t_{WCSS}		200		ns	

Note 13) Each timing is specified based on $0.2xV_{DD}$ and $0.8xV_{DD}$.

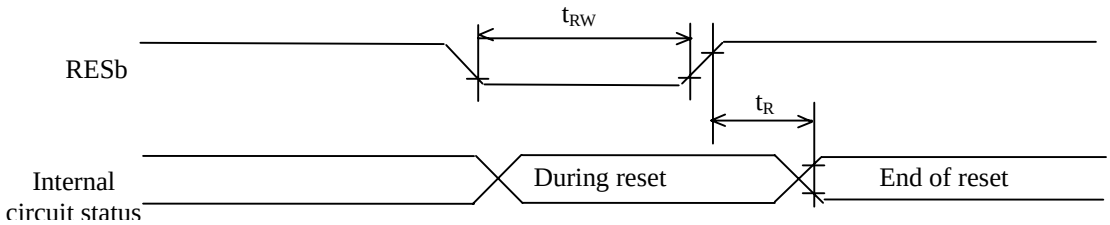
- External clock input timing



(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
External clock frequency	f_{CP}	-	200	OSC1	kHz
External clock duty	duty	35	65		%

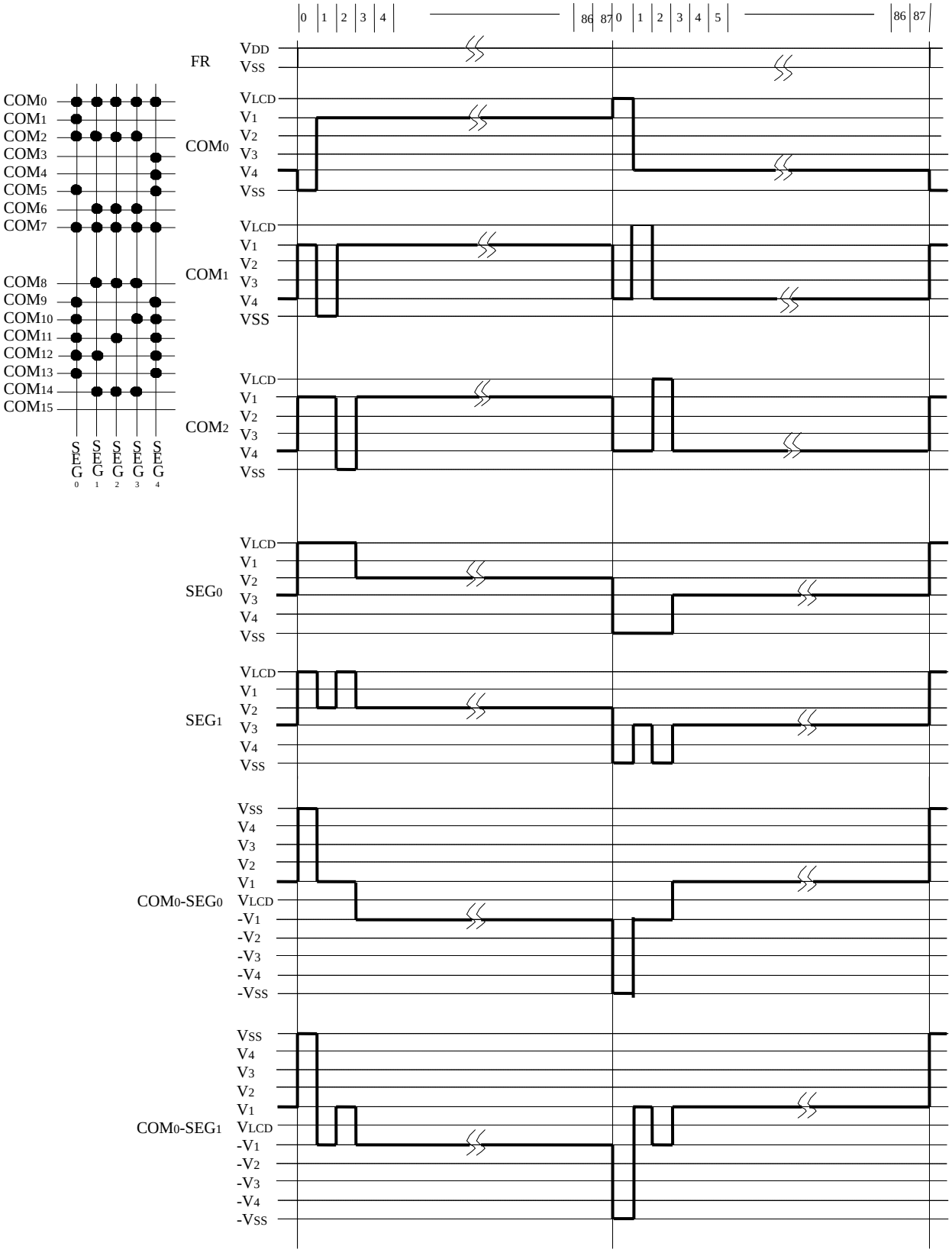
- Reset input timing



(VSS=0V, VDD=2.7 to 5.5V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
Reset Time	t_R	-	1		μs
Reset “L” Puls width	t_{RW}	1	-		ms

■ LCD DRIVING WAVEFORM

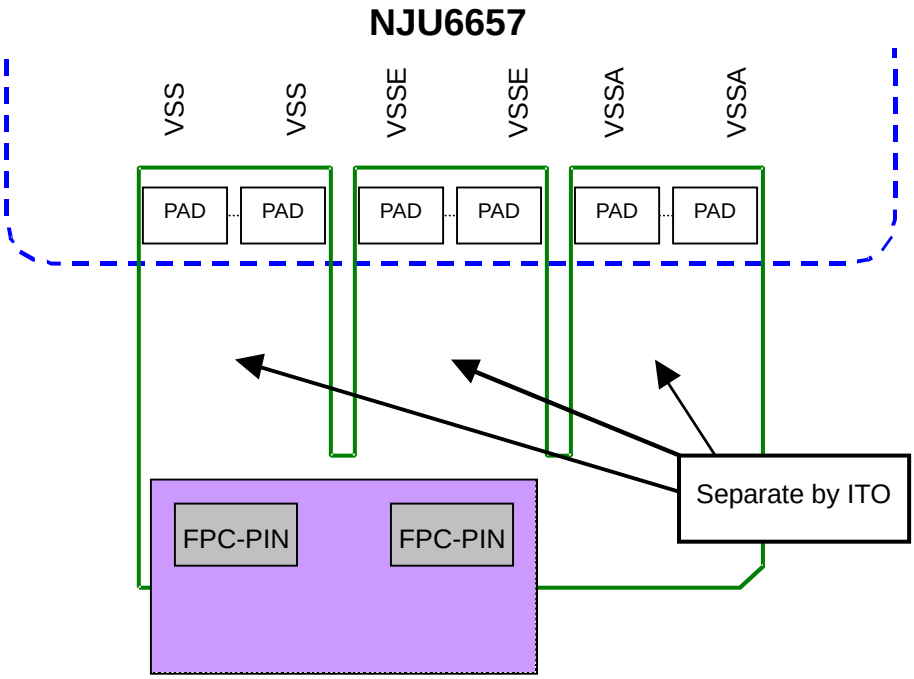


■ Precautions In Mounting COG

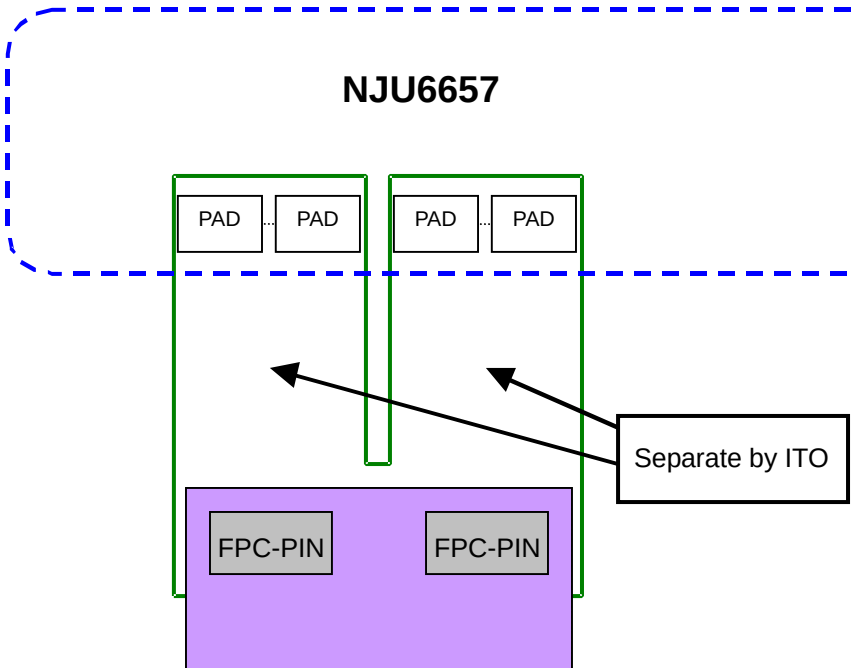
Power supply voltage may drop instantaneously in synchronization with the timing of generating instantaneous current as in the time when the display clock is switched. If the ITO wiring resistance of the power supply pin is high at this time, power supply voltge in the IC chip may greatly, leading to malfunction. To supply stable power to the IC, decrease the wiring impedance of the power line as low as possible.

The ITO layout suggestion is shown as below;

(i) VSS, VSSA, VSSE. (Connects to system GND.)



(**ii**) VDD,VEE. (Connects to system VDD.)



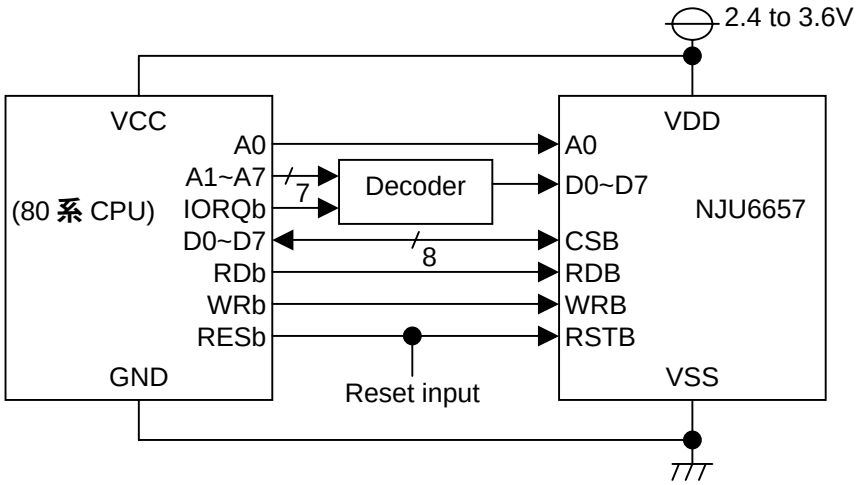
■ APPLICATION CIRCUIT

(1) Microprocessor Interface Example

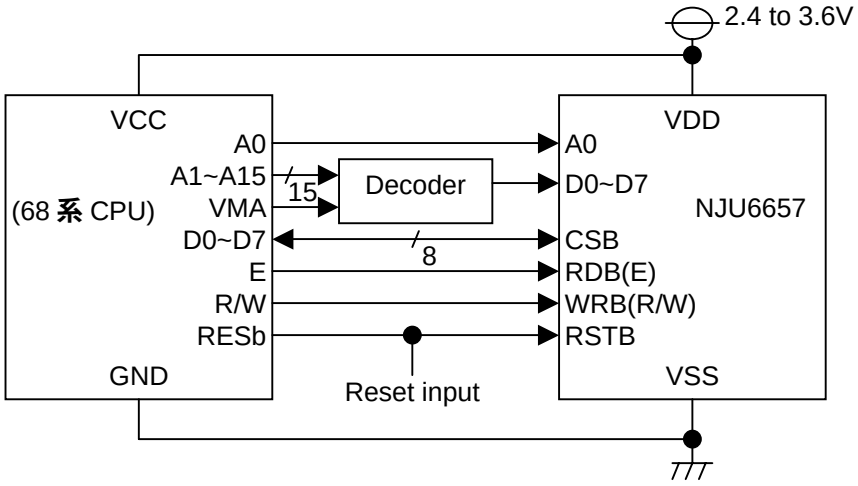
The **NJU6657** interfaces to 80 type or 68 type MPU directly. And the serial interface also communicate with MPU.

* : C86 terminal must be fixed VDD or VSS.

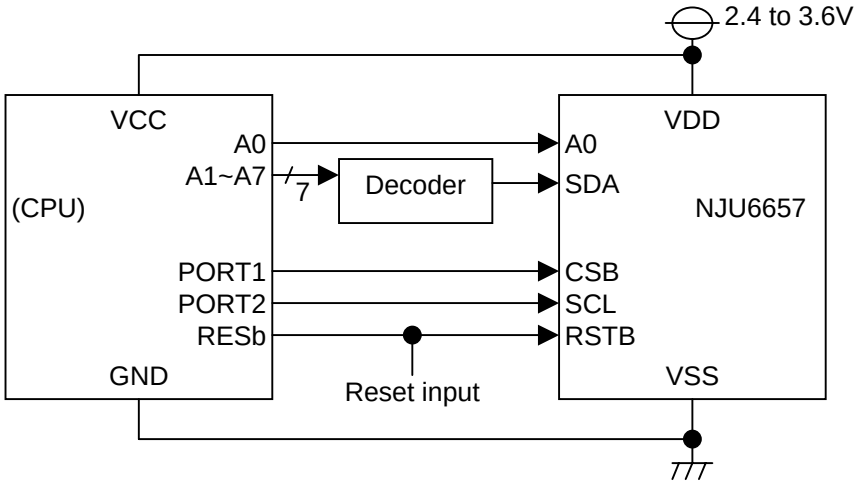
● 80 Type MPU



● 68 Type MPU



● Serial Interface



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