25-common x 100-segment BITMAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6673** is a 25-common x 100-segment bit map LCD driver to display graphics or characters.

It contains 2,500 bits display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.

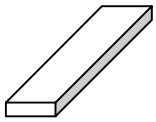
An image data from MPU through the serial or 8-bit parallel interface are stored into the 2,500 bits internal displayed on the LCD panel through the commons and segments drivers.

The **NJU6673** displays 25 x 100 dots graphics or 7-character 2-line by 12 x 13 dots character.

The **NJU6673** contains a built-in OSC circuit for reducing external components. And it features an electrical variable resistor. As result, it reduces the operating current.

The operating voltage from 2.4V to 5.5V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE

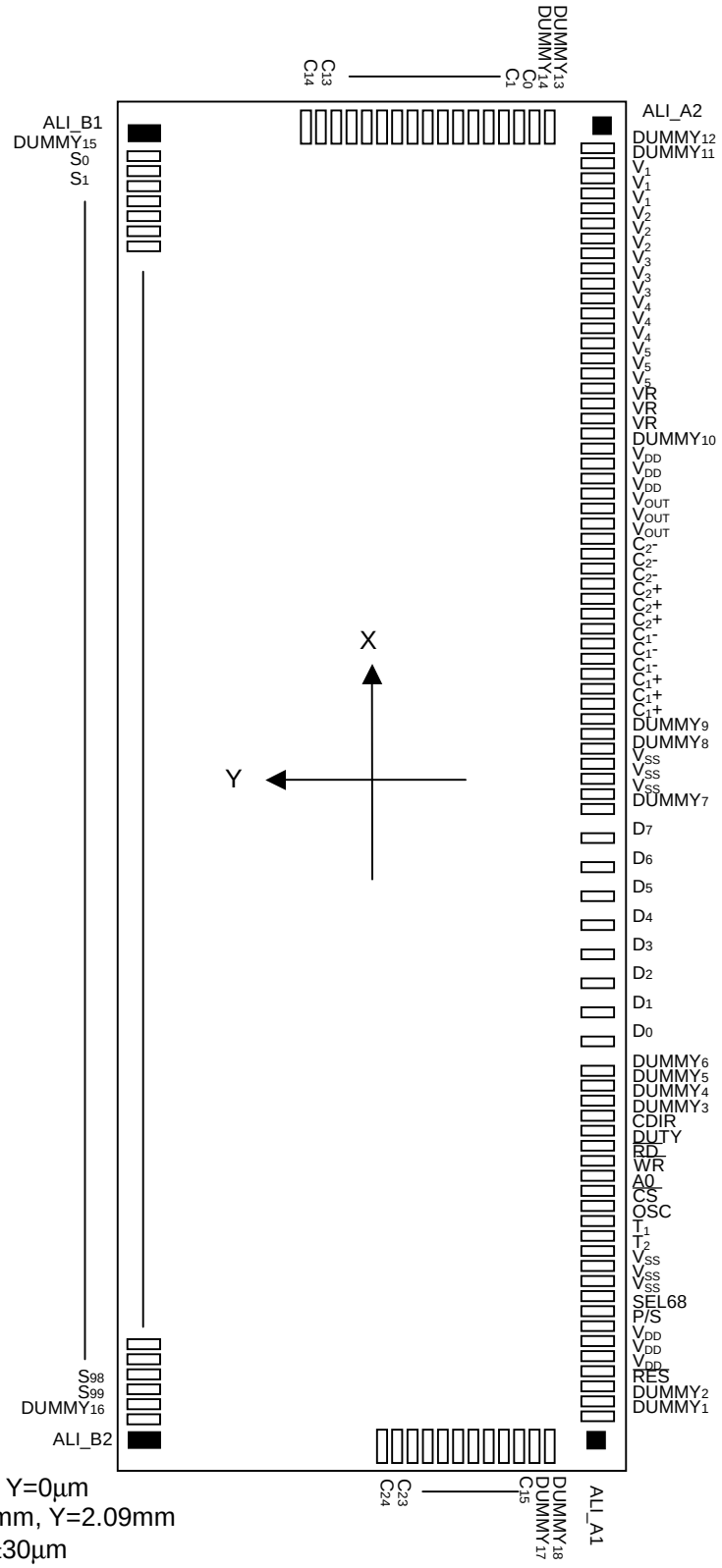


NJU6673CL

■ FEATURES

- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Data RAM 2,500 bits
- LCD Drivers 25-common and 100-segment
- Selectable Duty and Bias Ratio ; 1/25 Duty 1/6 Bias or 1/15 Duty 1/5 Bias
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface (SI, SCL, A0, $\overline{CS}$)
- Useful instruction set
  Display ON/OFF, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Write Display Data, Read Display Data, Normal or Inverse ON/OFF Set, Static Drive ON/Normal Display, EVR Register Set, Read Modify Write, End, Reset, Internal Power Supply ON/OFF, Driver Output ON/OFF, Power Save and ADC select.
- Power Supply Circuits for LCD;
  Available attractive operation for small LCD panel without external capacitors for bias stabilization.
  Booster Circuits(3 times maximum, Voltage boosting polarity : Negative (V_{DD} Common)),
  Regulator, Voltage Follower(x 4)
- Precision Electrical Variable Resistance (16 Steps)
- Low Power Consumption
- Operating Voltage 2.4V to 5.5V
- LCD Driving Voltage 4.0V to 10.0V
- Package Outline Bumped Chip
- C-MOS Technology (Substrate : N)

■ PAD LOCATION



Chip Center : X=0µm, Y=0µm
Chip Size : X=7.54mm, Y=2.09mm
Chip Thickness : 400µm±30µm
Bump Size : 78.16µm x 48.10µm
Pad Pitch : 70µm(Min.)
Bump Height : 15µm(Typ.)
Bump Material : Au
Voltage boosting polarity : Negative Voltage(V_{DD} Common)
Substrate : N

■ TERMINAL DESCRIPTION

Chip Size 7.54x2.09mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X= μm	Y= μm
1	$DUMMY_1$	-3536	-891
2	$DUMMY_2$	-3466	-891
3	$\overline{RES}$	-3396	-891
4	V_{DD}	-3326	-891
5	V_{DD}	-3256	-891
6	V_{DD}	-3186	-891
7	P/S	-3116	-891
8	SEL68	-3046	-891
9	V_{SS}	-2976	-891
10	V_{SS}	-2906	-891
11	V_{SS}	-2836	-891
12	T2	-2766	-891
13	T1	-2696	-891
14	OSC_1	-2626	-891
15	$\overline{CS}$	-2556	-891
16	A0	-2486	-891
17	$\overline{WR}$	-2416	-891
18	$\overline{RD}$	-2346	-891
19	DUTY	-2276	-891
20	CDIR	-2206	-891
21	$DUMMY_3$	-2136	-891
22	$DUMMY_4$	-2066	-891
23	$DUMMY_5$	-1996	-891
24	$DUMMY_6$	-1926	-891
25	D_0	-1715	-891
26	D_1	-1435	-891
27	D_2	-1155	-891
28	D_3	-875	-891
29	D_4	-595	-891
30	D_5	-315	-891
31	D_6(SCL)	-35	-891
32	D_7(SI)	245	-891
33	$DUMMY_7$	455	-891
34	V_{SS}	525	-891
35	V_{SS}	595	-891
36	V_{SS}	665	-891
37	$DUMMY_8$	735	-891
38	$DUMMY_9$	805	-891
39	$C1^+$	875	-891
40	$C1^+$	945	-891
41	$C1^+$	1015	-891
42	$C1^-$	1085	-891
43	$C1^-$	1155	-891
44	$C1^-$	1225	-891
45	$C2^+$	1295	-891
46	$C2^+$	1365	-891
47	$C2^+$	1435	-891
48	$C2^-$	1505	-891
49	$C2^-$	1575	-891
50	$C2^-$	1645	-891

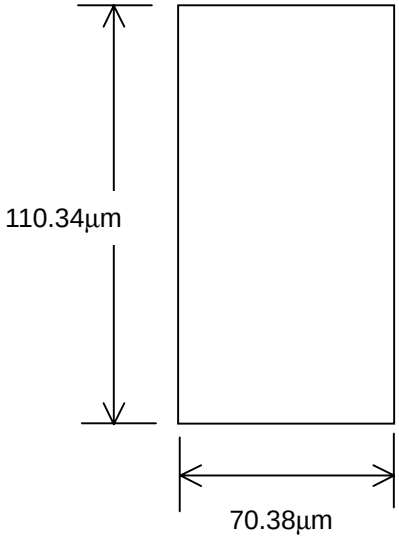
PAD No.	Terminal	X= μm	Y= μm
51	V_{OUT}	1715	-891
52	V_{OUT}	1786	-891
53	V_{OUT}	1856	-891
54	V_{DD}	1926	-891
55	V_{DD}	1996	-891
56	V_{DD}	2066	-891
57	$DUMMY_{10}$	2136	-891
58	VR	2206	-891
59	VR	2276	-891
60	VR	2346	-891
61	V_5	2416	-891
62	V_5	2486	-891
63	V_5	2556	-891
64	V_4	2626	-891
65	V_4	2696	-891
66	V_4	2766	-891
67	V_3	2836	-891
68	V_3	2906	-891
69	V_3	2976	-891
70	V_2	3046	-891
71	V_2	3116	-891
72	V_2	3186	-891
73	V_1	3256	-891
74	V_1	3326	-891
75	V_1	3396	-891
76	$DUMMY_{11}$	3466	-891
77	$DUMMY_{12}$	3536	-891
78	ALI_A2	3616	-891
79	$DUMMY_{13}$	3616	-745
80	$DUMMY_{14}$	3616	-675
81	C_0	3616	-605
82	C_1	3616	-535
83	C_2	3616	-465
84	C_3	3616	-395
85	C_4	3616	-325
86	C_5	3616	-255
87	C_6	3616	-185
88	C_7	3616	-115
89	C_8	3616	-45
90	C_9	3616	25
91	C_{10}	3616	95
92	C_{11}	3616	166
93	C_{12}	3616	236
94	C_{13}	3616	306
95	C_{14}	3616	376
96	ALI_B1	3616	873
97	$DUMMY_{15}$	3536	891
98	S_0	3466	891
99	S_1	3396	891
100	S_2	3326	891

PAD No.	Terminal	X= µm	Y= µm
101	S_3	3256	891
102	S_4	3186	891
103	S_5	3116	891
104	S_6	3046	891
105	S_7	2976	891
106	S_8	2906	891
107	S_9	2836	891
108	S_{10}	2766	891
109	S_{11}	2696	891
110	S_{12}	2626	891
111	S_{13}	2556	891
112	S_{14}	2486	891
113	S_{15}	2416	891
114	S_{16}	2346	891
115	S_{17}	2276	891
116	S_{18}	2206	891
117	S_{19}	2136	891
118	S_{20}	2066	891
119	S_{21}	1996	891
120	S_{22}	1926	891
121	S_{23}	1856	891
122	S_{24}	1786	891
123	S_{25}	1715	891
124	S_{26}	1645	891
125	S_{27}	1575	891
126	S_{28}	1505	891
127	S_{29}	1435	891
128	S_{30}	1365	891
129	S_{31}	1295	891
130	S_{32}	1225	891
131	S_{33}	1155	891
132	S_{34}	1085	891
133	S_{35}	1015	891
134	S_{36}	945	891
135	S_{37}	875	891
136	S_{38}	805	891
137	S_{39}	735	891
138	S_{40}	665	891
139	S_{41}	595	891
140	S_{42}	525	891
141	S_{43}	455	891
142	S_{44}	385	891
143	S_{45}	315	891
144	S_{46}	245	891
145	S_{47}	175	891
146	S_{48}	105	891
147	S_{49}	35	891
148	S_{50}	-35	891
149	S_{51}	-105	891
150	S_{52}	-175	891

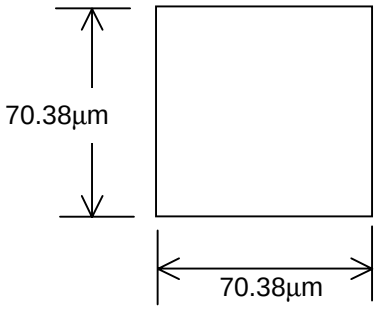
PAD No.	Terminal	X= µm	Y= µm
151	S_{53}	-245	891
152	S_{54}	-315	891
153	S_{55}	-385	891
154	S_{56}	-455	891
155	S_{57}	-525	891
156	S_{58}	-595	891
157	S_{59}	-665	891
158	S_{60}	-735	891
159	S_{61}	-805	891
160	S_{62}	-875	891
161	S_{63}	-945	891
162	S_{64}	-1015	891
163	S_{65}	-1085	891
164	S_{66}	-1155	891
165	S_{67}	-1225	891
166	S_{68}	-1295	891
167	S_{69}	-1365	891
168	S_{70}	-1435	891
169	S_{71}	-1505	891
170	S_{72}	-1575	891
171	S_{73}	-1645	891
172	S_{74}	-1715	891
173	S_{75}	-1786	891
174	S_{76}	-1856	891
175	S_{77}	-1926	891
176	S_{78}	-1996	891
177	S_{79}	-2066	891
178	S_{80}	-2136	891
179	S_{81}	-2206	891
180	S_{82}	-2276	891
181	S_{83}	-2346	891
182	S_{84}	-2416	891
183	S_{85}	-2486	891
184	S_{86}	-2556	891
185	S_{87}	-2626	891
186	S_{88}	-2696	891
187	S_{89}	-2766	891
188	S_{90}	-2836	891
189	S_{91}	-2906	891
190	S_{92}	-2976	891
191	S_{93}	-3046	891
192	S_{94}	-3116	891
193	S_{95}	-3186	891
194	S_{96}	-3256	891
195	S_{97}	-3326	891
196	S_{98}	-3396	891
197	S_{99}	-3466	891
198	$DUMMY_{16}$	-3536	891
199	ALI_B2	-3616	873
200	C_{24}	-3616	25

PAD No.	Terminal	X= µm	Y= µm
201	C_{23}	-3616	-45
202	C_{22}	-3616	-115
203	C_{21}	-3616	-185
204	C_{20}	-3616	-255
205	C_{19}	-3616	-325
206	C_{18}	-3616	-395
207	C_{17}	-3616	-465
208	C_{16}	-3616	-535
209	C_{15}	-3616	-605
210	$DUMMY_{17}$	-3616	-675
211	$DUMMY_{18}$	-3616	-745
212	ALI_A1	-3616	-891

- Alignment marks



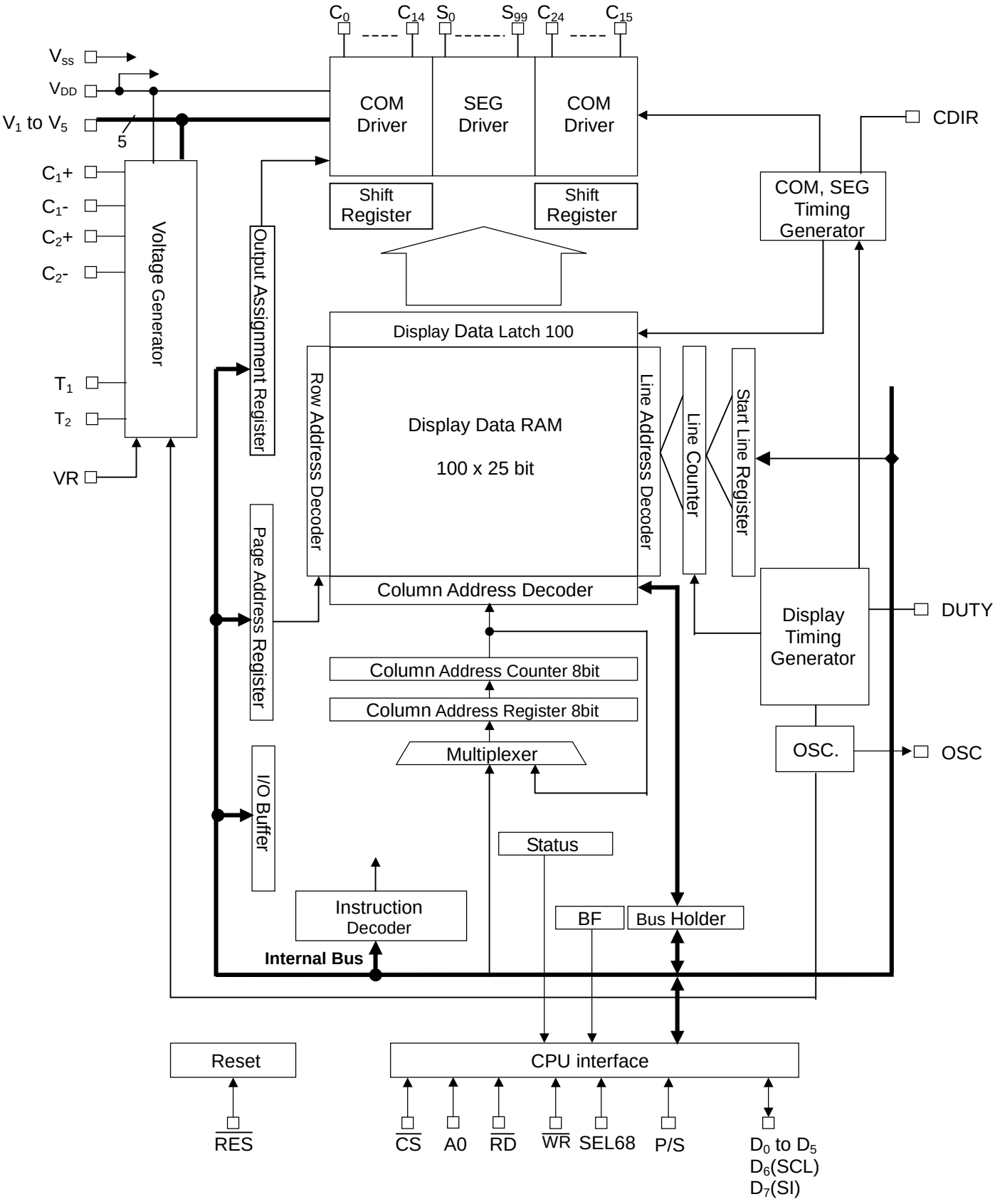
ALI_B1, ALI_B2



ALI_A1, ALI_A2

Note) Alignment Marks are not contains window.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1,
2,
21-
24,
33,
37,
38,
57,
76,
77,
79,
80,
97,
198,
210,
211</td><td>DUMMY$_1$
DUMMY$_2$
DUMMY$_3$ -
DUMMY$_6$
DUMMY$_7$
DUMMY$_8$
DUMMY$_9$
DUMMY$_{10}$
DUMMY$_{11}$
DUMMY$_{12}$
DUMMY$_{13}$
DUMMY$_{14}$
DUMMY$_{15}$
DUMMY$_{16}$
DUMMY$_{17}$
DUMMY$_{18}$</td><td></td><td>Dummy Terminal.
These are open terminals electrically.</td></tr>
<tr><td>4,5,6,
54-56</td><td>V_{DD}</td><td>Power</td><td>Power supply terminal. (+2.4 to +5.5V)</td></tr>
<tr><td>9-11,
34-36</td><td>V_{SS}</td><td>GND</td><td>Ground terminal. (0V)</td></tr>
<tr><td>73-75
70-72
67-69
64-66
61-63</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminals.
In case of external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation.
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$
In case of internal power supply, LCD driving voltages V_1 to V_4 depending on the bias selection are supplied as shown in follows;
<table>
<tr><th>Duty</th><th>Bias</th><th>V_1</th><th>V_2</th><th>V_3</th><th>V_4</th></tr>
<tr><td>1/15 Duty</td><td>1/5 Bias</td><td>V_5+4/5 V_{LCD}</td><td>V_5+3/5 V_{LCD}</td><td>V_5+2/5 V_{LCD}</td><td>V_5+1/5 V_{LCD}</td></tr>
<tr><td>1/25 Duty</td><td>1/6 Bias</td><td>V_5+5/6 V_{LCD}</td><td>V_5+4/6 V_{LCD}</td><td>V_5+2/6 V_{LCD}</td><td>V_5+1/6 V_{LCD}</td></tr>
</table>
$V_{LCD}=V_{DD}-V_5$</td></tr>
<tr><td>39-41
42-44
45-47
48-50</td><td>C_1+
C_1-
C_2+
C_2-</td><td>O</td><td>Condenser connecting terminals for internal Voltage Booster.
Boosting time is selected by each connected condenser.
In case of 3-time boost operation, connect the condenser between C_1+ and C_1-, C_2+ and C_2-.
In case of 2-time boost operation, connect the condenser between C_2+ and C_2-, connect C_2+ to C_1+, and C_1- should be open.</td></tr>
<tr><td>51-53</td><td>V_{OUT}</td><td>O</td><td>Boosted voltage output terminal. Connects the capacitor between V_{OUT} terminal and V_{SS}.</td></tr>
<tr><td>58-60</td><td>VR</td><td>I</td><td>V_{LCD} voltage adjustment terminal. The gain of V_{LCD} setup circuit for V_5 level is adjusted by external resistor.</td></tr>
<tr><td>13
12</td><td>T_1,
T_2</td><td>I</td><td>LCD bias voltage control terminals.
<table>
<tr><th>T_1</th><th>T_2</th><th>Voltage booster circuit</th><th>Voltage adjustor</th><th>V/F circuit</th></tr>
<tr><td>L</td><td>H/L</td><td>Available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>L</td><td>Not available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>H</td><td>Not available</td><td>Not available</td><td>Available</td></tr>
</table></td></tr>
<tr><td>25
26
27
28
29
30
31
32</td><td>D_0
D_1
D_2
D_3
D_4
D_5
D_6(SCL)
D_7(SI)</td><td>I/O</td><td>Data input / output terminals.
In parallel interface Mode (P/S=”H”)
I/O terminals of 8-bit bus.
In Serial interface Mode(P/S=”L”)
D_7:Input terminal of serial data (SI).
D_6:Input terminal of serial data clock (SCL).
D_5 to D_0 terminals are High impedance.
When $\overline{CS}$=”H” , D_0 to D_7 terminals are high-impedance.</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>16</td><td>A0</td><td>I</td><td>Data discremination signal input terminal. The signal from MPU discreminates transmitted data between Display data and Instruction.
<table>
<tr><td>A0</td><td>H</td><td>L</td></tr>
<tr><td>Discremination</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>3</td><td>$\overline{RES}$</td><td>I</td><td>Reset terminal.
Reset operation is executing during “L” state of $\overline{RES}$.</td></tr>
<tr><td>15</td><td>$\overline{CS}$</td><td>I</td><td>Chip select signal input terminal.
Data Input/Output are available during $\overline{CS}$ ="L".</td></tr>
<tr><td>18</td><td>$\overline{RD}$ (E)</td><td>I</td><td>$\overline{RD}$(80 type) or E(68 type) signal input terminal.
<In 80 type MPU mode>(SEL68=”L”)
$\overline{RD}$ signal from 80 type MPU input terminal. Active”L”.
D_0 to D_7 terminals are output during ”L” level.
<In 68 type MPU mode>(SEL68=”H”)
Enable signal from 68 type MPU input terminal. Active "H"</td></tr>
<tr><td>17</td><td>$\overline{WR}$(R/W)</td><td>I</td><td>$\overline{WR}$ (80 type) or $\overline{R/W}$(68 type) signal input terminal.
<In 80 Type MPU mode>(SEL68=”L”)
$\overline{WR}$ signal from 80 type MPU input . Active "L".
The data transmitted during $\overline{WR}$=”L” are fetched at the rising edge of $\overline{WR}$.
<In 68 Type MPU mode>
R/w signal from 68 type MPU input terminal.
<table>
<tr><td>$\overline{R/W}$</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>8</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal.
This terminal must connect to V_{DD} or V_{SS}
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 type</td><td>80 type</td></tr>
</table></td></tr>
<tr><td>7</td><td>P/S</td><td>I</td><td>Parallel or Serial interface selection signal input terminal.
<table>
<tr><td>P/S</td><td>Inter face</td><td>Chip Select</td><td>Data /Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr>
<tr><td>“H”</td><td>Parallel</td><td>$\overline{CS}$</td><td>A0</td><td>D_0-D_7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>-</td></tr>
<tr><td>“L”</td><td>Serial</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr>
</table>
In case of the serial interface (P/S="L")
RAM data and status read operation do not work in mode of the serial interface. $\overline{RD}$ and $\overline{WR}$ terminals must fix to "H" or "L".
D_0 to D_5 terminals are high impedance.</td></tr>
<tr><td>14</td><td>OSC</td><td>O</td><td>Maker Testing Clock output terminal.
The terminal is recommended to open.</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>81-95</td><td>C_0-C_{14}</td><td>O</td><td rowspan="3">LCD driving signal output terminals.
● Common output terminals :C_0 to C_{24}
● Segment output terminals :S_0 to S_{99}
• Common Output Terminal
Following output voltages is selected by the combination of alternating(FR) signal and Common scanning data.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table>
• Segment output terminal
Following output voltages is selected by the combination of alternating(FR) signal and display data in the DD RAM.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>98-197</td><td>S_0-S_{99}</td><td>O</td></tr>
<tr><td>200-209</td><td>C_{24}-C_{15}</td><td>O</td></tr>
<tr><td>19</td><td>DUTY</td><td>I</td><td>Duty and Bias selection terminal.
<table>
<tr><th>DUTY</th><th>Duty</th><th>Bias</th></tr>
<tr><td>H</td><td>1/15</td><td>1/5</td></tr>
<tr><td>L</td><td>1/25</td><td>1/6</td></tr>
</table></td></tr>
<tr><td>20</td><td>CDIR</td><td>I</td><td>Common Driver Assignment selection terminal.
<table>
<tr><th>CDIR</th><th>Common Output terminals</th></tr>
<tr><td>H</td><td>Reverse ($C_{24}\rightarrow C_0$)</td></tr>
<tr><td>L</td><td>Normal ($C_0\rightarrow C_{24}$)</td></tr>
</table></td></tr>
</table>

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Busy Flag (BF)

The Busy Flag (BF) is set to logical "1" in busy of internal execution by an instruction, and any instruction excepting for the "Status Read" is disable at this time. Busy Flag is outputted through D_7 terminal by "Status Read" instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in ■ BUS TIMING CHARACTERISTICS is secured completely.

(1-2) Display Start Line Register

The Display Start Line Register is a register to set a display data RAM address corresponding to the COM_0 display line (the top line normally) for the vertical scroll on the LCD, Page address change and so forth. The Display Start Line Address set instruction sets the 8-bit display start address into this register.

(1-3) Line Counter

Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6673**.

(1-4) Column Address Counter

Column Address Counter is the 8-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Fig. 1. The counter is incremented automatically after the display data read/write instructions execution. When the Column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Page Address Register.

By the address inverse instruction (ADC select) as shown in Fig. 1, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Page Address Register

Page Address Register assigns the page address of the display data RAM as shown in Fig. 1. In case of accessing from the MPU with changing the page address, Page Address Set instruction is required.

(1-6) Display Data RAM

The Display data RAM (DD RAM) is the bit map RAM consisting of 2,500 bits to store the display data corresponding to the LCD pixel on LCD panel.

In Normal Display : "1" Turn-On Display, "0"=Turn-Off Display
In Reveres Display : "1" Turn-Off Display, "0"=Turn-On Display

DD RAM output 100 bits parallel data addressed by line address counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the MPU and latch to the display data latch operation are done independently.

(1-7) Common Driver Assignment

The scanning order can be assigned by set Common Driver Assignment selection terminal as shown on Table 1.

Table 1 Common Driver Order Assignment

		COM Outputs Terminals					
	PAD No.	81		95	200		209
	Pin name	C_0		C_{14}	C_{24}		C_{15}
COM Driver Assignment selection terminal	"L"	COM_0	→	COM_{14}	COM_{24}	←	COM_{15}
	"H"	COM_{24}	←	COM_{10}	COM_0	→	COM_9

The duty ratio setting and output assignment register are so controlled to operate independently that duty ratio setting required to corresponding duty ratio for output assignment.

Page Address	Data	Display Pattern									Line Address	COM output example 1	COM output example 2
D_1, D_0 (0, 0)	D_0	■				■		Page 0			00	C_{17}	
	D_1	■				■					01	C_{18}	
	D_2	■	■			■					02	C_{19}	
	D_3	■		■		■					03	C_{20}	
	D_4	■			■	■					04	C_{21}	
	D_5	■				■					05	C_{22}	COM
	D_6	■				■					06	C_{23}	output
	D_7										07	C_{24}	example 2
D_1, D_0 (0, 1)	D_0							Page 1			08	C_0	C_0
	D_1										09	C_1	C_1
	D_2										0A	C_2	C_2
	D_3										0B	C_3	C_3
	D_4										0C	C_4	C_4
	D_5										0D	C_5	C_5
	D_6										0E	C_6	C_6
	D_7										0F	C_7	C_7
D_1, D_0 (1, 0)	D_0							Page 2			10	C_8	C_8
	D_1										11	C_9	C_9
	D_2										12	C_{10}	C_{10}
	D_3										13	C_{11}	C_{11}
	D_4										14	C_{12}	C_{12}
	D_5										15	C_{13}	C_{13}
	D_6										16	C_{14}	C_{14}
	D_7										17	C_{15}	
D_1, D_0(1, 1)	D_0							Page 3			18	C_{16}	
Column Address(ADC)	D_0=0	00	01	02	03	04	05	••••••••••	62	63			
	D_0=1	63	62	61	60	5F	5E	••••••••••	01	00			

Segment output	S_0	S_1	S_2	S_3	S_4	S_5	••••••••••	S_{98}	S_{99}

COM output example1 : 1/25Duty, set Display Start Line 08_H
COM output example2 : 1/15Duty, set Display Start Line 08_H

Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit

Reset circuit operates the following initializations when the condition of $\overline{RES}$ terminal goes to "L" level.

- Initialization
  1. Display Off
  2. Normal Display (Non-inverse display)
  3. ADC Select : Normal (ADC Instruction D_0="0")
  4. Read Modify Write Mode Off
  5. Voltage Booster off, Voltage Regulator off, Voltage follower off
  6. Clear the serial interface register
  7. Driver Output Off
  8. Set the Display Start Line Register to 00_H
  9. Set the Column Address Counter to 00_H
  10. Set the Page Address Register to page "0"
  11. Set the EVR register to 00_H

The $\overline{RES}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in "the MPU interface" in the Application Circuit section. The "L" level input signal as reset signal must keep the period over than 10μs as shown in DC Characteristics. The **NJU6673** takes 1μs for the reset operation after the rising edge of the $\overline{RES}$ signal.

The reset operation by $\overline{RES}$ ="L" initializes each resister setting as above reset status, but the internal oscillation circuit and output terminals (D_0 to D_7) are not affected.

To avoid the lock-up, the reset operation by the $\overline{RES}$ terminal must be required every time when power terns on. The reset operation by the reset instruction, function 8 to 11 operations mentioned above is performed.

The $\overline{RES}$ terminal must be keep "L" level when the power terns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving

(a) LCD Driving Circuits

LCD driver is 125 sets of multiplexer consisting of 100 segments and 25 commons drivers to output LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in ■ LCD DRIVING WAVEFORM.

(b) Display Data Latch Circuits

Display Data Latch Circuit latches the 100 bits display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display, Display On/Off, Static drive On/Off instruction processes only stored data in this Display Data Latch Circuit.

(c) Line Counter and Latch signal of Latch Circuits

The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 100 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to LCD driving circuits.

The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(d) Display Timing Generaton Circuit

The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

(e) Common Timing Generation

The Common Timing Generator generates the common timing signal from the display clock (CL).

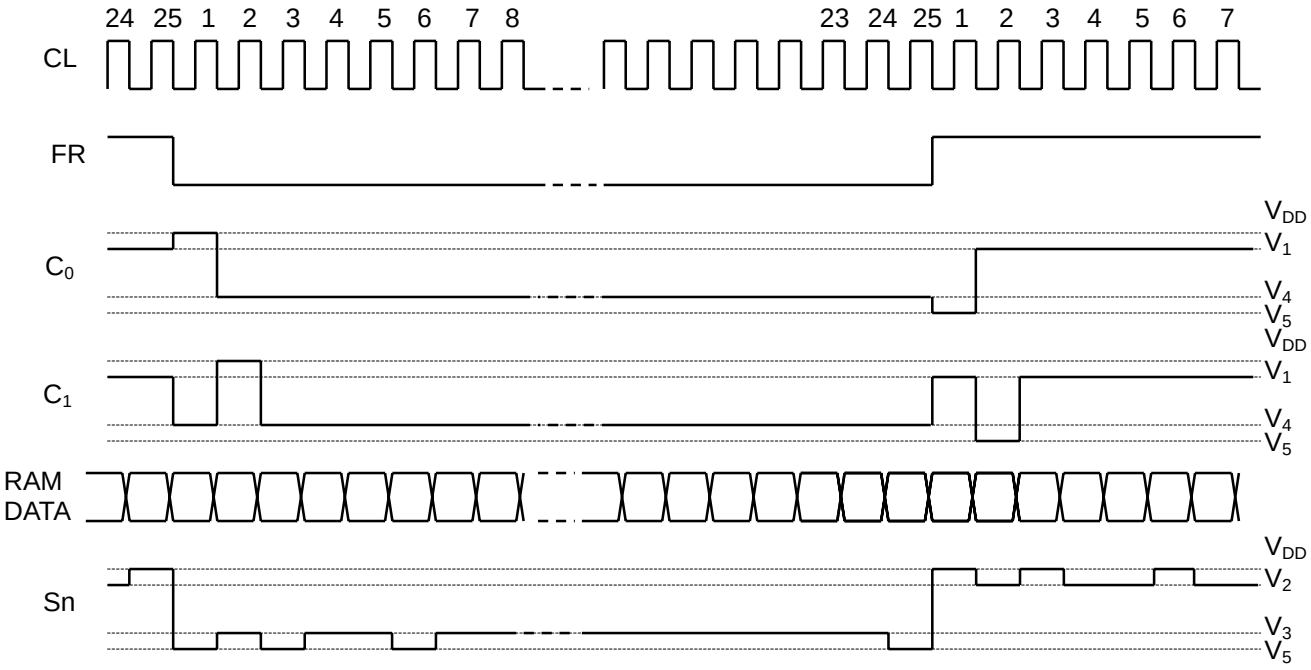


Fig. 2

(f) Oscillation Circuit

The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

Table 2 The relation between duty and divide

Duty	1/15	1/25
Divide	1/10	1/6

(g) Power Supply Circuit

The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (3-Time maximum), voltage regulator circuits, and voltage followers.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4, V_5 and V_{OUT} for the LCD should be supplied from outside, terminals C_1+, C_1-, C_2+, C_2- and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminals. Furthermore the external power supply operates with some of internal power supply function.

Table3 The Relation Between Power Supply Circuit And T_1, T_2 Terminal

T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Power Supply	C_1+, C_1-, C_2+, C_2-	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5, V_{OUT}	Open	Open

When (T_1, T_2)=(H, L), C_1+, C_1-, C_2+, C_2- terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

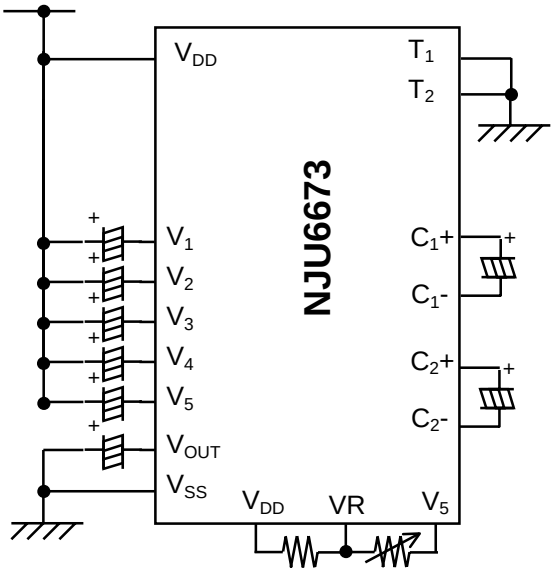
When (T_1, T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6673** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition.

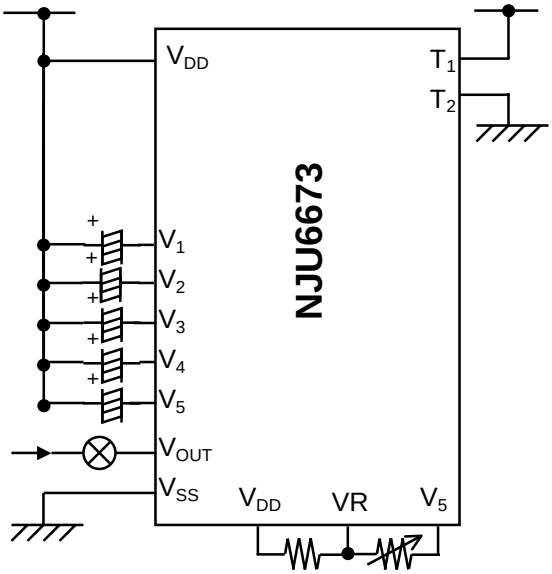
The external capacitors to V_1 to V_5 for Bias voltage stabilization may be removed in use of small size LCD panel. The equivalent load of LCD panel may be changed depending on display patterns. Therefore, it require display quality check on various display patterns actually without external capacitors. If the display quality is not so good, external capacitors should connects as show in (3-4)LCD Driving Voltage Generation Circuits -Fig. 4. (If no need external capacitors as result of experiment, the application patterns (wiring) should be prepared for recovery.)

○ Power Supply applications

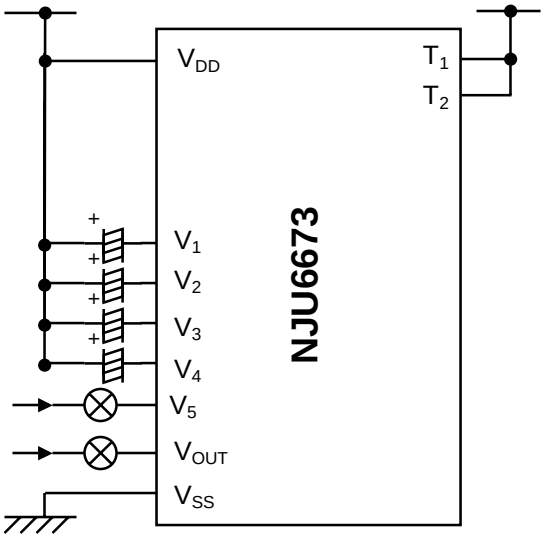
(1) Internal power supply example.
All of the Internal Booster, Voltage Regulator, Voltage Follower using.
Internal power supply ON (instruction)
(T_1, T_2)=(L, L)



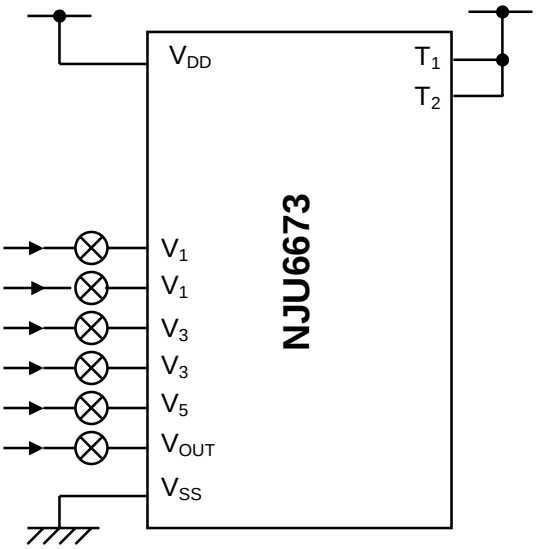
(2) Only V_{OUT} Supply from outside Example.
Internal Voltage Regulator,
Voltage Follower using
Internal power supply ON (Instruction)
(T_1, T_2)=(H, L)



(3) V_{OUT} and V_5 supply from outside Example.
Internal Voltage Follower using.
Internal power supply (Instruction)
(T_1, T_2)=(H, H)



(4) External Power Supply Example.
All of V_1 to V_5 and V_{OUT} supply from outside
Internal power supply (Instruction)
(T_1, T_2)=(H, H)



⊗: These switches should be open during the power save mode.

(2) Instruction

The **NJU6673** distinguishes the signal on the data bus D_0 to D_7 as an Instruction by combination of A0 , $\overline{RD}$ and $\overline{WR}$(R/W). The decode of the instruction and execution performs with only high speed Internal timing without relation to the external clock. Therefore no busy flag check required normally. In case of serial interface, the data input as MSB(D_7) first serially. The Table. 4 shows the instruction codes of the **NJU6673**.

Table 4 Instruction Code

(*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(a)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display ON/OFF D_0=0:OFF D_0=1:ON
(b)	Display Start Line Set	0	1	0	0	1	*	Start address					Determine the Display Line of RAM to COM $_0$
(c)	Page Address Set	0	1	0	1	0	1	1	*	*	Page Address		Set the page of DD RAM to the Page Address Register
(d)	Column Address Set High Order 3bits	0	1	0	0	0	0	1	0	High Order Column			Set the Higher order 3 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add				Set the Lower order 4 bits Column Address to the Reg.
(e)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(f)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(g)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(h)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the ON and OFF Display
(i)	Static Drive ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns ON D_0=0: Normal D_0=1: Whole Disp. ON
(j)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V_5 output level to the EVR register
(k)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when writing but no-change when reading
(l)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify write Mode
(m)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the Internal Circuits
(n)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0/1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(o)	Driver Outputs ON/OFF	0	1	0	1	0	1	0	1	0	1	0/1	D_0=0: LCD Driver Outputs OFF D_0=1: LCD Driver Outputs ON
(p)	Power Save (Complex command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power Save Mode (LCD Display OFF + Static Drive ON)
(q)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment D_0=0 :Normal D_0= 1:Inverse

(2-1) Explanation of Instruction Code

(a) Display On/Off

It executes the On/Off control of the whole display without relation to the DD RAM or any internal conditions.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Display Start Line

It sets the DD RAM line address corresponding to the COM_0 terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	*	A_4	A_3	A_2	A_1	A_0

A_4	A_3	A_2	A_1	A_0	Line Address(HEX)
0	0	0	0	0	00
0	0	0	0	1	01
		:			:
		:			:
1	1	0	0	0	18

(c) Page Address Set

When MPU accesses to the DD RAM, a page address is set by page Address Set instruction before writing the data (Note:the change of page address is not affected to the display).

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	*	*	A_1	A_0

*:Don't Care

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

(d) Column Address

When MPU accesses to the DD RAM, row address set by Page Address Set instruction is required with the column address before writing the data. The column address set requires twice address set which are higher order 3 bits address set and lower order 4 bits. When the MPU accesses to the DDRAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of the column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	0	0	1	0	A_6	A_5	A_4	Higher Order
0	1	0	0	0	0	0	A_3	A_2	A_1	A_0	Lower Order

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address (HEX)
0	0	0	0	0	0	0	00
0	0	0	0	0	0	1	01
			:				:
			:				:
1	1	0	0	0	1	1	63

(e) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET" as follows.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY:BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0: Counterclockwise Output (Inverse)
1: Clockwise Output (Normal)
Note) The data “0=Inverse” and “1=Normal” of ADC status is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF: Indicate the whole display On/Off status.
0: Whole Display "On”
1: Whole Display "Off"
Note) The data "0=On" and "1=Off" of Display On/Off status is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET :Indicate the initializing by $\overline{RES}$ signal or reset instruction.
0: Not Reset status
1: In the Reset status

(f) Write Display Data

It writes the data on the data bus into the DD RAM column address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuosly without the address setting at every writing time once the starting address is set.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write Data							

(g) Read Display Data

This instruction reads out the 8-bit data from DD RAM addressed by the column and the page address.The column address automatically increments after the 8-bit read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see"(4-4)Access to the DD RAM and the Internal Register"). In the serial interface mode, the display data is unable to read out.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read Data							

(h) Normal or Inverse On/Off Set

It changes the display condition of normal or reverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"

1: Inverse RAM data "0" correspond to "On"

(i) Static Drive

This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the "Normal or Inverse On/Off Set" instruction.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display

1: Whole Display turns On

(j) EVR Register Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage "V_5". By data setting into the EVR register, the LCD driving voltage "V_5" selects out of 16 steps of regulated voltage. The voltage adjustable range of "D_5" is fixed by the external resistors. For details, refer the section"(3-2) Voltage Adjust Circuits".

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	0	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	V_{LCD}
0	0	0	0	Low
		:		:
		:		:
1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$

When EVR doesn't use, set the EVR register to (0,0,0,0).

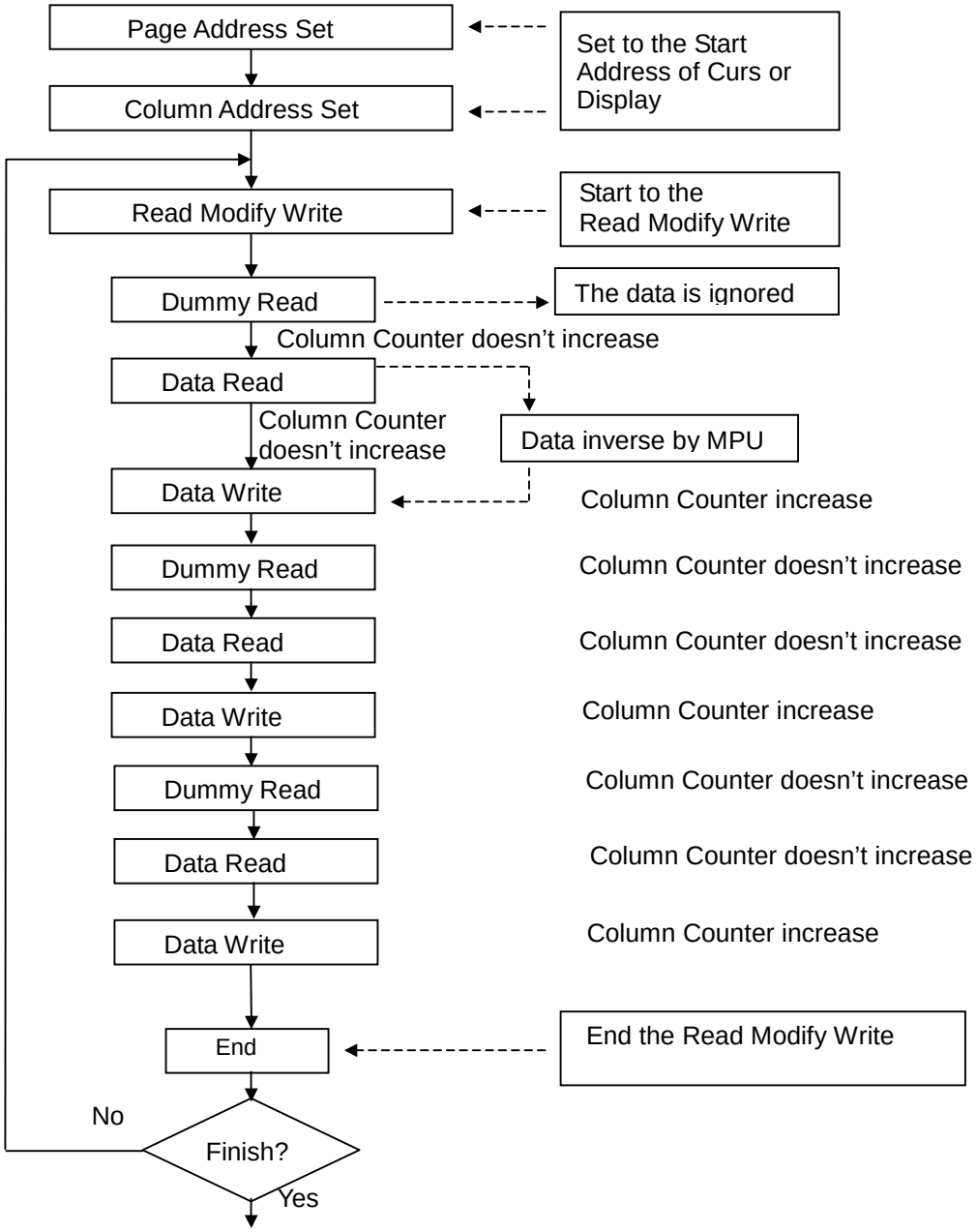
(k) Read Modify Write

This instruction sets the Read Modify Write controlling the page address increment. In this mode, the Column Address only increments when execute the display data "Write instruction; but no change when the display data "Read " Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Address goes back to the start address before the execution of this "Read Modify Write" instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink)

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	0	0	0	0

Note) In this "Read Modify Write" mode, out of display data "Read"/"Write", any instructions except "Column Address Set" can be executed.

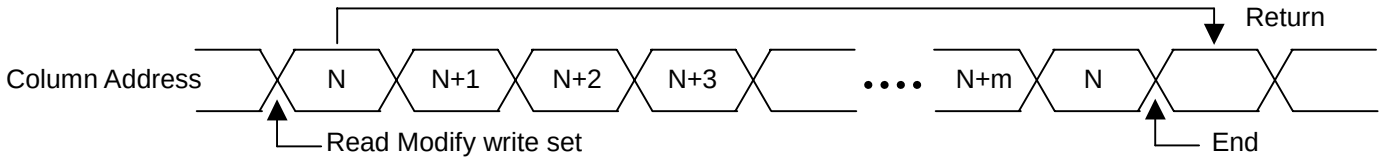
● The Example of Read Modify Write Sequence



(l) End

This instruction releases the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	1	1	1	0



(m) Reset

This instruction executes the following initialization. The reset by the reset signal input to the $\overline{RES}$ terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

1) Set the Display Start Line Register to 00_H.
2) Set the Column Address Counter to 00_H.
3) Set the page Page Address Register to page “0”.
4) Set the EVR Register to 0_H.

The DD RAM is not affected of this initialization.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	0	0	1	0

(n) Internal Power Supply ON/OFF

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, V_{DD} and V_{LCD}. Therefore it requires the actual evaluation using the LCD module to get the correct time.(Refer to the (3-4) Fig.4)

(o) Driver Outputs ON/OFF

This instruction controlls ON/OFF of the LCD Driver Outputs.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	0	1	D

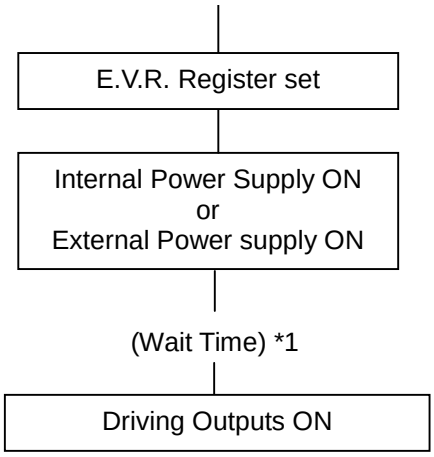
D 0: LCD driving waveform output Off
1: LCD driving waveform output On

The **NJU6673** implements low power LCD driving voltage generator circuit and requires the following Power supply ON/OFF sequence.

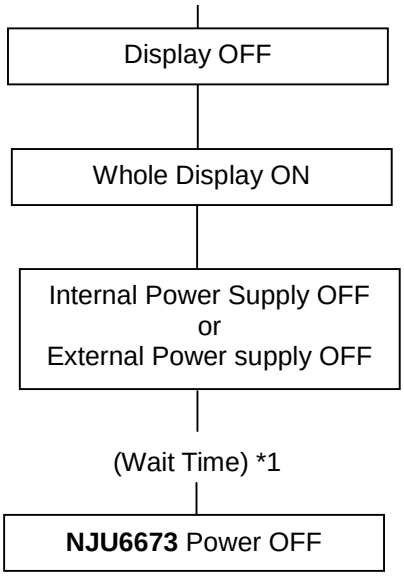
- LCD Driving power supply ON/OFF sequences

The sequences below are required when the power supply turns ON/OFF.For the power supply turning on operation after the power-save mode, refer the “power save release sequence” mentioned after.

Turn ON sequence



Turn OFF sequence



*1 : The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$ External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctly, test by using the actual LCD module.

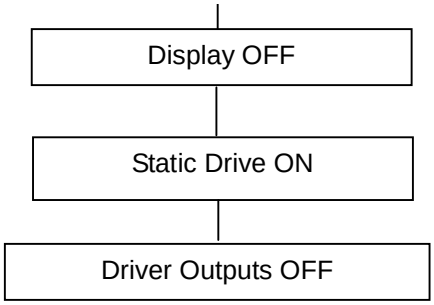
(p) Power Save(complex command)

When Static Drive ON at the Display OFF status(inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current. The internal status in the Power Save Mode is shown as follows;

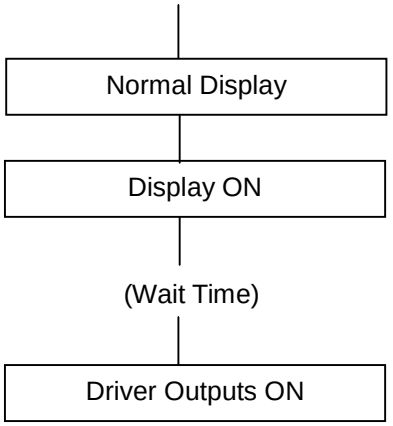
1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage(V_1 to V_5) is fixed to the V_{DD} level.

The power save and its release perform according to the following sequences.

O Power Save Sequence



O Power Save Release Sequence



The **NJU6673** constantly spends the current without the execution of the Driver Outputs OFF instruction. The LCD drive waveform is not output until the Driver Outputs ON instruction is executed.

*1 : In the Power Save sequence, the Power Save Mode starts after the Static Drive ON bcommand is executed.
*2 : In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
*3 : The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctry, test by using the actual LCD module.
*4 : LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
*5 : In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage of V_{OUT} terminal. In this time, V_{OUT} terminal also should be made codition like as disconection to the lowest voltage of the system.

(q) ADC Select

This instruction determines the correspondence of Column in the DD RAM with the Segment Driver Outputs. Segment Driver Outout order is inverse when this instruction executes, therefore, the placement the **NJU6673** against the LCD panel becomes easy.

A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	0/1

D 0: Clokwise Output(Normal)
1: Counterclockwise Output(Inverse)

(3) Internal Power Supply

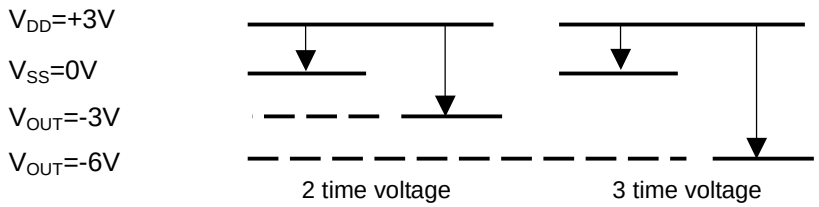
(3-1) Voltage tripler

The 3-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 3 times of V_{DD}-V_{SS} from the V_{OUT} terminal with connecting the five capacitors between C_1+ and C_1-, C_2+ and C_2-, and V_{SS} and V_{OUT}. In case of the 2-time voltage booster operation, connect the two capacitor between C_2+ and C_2-, V_{SS} and V_{OUT}, then connect the C_1+ and C_2+ terminals. Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal. therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.

The boosted voltage of V_{DD}-V_{OUT} must be 10V or less.

The boost voltage and the capacitor connection are shown below.

- The boosted voltage and V_{DD}, V_{SS}



(3-2) Voltage Adjust Circuits

The boosted voltage of V_{OUT} outputs V_5 for LCD driving through the voltage adjust circuits. The output voltage of V_5 is adjusted by Ra and Rb within the range of $|V_5| < |V_{OUT}|$.

The output is calculated by the following formula(1).

$$V_{LCD} = V_{DD}-V_5 = (1+Rb/Ra)V_{REG} \cdots\cdots\cdots\cdots (1)$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder registance. V_{REG} is adjustable by EVR functions (see section 3-3).

For minor adjustment of V_5, it is recommended that the Ra and Rb is composed of R_2 as variable resistor and R_1 and R_3 as fixed resistors, constant should be connected to V_{DD} terminal,VR and V_5 ,as shown below.

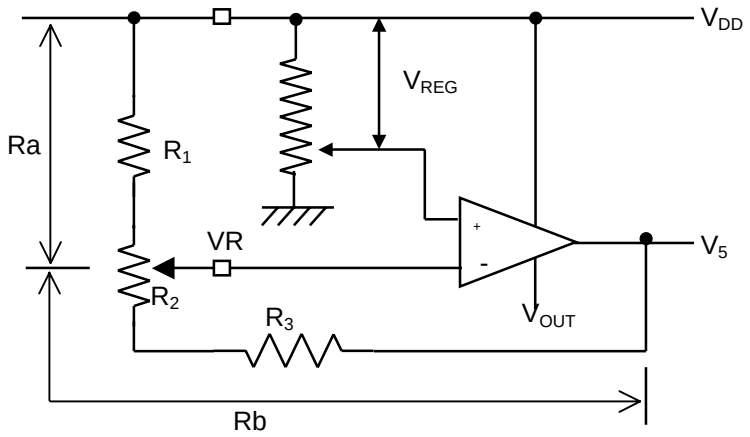


Fig-3 Voltage Adjust Circuit

<Design example for R_1, R_2 and R_3 / Reference>

- R_1+R_2+R_3=3.1MΩ
  (Determined by the current flown between V_{DD}- V_5)
- Variable voltage range by the R2. -3.2V to -6.3V (V_{LCD}= V_{DD}- V_5=6.2V to 9.3V)
  (Determined by the LCD electrical characteristics)
- V_{REG}=3V(In case of EVR=$(F)_H$)
- - R_1, R_2 and R_3 are calculated by above conditions and the formula of (1) to mentioned below;

  R_1=1.0MΩ, R_2=0.5MΩ, R_3=1.6MΩ

Note) V_5 voltage is generated referencing with V_{REG} voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above figure. Therefore, V_{LCD} (V_{DD}-V_5) is affected including the gain (Rb/Ra) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V_5 stable operation.

(3-3) Contrast Adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 16 conditions by setting 4-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V_5.

A step with EVR is set like table shown below.

EVR register		V_{REG} [V]	V_{LCD}
0_H	(0, 0, 0, 0)	(135/150)(V_{DD}-V_{SS})	Low
1_H	(0, 0, 0, 1)	(136/150)(V_{DD}-V_{SS})	:
2_H	(0, 0, 1, 0)	(137/150)(V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
E_H	(1, 1, 1, 0)	(149/150)(V_{DD}-V_{SS})	:
F_H	(1, 1, 1, 1)	(150/150)(V_{DD}-V_{SS})	High

* In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD} =3.0V, V_{SS}=0V

Ra=1MΩ, Rb=1MΩ (Ra:Rb=1:1)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting 00_H in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra) V_{REG}
= (2/1)[(135/150)3.0]
= 5.4V

In case of setting $0F_H$ in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra) V_{REG}
= (2/1)[(150/150)3.0]
= 6.0V

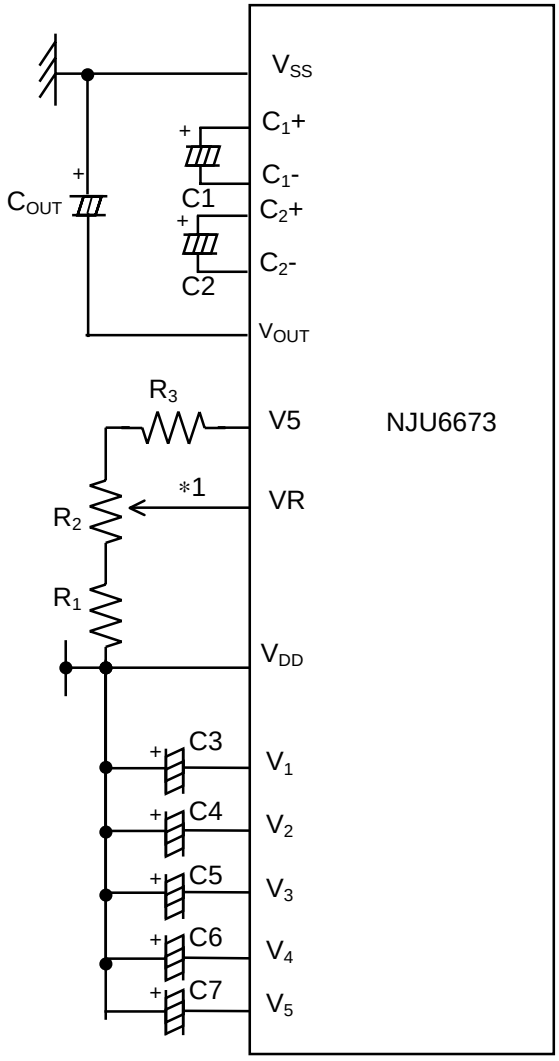
	(min.)0_H	(max.)F_H
Adjustable Range	5.4 ••••••••••••••••••••••••••••••••••••	6.0 [V]
Step Voltage	40	[mV]

(3-4) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1,V_2,V_3,V_4 are generated by dividing the V_5 voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.

The external capacitors to V_1 to V_5 for Bias voltage stabilization may be removed in use of small size LCD panel. The equivalent load of LCD panel may be changed depending on display patterns. Therefore, it require display quality check on various display patterns actually without external capacitors. If the display quality is not so good, external capacitors should connects as show in Fig. 4. (If no need external capacitors as result of experiment, the application patterns (wiring) should be prepared for recovery.)

Using the internal Power Supply



Using the external Power Supply

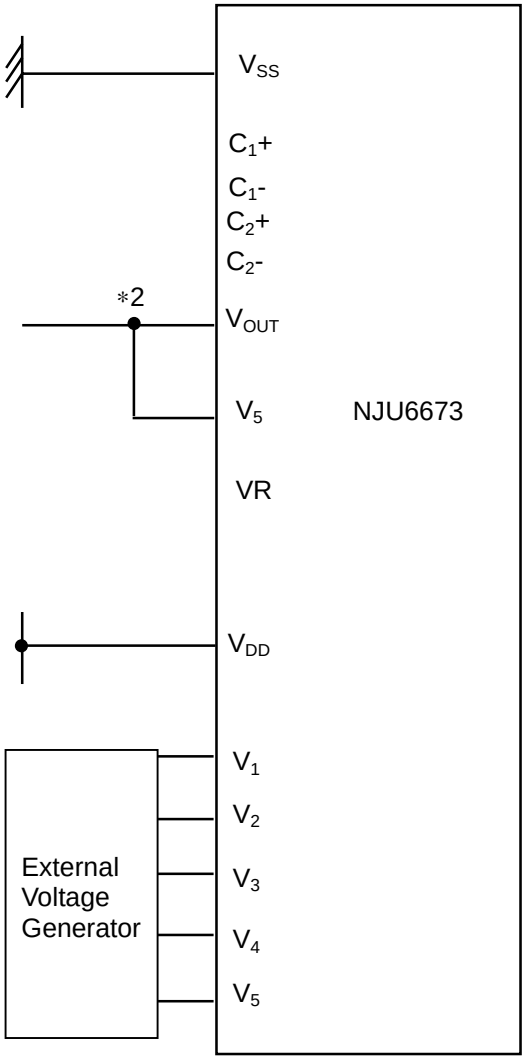


Fig.4

Reference set up value $V_{LCD}=V_{DD}- V_5$≒6.2-9.3V

∗1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

∗2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS}>V_5$, $V_{OUT}=V_5$

When $V_{SS}\leq V_5$, $V_{OUT}=V_{SS}$

C_{OUT}	to 1.0μF
C_1, C_2	to 1.0μF
C3-C7	0.1 to 0.47 μF
R_1	1MΩ
R_2	500kΩ
R_3	1.6MΩ

(4) MPU Interface

(4-1) Interface type selection

Two MPU interface types are available in the **NJU6673**: by 1) 8-bit bi-directional data bus (D_7 to D_0), 2) serial data input (SI:D_7). The interface type (the 8 bit parallel or serial interface) is determined by the condition of the P/S terminals connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed..

Table 5

P/S	I/F type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_5-D_0
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_5-D_0
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	Hi-Z

Parallel Interface

The **NJU6673** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S="H" is selected.

The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_7-D_0
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D_7-D_0
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D_7-D_0

(4-2) Discrimination of Data Bus Signal

The **NJU6673** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$, $\overline{WR}$) signals as shown in Table 7.

Table 7

common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
H	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface.(P/S="L")

The serial interface of the **NJU6673** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($\overline{CS}$=L), the input to D_7(SI) and D_6(SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.

The data input from the terminal(SI) is MSB first like as the order of D_7, D_6,------ D_0, by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.

It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0="H" and instruction by A0="L" A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.

However,in case of $\overline{RES}$="H" to "L" or $\overline{CS}$="L" to "H" with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.

The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

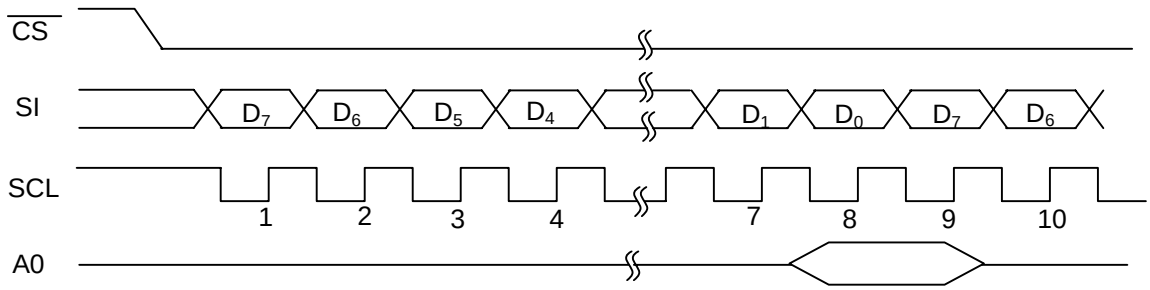


Fig.5

(4-4) Access to the Display Data RAM and Internal Register.

The **NJU6673** transfers data to the MPU through the bus holder with the internal data bus.

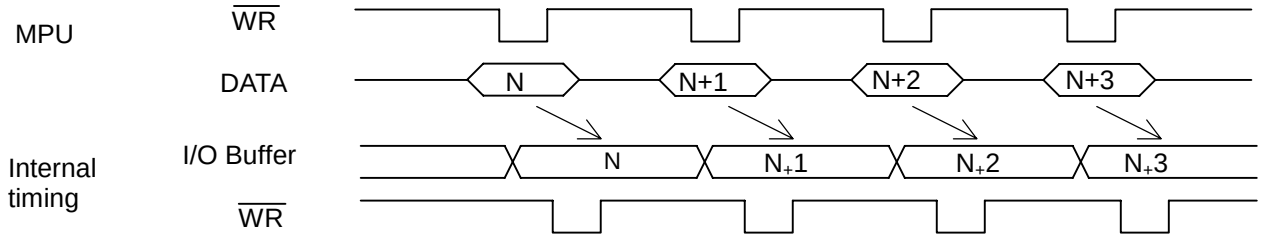
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6673** from MPU side is not access time (t_{ACC},t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the satisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 6)

The example of Read Modify Write operation is mentioned in (2-1)Instruction -k)The sequence of Inverse Display.

● Write Operation



● Read Operation

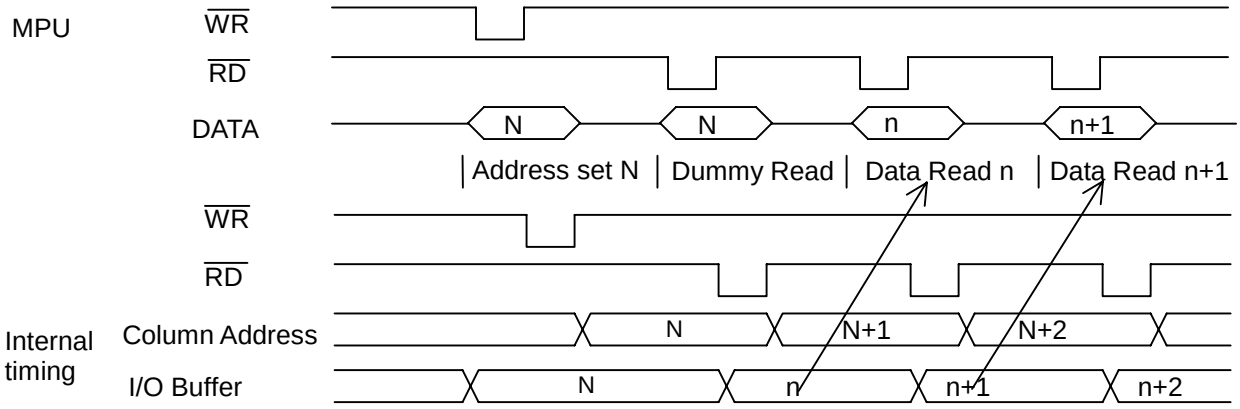


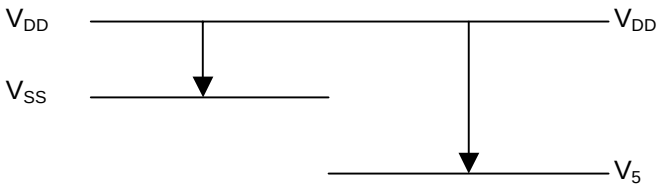
Fig.6

(4-5) Chip Select

$\overline{CS}$ is Chip Select terminal. In case of $\overline{CS}$="L". the interface with MPU is available. In case of $\overline{CS}$="H", the D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL inputs are ignored. If the serial interface is selected when $\overline{CS}$="H" the shift register and counter are reset. However, the reset is always operated in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(1)	V_{DD}	-0.3 - +7.0	V
		-0.3 -+3.6(Used Tripler)	
Supply Voltage(2)	V_5	V_{DD}-11.0 - V_{DD}+0.3	V
Supply Voltage(3)	V_1,V_2,V_3,V_4	V_5-V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3-V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30-+80	°C
Strage temperature	T_{stg}	-55-+125	°C



Note 1) All voltage values are specified as V_{SS}=0V.

Note 2) The relation of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 > V_{OUT}$; $V_{DD} > V_{SS} \geq V_{OUT}$ must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to **NJU6673** at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .
In use of the voltage boost circuit, the condition that the supply voltage: 11.0V$\geq$ V_{DD} -V_{OUT} is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=2.4V-3.6V, V_{SS}=0V, Ta=-20 to 75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating voltage(1)	Recommend	V_{DD}			2.4	3.0	3.6	V	1
	Available				2.4		5.5		
Operating voltage(2)	Recommend	V_5			V_{DD}-10.0		V_{DD}-4.0	V	
	Available				V_{DD}-10.0				
	Available	V_1,V_2	V_{LCD}=V_{DD}-V_5		V_{DD}-0.6V_{LCD}		V_{DD}		
	Available	V_3,V_4			V_5		V_{DD}-0.4V_{LCD}		
Input Voltage	High Level	V_{IHC}	A0, D_0-D_7, $\overline{RD}$, $\overline{WR}$, $\overline{RES}$, $\overline{CS}$ P/S, SEL68, DUTY, CDIR Terminal		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC}			V_{SS}		0.2V_{DD}		
Output Voltage	High Level	V_{OHC}	D_0-D_7 Terminal	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}		
Input Leagage Current		I_{LI}	All input terminals		-1.0		1.0	µA	
		I_{L0}	D_0 to D_7 terminals, Hi-Z state		-3.0		3.0		
Driver On-resistance		R_{ON}	Ta=25°C, V_{LCD}=8.0V			3.0	4.5	kΩ	2
Stand-by Current		I_{DDQ}	During Power Save Mode			0.05	5.0	µA	3
Input Terminal Capacitance		C_{IN}	Ta=25°C			10		pF	4
Oscillation Frequency		f_{OSC}	V_{DD}= 3.0V Ta =25°C		9.3	11.4	13.5	kHz	
Reset Time		t_R	$\overline{RES}$ terminal		1.0			µs	5
Reset "L" level pulse Width		t_{RW}			10			µs	6

Voltage booster	Input voltage	V_{DD1}			2.4		5.5	V	
		V_{DD2}	3-times boost		2.4		3.3		7
	Output voltage	V_{OUT1}	3-times boost,V_{DD}=3.0V		-6.6		-5.5	V	
	On-resistance	R_{TRI}	3-times boost, V_{DD}=3.0V, C_{OUT}=1.0µF			1600	2600	Ω	
	Adjustment range LCD driving oltage	V_{OUT2}	Voltage boost operation off		V_{DD}-10.0V		V_{DD}-4.0V	V	8
	Voltage Follower	V_5	Voltage adjustment circuit "OFF"		V_{DD}-10.0V		V_{DD}-4.0V	V	
	Voltage Regulator	$V_{REG\%}$	V_{DD}=3.0V; Ta =25°C				3.0	%	

Operating Current	I_{OUT1}	V_{DD}=3.0V, V_{LCD}=8V, Display Checkerd pattern		50	105	µA	9
	I_{OUT2}			16	25	µA	

Note 1) Although the **NJU6673** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

Note 2) R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V_1,V_2,V_3,V_4) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).

Note 3) Apply no access from MPU.

Note 4) Apply A0, D_0 to D_7,$\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,P/S,T_1,T_2,DUTY,CDIR terminals.

Note 5) t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the $\overline{RES}$ signal.

Note 6) Apply minimum pulse width of the $\overline{RES}$ signal. To reset, the "L" pulse over t_{RW} shall be input. .

Note 7) Apply to the V_{DD} when using 3-times boost.

Note 8) The voltage adjustment circuit controls V_5 within the range of the voltage follower operating voltage.

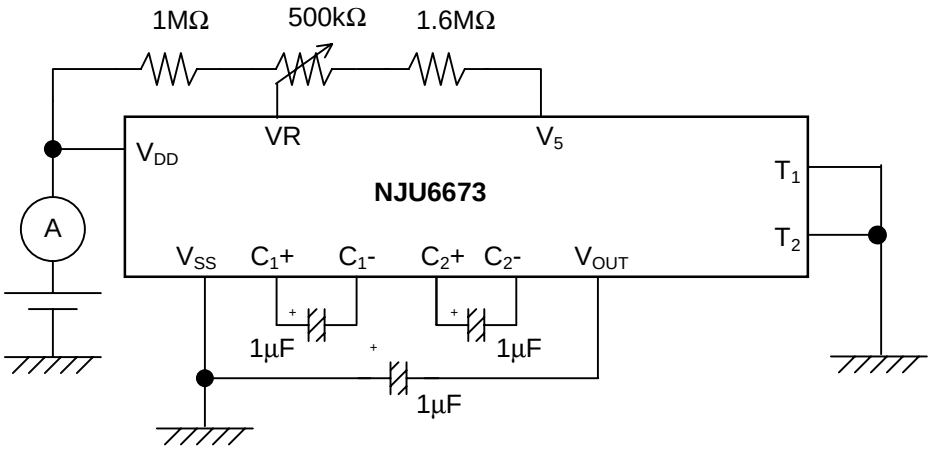
Note 9) Each operating current shall be defined as being measured in the following condition.

SYMBOL	Status		Oprating Condition			External Voltage Supply (Input terminal)
	T_1	T_2	Voltage booster	Voltage adjustment	Voltage Follower	
I_{OUT1}	L	L/H	Validity	Validity	Validity	Unuse
I_{OUT2}	H	H	Invalidity	Invalidity	Invalidity	Use (V_{OUT},V_5)

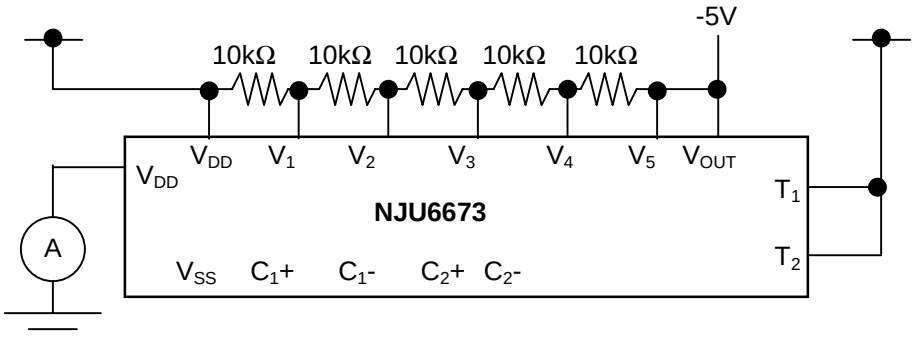
LCD output terminal Open.
Display on, Display checered pattern, No access from MPU
Set V_{LCD}=8V
Internal Oscillator : Validity

MEASUREMENT BLOCK DIAGRAM

: I_{OUT1}

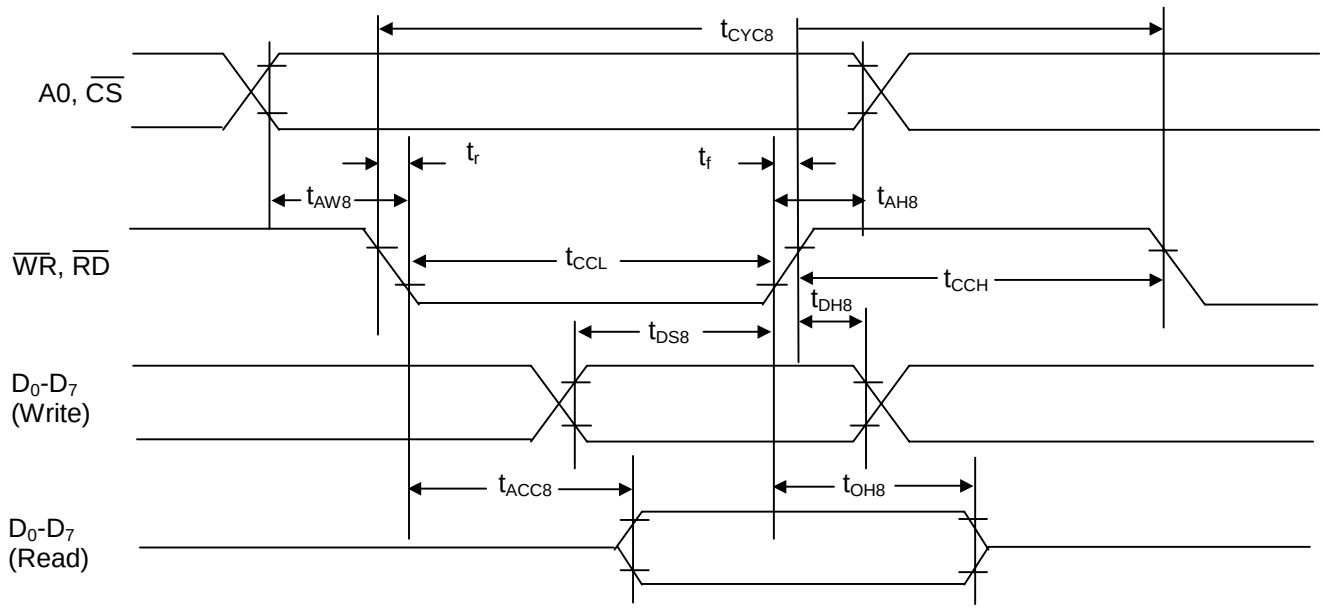


: I_{OUT2}



■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence(80 type MPU)

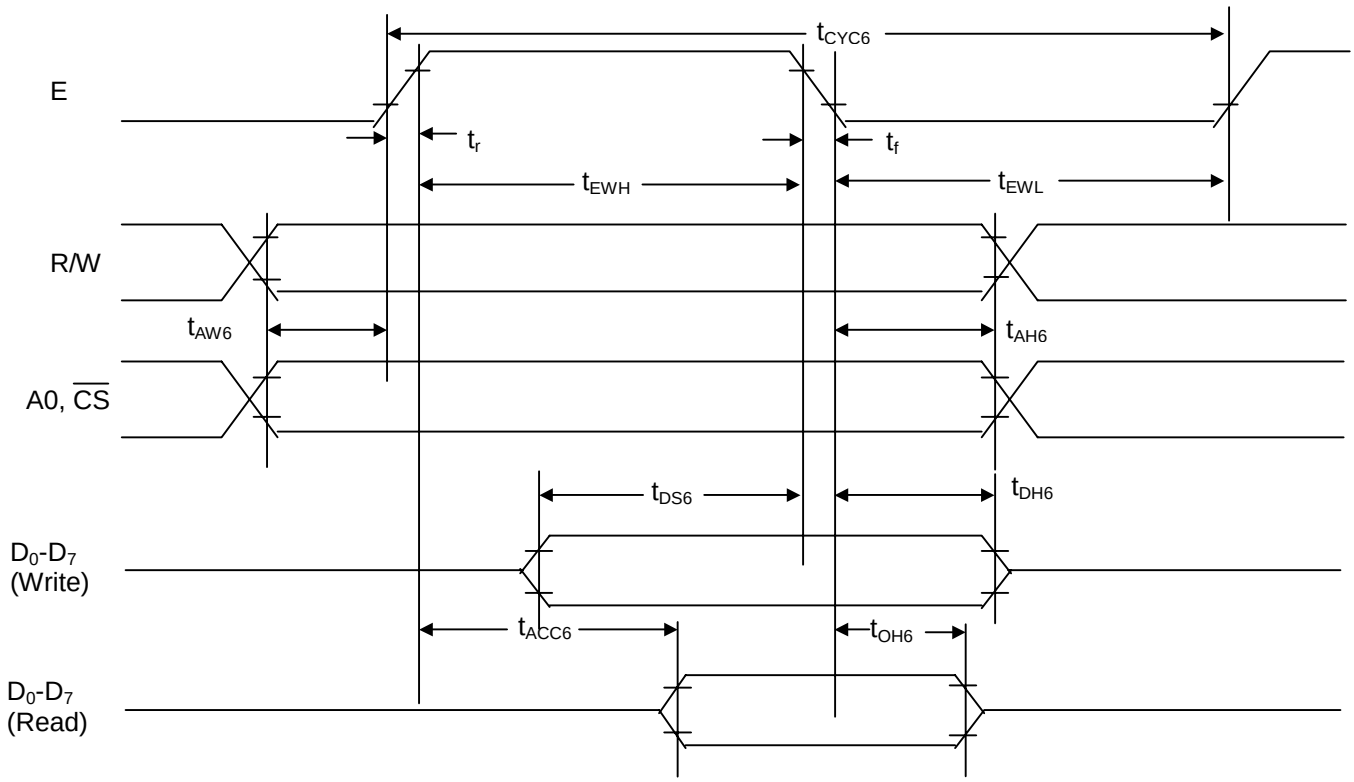


(V_{DD}=2.4V to 3.6V, Ta=-20 to 75°C)

PARAMETER		SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Address Hold Time		t_{AH8}	A0, $\overline{CS}$		32			ns
Address Setup Time		t_{AW8}			0			
System Cycle Time		t_{CYC8}	$\overline{WR}$, $\overline{RD}$		560			
Control Pulse Width	$\overline{WR}$, "L"	$t_{CCL(W)}$			75			
	$\overline{RD}$, "L"	$t_{CCL(R)}$			250			
	"H"	t_{CCH}			275			
Data Setup Time		t_{DS8}	D_D-D_7		150			
Data Hold Time		t_{DH8}			30			
$\overline{RD}$ Access Time		t_{ACC8}		CL=100pF			175	
Output Disable Time		t_{OH8}			0		44	
Rise Time, Fall Time		t_r, t_f	$\overline{CS}$,$\overline{WR}$,$\overline{RD}$ A0, D_0-D_7				15	

Note 1) All timing based on 20% and 80% of V_{DD} voltage level.

Read/Write operation sequence(68 type MPU)

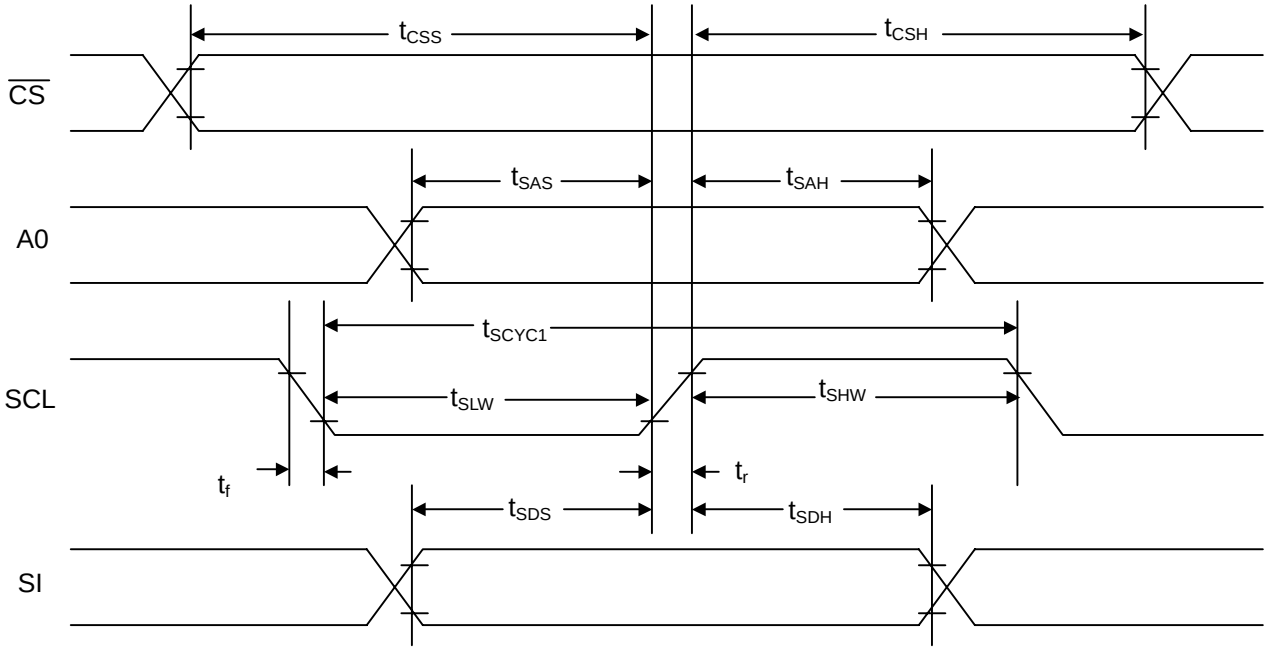


(V_{DD}=2.4V to 3.6V, Ta=-20 to 75°C)

PARAMETER		SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Address Hold Time		t_{AH6}	A0, $\overline{CS}$ R/W		32			ns
Address Setup Time		t_{AW6}			32			
System Cycle Time		t_{CYC6}	E		560			
Enable Pulse Width	READ	t_{EWH}	E		250			
	WRITE				62			
Data Setup Time		t_{DS6}	D_0-D_7		150			
Data Hold Time		t_{DH6}			50			
Access Time		t_{ACC6}		CL=100pF	0		175	
Output Disable Time		t_{OH6}			0		56	
Rise Time, Fall Time		t_r, t_f	E, R/W, A0, D_0-D_7				15	

Note 1) All timing based on 20% and 80% of V_{DD} voltage level.
Note 2) t_{CYC6} shows the cycle of the E signal in active $\overline{CS}$.

Write operation sequence(Serial Interface)

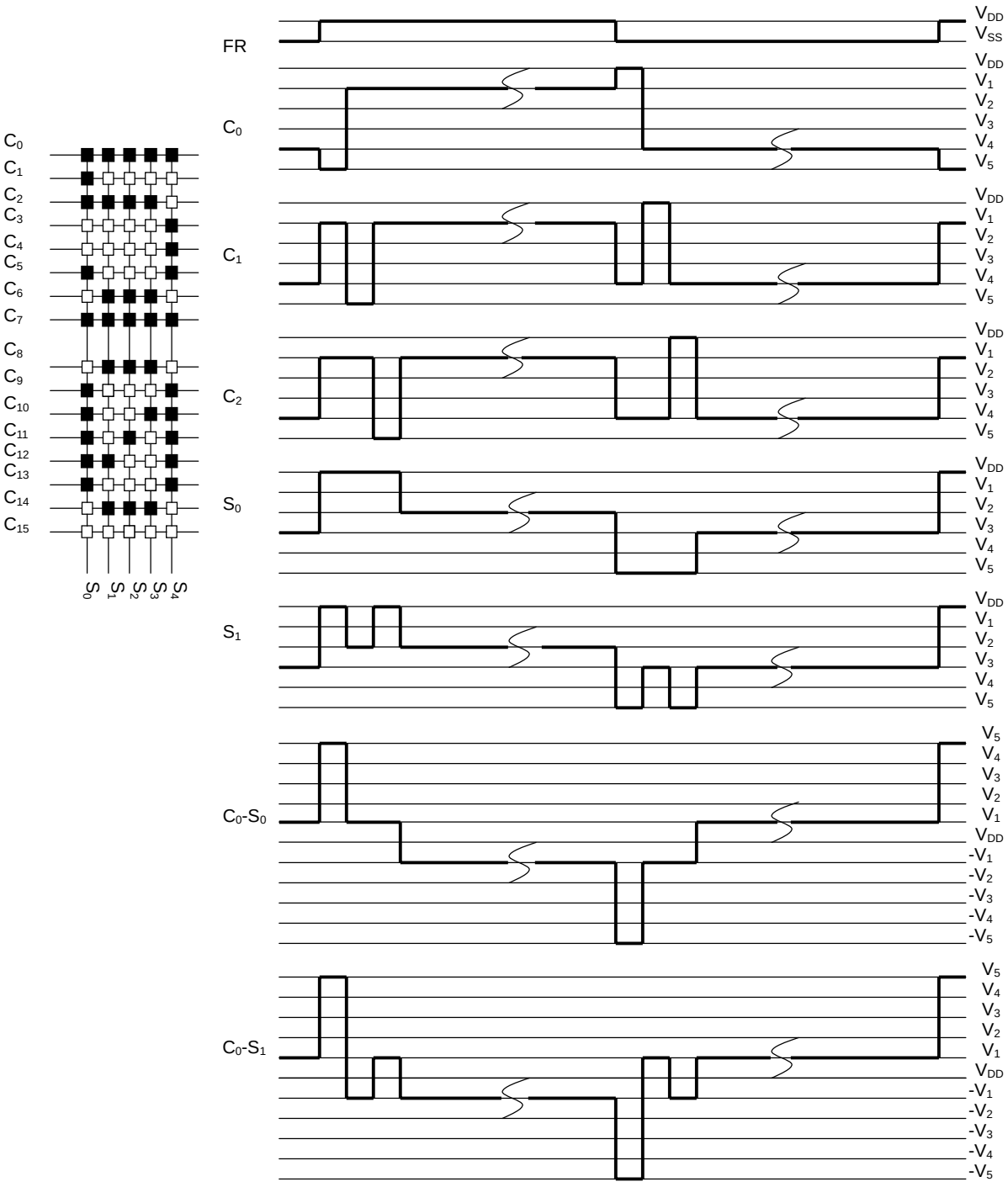


(V_{DD}=2.4V-3.6V, Ta=-20 to 75°C)

PARAMETER	SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Serial Clock cycle	t_{SCYC}	SCL		1000			ns
SCL "H" Pulse width	t_{SHW}			300			
SCL "L" Pulse width	t_{SLW}			300			
Address Setup Time	t_{SAS}	A0		250			
Address Hold Time	t_{SAH}			400			
Data Setup Time	t_{SDS}	SI		250			
Data Hold Time	t_{SDH}			100			
$\overline{CS}$-SCL Time	t_{CSS}	$\overline{CS}$		60			
	t_{CSH}			800			
Rise time, Fall Time	t_f, t_r	$\overline{CS}$, SCL SI, A0				15	

Note 1) All timing are based on 20% and 80% of V_{DD} voltage level.

■ LCD DRIVING WAVERORM



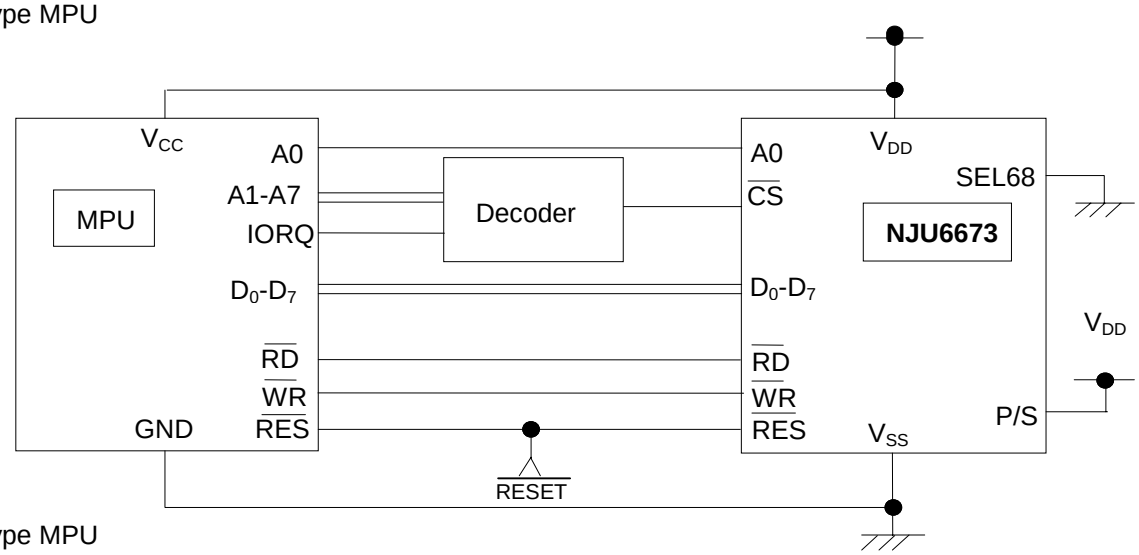
■ APPLICATION CIRCUIT

Microprocessor Interface Example

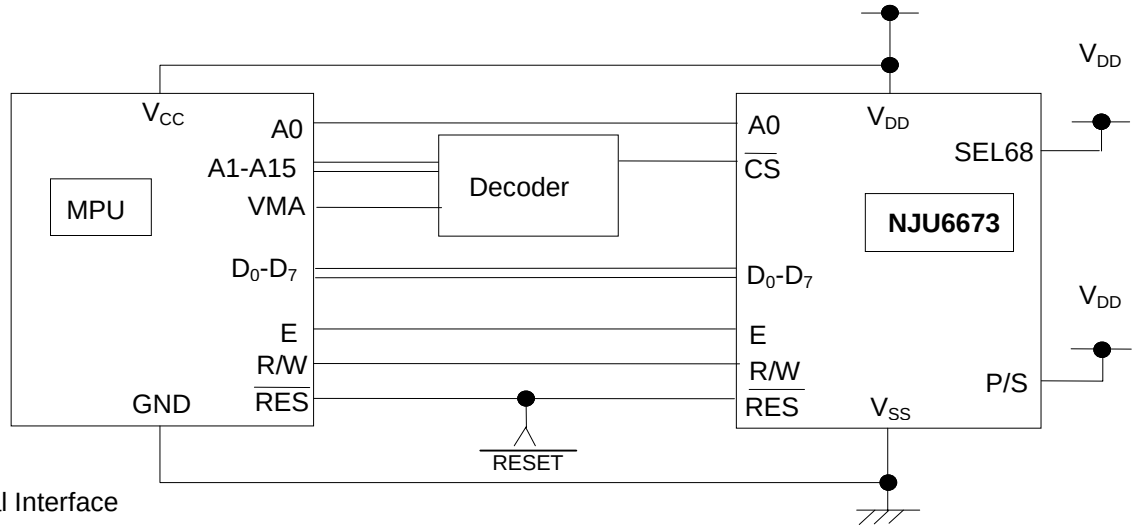
The **NJU6673** is connectable to 80-type MPU or 68-type. In use of Serial Interface, it is possible to be controlled by the signal line with the more small being.

*:SEL68 terminal shall be connected to V_{DD} or V_{SS}.

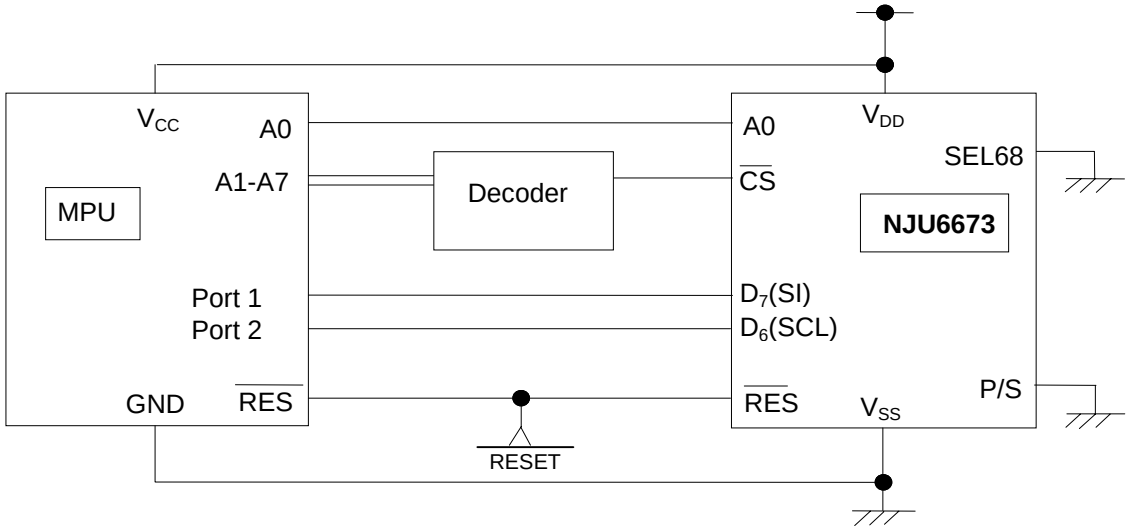
● 80 type MPU



● 68 type MPU



● Serial Interface



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