



40-common x 128RGB-Segment, in 4096-Color 4096-Color STN LCD DRIVER

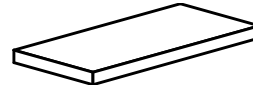
■ GENERAL DESCRIPTION

The **NJU6820** is a STN LCD driver with 40-common x 128RGB-segment in 4096-color. It consists of 384(128xRGB)-segment segment, 40-common drivers, serial and parallel MPU interface circuits, internal power supply circuits, gradation palettes and 61,440-bit for graphic display data RAM.

Each segment driver outputs 16-gradation level out of 32-gradation level of gradation palette.

Since the **NJU6820** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

■ PACKAGE OUTLINE



NJU6820CJ

■ FEATURES

- 4096-color STN LCD driver
- LCD drivers 40 commons, 128 RGB-segments,
- Display data RAM (DDRAM) 61,440-bit for graphic display
- Color display mode 16 gradation level out of 32 gradation level of gradation palette
- Black & white display mode 40 x 384 pixels in 16 gradation level or 40 x 384 pixels in B&W display
- 256-color driving mode
- 8/16bit Parallel interface directly-connective to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- 3-/4-line Serial interface
- Programmable duty and bias ratios
- Programmable internal voltage booster (maximum 5-times)
- Programmable contrast control using 128-step EVR
- Various instructions
 - Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF,
 - Column address, row address, N-line inversion, Initial display line, Initial COM line,
 - Read-modify-write, Gradation mode control, Increment control, Data bus length,
 - Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control,
 - Power save ON/OFF, etc
- Internal voltage regulator
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS technology
- Rectangle out look for COG
- Package Bumped chip / TCP

■ PAD COORDINATES 1

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
1	DMY ₀	-8967	-990	51	DMY ₂₄	-6699	-990	101	DMY ₄₈	-3507	-990
2	DMY ₁	-8925	-990	52	DMY ₂₅	-6573	-990	102	DMY ₄₉	-3381	-990
3	DMY ₂	-8883	-990	53	D ₂	-6531	-990	103	D ₁₄	-3339	-990
4	V _{SSA}	-8841	-990	54	D ₂	-6489	-990	104	D ₁₄	-3297	-990
5	V _{SSA}	-8799	-990	55	DMY ₂₆	-6447	-990	105	DMY ₅₀	-3255	-990
6	DMY ₃	-8757	-990	56	DMY ₂₇	-6321	-990	106	DMY ₅₁	-3129	-990
7	SEL68	-8715	-990	57	D ₃	-6279	-990	107	D ₁₅	-3087	-990
8	SEL68	-8673	-990	58	D ₃	-6237	-990	108	D ₁₅	-3045	-990
9	DMY ₄	-8631	-990	59	DMY ₂₈	-6195	-990	109	DMY ₅₂	-3003	-990
10	V _{DDA}	-8589	-990	60	DMY ₂₉	-6069	-990	110	DMY ₅₃	-2877	-990
11	V _{DDA}	-8547	-990	61	D ₄	-6027	-990	111	V _{DD}	-2835	-990
12	DMY ₅	-8505	-990	62	D ₄	-5985	-990	112	V _{DD}	-2793	-990
13	PS	-8463	-990	63	DMY ₃₀	-5943	-990	113	V _{DD}	-2751	-990
14	PS	-8421	-990	64	DMY ₃₁	-5817	-990	114	V _{DD}	-2709	-990
15	DMY ₆	-8379	-990	65	D ₅	-5775	-990	115	V _{DD}	-2667	-990
16	V _{SSA}	-8337	-990	66	D ₅	-5733	-990	116	V _{DD}	-2625	-990
17	V _{SSA}	-8295	-990	67	DMY ₃₂	-5691	-990	117	V _{DD}	-2583	-990
18	DMY ₇	-8253	-990	68	DMY ₃₃	-5565	-990	118	V _{DD}	-2541	-990
19	RESB	-8211	-990	69	D ₆	-5523	-990	119	V _{DD}	-2499	-990
20	RESB	-8169	-990	70	D ₆	-5481	-990	120	V _{DD}	-2457	-990
21	DMY ₈	-8127	-990	71	DMY ₃₄	-5439	-990	121	V _{DD}	-2415	-990
22	DMY ₉	-8085	-990	72	DMY ₃₅	-5313	-990	122	DMY ₅₄	-2289	-990
23	DMY ₁₀	-8043	-990	73	D ₇	-5271	-990	123	DMY ₅₅	-2163	-990
24	CSb	-8001	-990	74	D ₇	-5229	-990	124	CL	-2121	-990
25	CSb	-7959	-990	75	DMY ₃₆	-5187	-990	125	CL	-2079	-990
26	DMY ₁₁	-7917	-990	76	V _{SSA}	-5061	-990	126	DMY ₅₆	-2037	-990
27	DMY ₁₂	-7875	-990	77	V _{SSA}	-5019	-990	127	DMY ₅₇	-1911	-990
28	DMY ₁₃	-7833	-990	78	DMY ₃₇	-4893	-990	128	FLM	-1869	-990
29	RS	-7791	-990	79	D ₈	-4851	-990	129	FLM	-1827	-990
30	RS	-7749	-990	80	D ₈	-4809	-990	130	DMY ₅₈	-1785	-990
31	DMY ₁₄	-7707	-990	81	DMY ₃₈	-4767	-990	131	DMY ₅₉	-1659	-990
32	DMY ₁₅	-7665	-990	82	DMY ₃₉	-4641	-990	132	FR	-1617	-990
33	DMY ₁₆	-7623	-990	83	D ₉	-4599	-990	133	FR	-1575	-990
34	WRb	-7581	-990	84	D ₉	-4557	-990	134	DMY ₆₀	-1533	-990
35	WRb	-7539	-990	85	DMY ₄₀	-4515	-990	135	DMY ₆₁	-1407	-990
36	DMY ₁₇	-7497	-990	86	DMY ₄₁	-4389	-990	136	CLK	-1365	-990
37	DMY ₁₈	-7455	-990	87	D ₁₀	-4347	-990	137	CLK	-1323	-990
38	DMY ₁₉	-7413	-990	88	D ₁₀	-4305	-990	138	DMY ₆₂	-1281	-990
39	RDb	-7371	-990	89	DMY ₄₂	-4263	-990	139	DMY ₆₃	-1155	-990
40	RDb	-7329	-990	90	DMY ₄₃	-4137	-990	140	OSC ₁	-1113	-990
41	DMY ₂₀	-7287	-990	91	D ₁₁	-4095	-990	141	OSC ₁	-1071	-990
42	V _{DDA}	-7245	-990	92	D ₁₁	-4053	-990	142	DMY ₆₄	-1029	-990
43	V _{DDA}	-7203	-990	93	DMY ₄₄	-4011	-990	143	OSC ₂	-903	-990
44	DMY ₂₁	-7077	-990	94	DMY ₄₅	-3885	-990	144	OSC ₂	-861	-990
45	D ₀	-7035	-990	95	D ₁₂	-3843	-990	145	DMY ₆₅	-735	-990
46	D ₀	-6993	-990	96	D ₁₂	-3801	-990	146	V _{SS}	-693	-990
47	DMY ₂₂	-6951	-990	97	DMY ₄₆	-3759	-990	147	V _{SS}	-651	-990
48	DMY ₂₃	-6825	-990	98	DMY ₄₇	-3633	-990	148	V _{SS}	-609	-990
49	D ₁	-6783	-990	99	D ₁₃	-3591	-990	149	V _{SS}	-567	-990
50	D ₁	-6741	-990	100	D ₁₃	-3549	-990	150	V _{SS}	-525	-990

■ PAD COORDINATES 2

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
151	V _{SS}	-483	-990	201	V ₄	1953	-990	251	V _{OUT}	4179	-990
152	V _{SS}	-441	-990	202	V ₄	1995	-990	252	V _{OUT}	4221	-990
153	V _{SS}	-399	-990	203	V ₄	2037	-990	253	V _{OUT}	4263	-990
154	V _{SS}	-357	-990	204	V ₄	2079	-990	254	V _{OUT}	4305	-990
155	V _{SS}	-315	-990	205	DMY ₆₉	2121	-990	255	V _{OUT}	4347	-990
156	V _{SS}	-273	-990	206	V _{REG}	2163	-990	256	V _{OUT}	4389	-990
157	DMY ₆₆	-147	-990	207	V _{REG}	2205	-990	257	V _{OUT}	4431	-990
158	V _{LCD}	-21	-990	208	V _{REG}	2247	-990	258	V _{OUT}	4473	-990
159	V _{LCD}	21	-990	209	V _{REG}	2289	-990	259	DMY ₇₃	4641	-990
160	V _{LCD}	63	-990	210	V _{REG}	2331	-990	260	V _{EE}	4683	-990
161	V _{LCD}	105	-990	211	V _{REG}	2373	-990	261	V _{EE}	4725	-990
162	V _{LCD}	147	-990	212	V _{REG}	2415	-990	262	V _{EE}	4767	-990
163	V _{LCD}	189	-990	213	V _{REG}	2457	-990	263	V _{EE}	4809	-990
164	V _{LCD}	231	-990	214	V _{REG}	2499	-990	264	V _{EE}	4851	-990
165	V _{LCD}	273	-990	215	V _{REG}	2541	-990	265	V _{EE}	4893	-990
166	V _{LCD}	315	-990	216	DMY ₇₀	2583	-990	266	V _{EE}	4935	-990
167	DMY ₆₇	357	-990	217	V _{REF}	2625	-990	267	V _{EE}	4977	-990
168	V ₁	399	-990	218	V _{REF}	2667	-990	268	V _{EE}	5019	-990
169	V ₁	441	-990	219	V _{REF}	2709	-990	269	V _{EE}	5061	-990
170	V ₁	483	-990	220	V _{REF}	2751	-990	270	DMY ₇₄	5187	-990
171	V ₁	525	-990	221	V _{REF}	2793	-990	271	C1+	5229	-990
172	V ₁	567	-990	222	V _{REF}	2835	-990	272	C1+	5271	-990
173	V ₁	609	-990	223	V _{REF}	2877	-990	273	C1+	5313	-990
174	V ₁	651	-990	224	V _{REF}	2919	-990	274	C1+	5355	-990
175	V ₁	693	-990	225	V _{REF}	2961	-990	275	C1+	5397	-990
176	V ₁	735	-990	226	V _{REF}	3003	-990	276	C1+	5439	-990
177	V ₂	861	-990	227	DMY ₇₁	3045	-990	277	C1+	5481	-990
178	V ₂	903	-990	228	V _{BA}	3087	-990	278	C1+	5523	-990
179	V ₂	945	-990	229	V _{BA}	3129	-990	279	C1+	5565	-990
180	V ₂	987	-990	230	V _{BA}	3171	-990	280	C1+	5607	-990
181	V ₂	1029	-990	231	V _{BA}	3213	-990	281	DMY ₇₅	5649	-990
182	V ₂	1071	-990	232	V _{BA}	3255	-990	282	C1-	5691	-990
183	V ₂	1113	-990	233	V _{BA}	3297	-990	283	C1-	5733	-990
184	V ₂	1155	-990	234	V _{BA}	3339	-990	284	C1-	5775	-990
185	V ₂	1197	-990	235	V _{BA}	3381	-990	285	C1-	5817	-990
186	DMY ₆₈	1239	-990	236	V _{BA}	3423	-990	286	C1-	5859	-990
187	V ₃	1281	-990	237	V _{BA}	3465	-990	287	C1-	5901	-990
188	V ₃	1323	-990	238	DMY ₇₂	3507	-990	288	C1-	5943	-990
189	V ₃	1365	-990	239	V _{SS}	3549	-990	289	C1-	5985	-990
190	V ₃	1407	-990	240	V _{SS}	3591	-990	290	C1-	6027	-990
191	V ₃	1449	-990	241	V _{SS}	3633	-990	291	C1-	6069	-990
192	V ₃	1491	-990	242	V _{SS}	3675	-990	292	DMY ₇₆	6111	-990
193	V ₃	1533	-990	243	V _{SS}	3717	-990	293	C2+	6153	-990
194	V ₃	1575	-990	244	V _{SS}	3759	-990	294	C2+	6195	-990
195	V ₃	1617	-990	245	V _{SS}	3801	-990	295	C2+	6237	-990
196	V ₄	1743	-990	246	V _{SS}	3843	-990	296	C2+	6279	-990
197	V ₄	1785	-990	247	V _{SS}	3885	-990	297	C2+	6321	-990
198	V ₄	1827	-990	248	V _{SS}	3927	-990	298	C2+	6363	-990
199	V ₄	1869	-990	249	V _{OUT}	4095	-990	299	C2+	6405	-990
200	V ₄	1911	-990	250	V _{OUT}	4137	-990	300	C2+	6447	-990

■ PAD COORDINATES 3

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
301	C2+	6489	-990	351	C4-	8589	-990	401	SEGA ₃	7665	990
302	C2+	6531	-990	352	C4-	8631	-990	402	SEGB ₃	7623	990
303	DMY ₇₇	6573	-990	353	C4-	8673	-990	403	SEGC ₃	7581	990
304	C2-	6615	-990	354	C4-	8715	-990	404	SEGA ₄	7539	990
305	C2-	6657	-990	355	C4-	8757	-990	405	SEGB ₄	7497	990
306	C2-	6699	-990	356	C4-	8799	-990	406	SEGC ₄	7455	990
307	C2-	6741	-990	357	C4-	8841	-990	407	SEGA ₅	7413	990
308	C2-	6783	-990	358	DMY ₈₂	8883	-990	408	SEGB ₅	7371	990
309	C2-	6825	-990	359	DMY ₈₃	8925	-990	409	SEGC ₅	7329	990
310	C2-	6867	-990	360	DMY ₈₄	8967	-990	410	SEGA ₆	7287	990
311	C2-	6909	-990	361	DMY ₈₅	9225	-910	411	SEGB ₆	7245	990
312	C2-	6951	-990	362	DMY ₈₆	9225	-868	412	SEGC ₆	7203	990
313	C2-	6993	-990	363	DMY ₈₆	9225	-826	413	SEGA ₇	7161	990
314	DMY ₇₈	7035	-990	364	DMY ₈₆	9225	-784	414	SEGB ₇	7119	990
315	C3+	7077	-990	365	DMY ₈₇	9225	-742	415	SEGC ₇	7077	990
316	C3+	7119	-990	366	DMY ₈₈	9135	990	416	SEGA ₈	7035	990
317	C3+	7161	-990	367	DMY ₈₉	9093	990	417	SEGB ₈	6993	990
318	C3+	7203	-990	368	DMY ₉₀	9051	990	418	SEGC ₈	6951	990
319	C3+	7245	-990	369	COM ₁₉	9009	990	419	SEGA ₉	6909	990
320	C3+	7287	-990	370	COM ₁₈	8967	990	420	SEGB ₉	6867	990
321	C3+	7329	-990	371	COM ₁₇	8925	990	421	SEGC ₉	6825	990
322	C3+	7371	-990	372	COM ₁₆	8883	990	422	SEGA ₁₀	6783	990
323	C3+	7413	-990	373	COM ₁₅	8841	990	423	SEGB ₁₀	6741	990
324	C3+	7455	-990	374	COM ₁₄	8799	990	424	SEGC ₁₀	6699	990
325	DMY ₇₉	7497	-990	375	COM ₁₃	8757	990	425	SEGA ₁₁	6657	990
326	C3-	7539	-990	376	COM ₁₂	8715	990	426	SEGB ₁₁	6615	990
327	C3-	7581	-990	377	COM ₁₁	8673	990	427	SEGC ₁₁	6573	990
328	C3-	7623	-990	378	COM ₁₀	8631	990	428	SEGA ₁₂	6531	990
329	C3-	7665	-990	379	COM ₉	8589	990	429	SEGB ₁₂	6489	990
330	C3-	7707	-990	380	COM ₈	8547	990	430	SEGC ₁₂	6447	990
331	C3-	7749	-990	381	COM ₇	8505	990	431	SEGA ₁₃	6405	990
332	C3-	7791	-990	382	COM ₆	8463	990	432	SEGB ₁₃	6363	990
333	C3-	7833	-990	383	COM ₅	8421	990	433	SEGC ₁₃	6321	990
334	C3-	7875	-990	384	COM ₄	8379	990	434	SEGA ₁₄	6279	990
335	C3-	7917	-990	385	COM ₃	8337	990	435	SEGB ₁₄	6237	990
336	DMY ₈₀	7959	-990	386	COM ₂	8295	990	436	SEGC ₁₄	6195	990
337	C4+	8001	-990	387	COM ₁	8253	990	437	SEGA ₁₅	6153	990
338	C4+	8043	-990	388	COM ₀	8211	990	438	SEGB ₁₅	6111	990
339	C4+	8085	-990	389	DMY ₉₁	8169	990	439	SEGC ₁₅	6069	990
340	C4+	8127	-990	390	DMY ₉₂	8127	990	440	SEGA ₁₆	6027	990
341	C4+	8169	-990	391	DMY ₉₃	8085	990	441	SEGB ₁₆	5985	990
342	C4+	8211	-990	392	SEGA ₀	8043	990	442	SEGC ₁₆	5943	990
343	C4+	8253	-990	393	SEGB ₀	8001	990	443	SEGA ₁₇	5901	990
344	C4+	8295	-990	394	SEGC ₀	7959	990	444	SEGB ₁₇	5859	990
345	C4+	8337	-990	395	SEGA ₁	7917	990	445	SEGC ₁₇	5817	990
346	C4+	8379	-990	396	SEGB ₁	7875	990	446	SEGA ₁₈	5775	990
347	DMY ₈₁	8421	-990	397	SEGC ₁	7833	990	447	SEGB ₁₈	5733	990
348	C4-	8463	-990	398	SEGA ₂	7791	990	448	SEGC ₁₈	5691	990
349	C4-	8505	-990	399	SEGB ₂	7749	990	449	SEGA ₁₉	5649	990
350	C4-	8547	-990	400	SEGC ₂	7707	990	450	SEGB ₁₉	5607	990

■ PAD COORDINATES 4

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
451	SEGC ₁₉	5565	990	501	SEGB ₃₆	3465	990	551	SEGA ₅₃	1365	990
452	SEGA ₂₀	5523	990	502	SEGC ₃₆	3423	990	552	SEGB ₅₃	1323	990
453	SEGB ₂₀	5481	990	503	SEGA ₃₇	3381	990	553	SEGC ₅₃	1281	990
454	SEGC ₂₀	5439	990	504	SEGB ₃₇	3339	990	554	SEGA ₅₄	1239	990
455	SEGA ₂₁	5397	990	505	SEGC ₃₇	3297	990	555	SEGB ₅₄	1197	990
456	SEGB ₂₁	5355	990	506	SEGA ₃₈	3255	990	556	SEGC ₅₄	1155	990
457	SEGC ₂₁	5313	990	507	SEGB ₃₈	3213	990	557	SEGA ₅₅	1113	990
458	SEGA ₂₂	5271	990	508	SEGC ₃₈	3171	990	558	SEGB ₅₅	1071	990
459	SEGB ₂₂	5229	990	509	SEGA ₃₉	3129	990	559	SEGC ₅₅	1029	990
460	SEGC ₂₂	5187	990	510	SEGB ₃₉	3087	990	560	SEGA ₅₆	987	990
461	SEGA ₂₃	5145	990	511	SEGC ₃₉	3045	990	561	SEGB ₅₆	945	990
462	SEGB ₂₃	5103	990	512	SEGA ₄₀	3003	990	562	SEGC ₅₆	903	990
463	SEGC ₂₃	5061	990	513	SEGB ₄₀	2961	990	563	SEGA ₅₇	861	990
464	SEGA ₂₄	5019	990	514	SEGC ₄₀	2919	990	564	SEGB ₅₇	819	990
465	SEGB ₂₄	4977	990	515	SEGA ₄₁	2877	990	565	SEGC ₅₇	777	990
466	SEGC ₂₄	4935	990	516	SEGB ₄₁	2835	990	566	SEGA ₅₈	735	990
467	SEGA ₂₅	4893	990	517	SEGC ₄₁	2793	990	567	SEGB ₅₈	693	990
468	SEGB ₂₅	4851	990	518	SEGA ₄₂	2751	990	568	SEGC ₅₈	651	990
469	SEGC ₂₅	4809	990	519	SEGB ₄₂	2709	990	569	SEGA ₅₉	609	990
470	SEGA ₂₆	4767	990	520	SEGC ₄₂	2667	990	570	SEGB ₅₉	567	990
471	SEGB ₂₆	4725	990	521	SEGA ₄₃	2625	990	571	SEGC ₅₉	525	990
472	SEGC ₂₆	4683	990	522	SEGB ₄₃	2583	990	572	SEGA ₆₀	483	990
473	SEGA ₂₇	4641	990	523	SEGC ₄₃	2541	990	573	SEGB ₆₀	441	990
474	SEGB ₂₇	4599	990	524	SEGA ₄₄	2499	990	574	SEGC ₆₀	399	990
475	SEGC ₂₇	4557	990	525	SEGB ₄₄	2457	990	575	SEGA ₆₁	357	990
476	SEGA ₂₈	4515	990	526	SEGC ₄₄	2415	990	576	SEGB ₆₁	315	990
477	SEGB ₂₈	4473	990	527	SEGA ₄₅	2373	990	577	SEGC ₆₁	273	990
478	SEGC ₂₈	4431	990	528	SEGB ₄₅	2331	990	578	SEGA ₆₂	231	990
479	SEGA ₂₉	4389	990	529	SEGC ₄₅	2289	990	579	SEGB ₆₂	189	990
480	SEGB ₂₉	4347	990	530	SEGA ₄₆	2247	990	580	SEGC ₆₂	147	990
481	SEGC ₂₉	4305	990	531	SEGB ₄₆	2205	990	581	SEGA ₆₃	105	990
482	SEGA ₃₀	4263	990	532	SEGC ₄₆	2163	990	582	SEGB ₆₃	63	990
483	SEGB ₃₀	4221	990	533	SEGA ₄₇	2121	990	583	SEGC ₆₃	21	990
484	SEGC ₃₀	4179	990	534	SEGB ₄₇	2079	990	584	SEGA ₆₄	-21	990
485	SEGA ₃₁	4137	990	535	SEGC ₄₇	2037	990	585	SEGB ₆₄	-63	990
486	SEGB ₃₁	4095	990	536	SEGA ₄₈	1995	990	586	SEGC ₆₄	-105	990
487	SEGC ₃₁	4053	990	537	SEGB ₄₈	1953	990	587	SEGA ₆₅	-147	990
488	SEGA ₃₂	4011	990	538	SEGC ₄₈	1911	990	588	SEGB ₆₅	-189	990
489	SEGB ₃₂	3969	990	539	SEGA ₄₉	1869	990	589	SEGC ₆₅	-231	990
490	SEGC ₃₂	3927	990	540	SEGB ₄₉	1827	990	590	SEGA ₆₆	-273	990
491	SEGA ₃₃	3885	990	541	SEGC ₄₉	1785	990	591	SEGB ₆₆	-315	990
492	SEGB ₃₃	3843	990	542	SEGA ₅₀	1743	990	592	SEGC ₆₆	-357	990
493	SEGC ₃₃	3801	990	543	SEGB ₅₀	1701	990	593	SEGA ₆₇	-399	990
494	SEGA ₃₄	3759	990	544	SEGC ₅₀	1659	990	594	SEGB ₆₇	-441	990
495	SEGB ₃₄	3717	990	545	SEGA ₅₁	1617	990	595	SEGC ₆₇	-483	990
496	SEGC ₃₄	3675	990	546	SEGB ₅₁	1575	990	596	SEGA ₆₈	-525	990
497	SEGA ₃₅	3633	990	547	SEGC ₅₁	1533	990	597	SEGB ₆₈	-567	990
498	SEGB ₃₅	3591	990	548	SEGA ₅₂	1491	990	598	SEGC ₆₈	-609	990
499	SEGC ₃₅	3549	990	549	SEGB ₅₂	1449	990	599	SEGA ₆₉	-651	990
500	SEGA ₃₆	3507	990	550	SEGC ₅₂	1407	990	600	SEGB ₆₉	-693	990

■ PAD COORDINATES 5

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

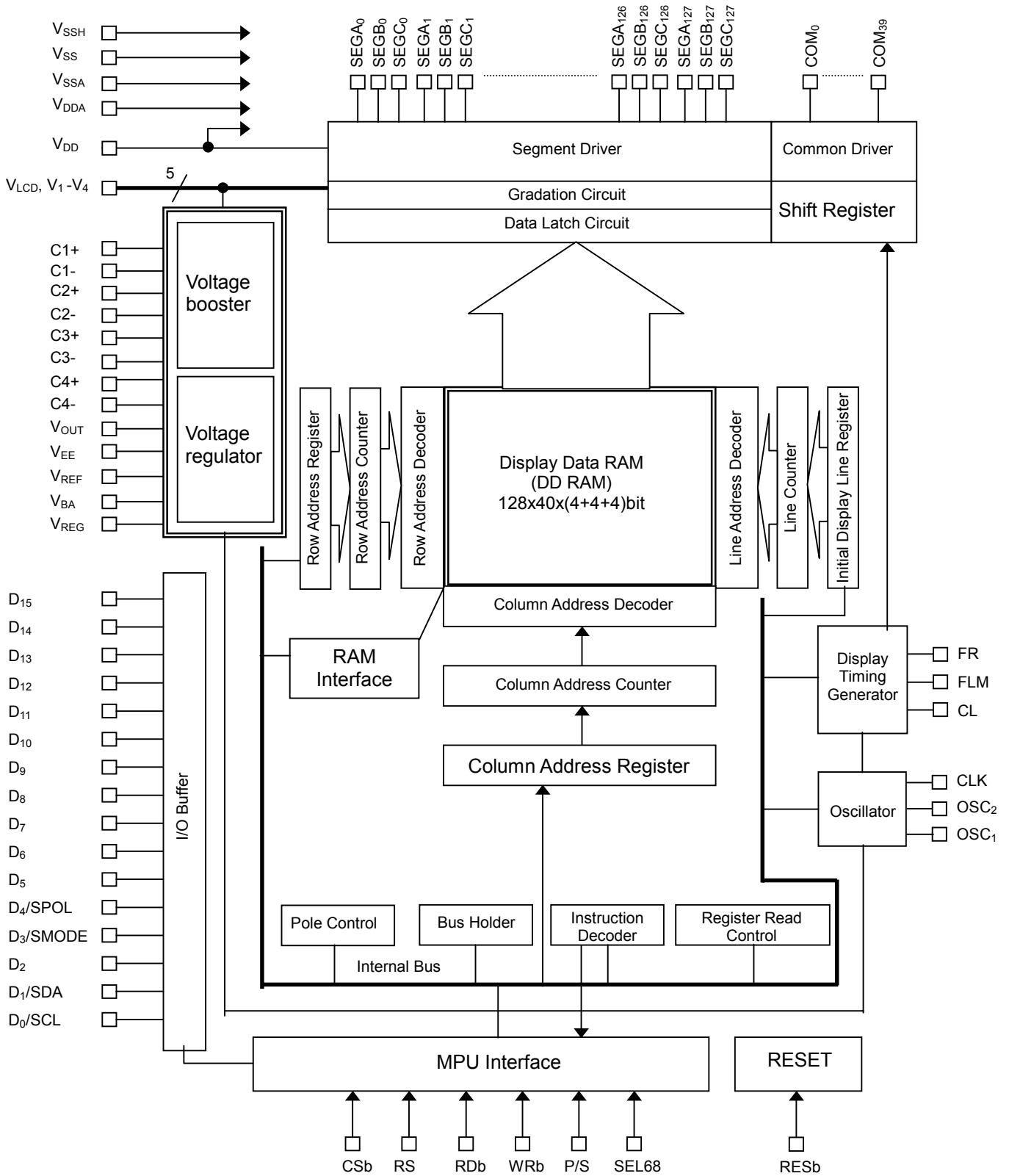
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
601	SEGC ₆₉	-735	990	651	SEGB ₈₆	-2835	990	701	SEGA ₁₀₃	-4935	990
602	SEGA ₇₀	-777	990	652	SEGC ₈₆	-2877	990	702	SEGB ₁₀₃	-4977	990
603	SEGB ₇₀	-819	990	653	SEGA ₈₇	-2919	990	703	SEGC ₁₀₃	-5019	990
604	SEGC ₇₀	-861	990	654	SEGB ₈₇	-2961	990	704	SEGA ₁₀₄	-5061	990
605	SEGA ₇₁	-903	990	655	SEGC ₈₇	-3003	990	705	SEGB ₁₀₄	-5103	990
606	SEGB ₇₁	-945	990	656	SEGA ₈₈	-3045	990	706	SEGC ₁₀₄	-5145	990
607	SEGC ₇₁	-987	990	657	SEGB ₈₈	-3087	990	707	SEGA ₁₀₅	-5187	990
608	SEGA ₇₂	-1029	990	658	SEGC ₈₈	-3129	990	708	SEGB ₁₀₅	-5229	990
609	SEGB ₇₂	-1071	990	659	SEGA ₈₉	-3171	990	709	SEGC ₁₀₅	-5271	990
610	SEGC ₇₂	-1113	990	660	SEGB ₈₉	-3213	990	710	SEGA ₁₀₆	-5313	990
611	SEGA ₇₃	-1155	990	661	SEGC ₈₉	-3255	990	711	SEGB ₁₀₆	-5355	990
612	SEGB ₇₃	-1197	990	662	SEGA ₉₀	-3297	990	712	SEGC ₁₀₆	-5397	990
613	SEGC ₇₃	-1239	990	663	SEGB ₉₀	-3339	990	713	SEGA ₁₀₇	-5439	990
614	SEGA ₇₄	-1281	990	664	SEGC ₉₀	-3381	990	714	SEGB ₁₀₇	-5481	990
615	SEGB ₇₄	-1323	990	665	SEGA ₉₁	-3423	990	715	SEGC ₁₀₇	-5523	990
616	SEGC ₇₄	-1365	990	666	SEGB ₉₁	-3465	990	716	SEGA ₁₀₈	-5565	990
617	SEGA ₇₅	-1407	990	667	SEGC ₉₁	-3507	990	717	SEGB ₁₀₈	-5607	990
618	SEGB ₇₅	-1449	990	668	SEGA ₉₂	-3549	990	718	SEGC ₁₀₈	-5649	990
619	SEGC ₇₅	-1491	990	669	SEGB ₉₂	-3591	990	719	SEGA ₁₀₉	-5691	990
620	SEGA ₇₆	-1533	990	670	SEGC ₉₂	-3633	990	720	SEGB ₁₀₉	-5733	990
621	SEGB ₇₆	-1575	990	671	SEGA ₉₃	-3675	990	721	SEGC ₁₀₉	-5775	990
622	SEGC ₇₆	-1617	990	672	SEGB ₉₃	-3717	990	722	SEGA ₁₁₀	-5817	990
623	SEGA ₇₇	-1659	990	673	SEGC ₉₃	-3759	990	723	SEGB ₁₁₀	-5859	990
624	SEGB ₇₇	-1701	990	674	SEGA ₉₄	-3801	990	724	SEGC ₁₁₀	-5901	990
625	SEGC ₇₇	-1743	990	675	SEGB ₉₄	-3843	990	725	SEGA ₁₁₁	-5943	990
626	SEGA ₇₈	-1785	990	676	SEGC ₉₄	-3885	990	726	SEGB ₁₁₁	-5985	990
627	SEGB ₇₈	-1827	990	677	SEGA ₉₅	-3927	990	727	SEGC ₁₁₁	-6027	990
628	SEGC ₇₈	-1869	990	678	SEGB ₉₅	-3969	990	728	SEGA ₁₁₂	-6069	990
629	SEGA ₇₉	-1911	990	679	SEGC ₉₅	-4011	990	729	SEGB ₁₁₂	-6111	990
630	SEGB ₇₉	-1953	990	680	SEGA ₉₆	-4053	990	730	SEGC ₁₁₂	-6153	990
631	SEGC ₇₉	-1995	990	681	SEGB ₉₆	-4095	990	731	SEGA ₁₁₃	-6195	990
632	SEGA ₈₀	-2037	990	682	SEGC ₉₆	-4137	990	732	SEGB ₁₁₃	-6237	990
633	SEGB ₈₀	-2079	990	683	SEGA ₉₇	-4179	990	733	SEGC ₁₁₃	-6279	990
634	SEGC ₈₀	-2121	990	684	SEGB ₉₇	-4221	990	734	SEGA ₁₁₄	-6321	990
635	SEGA ₈₁	-2163	990	685	SEGC ₉₇	-4263	990	735	SEGB ₁₁₄	-6363	990
636	SEGB ₈₁	-2205	990	686	SEGA ₉₈	-4305	990	736	SEGC ₁₁₄	-6405	990
637	SEGC ₈₁	-2247	990	687	SEGB ₉₈	-4347	990	737	SEGA ₁₁₅	-6447	990
638	SEGA ₈₂	-2289	990	688	SEGC ₉₈	-4389	990	738	SEGB ₁₁₅	-6489	990
639	SEGB ₈₂	-2331	990	689	SEGA ₉₉	-4431	990	739	SEGC ₁₁₅	-6531	990
640	SEGC ₈₂	-2373	990	690	SEGB ₉₉	-4473	990	740	SEGA ₁₁₆	-6573	990
641	SEGA ₈₃	-2415	990	691	SEGC ₉₉	-4515	990	741	SEGB ₁₁₆	-6615	990
642	SEGB ₈₃	-2457	990	692	SEGA ₁₀₀	-4557	990	742	SEGC ₁₁₆	-6657	990
643	SEGC ₈₃	-2499	990	693	SEGB ₁₀₀	-4599	990	743	SEGA ₁₁₇	-6699	990
644	SEGA ₈₄	-2541	990	694	SEGC ₁₀₀	-4641	990	744	SEGB ₁₁₇	-6741	990
645	SEGB ₈₄	-2583	990	695	SEGA ₁₀₁	-4683	990	745	SEGC ₁₁₇	-6783	990
646	SEGC ₈₄	-2625	990	696	SEGB ₁₀₁	-4725	990	746	SEGA ₁₁₈	-6825	990
647	SEGA ₈₅	-2667	990	697	SEGC ₁₀₁	-4767	990	747	SEGB ₁₁₈	-6867	990
648	SEGB ₈₅	-2709	990	698	SEGA ₁₀₂	-4809	990	748	SEGC ₁₁₈	-6909	990
649	SEGC ₈₅	-2751	990	699	SEGB ₁₀₂	-4851	990	749	SEGA ₁₁₉	-6951	990
650	SEGA ₈₆	-2793	990	700	SEGC ₁₀₂	-4893	990	750	SEGB ₁₁₉	-6993	990

■ PAD COORDINATES 6

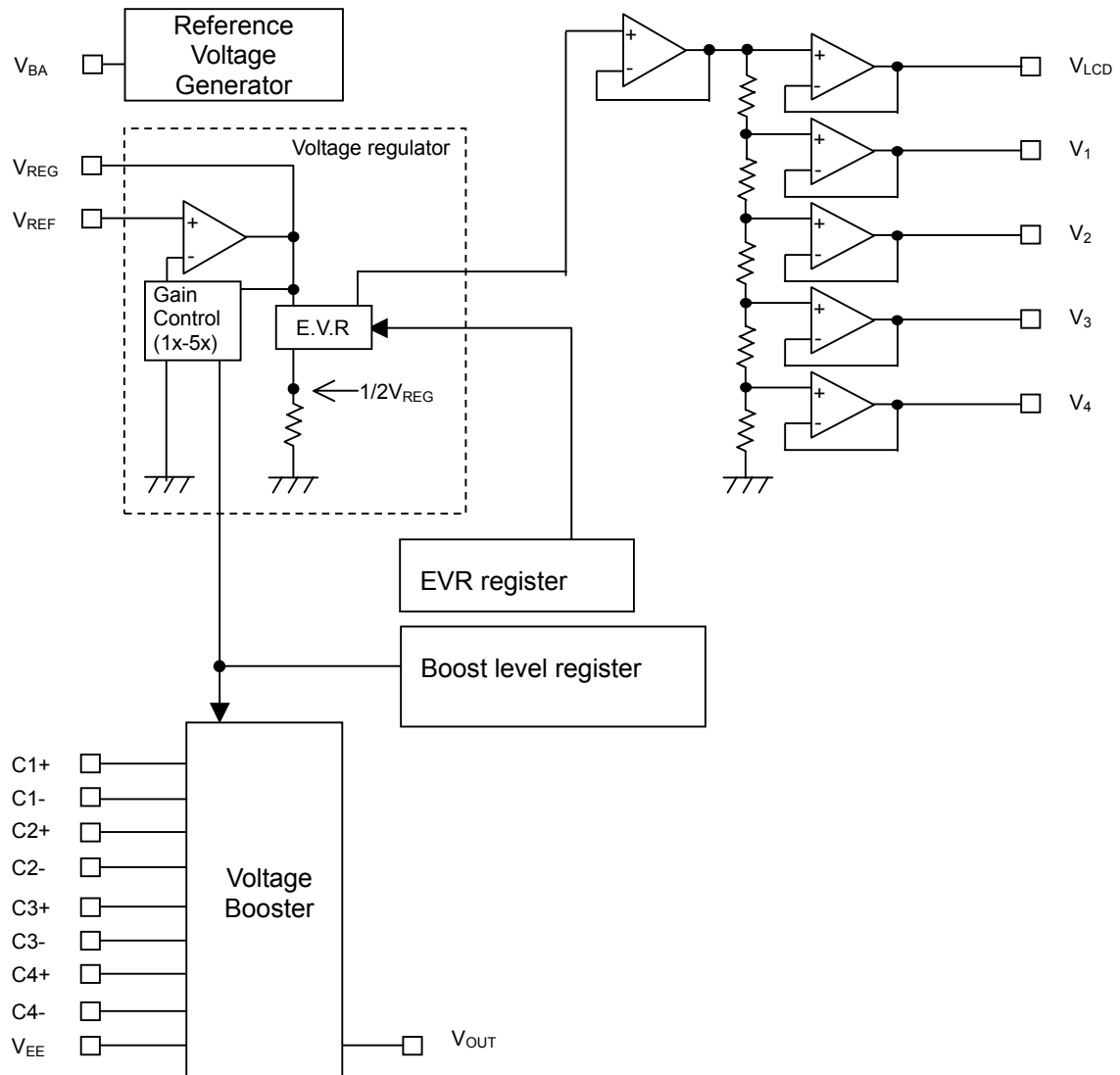
Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
751	SEGC ₁₁₉	-7035	990	801	DMY ₉₉	-9135	990				
752	SEGA ₁₂₀	-7077	990	802	DMY ₁₀₀	-9225	-742				
753	SEGB ₁₂₀	-7119	990	803	DMY ₁₀₁	-9225	-784				
754	SEGC ₁₂₀	-7161	990	804	DMY ₁₀₁	-9225	-826				
755	SEGA ₁₂₁	-7203	990	805	DMY ₁₀₁	-9225	-868				
756	SEGB ₁₂₁	-7245	990	806	DMY ₁₀₂	-9225	-910				
757	SEGC ₁₂₁	-7287	990	801	DMY ₉₉	-9135	990				
758	SEGA ₁₂₂	-7329	990	802	DMY ₁₀₀	-9225	-742				
759	SEGB ₁₂₂	-7371	990	803	DMY ₁₀₁	-9225	-784				
760	SEGC ₁₂₂	-7413	990	804	DMY ₁₀₁	-9225	-826				
761	SEGA ₁₂₃	-7455	990	805	DMY ₁₀₁	-9225	-868				
762	SEGB ₁₂₃	-7497	990	806	DMY ₁₀₂	-9225	-910				
763	SEGC ₁₂₃	-7539	990	801	DMY ₉₉	-9135	990				
764	SEGA ₁₂₄	-7581	990	802	DMY ₁₀₀	-9225	-742				
765	SEGB ₁₂₄	-7623	990								
766	SEGC ₁₂₄	-7665	990								
767	SEGA ₁₂₅	-7707	990								
768	SEGB ₁₂₅	-7749	990								
769	SEGC ₁₂₅	-7791	990								
770	SEGA ₁₂₆	-7833	990								
771	SEGB ₁₂₆	-7875	990								
772	SEGC ₁₂₆	-7917	990								
773	SEGA ₁₂₇	-7959	990								
774	SEGB ₁₂₇	-8001	990								
775	SEGC ₁₂₇	-8043	990								
776	DMY ₉₄	-8085	990								
777	DMY ₉₅	-8127	990								
778	DMY ₉₆	-8169	990								
779	COM ₂₀	-8211	990								
780	COM ₂₁	-8253	990								
781	COM ₂₂	-8295	990								
782	COM ₂₃	-8337	990								
783	COM ₂₄	-8379	990								
784	COM ₂₅	-8421	990								
785	COM ₂₆	-8463	990								
786	COM ₂₇	-8505	990								
787	COM ₂₈	-8547	990								
788	COM ₂₉	-8589	990								
789	COM ₃₀	-8631	990								
790	COM ₃₁	-8673	990								
791	COM ₃₂	-8715	990								
792	COM ₃₃	-8757	990								
793	COM ₃₄	-8799	990								
794	COM ₃₅	-8841	990								
795	COM ₃₆	-8883	990								
796	COM ₃₇	-8925	990								
797	COM ₃₈	-8967	990								
798	COM ₃₉	-9009	990								
799	DMY ₉₇	-9051	990								
800	DMY ₉₈	-9093	990								

■ BLOCK DIAGRAM



POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function						
111-121	V_{DD}	Power	Power supply for logic circuits						
146-156	V_{SS}	Power	GND for logic circuits						
239-248	V_{SSH}	Power	GND for high voltage circuits						
10,11, 42,43,	V_{DDA}	Power	This terminal is internally connected to the V_{DD} level. <ul style="list-style-type: none"> •This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.						
4,5, 16,17, 76,77,	V_{SSA}	Power	This terminal is internally connected to the V_{SS} level. <ul style="list-style-type: none"> •This terminal is used to fix the selection terminals to the V_{SS} level. Note) Do not use this terminal for a main GND.						
158-166 168-176 177-185 187-195 196-204	V_{LCD} V_1 V_2 V_3 V_4	Power/O	LCD driving voltages <ul style="list-style-type: none"> •When the internal voltage booster is not used, external LCD driving voltages (V_1 to V_4 and V_{LCD}) must be supplied on these terminals. The external voltages must be maintained with the following relation. $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD}$ • When the internal voltage booster is used, the LCD driving voltages (V_1 to V_4 and V_{LCD}) are enabled by the "Power control" instruction. The capacitors between the V_{SS} and these terminals are necessary. 						
271-280 282-291	C1+ C1-	O	Capacitor connection terminals for the voltage booster						
293-302 304-313	C2+ C2-	O	Capacitor connection terminals for the voltage booster						
315-324 326-335	C3+ C3-	O	Capacitor connection terminals for the voltage booster						
337-346 348-357	C4+ C4-	O	Capacitor connection terminals for the voltage booster						
228-237	V_{BA}	O	Output of the reference-voltage generator						
217-226	V_{REF}	I	Input of the voltage regulator						
260-269	V_{EE}	Power	Input of the voltage booster <ul style="list-style-type: none"> •This terminal is normally connected to the V_{DD} level. 						
249-258	V_{OUT}	Power/O	Output of the voltage booster Input for high voltage circuits in using external power supply						
206-215	V_{REG}	O	Output of the voltage regulator						
19,20	RESb	I	Reset Active "0"						
7,8	SEL68	I	MPU interface type select <table border="1" style="margin-left: 20px;"> <tr> <td>SEL68</td> <td>H</td> <td>L</td> </tr> <tr> <td>Status</td> <td>68 series</td> <td>80 series</td> </tr> </table>	SEL68	H	L	Status	68 series	80 series
SEL68	H	L							
Status	68 series	80 series							

■ TERMINAL DESCRIPTION 2

No.	Symbol	I/O	Function						
45,46	D ₀ /SCL	I/O	<p><u>Parallel interface:</u> D₇ to D₀ : 8-bit bi-directional bus</p> <ul style="list-style-type: none"> In the parallel interface mode (P/S="1"), these terminals connect to 8-bit bi-directional MPU bus. <p><u>Serial interface:</u> SDA : serial data SCL : serial clock SMODE : 3-/4-line serial interface mode selection SPOL : RS polarity selection (in the 3-line serial interface mode)</p> <ul style="list-style-type: none"> In the 3-/4-line serial interface mode (P/S="0"), the D₀ terminal is assigned to the SCL and the D₁ terminal to the SDA. In the 3-line serial interface mode, the D₄ terminal is assigned to the SPOL. Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D₇, D₆...D₀, and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal. The SCL signal must be set to "0" after data transmissions or during non-access. 						
49,50	D ₁ /SDA	I/O							
57,58	D ₃ /SMODE	I/O							
61,62	D ₄ /SPOL	I/O							
53,54 65,66 69,70 73,74	D ₂ D ₅ D ₆ D ₇	I/O							
79,80 83,84 87,88 91,92 95,96 99,100 103,104 107,108	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	<p>8-bit bi-directional bus</p> <ul style="list-style-type: none"> In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus. In the serial interface mode or 8-bit data bus mode of the parallel interface, these terminals must be fixed to "1" or "0". 						
24,25	CSb	I	Chip select Active "0"						
29,30	RS	I	<p>Resister select</p> <ul style="list-style-type: none"> This signal distinguishes transferred data as an instruction or display data as follows. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>RS</td> <td>H</td> <td>L</td> </tr> <tr> <td>Distinct.</td> <td>Instruction</td> <td>Display data</td> </tr> </table>	RS	H	L	Distinct.	Instruction	Display data
RS	H	L							
Distinct.	Instruction	Display data							
39,40	RDb (E)	I	<p>80 series MPU interface (P/S="1", SEL68="0") RDb signal. Active "L".</p> <p>68 series MPU interface (P/S="1", SEL68="1") Enable signal. Active "H".</p>						
34,35	WRb (R/W)	I	<p>80 series MPU interface (P/S="1", SEL68="0") WRb signal. Active "L".</p> <p>68 series MPU interface (P/S="1", SEL68="1") R/W signal.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>R/W</td> <td>H</td> <td>L</td> </tr> <tr> <td>Status</td> <td>Read</td> <td>Write</td> </tr> </table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Symbol	I/O	Function																		
13,14	P/S	I	Parallel / serial interface mode selection <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data/ Instruction</th> <th>Data</th> <th>Read/Write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>CSb</td> <td>RS</td> <td>D₀ ~ D₇</td> <td>RDb, WRb</td> <td>-</td> </tr> <tr> <td>L</td> <td>CSb</td> <td>RS</td> <td>SDA (D₁)</td> <td>Write only</td> <td>SCL (D₀)</td> </tr> </tbody> </table> <ul style="list-style-type: none"> •Since the D₁₅ to D₅ and D₂ terminals are in the high impedance in the serial inter face mode (P/S="0"), they must be fixed to "1" or "0". The RDb and WRb terminals also must be "1" or "0". 	P/S	Chip Select	Data/ Instruction	Data	Read/Write	Serial clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D ₁)	Write only	SCL (D ₀)
P/S	Chip Select	Data/ Instruction	Data	Read/Write	Serial clock																
H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-																
L	CSb	RS	SDA (D ₁)	Write only	SCL (D ₀)																
124,125	CL	O	This terminal must be opened.																		
128,129	FLM	O	This terminal must be opened.																		
132,133	FR	O	This terminal must be opened.																		
136,137	CLK	O	This terminal must be opened.																		
140,141 143,144	OSC ₁ OSC ₂	I O	OSC <ul style="list-style-type: none"> •When the internal oscillator clock is used, OSC₁ terminal must be fixed to "1" or "0", and the OSC₂ terminal must be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC₁ terminal and OSC₂. •When an external oscillator is used, external clock is input to the OSC₁ terminal or an external resistor is connected between the OSC₁ and OSC₂ terminals. 																		

■ TERMINAL DESCRIPTION 4

No.	Symbol	I/O	Function															
392-775	SEGA ₀ - SEGA ₁₂₇ , SEGB ₀ - SEGB ₁₂₇ , SEGC ₀ - SEGC ₁₂₇	O	<p>Segment output</p> <table border="1"> <thead> <tr> <th>REV Mode</th> <th>Turn-off</th> <th>Turn-on</th> </tr> </thead> <tbody> <tr> <td>Normal</td> <td>0</td> <td>1</td> </tr> <tr> <td>Reverse</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data.</p> <p><u>In the B/W mode</u></p> <p>FR signal</p> <p>Display data</p> <p>Normal display mode</p> <p>Reverse display mode</p>	REV Mode	Turn-off	Turn-on	Normal	0	1	Reverse	1	0						
REV Mode	Turn-off	Turn-on																
Normal	0	1																
Reverse	1	0																
369-388, 779-798,	COM ₀ -COM ₃₉	O	<p>Common output</p> <ul style="list-style-type: none"> • These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data. <table border="1"> <thead> <tr> <th>Data</th> <th>FR</th> <th>Output level</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V_{SS}</td> </tr> <tr> <td>L</td> <td>H</td> <td>V₁</td> </tr> <tr> <td>H</td> <td>L</td> <td>V_{LCD}</td> </tr> <tr> <td>L</td> <td>L</td> <td>V₄</td> </tr> </tbody> </table>	Data	FR	Output level	H	H	V _{SS}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄
Data	FR	Output level																
H	H	V _{SS}																
L	H	V ₁																
H	L	V _{LCD}																
L	L	V ₄																

Terminal No.

1-3, 12, 18, 21-23, 26-28, 31-33, 36-38, 41, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 81, 82, 85, 86, 89, 90, 93, 94, 97, 98, 101, 102, 105, 106, 109, 110, 122, 123, 126, 127, 130, 131, 134, 135, 138, 139, 142, 145, 157, 167, 186, 205, 216, 227, 238, 259, 270, 281, 292, 314, 325, 336, 347, 358-368, 389-391, 776-778, 799-806 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Selection of Parallel / serial interface mode select

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is possible to read out display data from the DDRAM and status from the internal registers.

Table1

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68	/	/	D ₇ -D ₀ (D ₁₅ -D ₀)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) “-” : Fix to “1” or “0”.

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type as shown in the following table.

Table2

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D ₇ -D ₀ (D ₁₅ -D ₀)
L	80 series MPU	CSb	RS	RDb	WRb	D ₇ -D ₀ (D ₁₅ -D ₀)

(1-3) Data distinction

In the parallel interface mode, the combination of RS, RDb, and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table3

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode as shown in the following table.

Table4

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

In the 4-line serial interface mode, when during the chip select is active (CSb="0"), the SDA and the SCL are enabled. When During the chip select is not active (CSb="1"), the SDA and the SCL are disabled and the internal shift register and the counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the D₇, D₆...D₀, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.

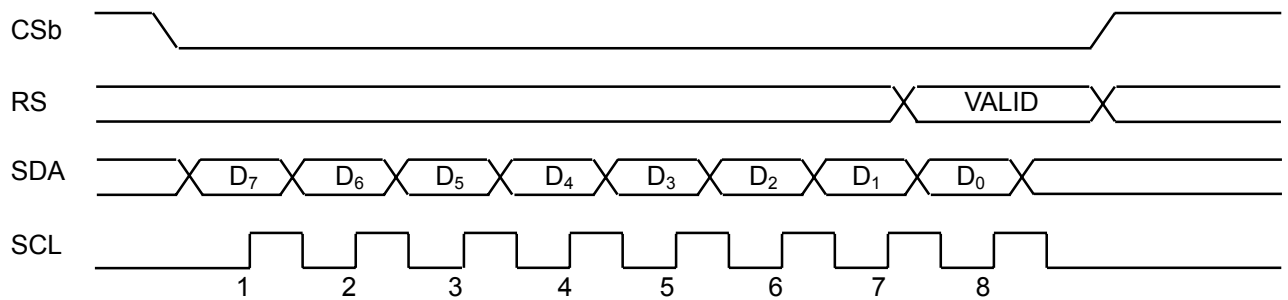


Fig1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, when the chip select is active (CSb="0"), the SDA and SCL are enabled. When the chip select is not active (CSb="1"), the SDA and SCL are disabled and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D₇, D₆...D₀, and the fetched data is converted into the 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of SDA data and the status of the SPOL, as follows.

Table6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

Since the serial interface operation is sensitive to external noises, the SCL must be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.

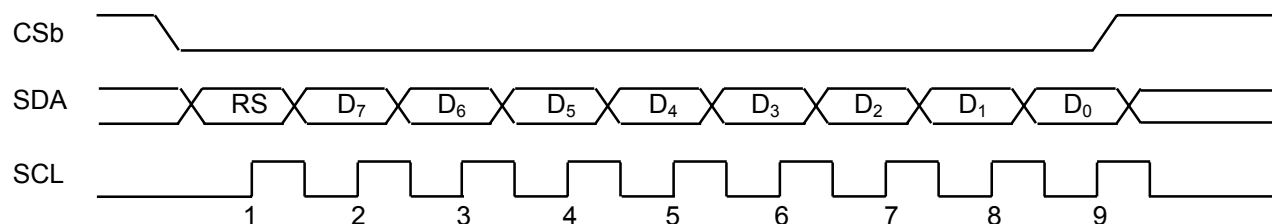


Fig2 3-line serial interface timing

(2) Access to the DDRAM

When the CSb signal is "0", the transferred data from MPU is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

When the RS signal is "1", the transferred data is distinguished as display data. After the "column address" and "row address" instructions are executed, the display data can be written into the DDRAM by the "display data write" instruction. The display data is written at the rising edge of the WRb signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table6

RS	Data
L	Display RAM Data
H	Internal Command Register

In the sequence of the "display data read" operation, the transferred data from MPU is temporarily held in the internal bus-holder and then transferred to the internal data-bus. When the "display data read" operation is executed just after the "column address" and "row address" instructions or "display data write" instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

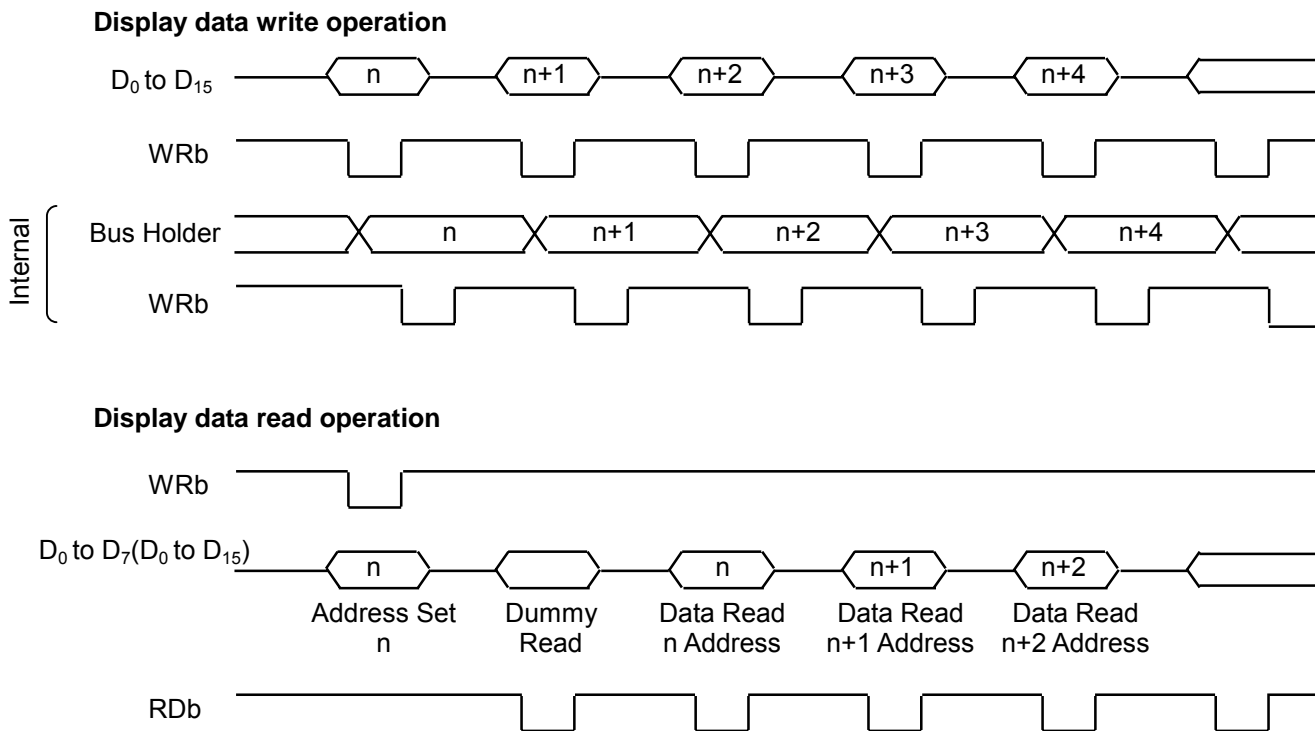


Fig3

Note) In the 16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each instruction registers is assigned to each address between 0_H and F_H , and the content of the instruction register can be read out by the combination of the "Instruction register address" and "Instruction register read".

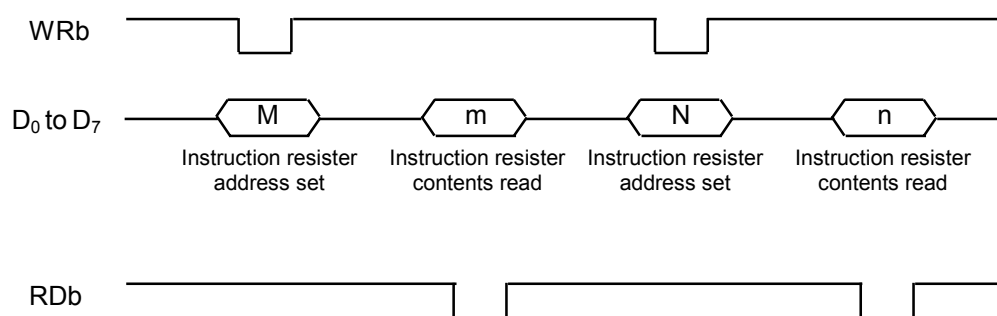


Fig4

(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the "WLS" of the "Data bus length" instruction.

In the 16-bit data bus mode, not only the display data but also the instruction data is required to be transferred by 16-bit data (D_{15} to D_0). However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table8

WLS	Data bus length mode
0	8-bit
1	16-bit

(5) Initial display line register

The initial display line register specifies the line address, corresponding to the initial COM line, by the "Initial display line" instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the "Initial COM line" instruction.

The line address, established in the initial display line register, is preset into the line counter whenever the FLM signal becomes "1". At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

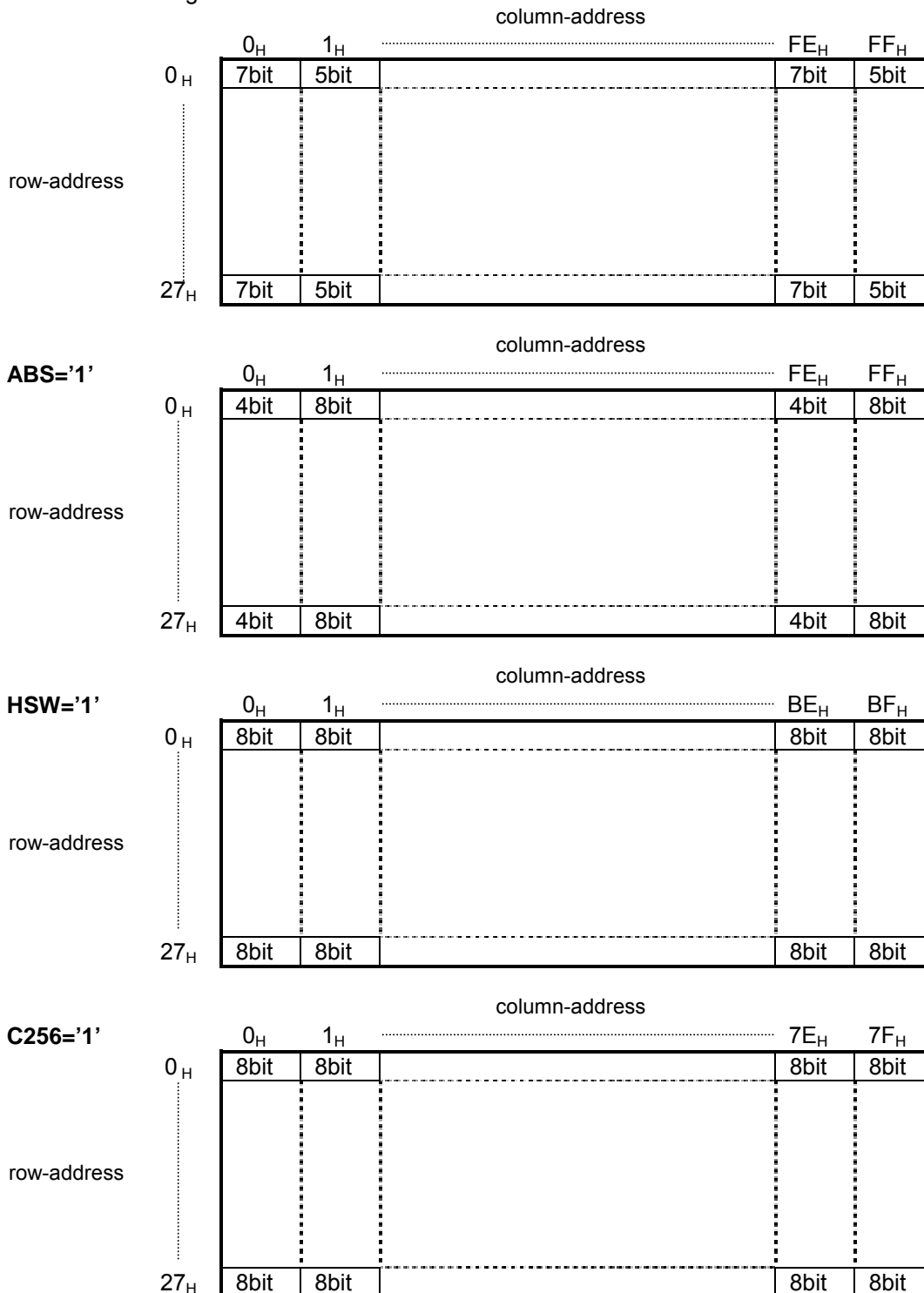
NJU6820

(6) DDRAM mapping

The DDRAM is capable of 1,536-bit (12-bit x 128-segment) for the column address and 40-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to successive 3-segment drivers, and each segment driver has 16-gradation. Therefore, the LSI can drive up to 128x40 pixels in 4096-color display (16-gradation x 16-gradation x 16-gradation).

- In the 8-bit data bus length mode



- In the 16-bit data bus length mode

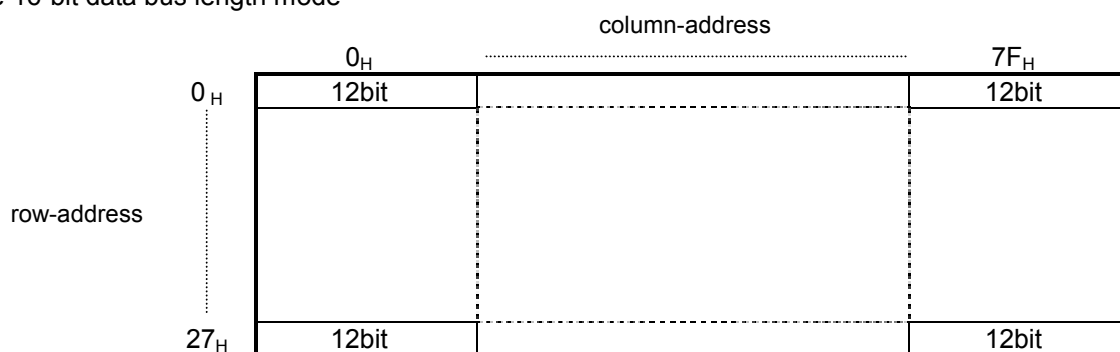


Fig6

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 384 x 40 pixels in the B&W and 128 x 40 pixels in the 8-gradation are available.

The range of the column address varies depending on data bus length. The range between 00_H and FF_H is used in the 8-bit data bus length and the range between 00_H and $7F_H$ is in the 16-bit data bus length.

The increments for the column address and row address are set to the auto-increment mode by programming the "AXI" and "AYI" registers of the "Increment control" instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column and row addresses for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

RAM Map 1

Mode	WLS	ABS	HSW	REF	256	SEGC0									SEGC1									SEGC126									SEGC127								
						Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0																		
1	0	X	0	0	0	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D4 D3 D2 D1	X=7EH												
1	0	X	1	0	0	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=7EH	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=00H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=01H	D15 D14 D13 D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1	X=7EH												
1	1	X	0	1	0	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=7FH	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	X=7EH												
0	0	0	0	0	0	D7 D6 D5 D4 D2 D1 D0	X=00H	D7 D6 D5 D4 D2 D1 D0	X=01H	D7 D6 D5 D4 D2 D1 D0	X=7FH	D7 D6 D5 D4 D2 D1 D0	X=00H	D7 D6 D5 D4 D2 D1 D0	X=01H	D7 D6 D5 D4 D2 D1 D0	X=7FH	D7 D6 D5 D4 D2 D1 D0	X=00H	D7 D6 D5 D4 D2 D1 D0	X=01H	D7 D6 D5 D4 D2 D1 D0	X=7FH	D7 D6 D5 D4 D2 D1 D0	X=00H	D7 D6 D5 D4 D2 D1 D0	X=01H	D7 D6 D5 D4 D2 D1 D0	X=7FH												
0	1	0	0	0	0	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FEH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FFH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FDH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FEH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FFH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FDH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FEH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FFH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FDH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FEH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FFH	D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=FDH												
0	X	1	0	0	0	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=7FH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=7FH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=7FH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=7FH												
0	X	1	0	0	0	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BEH(L)	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BFH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BDH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BEH(H)	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BFH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BDH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BEH(L)	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BFH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BDH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BEH(H)	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BFH	D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0	X=BDH												

RAM Map 2 (256 Color Mode)

Mode	WLS	ABS	HSW	REF	256	SEGC0									SEGC1									SEGC126									SEGC127								
						Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0																		
0	X	X	0	1	1	D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0	X=7EH	D7 D6 D5 D4 D3 D2 D1 D0	X=00H	D7 D6 D5 D4 D3 D2 D1 D0	X=01H	D7 D6 D5 D4 D3 D2 D1 D0	X=7EH												
8bit	0	X	X	1	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-										

SWAP

REF	SWAP	Palette A A3 A2 A1 A0	Palette B B3 B2 B1 B0	Palette C C3 C2 C1 C0
0	0	SEGCX	SEGBX	SEGCX
1	1	SEGCX	SEGBX	SEGCX
0	1	SEGCX	SEGBX	SEGCX

Note1) In the 256-color mode, the vacant LSB bit is filled with "1".
 Note2) The function of 256-color mode is different from that of fixed 8-gradation mode (fixed 256-color mode).
 Note3) The written data in the DD RAM in "C256"=0 in not compatible with the data in "C256"=1.
 Note4) In the 256-color mode, only 8-bit length mode is available, but 16-bit is not.

(7) Window addressing mode

In addition to the above usual DDRAM addressing, it is possible to access some part of DDRAM in using the window addressing mode, in which the start and end points are designated. The start point is determined by the "column address" and "row address" instructions, and the end point is determined by the "Window end column address" and "Window end row address" instructions. The setting example of the window addressing is listed, as follows.

1. Set WIN=1, AXI=1 and AYI=1 by the "Increment control" instruction
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode

In the window addressing mode (WIN=1, AXI=1, AYI=1), the read-modify-write operation is available by setting "0" to the "AIM" register of the "Increment control" instruction.

And in the window addressing mode, the following start and end point must be maintained to abide a malfunction.

$$AX \text{ (column address of start point)} \leq EX \text{ (column address of end point)} \leq \text{Maximum of column address}$$

$$AY \text{ (row address of start point)} \leq EY \text{ (row address of end point)} \leq \text{Maximum of row address}$$

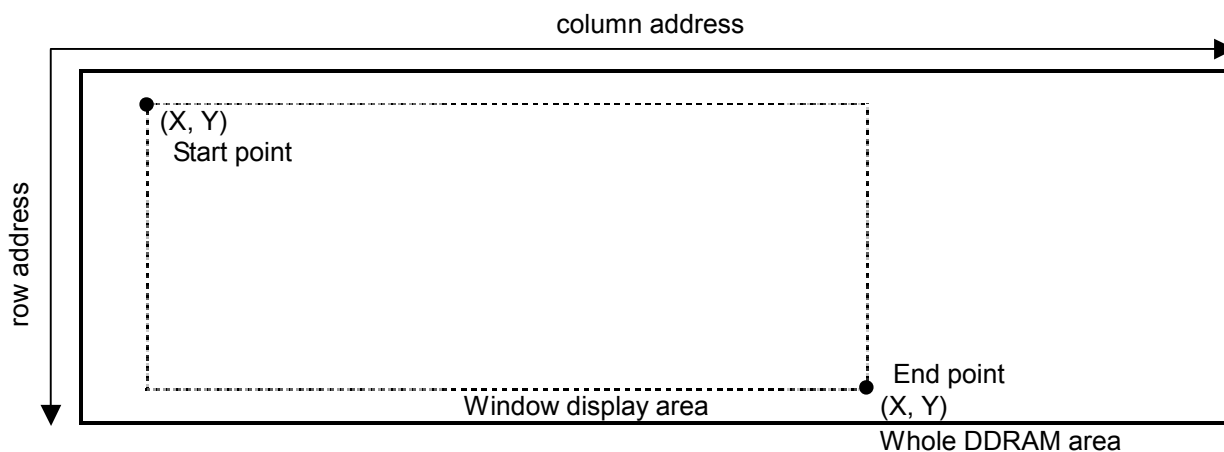


Fig7

(8) Reverse display ON/OFF

The "Reverse display ON/OFF" function is used to reverse the display data without changing the contents of the DDRAM.

Table9

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Segment direction

The "Segment direction" function is used to reverse the assignment for the segment drivers and column address, and it is possible to reduce the restrictions for the placement of the LSI on the LCD modules.

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(10) The relationship among the DDRAM column address, display data and segment drivers

In the color mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	0	0	0	X=00 _H										↔	X=7F _H													
*	0	1	1	X=7F _H										↔	X=00 _H													
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	0	0	1	X=00 _H										↔	X=7F _H													
*	0	1	0	X=7F _H										↔	X=00 _H													
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	1	0	0	X=00 _H										↔	X=7F _H													
*	1	1	1	X=7F _H										↔	X=00 _H													
				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	1	0	1	X=00 _H										↔	X=7F _H													
*	1	1	0	X=7F _H										↔	X=00 _H													
				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

In the color mode, and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																														
0	0	0	0	X=00 _H					X=01 _H					↔					X=FE _H					X=FF _H										
0	0	1	1	X=FE _H					X=FF _H					↔					X=00 _H					X=01 _H										
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				palette A					palette B					palette C					↕	palette A					palette B					palette C				
				SEGA ₀					SEGB ₀					SEGC ₀					↕	SEGA ₁₂₇					SEGB ₁₂₇					SEGC ₁₂₇				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																														
0	0	0	1	X=00 _H					X=01 _H					↔					X=FE _H					X=FF _H										
0	0	1	0	X=FE _H					X=FF _H					↔					X=00 _H					X=01 _H										
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				palette A					palette B					palette C					↕	palette A					palette B					palette C				
				SEGC ₀					SEGB ₀					SEGA ₀					↕	SEGC ₁₂₇					SEGB ₁₂₇					SEGA ₁₂₇				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																												
0	1	0	0	X=00 _H				X=01 _H								↔				X=FE _H				X=FF _H								
0	1	1	1	X=FE _H				X=FF _H								↔				X=00 _H				X=01 _H								
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
				palette A				palette B				palette C				↕	palette A				palette B				palette C							
				SEGA ₀				SEGB ₀				SEGC ₀				↕	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇							

HSW	ABS	REF	SWAP	Column address / bit / segment assign																												
0	1	0	1	X=00 _H				X=01 _H								↔				X=FE _H				X=FF _H								
0	1	1	0	X=FE _H				X=FF _H								↔				X=00 _H				X=01 _H								
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀				
				palette A				palette B				palette C				↕	palette A				palette B				palette C							
				SEGC ₀				SEGB ₀				SEGA ₀				↕	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇							

HSW	ABS	REF	SWAF	Column-address / bit / segment assign			
1	*	1	1				
SEGA 0	Palette A	D3	X=BEH				
		D2					
		D1					
		D0					
SEGB 0	Palette B	D7	X=BFH				
		D6					
		D5					
		D4					
SEGC 0	Palette C	D3	X=BFH				
		D2					
		D1					
		D0					
SEGA 1	Palette A	D7	X=BDH				
		D6					
		D5					
		D4					
SEGB 1	Palette B	D3	X=BDH				
		D2					
		D1					
		D0					
SEGC 1	Palette C	D7	X=BEH				
		D6					
		D5					
		D4					
SEGA 126	Palette A	D3	X=01H				
		D2					
		D1					
		D0					
SEGB 126	Palette B	D7	X=02H				
		D6					
		D5					
		D4					
SEGC 126	Palette C	D3	X=02H				
		D2					
		D1					
		D0					
SEGA 127	Palette A	D7	X=00H				
		D6					
		D5					
		D4					
SEGB 127	Palette B	D3	X=00H				
		D2					
		D1					
		D0					
SEGC 127	Palette C	D7	X=01H				
		D6					
		D5					
		D4					

HSW	ABS	REF	SWAF	Column-address / bit / segment assign			
1	*	1	0				
SEGC 0	Palette A	D3	X=BEH				
		D2					
		D1					
		D0					
SEGB 0	Palette B	D7	X=BFH				
		D6					
		D5					
		D4					
SEGA 0	Palette C	D3	X=BFH				
		D2					
		D1					
		D0					
SEGC 1	Palette A	D7	X=BDH				
		D6					
		D5					
		D4					
SEGB 1	Palette B	D3	X=BDH				
		D2					
		D1					
		D0					
SEGA 1	Palette C	D7	X=BEH				
		D6					
		D5					
		D4					
SEGC 126	Palette A	D3	X=01H				
		D2					
		D1					
		D0					
SEGB 126	Palette B	D7	X=02H				
		D6					
		D5					
		D4					
SEGA 126	Palette C	D3	X=02H				
		D2					
		D1					
		D0					
SEGC 127	Palette A	D7	X=00H				
		D6					
		D5					
		D4					
SEGB 127	Palette B	D3	X=00H				
		D2					
		D1					
		D0					
SEGA 127	Palette C	D7	X=01H				
		D6					
		D5					
		D4					

HSW	ABS	REF	SWAF	Column-address / bit / segment assign			
1	*	0	1				
SEGC 0	Palette A	D7	X=00H				
		D6					
		D5					
		D4					
SEGB 0	Palette B	D3	X=01H				
		D2					
		D1					
		D0					
SEGA 0	Palette C	D7	X=01H				
		D6					
		D5					
		D4					
SEGC 1	Palette A	D3	X=02H				
		D2					
		D1					
		D0					
SEGB 1	Palette B	D7	X=02H				
		D6					
		D5					
		D4					
SEGA 1	Palette C	D3	X=02H				
		D2					
		D1					
		D0					
SEGC 126	Palette A	D7	X=BDH				
		D6					
		D5					
		D4					
SEGB 126	Palette B	D3	X=BDH				
		D2					
		D1					
		D0					
SEGA 126	Palette C	D7	X=BEH				
		D6					
		D5					
		D4					
SEGC 127	Palette A	D3	X=BEH				
		D2					
		D1					
		D0					
SEGB 127	Palette B	D7	X=BFH				
		D6					
		D5					
		D4					
SEGA 127	Palette C	D3	X=BFH				
		D2					
		D1					
		D0					

HSW	ABS	REF	SWAF	Column-address / bit / segment assign			
1	*	0	0				
SEGA 0	Palette A	D7	X=00H				
		D6					
		D5					
		D4					
SEGB 0	Palette B	D3	X=01H				
		D2					
		D1					
		D0					
SEGC 0	Palette C	D7	X=01H				
		D6					
		D5					
		D4					
SEGA 1	Palette A	D3	X=02H				
		D2					
		D1					
		D0					
SEGB 1	Palette B	D7	X=02H				
		D6					
		D5					
		D4					
SEGC 1	Palette C	D3	X=02H				
		D2					
		D1					
		D0					
SEGA 126	Palette A	D7	X=BDH				
		D6					
		D5					
		D4					
SEGB 126	Palette B	D3	X=BDH				
		D2					
		D1					
		D0					
SEGC 126	Palette C	D7	X=BEH				
		D6					
		D5					
		D4					
SEGA 127	Palette A	D3	X=BEH				
		D2					
		D1					
		D0					
SEGB 127	Palette B	D7	X=BFH				
		D6					
		D5					
		D4					
SEGC 127	Palette C	D3	X=BFH				
		D2					
		D1					
		D0					

In the color mode, 8-bit data bus mode, and C256 mode (C256=1)

HSW	ABS	REF	SWAP	Column address / bit / segment assign																		
*	*	0	0	X=00 _H						↔	X=7F _H											
*	*	1	1	X=7F _H						↔	X=00 _H											
				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				palette A			palette B			palette C			↔	palette A			palette B			palette C		
				SEGA ₀			SEGB ₀			SEGC ₀			↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇		

HSW	ABS	REF	SWAP	Column address / bit / segment assign																		
*	*	0	1	X=00 _H						↔	X=7F _H											
*	*	1	0	X=7F _H						↔	X=00 _H											
				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				palette A			palette B			palette C			↔	palette A			palette B			palette C		
				SEGC ₀			SEGB ₀			SEGA ₀			↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇		

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In the B&W mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	0	0	0	X=00 _H								↔	X=7F _H																							
*	0	1	1	X=7F _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGA ₀					SEGB ₀						SEGA ₀					↔	SEGA ₁₂₇									SEGB ₁₂₇						

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	0	0	1	X=00 _H								↔	X=7F _H																							
*	0	1	0	X=7F _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGC ₀					SEGB ₀						SEGA ₀					↔	SEGC ₁₂₇									SEGB ₁₂₇						

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	1	0	0	X=00 _H								↔	X=7F _H																							
*	1	1	1	X=7F _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
								SEGA ₀								SEGC ₀				↔					SEGA ₁₂₇					SEGB ₁₂₇				SEGC ₁₂₇		

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	1	0	1	X=00 _H								↔	X=7F _H																							
*	1	1	0	X=7F _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
								SEGC ₀								SEGA ₀				↔					SEGC ₁₂₇					SEGB ₁₂₇				SEGA ₁₂₇		

In the B&W mode, and 8-bit data bus mode

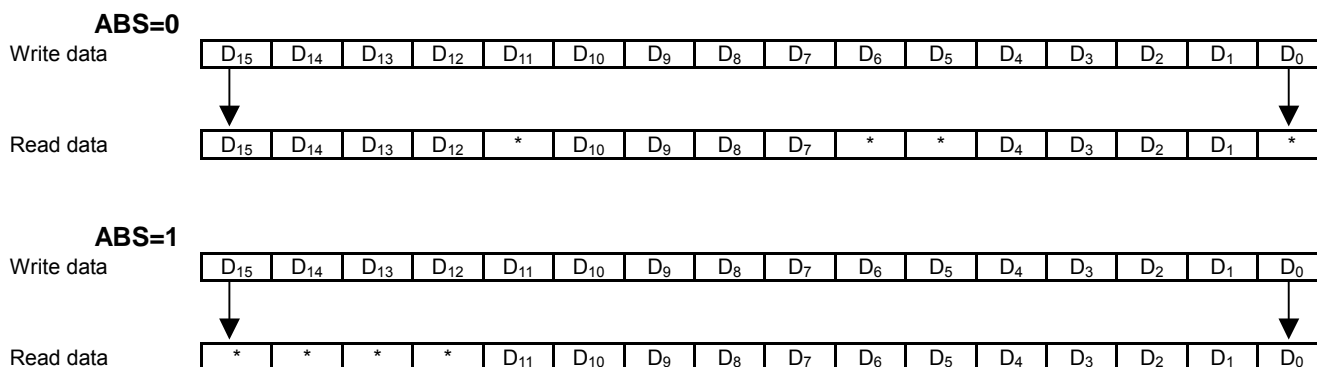
HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	0	0	0	X=00 _H				X=01 _H				↔	X=FE _H				X=FF _H												
0	0	1	1	X=FE _H				X=FF _H				↔	X=00 _H				X=01 _H												
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
				SEGA ₀				SEGB ₀					SEGC ₀					SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	0	0	1	X=00 _H				X=01 _H				↔	X=FE _H				X=FF _H												
0	0	1	0	X=FE _H				X=FF _H				↔	X=00 _H				X=01 _H												
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
				SEGC ₀				SEGB ₀					SEGA ₀					SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

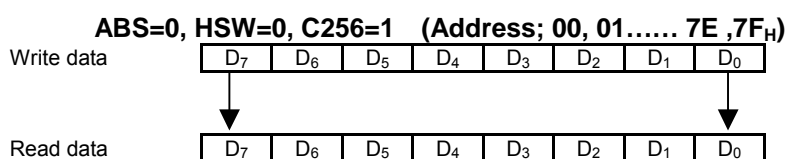
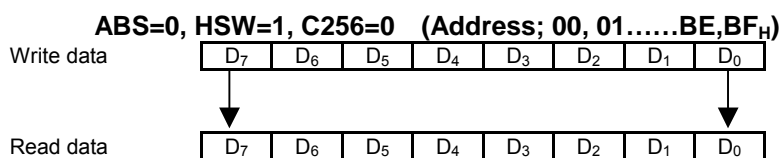
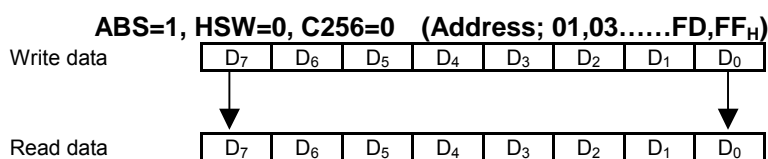
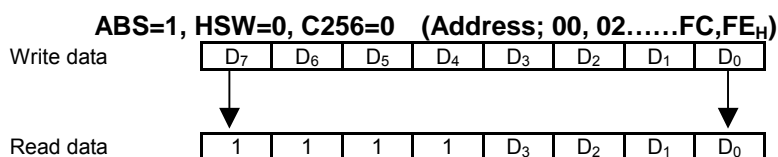
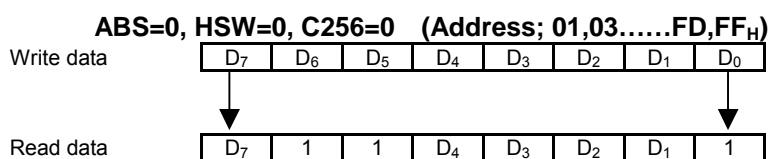
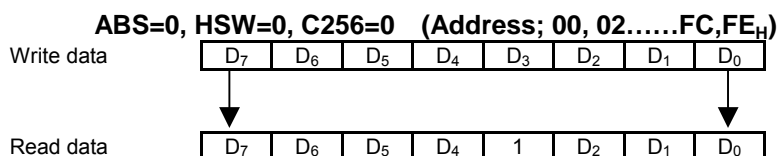
HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	1	0	0	X=00 _H				X=01 _H				↔	X=FE _H				X=FF _H												
0	1	1	1	X=FE _H				X=FF _H				↔	X=00 _H				X=01 _H												
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				SEGA ₀				SEGB ₀					SEGC ₀					SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	1	0	1	X=00 _H				X=01 _H				↔	X=FE _H				X=FF _H												
0	1	1	0	X=FE _H				X=FF _H				↔	X=00 _H				X=01 _H												
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				SEGC ₀				SEGB ₀					SEGA ₀					SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

Bit assignments between write and read data (in the 16-bit data bus mode)



Examples of write and read data (In the 8 bit bus mode)



* : Invalid data

(11) Gradation palette

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0: Variable gradation mode
(Select 16 gradation levels out of 32-gradation level of the gradation palette)

PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

In these mode, each of the gradation palettes Aj, Bj and Cj can select 16-gradation level out of 32-gradation level by setting 5-bit data to the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh).

For instance, the gradation palettes Aj correspond to the SEGAi, the Bj to SEGBi and the Cj to SEGCi (j=0 to 15, i=0 to 127).

Correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0
0	0	0	1	Palette 1	0 0 0 1
0	0	1	0	Palette 2	0 0 1 0
0	0	1	1	Palette 3	0 0 1 1
0	1	0	0	Palette 4	0 1 0 0
0	1	0	1	Palette 5	0 1 0 1
0	1	1	0	Palette 6	0 1 1 0
0	1	1	1	Palette 7	0 1 1 1
1	0	0	0	Palette 8	1 0 0 0
1	0	0	1	Palette 9	1 0 0 1
1	0	1	0	Palette 10	1 0 1 0
1	0	1	1	Palette 11	1 0 1 1
1	1	0	0	Palette 12	1 1 0 0
1	1	0	1	Palette 13	1 1 0 1
1	1	1	0	Palette 14	1 1 1 0
1	1	1	1	Palette 15	1 1 1 1

Gradation palette table (Variable gradation mode, PWM="0", MON="0")

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0	0	Palette 0(default)	1 0 0 0	16/31	
0 0 0 1	1/31		1 0 0 1	17/31	Palette 0(default)8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

Correspondence between display data and gradation level (B&W mode, MON="1")

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

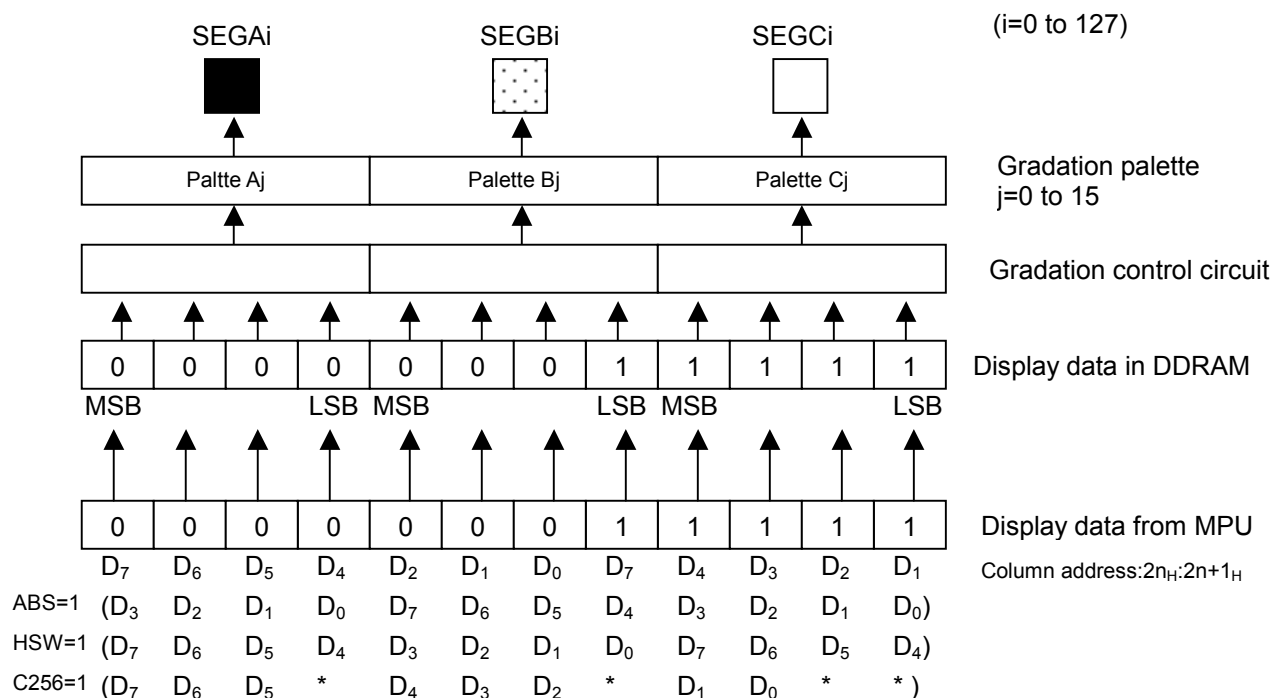
(12) Gradation control and display data

(12-1) Gradation mode

In the gradation mode, each pixel for RGB corresponds to successive 3 segment drivers, and each segment driver provides 16-gradation PWM output by controlling 4 bit display data of the DDRAM. Accordingly, the LSI can drive up to 128x40 pixels in 4096-color (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit).

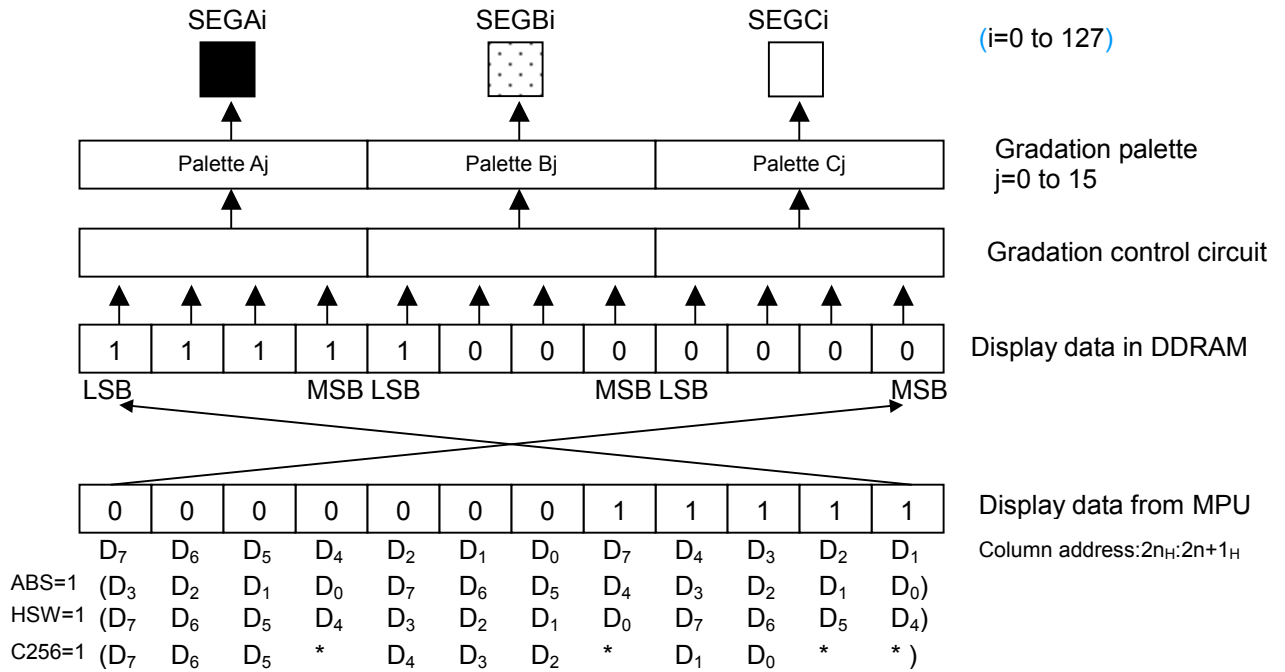
In addition, the LSI can transfer the display data for the RGB by 16-bit at once or 8-bit two-times. The data assignment between gradation palettes and segment drivers varies in accordance with setting for the "SWAP" and "REF" registers of the "Display control (2)" instruction.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address :2n_H, 2n_H+1_H (REF="0")
 :FE_H-2n_H, FF_H-(2n_H+1_H) (REF="1")
 HSW=1; 00_H to BF_H, C256=1; 00_H to 7F_H

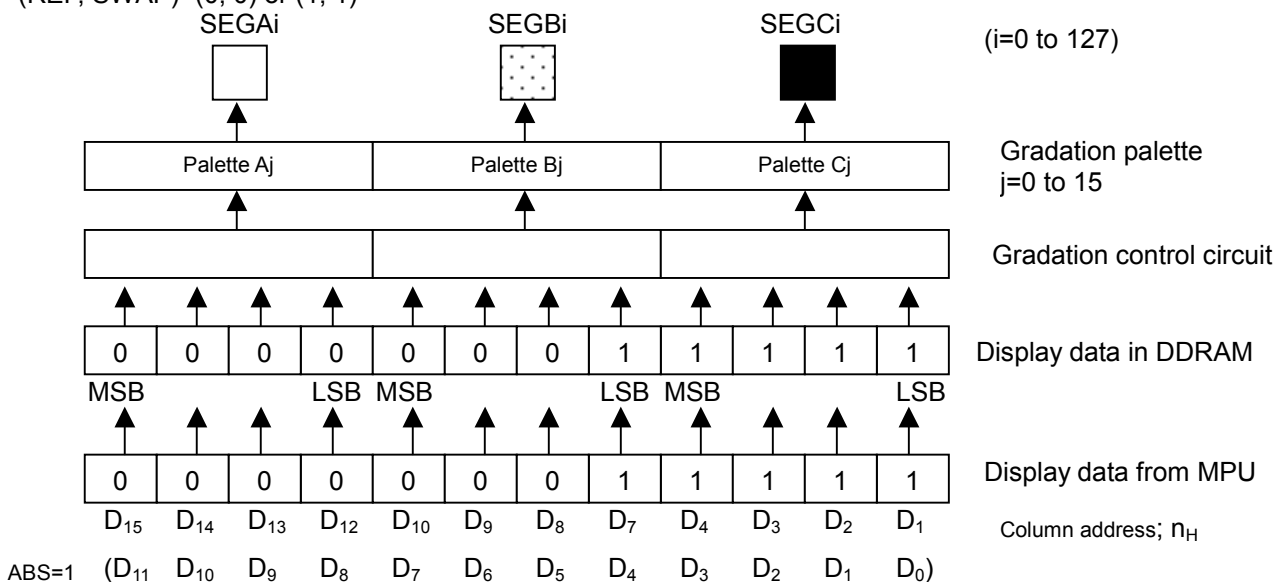
(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : $2n_H, 2n_H+1_H$ (REF="0")
 : $FE_H-2n_H, FF_H-(2n_H+1_H)$ (REF="1")
 HSW=1; 00_H to BF_H , C256=; 00_H to $7F_H$

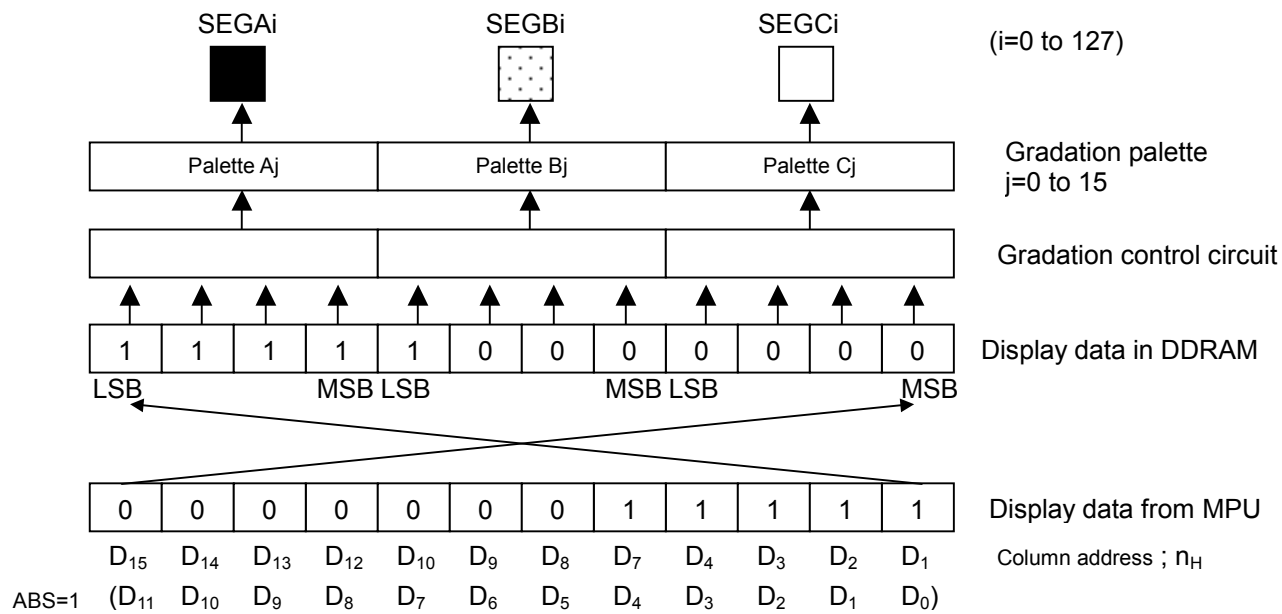
In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the "SWAP" and "REF" bit of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
 : $7F_H - n_H$ (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address :n_H (REF="0")
 :7F_H-n_H (REF="1")

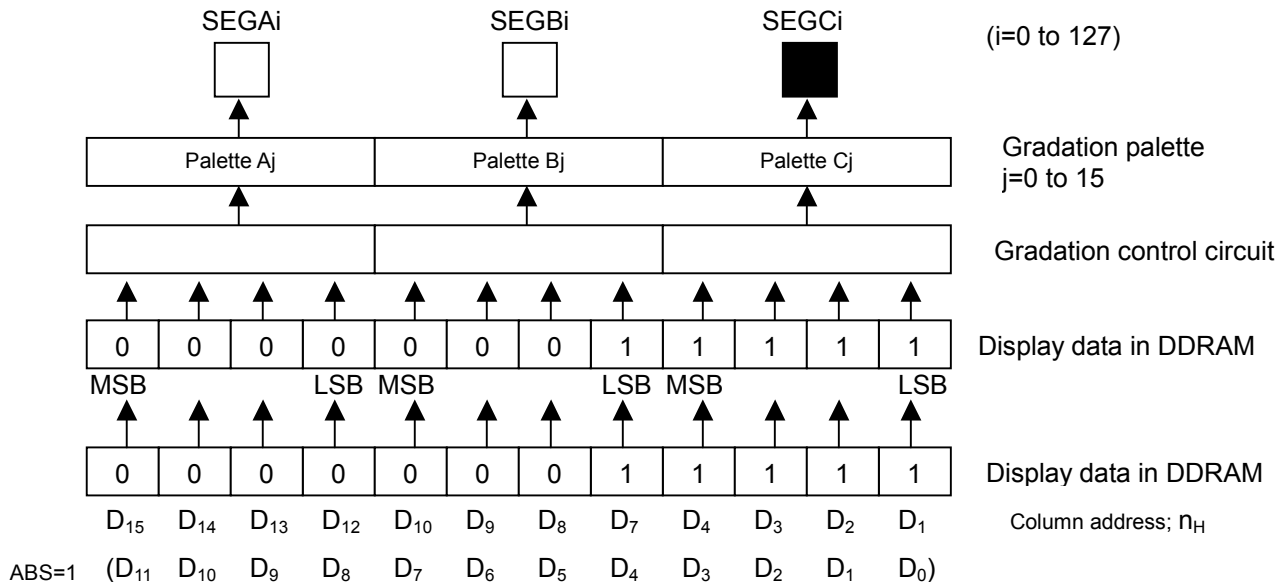
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(12-2) B&W mode (MON="1")

In the B&W mode, 3 bits of the MSB data are used in both of the 16-bit and 8-bit data bus modes.

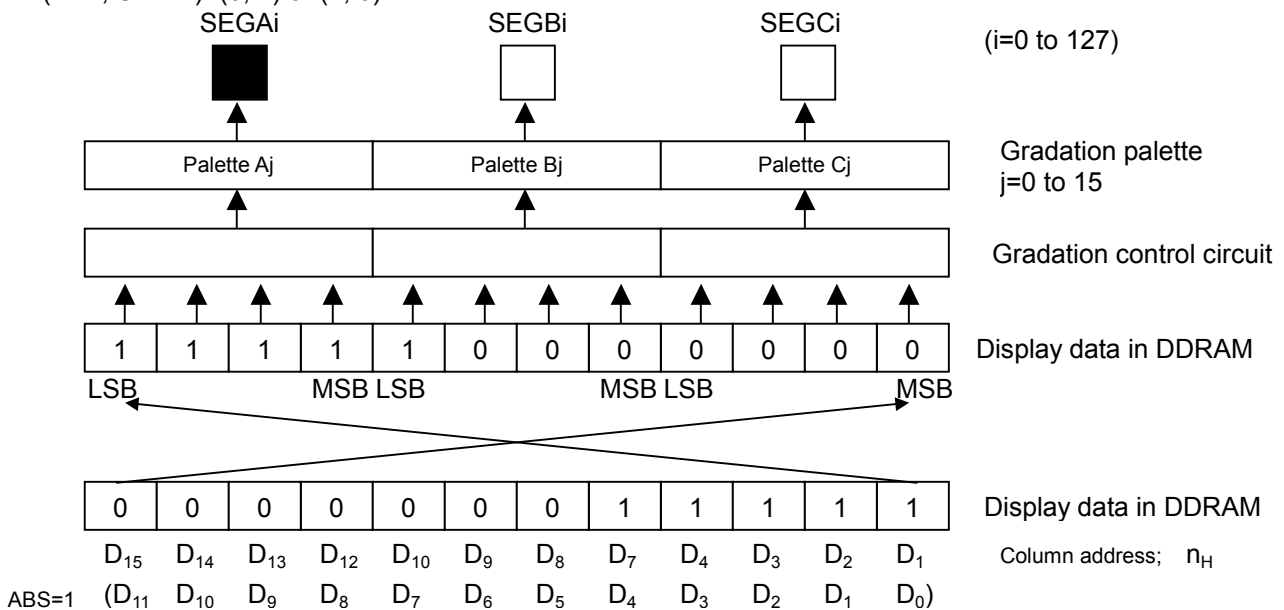
In the 16-bit data bus mode (Similarly 8-bit data bus access)

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
 : $7F_H-n_H$ (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : n_H (REF="0")
 : $7F_H-n_H$ (REF="1")

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resistor mode. The each of timing pulses is outputted through the each output terminals by "SON" = 1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits is completely independent of the access timing to the MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes "1".

(16) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The "All pixels ON/OFF", "Display ON/OFF" and "Reverse display ON/OFF" instructions change the display data in this circuit but do not change the display data of the DDRAM.

(17) Common and segment drivers

The LSI includes 384-segment drivers and 40-common drivers. The common drivers generate the LCD driving waveforms composed of the V_{LCD} , V_1 , V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate waveforms composed of the V_{LCD} , V_2 , V_3 and V_{SS} in accordance with the FR signal and display data.

LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/41 duty)

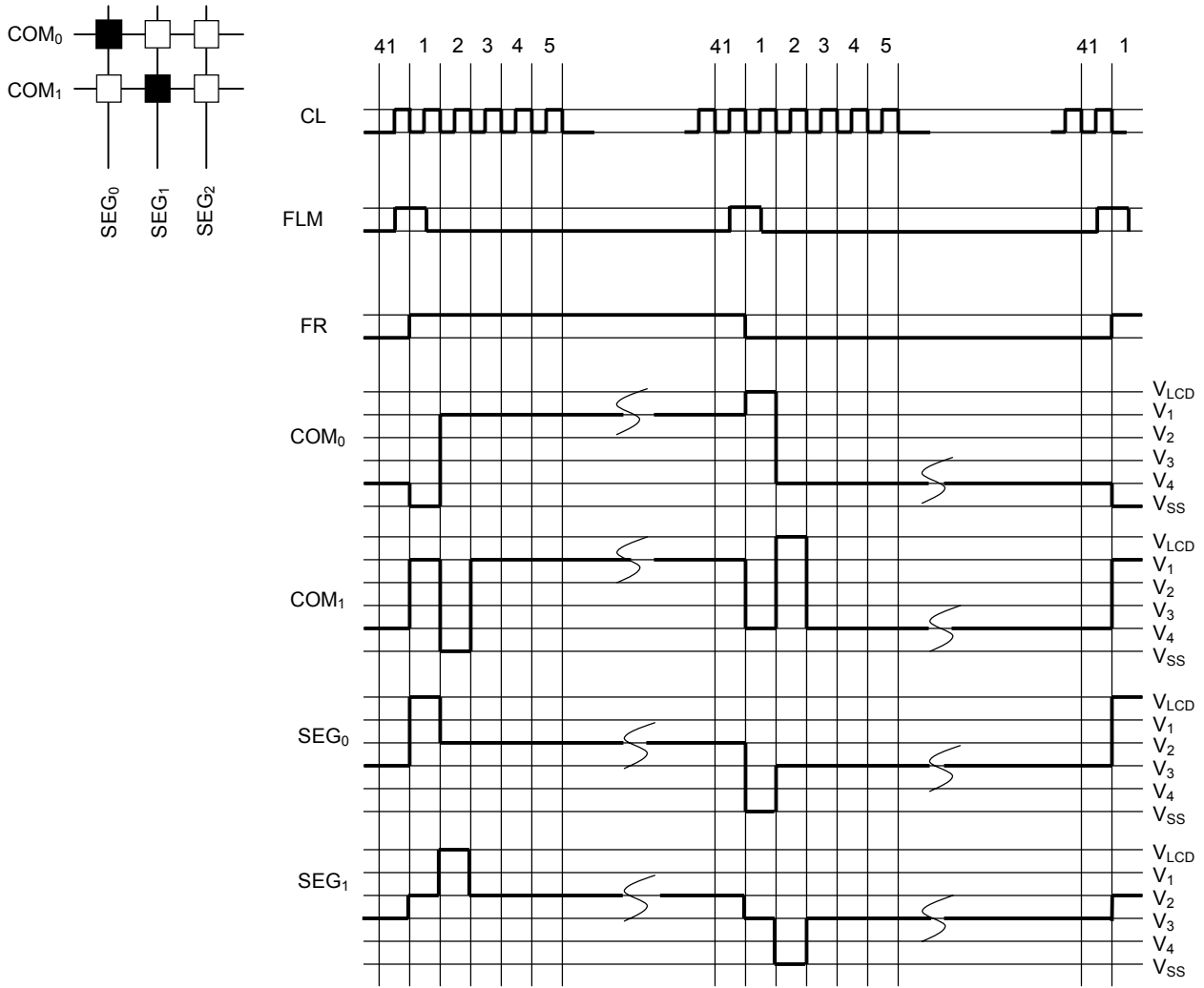


Fig 8

(18) Oscillator

The oscillator generates internal clocks for the display timing and the voltage booster. Since the LSI has internal capacitor (C) and resistor (R) for the oscillation, external capacitor and resistor are not usually required. However, in case that an external resistor is used, the resistor is connected between the OSC1 and OSC2 terminals. The external resistor becomes enabled by setting "1" to the "CKS" register of "Data bus length" instruction. When the internal oscillator is not used, the external clocks with 50% duty cycle ratio must be input to the OSC1 terminal.

In addition, the feed back resistor for the oscillation is varied by programming the "Rf" register of the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON (B&W /Gradation) and the PWM (Variable gradation /Fixed gradation) are described, as follows.

(18-1) Internal oscillation mode (CKS=0)

Symbol	MON	PWM	Display mode
f ₁	0	0	Variable gradation mode
f ₂	0	1	Fixed gradation mode
f ₃	1	*	B&W mode

*: Don't care

(18-2) External resistor oscillation mode(CKS=1)

The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(18-3) External clock input mode (CKS=1)

The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(19) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resistor (EVR), the voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, same parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

Table 14

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3
0	1	Disable	Enable	V _{OUT}	2, 3
1	1	Enable	Enable	-	-

Note1) The internal power circuits are not used. The external V_{OUT} is required and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4-, V_{OUT}, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4- and V_{EE} terminals must be open. The reference voltage is required to V_{REF} terminal.

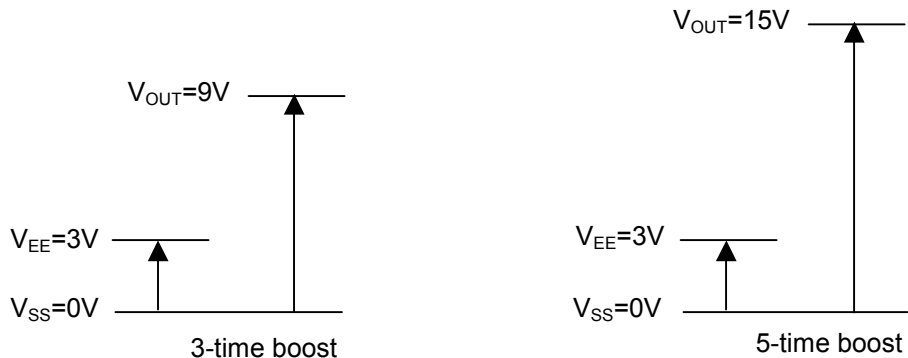
Note3) The relation among the voltages should be maintained as follows.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$$

(20) Voltage booster

The voltage booster generates maximum 5x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, and 5x by the "Boost level select" instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

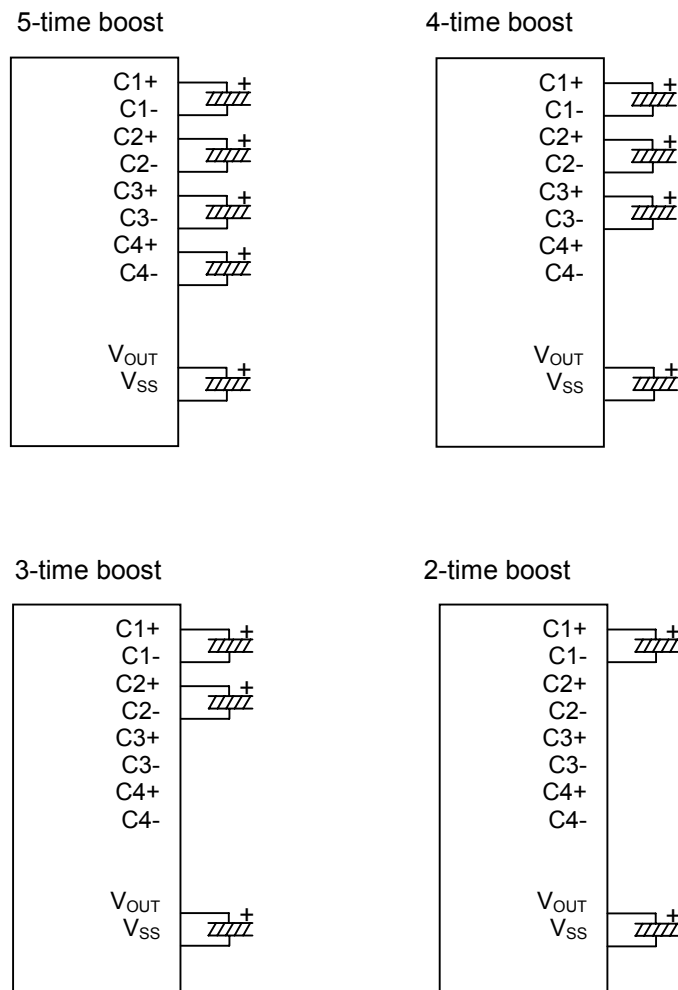


Fig 9

(21) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$$V_{BA} = V_{EE} \times 0.9$$

(22) Voltage regulator

The voltage regulator, composed of the gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuits, which is programmed by the "VU" register of the "Boost level" instruction.

$$V_{REG} = V_{REF} \times N \quad (N: \text{register value for the boost level})$$

(23) Electrical variable resistor (EVR)

The EVR, variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the "DV" register in the "EVR control" instruction, so that it is possible to optimize the contrast level for a LCD panels.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{register value for the EVR})$$

(24) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} voltage levels as V_{LCD} , V_1 , V_2 , V_3 and V_4 with internal E.V.R and the Bleeder resistors. The bias ratio of LCD driving voltage can be selected out of 1/4, 1/5, 1/6, 1/7 and 1/8.

In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the external power supply, the external LCD driving voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 are supplied and the internal power supply circuits must be set to "OFF" by $DCON = AMPON = "0"$. In this mode, voltage booster terminals such as $C1+$, $C1-$, $C2+$, $C2-$, $C3+$, $C3-$, $C4+$, $C4-$, V_{EE} , V_{REF} and V_{REG} must be opened.

In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the $C1+$, $C1-$, $C2+$, $C2-$, $C3+$, $C3-$, $C4+$ and $C4-$ terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

Connections of the capacitor for the voltage booster

Using all of the internal power supply circuits
(5-time boost)

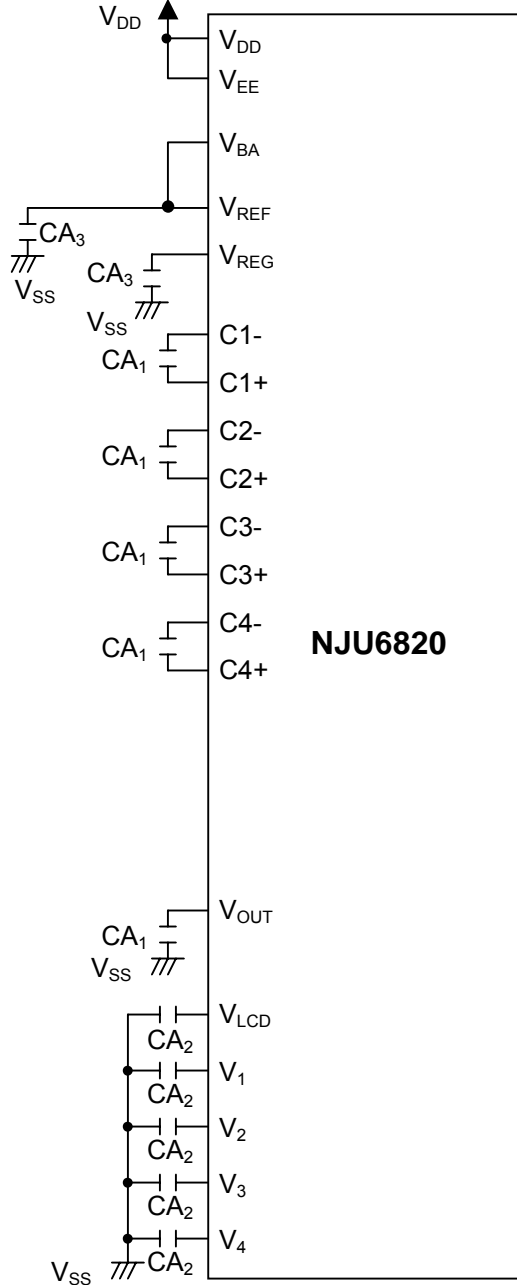


Fig 10

Using only external power supply circuits

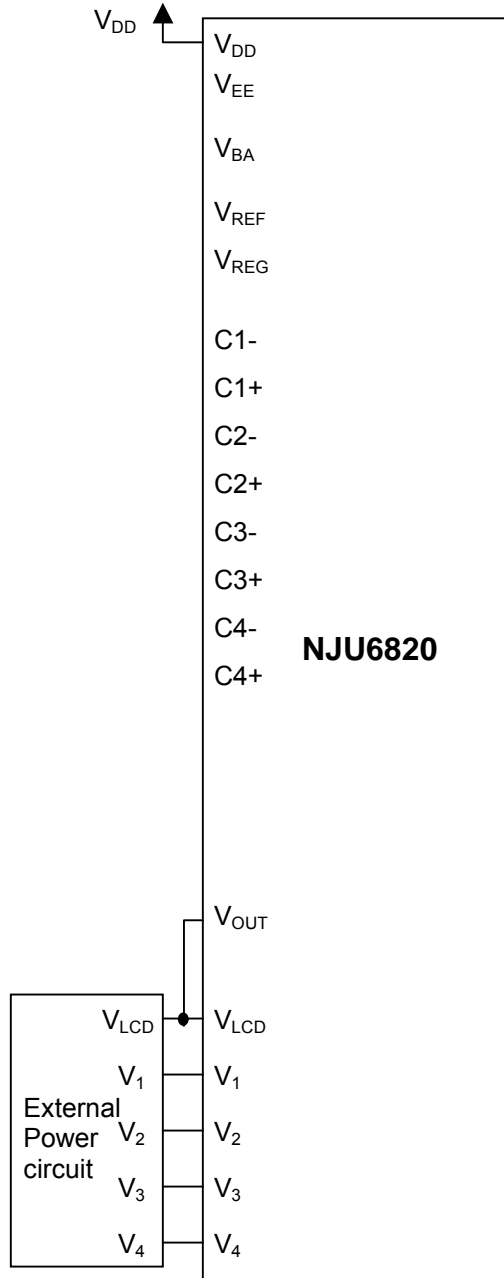


Fig11

Reference values

CA ₁	1.0 to 4.7uF
CA ₂	1.0 to 2.2uF
CA ₃	0.1uF

Note) B grade capacitors are required.

Using internal power supply circuits
Without the reference voltage generator(1)
(5-time boost)

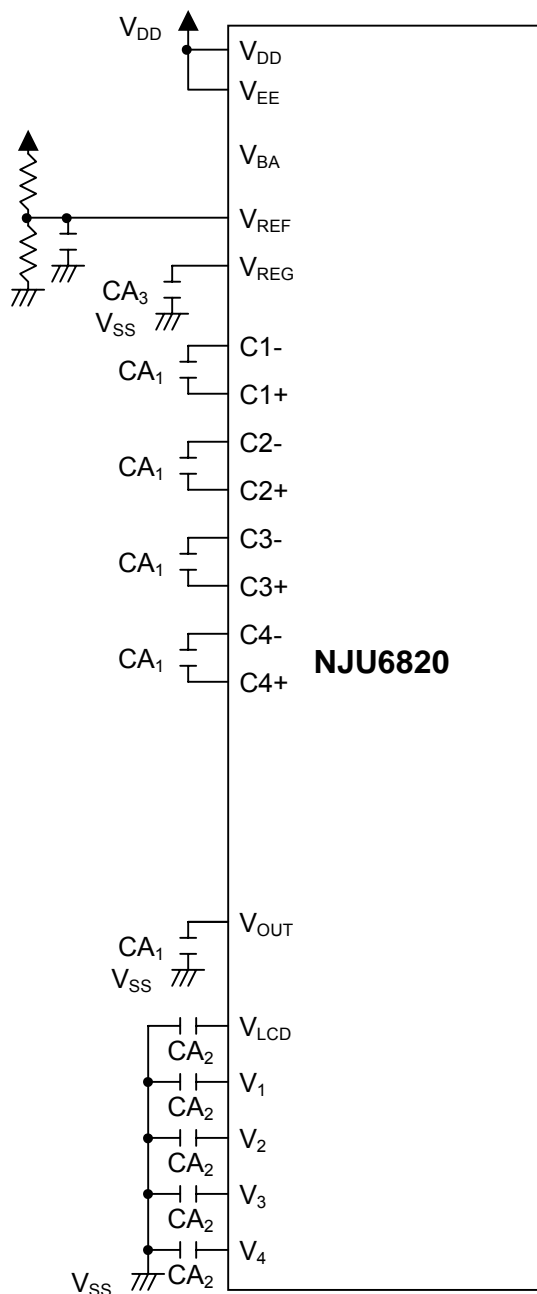


Fig 12

Using internal power supply circuit
Without the reference voltage generator(2)
(5-time boost)

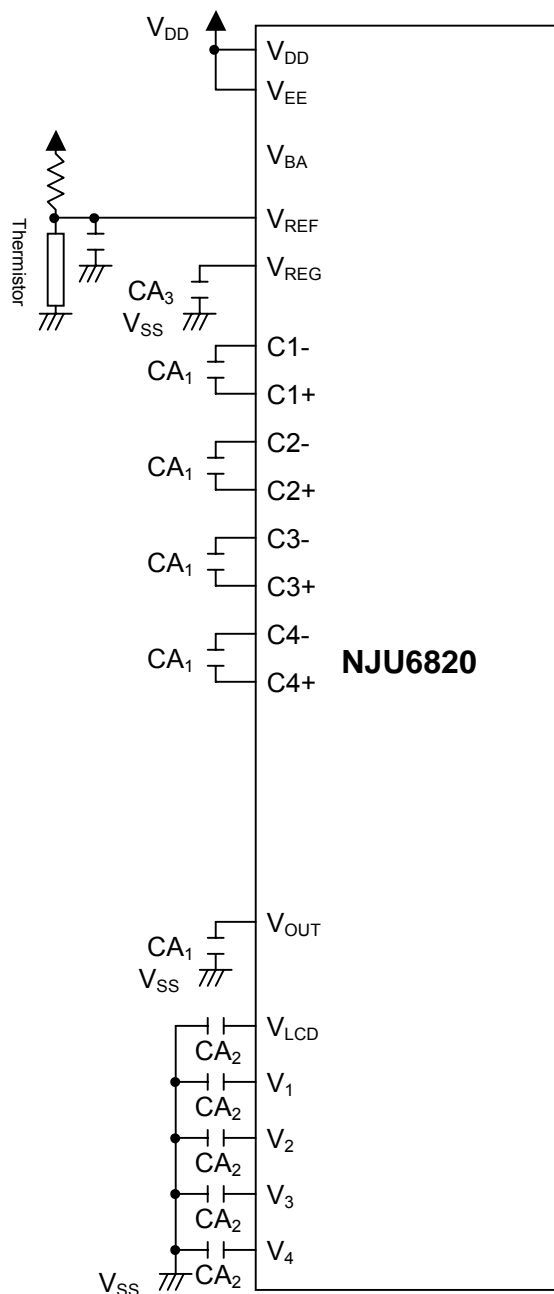


Fig 13

Reference value

CA ₁	1.0 to 4.7μF
CA ₂	1.0 to 2.2μF
CA ₃	0.1μF

Note) B grade capacitors are required.

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Using internal power supply circuits
Without the voltage booster

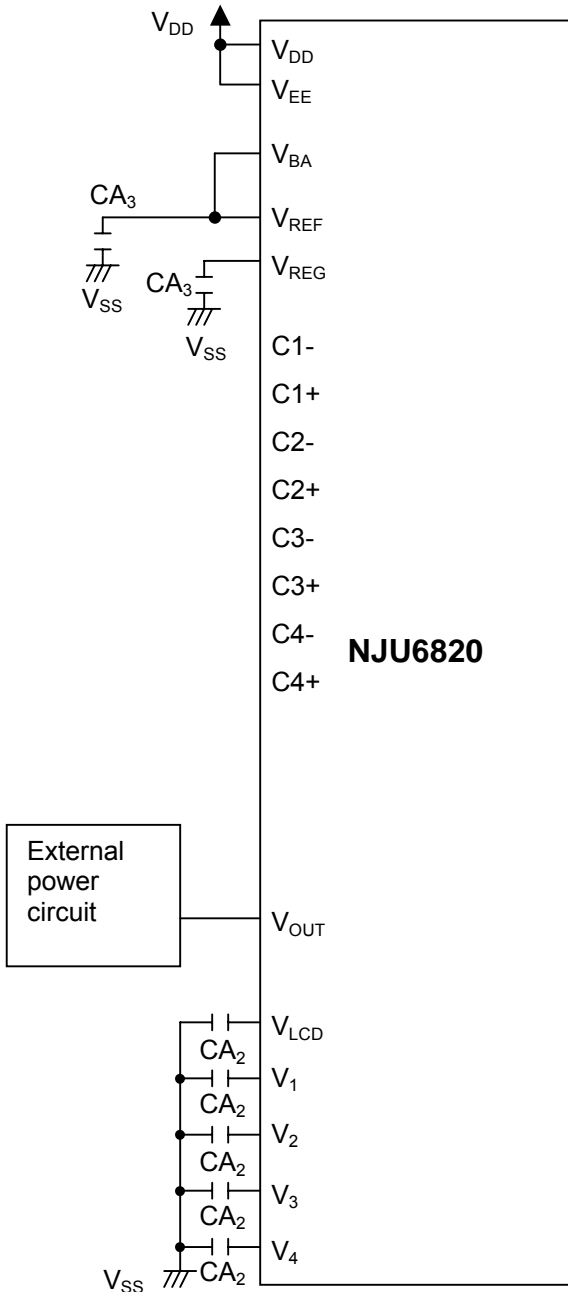


Fig 14

Reference value

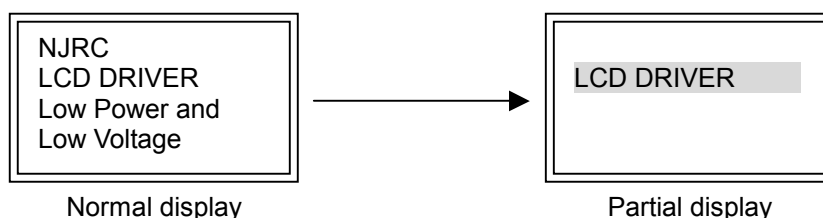
CA ₁	1.0 to 4.7μF
CA ₂	1.0 to 2.2μF
CA ₃	0.1μF

Note) B grade capacitors are required.

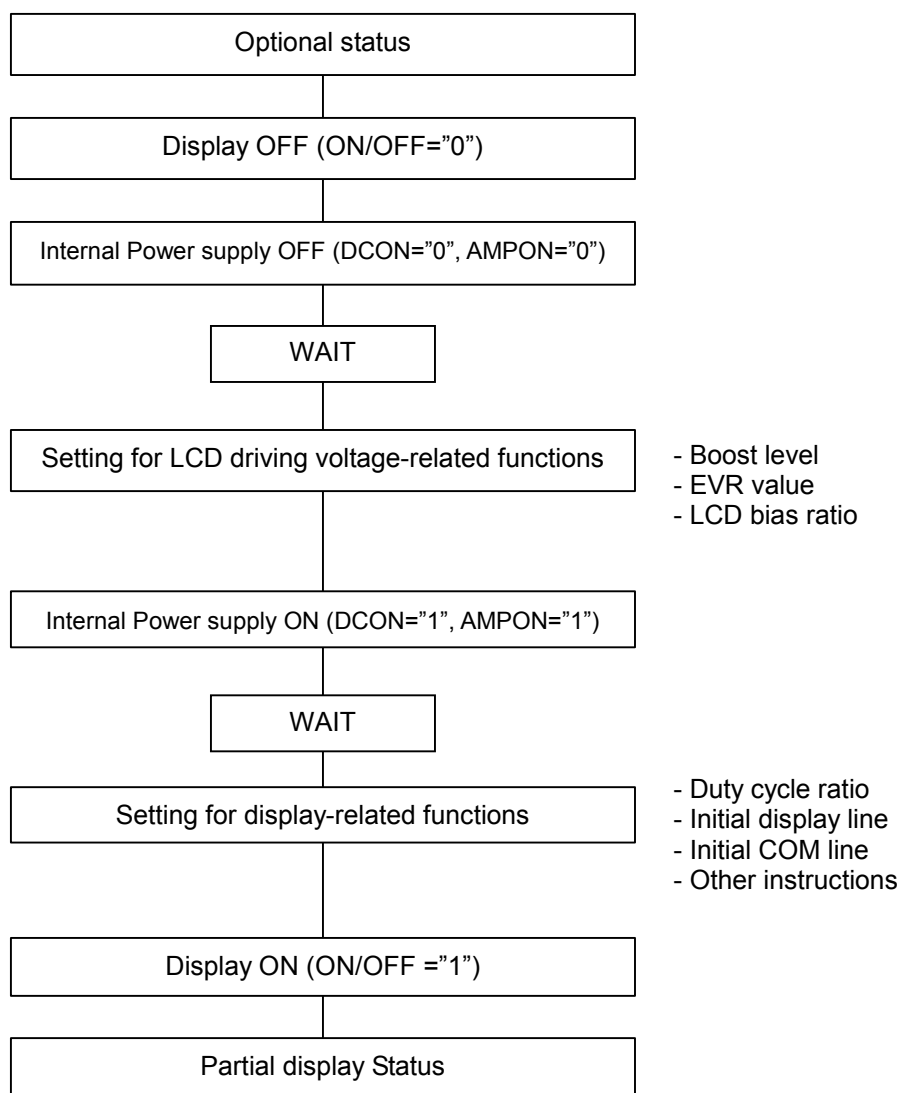
(25) Partial display function

The partial display function is used to partially specify some parts of display area on LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar, and is also used to optimize the LSI condition in accordance with the display size. It can be programmed to select the duty cycle ratio (1/5, 1/9, 1/13, 1/17, 1/21, 1/25, 1/29, 1/33, 1/37, 1/41 in case "DSE" is "0"), the LCD bias ratio, the boost level and the EVR value by the instructions.

Partial display image



Partial display sequence



(26) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and V_{LCD} terminals. This circuit is activated by setting "0" to the "DIS" register of the "Discharge" instruction or by setting "RESb" terminal to "0" level. The "Discharge ON/OFF" instruction is usually required just after the internal power supply is turned off by setting "0" into the "DCON" and "AMPON" registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(27) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to "0". The RESB terminal is usually required to connect to MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

● Default status

1. DDRAM display data	:Undefined
2. column address	:(00) _H
3. row address	:(00) _H
4. Initial display line	:(0) _H (1st line)
5. Display ON/OFF	:OFF
6. Reverse display ON/OFF	:OFF (normal)
7. Duty cycle ratio	:1/41 duty(DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM scan direction	:COM ₀ → COM ₃₉
10. Increment mode	:OFF
11. Reverse SEG direction	:OFF (normal)
12. SWAP mode	:OFF (normal)
13. EVR value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply	:OFF
15. Display mode	:Gradation display mode
16. LCD bias ratio	:1/8 bias
17. Gradation Palette 0	:(0, 0, 0, 0, 0)
18. Gradation Palette 1	:(0, 0, 0, 1, 1)
19. Gradation Palette 2	:(0, 0, 1, 0, 1)
20. Gradation Palette 3	:(0, 0, 1, 1, 1)
21. Gradation Palette 4	:(0, 1, 0, 0, 1)
22. Gradation Palette 5	:(0, 1, 0, 1, 1)
23. Gradation Palette 6	:(0, 1, 1, 0, 1)
24. Gradation Palette 7	:(0, 1, 1, 1, 1)
25. Gradation Palette 8	:(1, 0, 0, 0, 1)
26. Gradation Palette 9	:(1, 0, 0, 1, 1)
27. Gradation Palette 10	:(1, 0, 1, 0, 1)
28. Gradation Palette 11	:(1, 0, 1, 1, 1)
29. Gradation Palette 12	:(1, 1, 0, 0, 1)
30. Gradation Palette 13	:(1, 1, 0, 1, 1)
31. Gradation Palette 14	:(1, 1, 1, 0, 1)
32. Gradation Palette 15	:(1, 1, 1, 1, 1)
33. Gradation mode control	:Variable gradation mode
34. Data bus length	:8-bit data bus length
35. Discharge circuit	:(DIS/DIS2) : "0"

(28) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(28-1) Using an external power supply

- Power supply ON sequence

Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT} , the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input.

- Power supply OFF sequence

Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resistor between $50\ \Omega$ and $100\ \Omega$ is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(28-2) Using the internal power supply circuits

- Power supply ON sequence

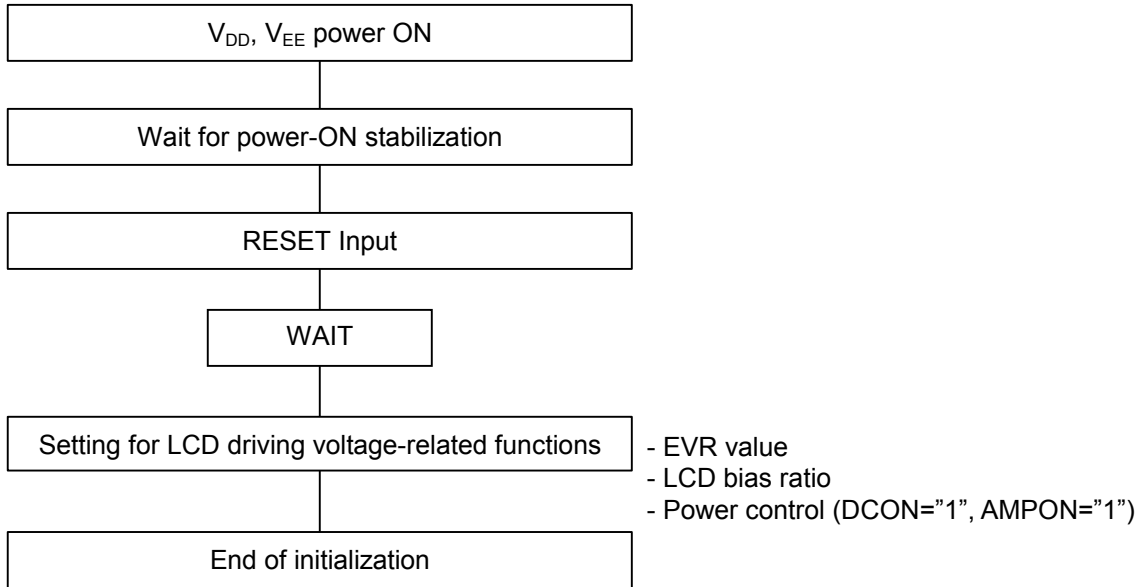
The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

- Power supply OFF sequence

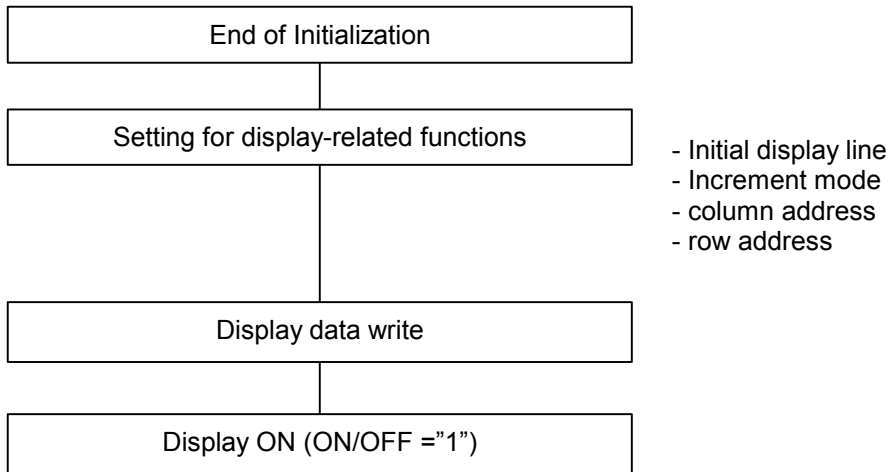
Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for V_{DD} , the V_{EE} is turned off first, and next the V_{DD} is turned off.

(29) Referential instruction sequences

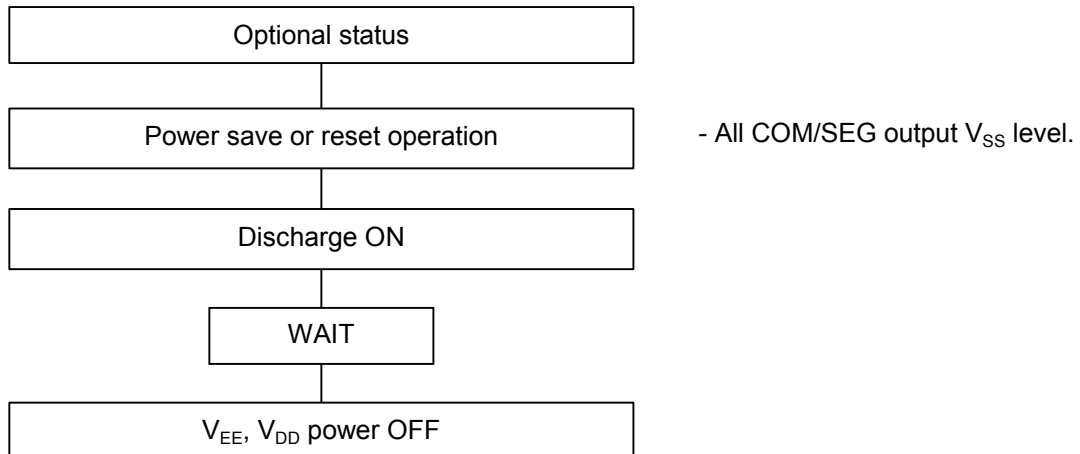
(29-1) Initialization in using the internal power supply circuits



(29-2) Display data writing



(29-3) Power OFF



(30) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0 _H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1 _H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2 _H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3 _H]	0	1	1	0	0	0	0	0	0	1	1	*	*	AY5	AY4	DDRAM row address
Initial display line (Lower) [4 _H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5 _H]	0	1	1	0	0	0	0	0	1	0	1	*	*	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6 _H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7 _H]	0	1	1	0	0	0	0	0	1	1	1	*	*	N5	N4	The number of N-line inversion
Display control (1) [8 _H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9 _H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF REF: Segment direction
Increment control [A _H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Window addressing mode ON/OFF AIM: Read-modify-write ON/OFF AYI: Row auto-increment mode ON/OFF AXI: column auto-increment mode ON/OFF
Power control [B _H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C _H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [D _H]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [E _H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A0/A8 (Lower) [0 _H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1 _H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2 _H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3 _H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4 _H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5 _H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6 _H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7 _H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8 _H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9 _H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A _H]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B _H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C _H]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D _H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code							Functions	
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
Gradation palette A7/A15 (Lower) [0 _H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1 _H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2 _H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3 _H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4 _H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5 _H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6 _H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7 _H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8 _H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9 _H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A _H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B _H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C _H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D _H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette B6/B14 (Lower) [0 _H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1 _H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2 _H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3 _H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4 _H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5 _H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6 _H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7 _H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8 _H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9 _H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A _H]	0	1	1	0	0	1	1	1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B _H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C _H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D _H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code							Functions	
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
Gradation palette C5/C13 (Lower) [0 _H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1 _H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2 _H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3 _H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4 _H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5 _H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6 _H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Sets scan-starting common driver
Display control Signal/ Duty Select [7 _H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display clock ON/OFF DSE : Duty-1 ON/OFF
Gradation mode control [8 _H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed gradation mode C256 : 256-Color Mode ON/OFF
Data bus length [9 _H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High speed access ON/OFF ABS : ABS mode ON/OFF CKS : Internal/external oscillation WLS : Display data Length
EVR control (Lower) [A _H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B _H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D _H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [E _H]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge the electric charge in capacitors on V ₁ to V ₄ and V _{LCD}
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag
Instruction register address [C _H]	0	1	1	0	1	0	0	1	1	0	0	Reading address				Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code							Functions	
	CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
Window end column address (Lower) [0 _H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1 _H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2 _H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3 _H]	0	1	1	0	1	0	1	0	0	1	1	*	*	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4 _H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5 _H]	0	1	1	0	1	0	1	0	1	0	1	*	*	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6 _H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7 _H]	0	1	1	0	1	0	1	0	1	1	1	*	*	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8 _H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting control / Icon SEG address [9 _H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : gradation setting
PWM control [A _H]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Sets PWM mode
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(31) Instruction descriptions

This chapter provides detail descriptions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(31-1) Display data write

The "Display data write" instruction is used to write 8-bit display data into the DDRAM.

CSB	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display data							

(31-2) Display data read

The "Display data read" instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the "column address" and "row address" instructions. The dummy read is required just after the "column address" and "row address" instructions.

CSB	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display data							

(31-3) Column address

The "column address" instruction is used to specify the column address for the display data's reading and writing operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 4-bit.

CSB	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX ₃	AX ₂	AX ₁	AX ₀

CSB	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX ₇	AX ₆	AX ₅	AX ₄

(31-4) Row address

The "row address" instruction is used to specify the row address for the display data read and write operations. It requires dual bytes for lower 4-bit and upper 2-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for upper 2-bit. The row address is specified in between 00_H and 27_H. The setting for nonexistent row address between 28_H and 3F_H is prohibited.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY ₃	AY ₂	AY ₁	AY ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	AY ₅	AY ₄

(31-5) Initial display line

The "Initial display line" instruction is used to specify the line address corresponding to the initial COM line. The initial COM line specified by the "Initial COM line" instruction and indicates the common driver that starts scanning data.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA ₃	LA ₂	LA ₁	LA ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	LA ₅	LA ₄

LA ₅	LA ₄	LA ₃	LA ₂	LA ₁	LA ₀	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
⋮						⋮
1	0	0	1	1	1	39

(31-6) N-line inversion

The "N-line inversion" instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 39, and the FR signal toggles once every N lines by setting "1" into the "NLIN" register of the "Display control (2)" instruction. When the N-line inversion is disabled by setting "0" into the "NLIN" register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N3	N2	N1	N0

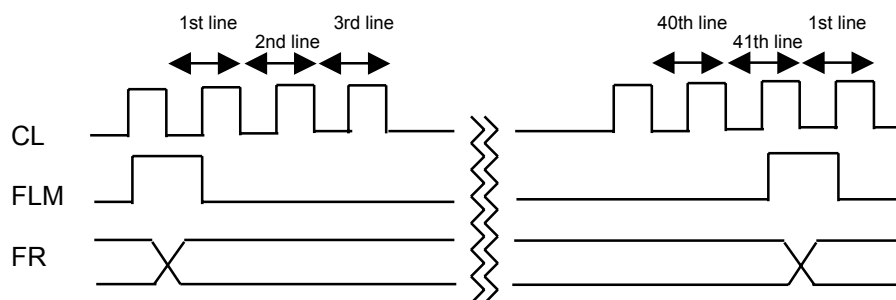
CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	N5	N4

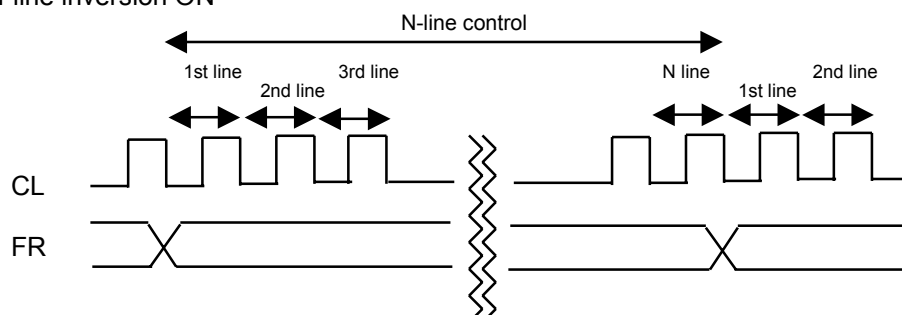
LA ₅	LA ₄	LA ₃	LA ₂	LA ₁	LA ₀	N value
0	0	0	0	0	0	Inhibited*
0	0	0	0	0	1	2
⋮						⋮
1	0	0	1	1	0	39

● N-line Inversion Timing (1/41 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(31-7) Display control (1)

The "Display control (1)" instruction is used to control display conditions by setting the "Display ON/OFF", "All pixels ON/OFF", Display mode" and "Common direction" registers.

CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

● ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output V_{ss} level.)
 ON/OFF=1 : Display ON

● All ON register

The "All pixels ON/OFF" register is used to turn on all pixels without changing display data of the DDRAM. The setting for the "All pixels ON/OFF" register has a priority over the "Reverse display ON/OFF" register.

ALLON=0 : Normal
 ALLON=1 : All pixels turn on.

● MON register

MON=0 : Gradation mode
 MON=1 : B&W mode

● SHIFT register

SHIFT=0 : COM₀ → COM₃₉
 SHIFT=1 : COM₃₉ → COM₀

(31-8) Display control (2)

The "Display control (2)" instruction is used to control display conditions by setting "Segment direction", "SWAP mode ON/OFF", "N-line inversion ON/OFF" and "Reverse display ON/OFF" registers.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	REF

- REF register

The "REF" register is used to reverse the assignment between segment drivers and column address, and it is possible to reduce restrictions for placement of the LSI on the LCD modules. For more information, see (10) "The relation among the DDRAM column address, display data and segment drivers".

- SWAP register

The "SWAP" register is used to reverse the arrangement of the display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
 SWAP=1 : SWAP mode ON

	SWAP="0"	SWAP="1"
Write data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀
	↓ ↓	↙ ↘
RAM data	D ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	d ₀ d ₁ d ₂ d ₃ d ₄ d ₅ d ₆ d ₇
	↓ ↓	↓ ↓
Read data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀

- NLIN register

The "NLIN" is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the frame.)
 NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

- REV register

The "REV" register is used to enable or disable the reverse display mode that reverses the polarity of the display data without changing the display data of the DDRAM.

REV=0 : Reverse display mode OFF
 REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(31-9) Increment control

The "Increment control" instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increments (+1) whenever the DDRAM is accessed by the "Display data write" or "Display data read" instruction. Therefore, once "Display data write" or "Display data read" instruction is established, it is possible to continuously access to the DDRAM without the "column address" and "row address" instructions. The settings for the "AIM", "AXI" and "AYI" registers are listed in the following tables.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	WIN	AIM	AYI	AXI

● AIM, AYI and AXI registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	1
1	Auto-increment for the display write operation (Read modify write)	2

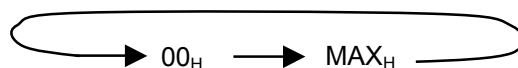
Note 1) It is effective for usual operations accessing successive addresses.

Note 2) It is effective for the read-modify-write operation.

AYI	AXI	Increment mode	Note
0	0	No auto-increment	1
0	1	Auto-increment for the column address	2
1	0	Auto-increment for the row address	3
1	1	Auto-increment for the column address and row address	4

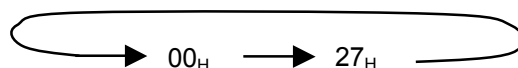
Note 1) Auto-increment is disabled regardless of the "AIM" register.

Note 2) Auto-increment of the column address is enabled in accordance with the "AIM" register.

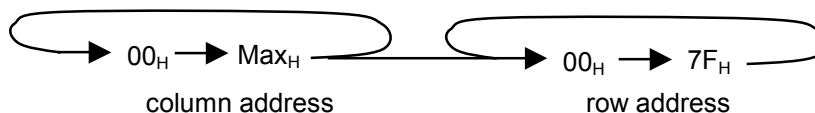


MAX_H in the 8-bit data bus mode : FF_H
 MAX_H in the 16-bit data bus mode : 7F_H

Note 3) Auto-increment of the row address is enabled in accordance with the "AIM" register.



Note 4) Auto-increment of the column address and the row address are enabled. The row address increments whenever the column address reaches to the MAX_H.



MAX_H in the 8-bit data bus mode : FF_H
 MAX_H in the 16-bit data bus mode : 7F_H

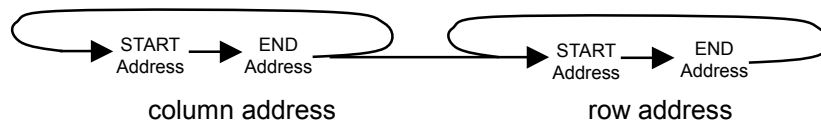
- WIN register

The "WIN" register is used to access to the DDRAM for the window display area, where the start point is determined by the "column address" and "row address" instructions, and the end point by the "Window end column address" and "Window end row address" instructions. The setting sequence for the window display area is listed as follows. For more detail, see (7) "Window addressing mode".

WIN=0 :Window addressing mode OFF

WIN=1 :Window addressing mode ON

1. Set WIN=1, AXI=1, and AYI=1 by "Increment control" instruction.
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode



(31-10) Power control

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

- ACL register

The "ACL" register is used to initialize the internal power supply circuits.

ACL=0 : Initialization OFF (Normal)

ACL=1 : Initialization ON

When the data of the "ACL register" is read out by the "Instruction register read" instruction, the read-out data is "1" during the initialization and "0" after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC₁. For this reason, the wait time for 2 clocks of the OSC₁ necessary until next instruction.

- DCON register

The "DCON" register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF

DCON=1 : Voltage booster ON

- HALT register

The "HALT" register is used to enable or disable the power save mode. It is possible reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)

HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output V_{SS} level.
- The clock input into the OSC₁ is inhibited.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V₁ to V₄ and V_{LCD} are in the high impedance.

As a power save ON sequence, the "Display OFF" must be executed first, next the "Power save ON" instruction, and then all common and segment drivers output the V_{SS} level. And as power save OFF sequence, the "Power save OFF" instruction is executed first, next the "Display ON" instruction. If the "Power save OFF" instruction is executed in the display ON status, unexpected pixels may instantly turn on.

- AMPON register

The "AMPON" register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, voltage regulator the EVR OFF

AMPON=1 : The voltage followers, voltage regulator the EVR ON

(31-11)Duty cycle ratio

The "Duty cycle ratio" instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI's conditions with extremely low power consumption.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS ₃	DS ₂	DS ₁	DS ₀

DS ₃	DS ₂	DS ₁	DS ₀	Duty cycle ratio		Row way displays
				DSE=0	DSE=1	
0	0	0	0	1/41	1/40	40 commons
0	0	0	1	1/37	1/36	37 commons
0	0	1	0	1/33	1/32	33 commons
0	0	1	1	1/29	1/28	29 commons
0	1	0	0	1/25	1/24	25 commons
0	1	0	1	1/21	1/20	21 commons
0	1	1	0	1/17	1/16	17 commons
0	1	1	1	1/13	1/12	13 commons
1	0	0	0	1/9	1/8	9 commons
1	0	0	1	1/5	1/4	5 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

The duty cycle ratio is controlled by the "DS₃ to DS₀" registers of the "Duty cycle ratio" instruction and the "DSE" register of the "Display Clock / Duty-1" instruction.

DSE="0" : The number of commons + 1 (Duty cycle ratio in the default setting)
 DSE="1" : The number of commons (Duty-1)

When the "DSE" is "0", all common drivers output non-selective levels in period of last common. And the segment drivers output the same data for the last line as the data for previous line: For instance they output the same data for the 40th and 41th lines when the duty cycle ratio is set to 1/41. For the setting of the "DSE" register, see (31-17) "Display clock / Duty-1".

(31-12)Boost level

The "Boost level" is used to select the multiple of the voltage booster for the partial display function.

CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	VU ₂	VU ₁	VU ₀

VU ₂	VU ₁	VU ₀	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(31-13) LCD bias ratio

The "LCD bias ratio" is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B ₂	B ₁	B ₀

B ₂	B ₁	B ₀	LCD bias ratio
0	0	0	1/8
0	0	1	1/7
0	1	0	1/6
0	1	1	1/5
1	0	0	1/4
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(31-14) RE flag

The "RE flag" registers are used to determine the contents for the RE registers (RE₂, RE₁ and RE₀) and it is possible to access to the instruction registers.

The data in the "TST₀" register must be "0", and it is used maker tests only.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀

(31-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₀₃ / PA ₈₃	PA ₀₂ / PA ₈₂	PA ₀₁ / PA ₈₁	PA ₀₀ / PA ₈₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₀₄ / PA ₈₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA ₁₃ / PA ₉₃	PA ₁₂ / PA ₉₂	PA ₁₁ / PA ₉₁	PA ₁₀ / PA ₉₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA ₁₄ / PA ₉₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA ₂₃ / PA ₁₀₃	PA ₂₂ / PA ₁₀₂	PA ₂₁ / PA ₁₀₁	PA ₂₀ / PA ₁₀₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA ₂₄ / PA ₁₀₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA ₃₃ / PA ₁₁₃	PA ₃₂ / PA ₁₁₂	PA ₃₁ / PA ₁₁₁	PA ₃₀ / PA ₁₁₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA ₃₄ / PA ₁₁₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA ₄₃ / PA ₁₂₃	PA ₄₂ / PA ₁₂₂	PA ₄₁ / PA ₁₂₁	PA ₄₀ / PA ₁₂₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA ₄₄ / PA ₁₂₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA ₅₃ / PA ₁₃₃	PA ₅₂ / PA ₁₃₂	PA ₅₁ / PA ₁₃₁	PA ₅₀ / PA ₁₃₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA ₅₄ / PA ₁₃₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA ₆₃ / PA ₁₄₃	PA ₆₂ / PA ₁₄₂	PA ₆₁ / PA ₁₄₁	PA ₆₀ / PA ₁₄₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA ₆₄ / PA ₁₄₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₇₃ / PA ₁₅₃	PA ₇₂ / PA ₁₅₂	PA ₇₁ / PA ₁₅₁	PA ₇₀ / PA ₁₅₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₇₄ / PA ₁₅₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₀₃ / PB ₈₃	PB ₀₂ / PB ₈₂	PB ₀₁ / PB ₈₁	PB ₀₀ / PB ₈₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₀₄ / PB ₈₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB ₁₃ / PB ₉₃	PB ₁₂ / PB ₉₂	PB ₁₁ / PB ₉₁	PB ₁₀ / PB ₉₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB ₁₄ / PB ₉₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB ₂₃ / PB ₁₀₃	PB ₂₂ / PB ₁₀₂	PB ₂₁ / PB ₁₀₁	PB ₂₀ / PB ₁₀₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB ₂₄ / PB ₁₀₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB ₃₃ / PB ₁₁₃	PB ₃₂ / PB ₁₁₂	PB ₃₁ / PB ₁₁₁	PB ₃₀ / PB ₁₁₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB ₃₄ / PB ₁₁₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB ₄₃ / PB ₁₂₃	PB ₄₂ / PB ₁₂₂	PB ₄₁ / PB ₁₂₁	PB ₄₀ / PB ₁₂₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB ₄₄ / PB ₁₂₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB ₅₃ / PB ₁₃₃	PB ₅₂ / PB ₁₃₂	PB ₅₁ / PB ₁₃₁	PB ₅₀ / PB ₁₃₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB ₅₄ / PB ₁₃₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB ₆₃ / PB ₁₄₃	PB ₆₂ / PB ₁₄₂	PB ₆₁ / PB ₁₄₁	PB ₆₀ / PB ₁₄₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB ₆₄ / PB ₁₄₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₇₃ / PB ₁₅₃	PB ₇₂ / PB ₁₅₂	PB ₇₁ / PB ₁₅₁	PB ₇₀ / PB ₁₅₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₇₄ / PB ₁₅₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₀₃ / PC ₈₃	PC ₀₂ / PC ₈₂	PC ₀₁ / PC ₈₁	PC ₀₀ / PC ₈₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₀₄ / PC ₈₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC ₁₃ / PC ₉₃	PC ₁₂ / PC ₉₂	PC ₁₁ / PC ₉₁	PC ₁₀ / PC ₉₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC ₁₄ / PC ₉₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC ₂₃ / PC ₁₀₃	PC ₂₂ / PC ₁₀₂	PC ₂₁ / PC ₁₀₁	PC ₂₀ / PC ₁₀₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC ₂₄ / PC ₁₀₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC ₃₃ / PC ₁₁₃	PC ₃₂ / PC ₁₁₂	PC ₃₁ / PC ₁₁₁	PC ₃₀ / PC ₁₁₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC ₃₄ / PC ₁₁₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC ₄₃ / PC ₁₂₃	PC ₄₂ / PC ₁₂₂	PC ₄₁ / PC ₁₂₁	PC ₄₀ / PC ₁₂₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC ₄₄ / PC ₁₂₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC ₅₃ / PC ₁₃₃	PC ₅₂ / PC ₁₃₂	PC ₅₁ / PC ₁₃₁	PC ₅₀ / PC ₁₃₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC ₅₄ / PC ₁₃₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC ₆₃ / PC ₁₄₃	PC ₆₂ / PC ₁₄₂	PC ₆₁ / PC ₁₄₁	PC ₆₀ / PC ₁₄₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC ₆₄ / PC ₁₄₄

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₇₃ / PC ₁₅₃	PC ₇₂ / PC ₁₅₂	PC ₇₁ / PC ₁₅₁	PC ₇₀ / PC ₁₅₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₇₄ / PC ₁₅₄

Gradation Palette Table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj, (j=0 to 15))

Palette Value	Gradation Level	Note	Palette Value	Gradation Level	Note
0 0 0 0 0	0/31	Gradation Palette 0 Initial Value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Gradation Palette 8 Initial Value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Gradation Palette 1 Initial Value	1 0 0 1 1	19/31	Gradation Palette 9 Initial Value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Gradation Palette2 Initial Value	1 0 1 0 1	21/31	Gradation Palette 10 Initial Value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Gradation Palette 3 Initial Value	1 0 1 1 1	23/31	Gradation Palette 11 Initial Value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Gradation Palette 4 Initial Value	1 1 0 0 1	25/31	Gradation Palette 12 Initial Value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Gradation Palette 5 Initial Value	1 1 0 1 1	27/31	Gradation Palette 13 Initial Value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Gradation Palette 6 Initial Value	1 1 1 0 1	29/31	Gradation Palette 14 Initial Value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Gradation Palette 7 Initial Value	1 1 1 1 1	31/31	Gradation Palette 15 Initial Value

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(31-16)Initial COM line

The "Initial COM line" instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the "Initial display line" instruction.

CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC ₃	SC ₂	SC ₁	SC ₀

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM ₀	COM ₃₉
0	0	0	1	COM ₄	COM ₃₁
0	0	1	0	COM ₈	COM ₂₇
0	0	1	1	COM ₁₆	COM ₂₃
0	1	0	0	COM ₂₀	COM ₁₉
0	1	0	1	COM ₂₄	COM ₁₅
0	1	1	0	COM ₂₈	COM ₁₁
0	1	1	1	COM ₃₂	COM ₇
1	0	0	0	COM ₃₆	COM ₃
1	0	0	1	Inhibited	Inhibited
1	0	1	0	Inhibited	Inhibited
1	0	1	1	Inhibited	Inhibited
1	1	0	0	Inhibited	Inhibited
1	1	0	1	Inhibited	Inhibited
1	1	1	0	Inhibited	Inhibited
1	1	1	1	Inhibited	Inhibited

SHIFT=0: Positive scan direction

(for instance, COM₀ → COM₃₉)

SHIFT=1: Negative scan direction

(for instance, COM₃₉ → COM₀)

(31-17)Display clock / Duty-1

The "Display clock / Duty-1" instruction is used to enable or disable the display clocks (CL, FLM, FR, and CLK), and to control ON/OFF of the "Duty-1". For more detail about the "Duty-1", see (31-11) "Duty cycle ratio".

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK outputs level "0".

SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Duty -1 OFF

DSE=1: Duty -1 ON

(31-18) Gradation mode control

The "Gradation mode control" is used select display mode as follows.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	*	*

- PWM register
 - PWM=0: Variable gradation mode
(Variable 16-gradation levels out of 32-gradation level of the gradation palette)
 - PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)
- C256 register
 - C256=0 256-color mode OFF (4,096-color in the default setting)
 - C256=1 256-color mode ON

(31-19) Data bus length

The "Data bus length" instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit (D₁₅ to D₀) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D₇ to D₀) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D₁₅ to D₀) is valid.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	HSW	ABS	CKS	WLS

- HSW register
 - HSW =0: High Speed access mode OFF
 - HSW=1: High Speed access mode ON (only in the 8-bit data bus length)
- ABS register
 - ABS=0: ABS mode OFF (normal)
 - ABS=1: ABS mode ON
- WLS register
 - WLS=0: 8-bit data bus length
 - WLS =1: 16-bit data bus length
- CKS register
 - CKS =0: Internal oscillation
(The OSC₁ terminal must be fixed "1" or "0".)
 - CKS =1: External oscillation
(By the external clock into the OSC₁ or external resistor between the OSC₁ and OSC₂. OSC₂ should be open when clock is inputted from OSC₁.)

(31-20)EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for a LCD panel.

This instruction must be programmed by upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the VLCD from being generated.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

$$V_{LCD} [V] = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$$

$$V_{BA} = V_{EE} \times 0.9$$

$$V_{REG} = V_{REF} \times N$$

- V_{BA} : Output voltage of the reference voltage generator
- V_{REF} : Input voltage of the voltage regulator
- V_{REG} : Output voltage of the voltage regulator
- N : Register value for the voltage booster
- M : Register value for the EVR

(31-21) Frequency control

The "Frequency control" instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	Rf ₂	Rf ₁	Rf ₀

- Rfx register (x=0, 1, 2)

The "Rfx" register is used to determine the feed back resistor value for the internal oscillator and it is possible to adjust the frame frequency for the LCD modules.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	0.7 x reference value
1	1	0	1.3 x reference value
1	1	1	Inhibited

(31-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V₁ to V₄ and the V_{LCD} terminals. The "Discharge ON/OFF" instruction is usually required just after the internal power supply is turned off by setting "0" into the "DCON" and "AMPON" registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	*	DIS2	DIS

DIS=0: Discharge OFF (Capacitors on the V_{LCD}, V₁, V₂, V₃ and V₄)

DIS=1: Discharge ON (Capacitors on the V_{LCD}, V₁, V₂, V₃ and V₄)

DIS2=0: Discharge OFF (Resistance between V_{OUT} and V_{EE})

DIS2=1: Discharge ON (Resistance between V_{OUT} and V_{EE})

Note) V_{OUT} and V_{EE} are internally connected with the resistor (100kΩ typical) in the power-ON.

(31-23) Instruction register address

The "Instruction register address" is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the "Instruction register read" instruction.

CSB	RS	RDB	WRB	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA ₃	RA ₂	RA ₁	RA ₀

(31-24) Instruction register read

The "Instruction register read" instruction is used to read out the contents of the instruction register in combination with the "Instruction register address" instruction.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data read			

(31-25) Window end column address

The "Window end column address" is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX ₃	EX ₂	EX ₁	EX ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX ₇	EX ₆	EX ₅	EX ₄

(31-26) Window end row address set

The "Window end row address" is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 2-bit data can be programmed.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY ₃	EY ₂	EY ₁	EY ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	EY ₅	EY ₄

(31-27) Initial reverse line

The "Initial reverse line" instruction is used to specify the initial reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 2-bit data. It is programmed in between 00_H and 27_H and the line address beyond 27_H is inhibited. The address relation: $LS_i < LE_i$ ($i=7$ to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS ₃	LS ₂	LS ₁	LS ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	LS ₅	LS ₄

(31-28) Last reverse line

The "Last reverse line" instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit must be programmed first, next upper 2-bit data. It is programmed in between 00_H and 27_H and the line address beyond 27_H is inhibited. The address relation: $LS_i < LE_i$ ($i=7$ to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE ₃	LE ₂	LE ₁	LE ₀

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	LE ₅	LE ₄

(31-29) Reverse line display ON/OFF

The "Reverse line display ON/OFF" is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

● LREV register

The "LREV" register is used to enable or disable the reverse line display.

LREV =0: Reverse line display OFF (Normal)

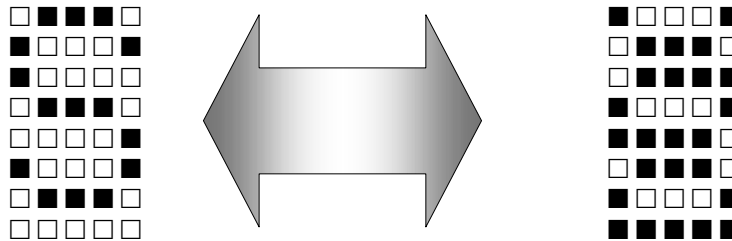
LREV =1: Reverse line display ON

● BT register

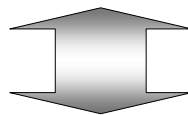
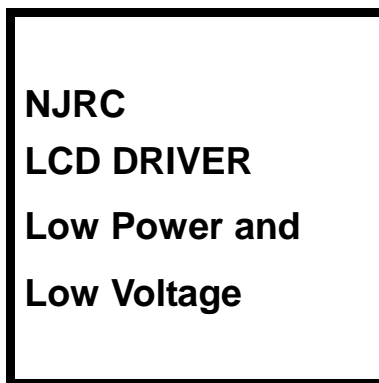
The "BT" register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

- BT =0: Normal reverse line display
- BT =1: Blink once every 32 frames

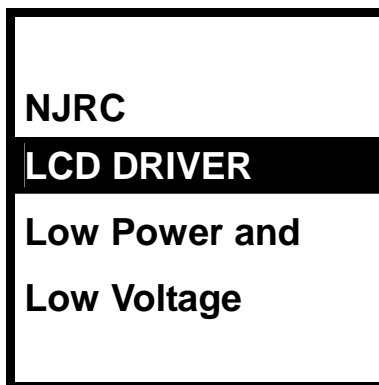
Display examples in the LREV="1" and BT="1"



Blink once every 32 frames



Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(31-30) Gradation Palette setting control

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PS

● PS register

- PS=0: Lower 8 Gradation setting
- PS=1: Upper 8 Gradation setting

(31-31) PWM control

The "PWM control" is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0-127) drivers.

CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

- PWMS register

PWMS=0: Type 1

PWMS=1: Type 2

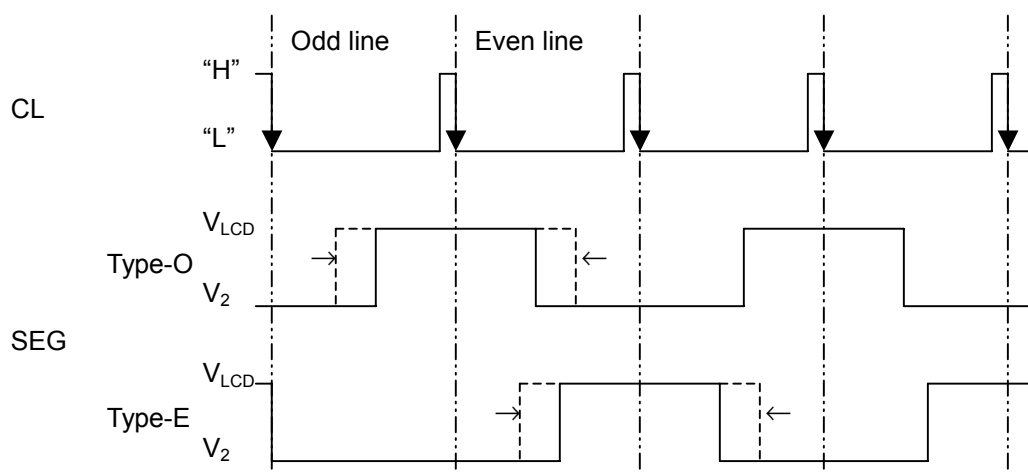
- PWMA, B and C registers

The "PWMA, PWMB and PWMC" registers are used to select the type 1-O or type 1-E.

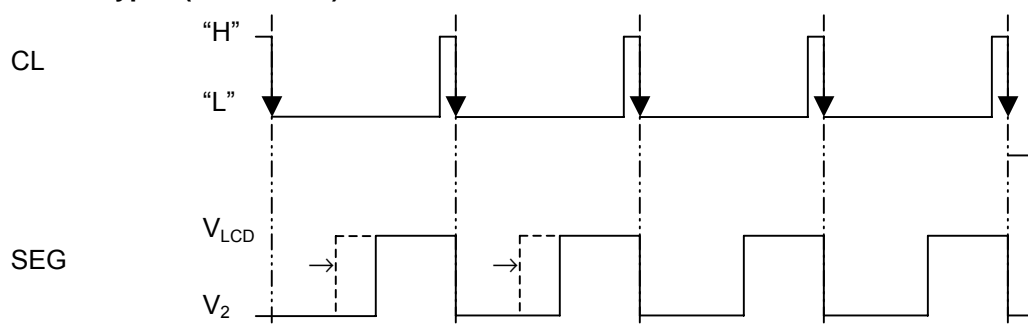
PWMZ=0 (Z=A, B and C): Type 1-O

PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS="0")



PWM type2 (PWMS="1")



(32) The relationship between Common drivers and row addresses

Row address assignment of common drivers is programmed by the " SHIFT " register of the " Display control (1) ", " Duty cycle ratio ", " Internal display line " and " Initial COM line " instructions.

When initial display line is "0"

If the " SHIFT " is " 0 ", the scan direction is normal. When the " LA₀ to LA₆ " registers of the " Initial display line " instruction is " 0 ", the " MY " corresponding to the initial COM line is " 0 " and is increasing during display.

When initial display line is not "0"

If the " SHIFT " is " 1 ", the scan direction is inversed. When the " LA₀ to LA₆ " registers of the " Initial display line " instruction is not " 0 ", the " MY " corresponding to the initial COM line is this setting value and is increasing during display.

The following are examples of setting the start-line 0 or 5 at 1/41, 1/17, or 1/17 duty.

(32-1) Initial display line "0", 1/41 duty cycle (Common forward scan)

SHIFT="0" (Common forward scan), DS _{3,2,1,0} ="0000", LA ₇ ...LA ₀ ="00000000" (Initial display line 0)													Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001					
COM ₀				0	36	32	28	24	20	16	12	8	4					
COM ₁					▼													
COM ₂					39													
COM ₃					0													
COM ₄						▼												
COM ₅						39												
COM ₆						0												
COM ₇							▼											
COM ₈							39											
COM ₉							0											
COM ₁₀								▼										
COM ₁₁								39										
COM ₁₂								0										
COM ₁₃									▼									
COM ₁₄									39									
COM ₁₅									0									
COM ₁₆										▼								
COM ₁₇										39								
COM ₁₈										0								
COM ₁₉											▼							
COM ₂₀											39							
COM ₂₁											0							
COM ₂₂												▼						
COM ₂₃												39						
COM ₂₄												0						
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COM ₂₈														▼				
COM ₂₉														39				
COM ₃₀														0				
COM ₃₁															▼			
COM ₃₂															39			
COM ₃₃															0			
COM ₃₄																▼		
COM ₃₅																39		
COM ₃₆																0		
COM ₃₇																	▼	
COM ₃₈																	39	
COM ₃₉																	0	
COM ₄₀																		▼
(40 th COM period) *1					39	35	31	27	23	19	15	11	7	3				

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40th COM period is not selected.

(32-2) Initial display line "0", 1/41 duty cycle (Common backward scan)

SHIFT="1" (Common backward scan), DS _{3,2,1,0} ="0000", LA ₇ ...LA ₀ ="00000000" (Initial display line 0)													Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001					
COM ₀				39	3	7	11	15	19	23	27	31	35					
COM ₁				▲	▲	▲	▲	▲	▲	▲	▲	▲	▲					
COM ₂					▲													
COM ₃					0													
COM ₄					39													
COM ₅					▲													
COM ₆					0													
COM ₇						▲												
COM ₈						0												
COM ₉							▲											
COM ₁₀							0											
COM ₁₁								▲										
COM ₁₂								0										
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COM ₃₉																		
COM ₄₀																		
(40 th COM period) *1					39	4	8	12	16	20	24	28	32	36				

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40th COM period is not selected.

(32-3) Initial display line "0", 1/17 duty cycle (Common forward scan)

		SHIFT="0" (Common forward scan), DS _{3,2,1,0} "0110", LA _{7...LA₀} "00000000" (Initial display line 0)										Inhibited								
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001							
COM ₀				0								12	8	4						
COM ₁																				
COM ₂												15								
COM ₃																				
COM ₄				0																
COM ₅																				
COM ₆																				
COM ₇																				
COM ₈						0														
COM ₉																				
COM ₁₀																				
COM ₁₁																				
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COM ₄₀																				
(17 th COM period) *1				16	16	16	16	16	16	16	16	15	11	7	3	16				

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(32-4) Initial display line "0", 1/17 duty cycle (Common backward scan)

		SHIFT="1" (Common backward scan), DS _{3,2,1,0} "0110", LA _{7...LA₀} "00000000" (Initial display line 0)										Inhibited								
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001							
COM ₀																				
COM ₁																				
COM ₂																				
COM ₃																				
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(17 th COM period) *1				16	16	16	16	16	16	16	16	12	8	4	16					

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(33) Initial display line "5", 1/41 duty cycle (Common forward scan)

		SHIFT="0" (Common forward scan), DS _{3,2,1,0} "0000", LA _{7...LA₀} "00000101" (Initial display line 0)										Inhibited								
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001							
COM ₀				5																
COM ₁					1															
COM ₂						37														
COM ₃							39													
COM ₄								0												
COM ₅					5															
COM ₆							39													
COM ₇								0												
COM ₈						5														
COM ₉									39											
COM ₁₀										0										
COM ₁₁							5													
COM ₁₂											39									
COM ₁₃												0								
COM ₁₄								5												
COM ₁₅													39							
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(40 th COM period) *1																				

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40th COM period is not selected.

(33-1) Initial display line "5", 1/41 duty cycle (Common backward scan)

		SHIFT="1" (Common backward scan), DS _{3,2,1,0} "0000", LA _{7...LA₀} "00000101" (Initial display line 0)										Inhibited									
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001								
COM ₀				4																	
COM ₁					39																
COM ₂						36															
COM ₃							32														
COM ₄								28													
COM ₅									24												
COM ₆										20											
COM ₇											16										
COM ₈												12									
COM ₉													8								
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(40 th COM period) *1																					

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40th COM period is not selected.

(33-6) Initial display line "0", 1/40 duty cycle (Common forward scan, DSE="1")

		SHIFT="0"(Common forward scan), DS _{3,2,1,0} ="0000", LA _{7...LA₀} ="00000000"(Initial display line 0) DSE="1"																
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM ₀				0	36	32	28	24	20	16	12	8	4					
COM ₁					▼													
COM ₂					39													
COM ₃					0													
COM ₄						▼												
COM ₅						39												
COM ₆						0												
COM ₇							▼											
COM ₈							39											
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COM ₃₆																0		
COM ₃₇																	▼	
COM ₃₈																		▼
COM ₃₉																		
					39	35	31	27	23	19	15	11	7	3				

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

Note 1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC₁, RESb, TEST₁, TEST₂, terminals.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
		V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

Note1) Applies to the condition when the reference voltage generator is not used.

Note2) Applies to the condition when the reference voltage generator is used.

Note3) Applies to the condition when the voltage booster is used.

Note4) The following relationship among the supply voltages must be maintained.

$$V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} \leq V_{OUT}$$

Note5) The relationship: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

$V_{SS} = 0V, V_{DD} = +1.7 \text{ to } +3.3V, T_a = -30 \text{ to } +85^\circ\text{C}$

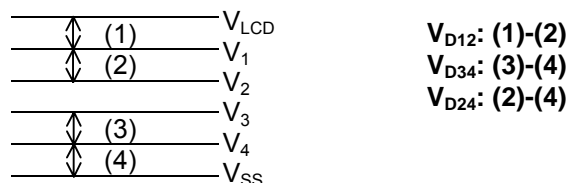
PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE	
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1	
Low level input voltage	V_{IL}		0		$0.2V_{DD}$	V	*1	
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2	
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2	
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3	
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3	
Input leakage current	I_{LI}	$V_i = V_{SS} \text{ or } V_{DD}$	-10		10	μA	*4	
Output leakage current	I_{LO}	$V_i = V_{SS} \text{ or } V_{DD}$	-10		10	μA	*5	
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$	1	2	k Ω	*6	
			$V_{LCD} = 6V$	2	4			
Stand-by current	I_{STB}	$CSb=H, T_a=25^\circ C$			15	μA	*7	
Internal oscillation Frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^\circ C$		152	186	220	kHz	*8
	f_{OSC2}			34	42	50		*9
	f_{OSC3}			4.9	6.0	7.1		*10
External oscillation Frequency	f_{r1}	$R_f=51k\Omega$		172		kHz	*11	
	f_{r2}	$R_f=240k\Omega$		40				
	f_{r3}	$R_f=1800k\Omega$		5.5				
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 5) $R_L = 500k\Omega (V_{OUT} - V_{SS})$	$(N \times V_{EE})$ $\times 0.95$			V	*12	
Supply current (1)	I_{DD1}	$V_{DD} = 3V, 5\text{-time booster}$ Whole ON pattern		520	780	μA	*13	
Supply current (2)	I_{DD2}	$V_{DD} = 3V, 5\text{-time booster}$ Checker pattern		650	980			
Supply current (3)	I_{DD3}	$V_{DD} = 3V, 4\text{-time booster}$ Whole ON pattern		360	540			
Supply current (4)	I_{DD4}	$V_{DD} = 3V, 4\text{-time booster}$ Checker pattern		450	680			
V_{BA} Operating voltage	V_{BA}	$V_{EE} = 2.4 \text{ to } 3.3V$	$(0.9 V_{EE})$ $\times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE})$ $\times 1.02$	V	*14	
V_{REG} Operating voltage	V_{REG}	$V_{EE} = 2.4 \text{ to } 3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time booster (N=2 to 5)	$(V_{REF} \times N)$ $\times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N)$ $\times 1.03$	V	*15	
Output Voltage	V_2		-100	0	+100	mV	*16	
	V_3		-100	0	+100			
	V_{D12}		-30	0	+30			
	V_{D34}		-30	0	+30			
	V_{D24}		-30	0	+30			

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/41 to 1/25	1/21 to 1/13	1/9	1/5	
Internal clock	f_{osc}	16 Gradation mode	$f_{osc} / (62xD)$	$f_{osc} / (62xDx2)$	$f_{osc} / (62xDx4)$	$f_{osc} / (62xDx8)$	FLM
		Simplified 8 gradation mode	$f_{osc} / (14xD)$	$f_{osc} / (14xDx2)$	$f_{osc} / (14xDx4)$	$f_{osc} / (14xDx8)$	
		B&W mode	$f_{osc} / (2xD)$	$f_{osc} / (2xDx2)$	$f_{osc} / (2xDx4)$	$f_{osc} / (2xDx8)$	
External clock	f_{ck}	16 Gradation mode	$f_{ck} / (62xD)$	$f_{ck} / (62xDx2)$	$f_{ck} / (62xDx4)$	$f_{ck} / (62xDx8)$	
		Simplified 8 gradation mode	$f_{ck} / (14xD)$	$f_{ck} / (14xDx2)$	$f_{ck} / (14xDx4)$	$f_{ck} / (14xDx8)$	
		B&W mode	$f_{ck} / (2xD)$	$f_{ck} / (2xDx2)$	$f_{ck} / (2xDx4)$	$f_{ck} / (2xDx8)$	

APPLIED TERMINALS and CONDITIONS

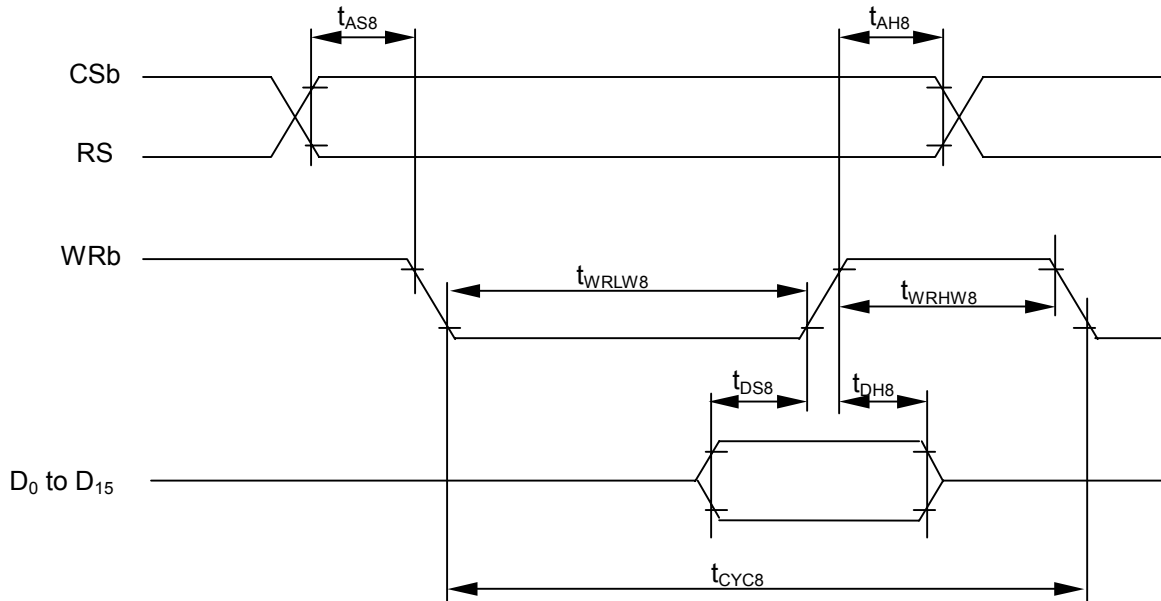
- Note 1) D_0 - D_{15} , CSb, RS, RDb, WRb, P/S, SEL68, RESb
- Note 2) D_0 - D_{15}
- Note 3) CL, FLM, FR, CLK
- Note 4) CSb, RS, SEL68, RDb, WRb, P/S, RESb, OSC₁
- Note 5) D_0 - D_{15} in the high impedance
- Note 6) SEGA₀-SEGA₁₂₇, SEGB₀-SEGB₁₂₇, SEGC₀-SEGC₁₂₇, COM₀-COM₃₉
 - Defines the resistance between the COM/SEG terminals and each of the power supply terminals (V_{LCD} , V_1 , V_2 , V_3 and V_4) at the condition of 0.5V deference and 1/8 LCD bias ratio.
- Note 7) V_{DD}
 - The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers
- Note 8) OSC
 - Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the variable gradation mode.
- Note 9) OSC
 - Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the fixed gradation mode.
- Note 10) OSC
 - Defines the internal oscillation frequency at (Rf_2 , Rf_1 , Rf_0)=(0,0,0) in the Black & White mode.
- Note 11) V_{DD} =3V, Ta=25°C
- Note 12) V_{OUT}
 - Applies to the condition when the internal voltage booster, the internal oscillator and internal power circuits are used.
 - V_{EE} =2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/4 to 1/8 LCD bias, 1/41 duty cycle, No-load on COM/SEG drivers
 - RL=500KΩ between the V_{OUT} and the V_{SS} , CA₁=CA₂=1.0uF, CA₃=0.1uF, DCON="1", AMPON="1"
- Note 13) V_{DD}
 - Applies to the condition using the internal oscillator and internal power circuits, no access between the LSI and MPU.
 - EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode.
 No-load on the COM/SEG drivers.
 - V_{DD} = V_{EE} , V_{REF} =0.9 V_{EE} , CA₁=CA₂=1.0uF, CA₃=0.1uF, DCON="1", AMPON="1", NLIN="0"
 1/41 Duty cycle, Ta=25°C
- Note 14) V_{BA}
 - Applies to the condition that V_{BA} = V_{REF} and voltage booster N= 1. DCON="0", V_{OUT} =13.5V input.
- Note 15) V_{REG}
 - V_{EE} =2.4V to 3.3V, V_{REF} =0.9 V_{EE} , V_{OUT} =18V, 1/4 to 1/8 LCD bias ratio, 1/41 duty cycle, EVR=(1,1,1,1,1,1,1)
 - Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 5
 CA₁=CA₂=1.0uF, CA₃=0.1uF, DCON="0", AMPON="1", NLIN="0"
- Note 16) V_{LCD} , V_1 , V_2 , V_3 , V_4
 - V_{EE} =3.0V, V_{REF} =0.9 V_{EE} , V_{OUT} =15V, 1/4 to 1/8 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5, CA₁=CA₂=1.0uF, CA₃=0.1uF, DCON="0", AMPON="1"



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AC CHARACTERISTICS

- Write operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	
Enable "L" level pulse width	t_{WRLW8}		35		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

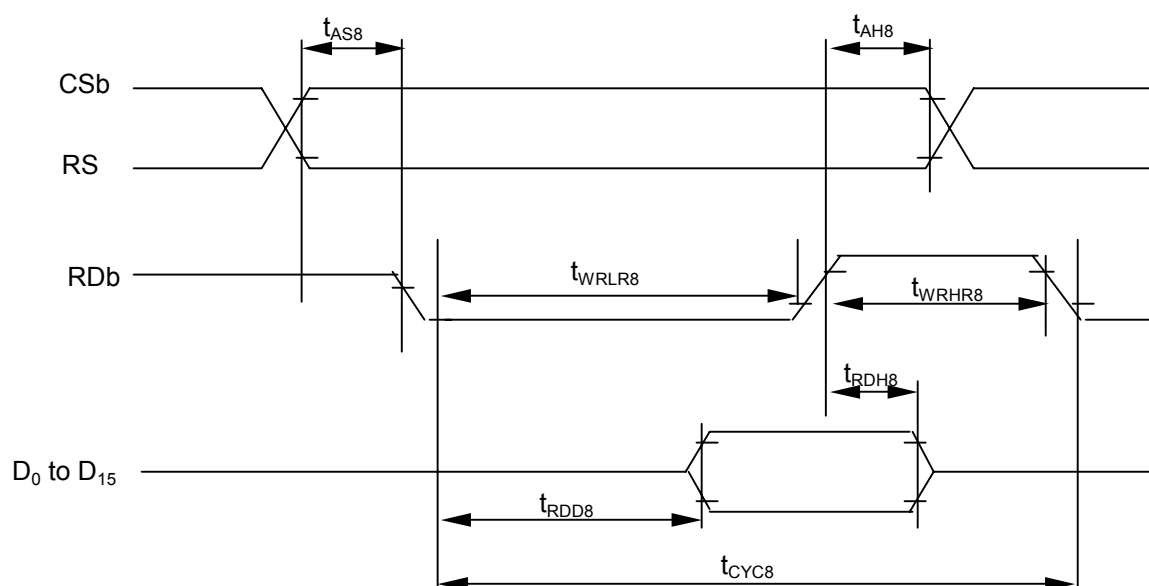
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	
Enable "L" level pulse width	t_{WRLW8}		70		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLW8}		80		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

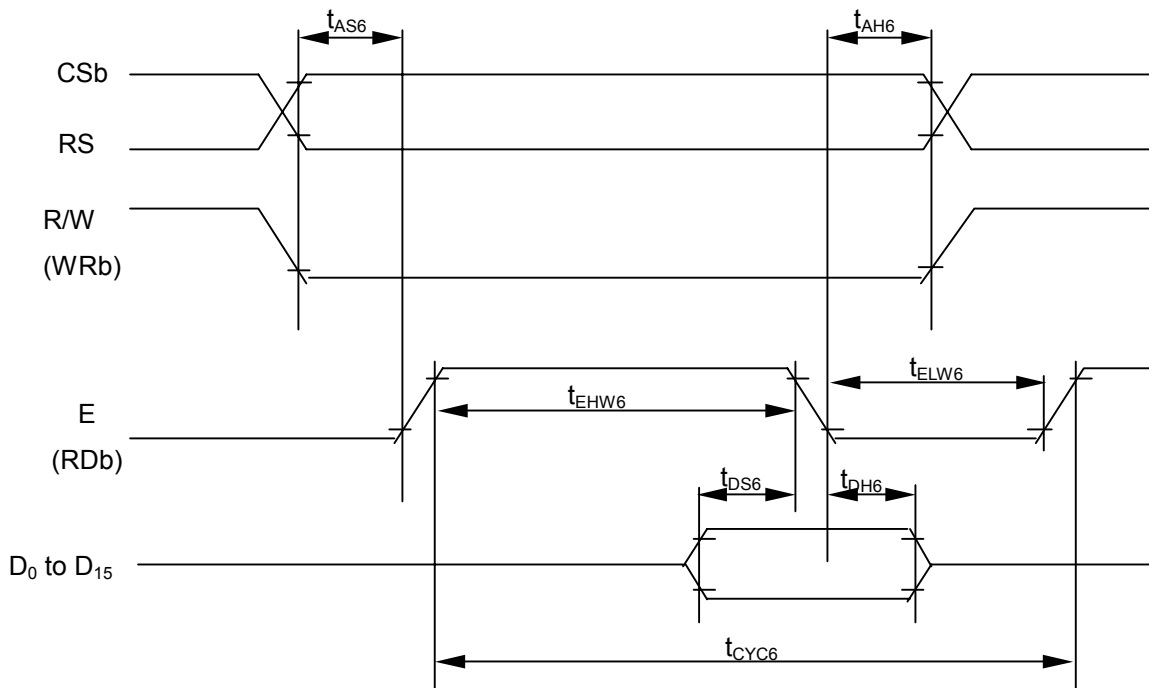
($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		250		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		120		ns	
Enable "H" level pulse width	t_{WRHR8}		120		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

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● Write operation (68-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

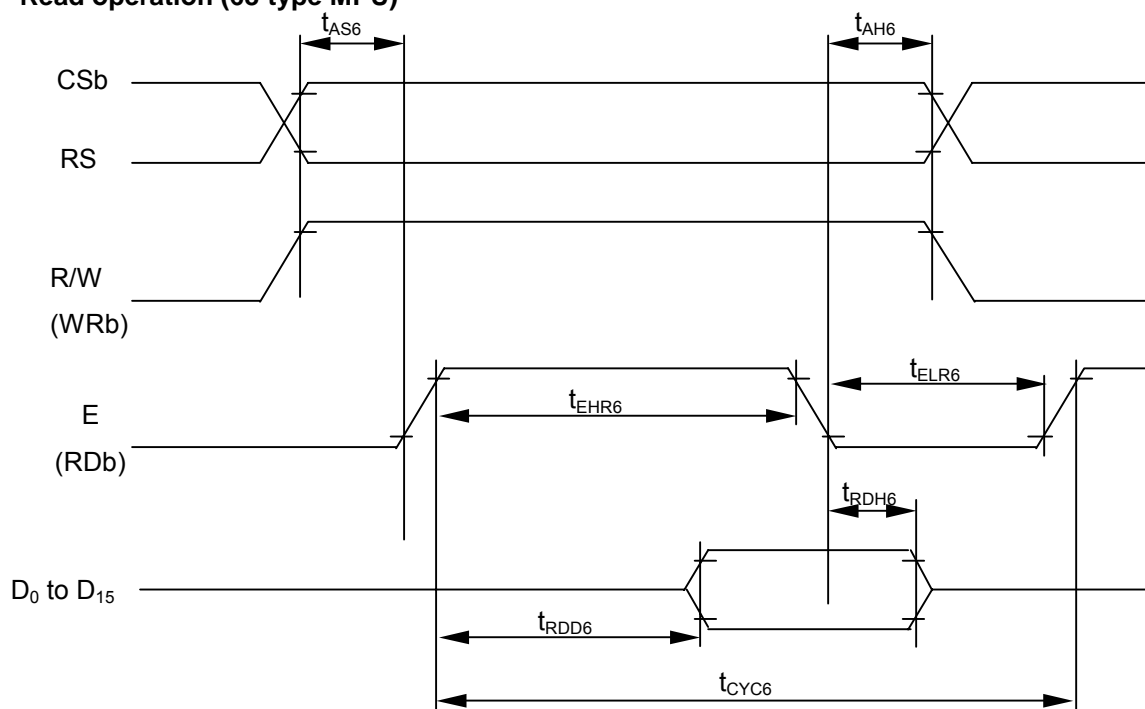
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (68-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

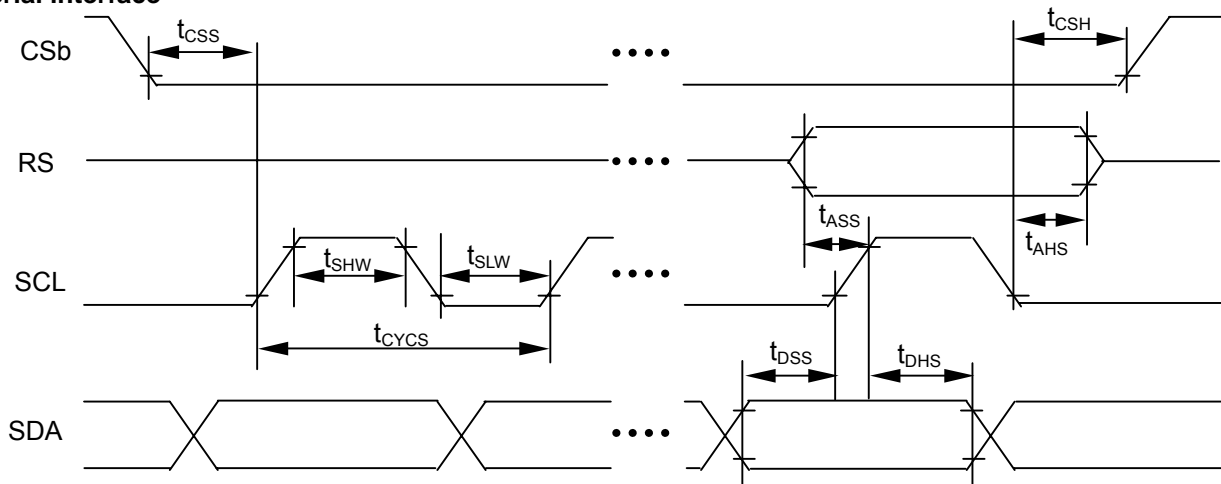
($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	E
Enable "L" level pulse width	t_{ELR6}		120		ns	
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

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Serial interface



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	
SCL "H" level pulse width	t_{SHW}		20		ns	SCL
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

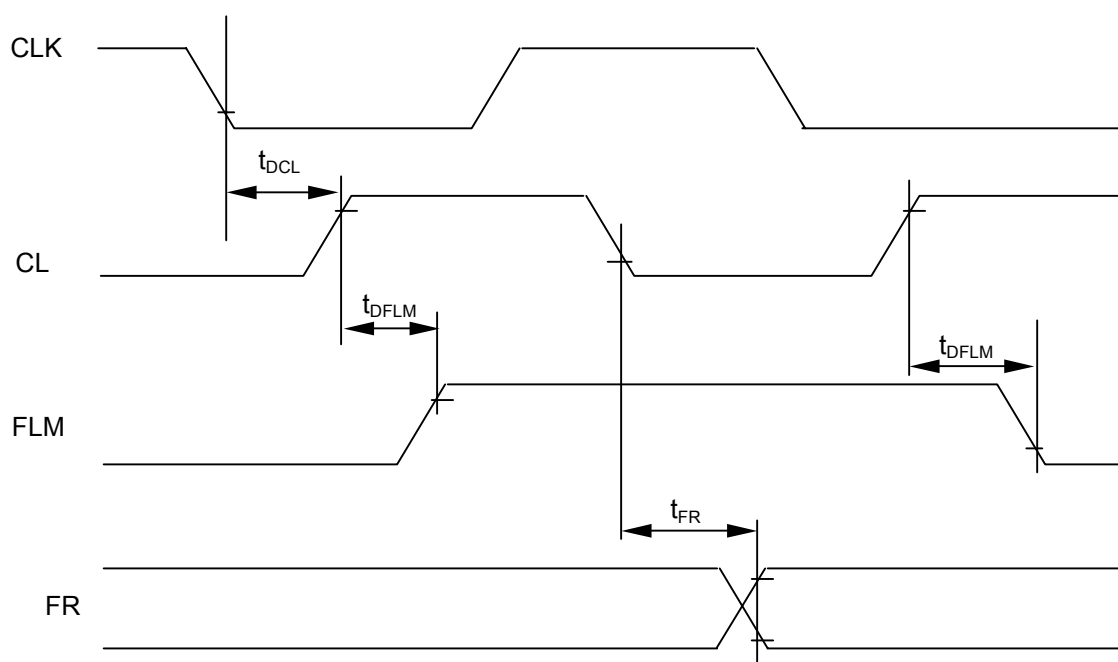
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	
SCL "H" level pulse width	t_{SHW}		20		ns	SCL
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	
SCL "H" level pulse width	t_{SHW}		35		ns	SCL
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Display control timing



Output timing

($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing

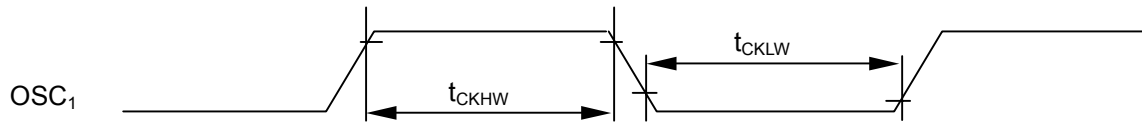
($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD} .

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- Input clock timing



(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC ₁ "H" level pulse width (1)	t _{CKHW1}		2.27	3.29	μs	OSC ₁
OSC ₁ "L" level pulse width (1)	t _{CKLW1}		2.27	3.29	μs	*1
OSC ₁ "H" level pulse width (2)	t _{CKHW2}		10	14.7	μs	OSC ₁
OSC ₁ "L" level pulse width (2)	t _{CKLW2}		10	14.7	μs	*2
OSC ₁ "H" level pulse width (3)	t _{CKHW3}		70	103	μs	OSC ₁
OSC ₁ "L" level pulse width (3)	t _{CKLW3}		70	103	μs	*3

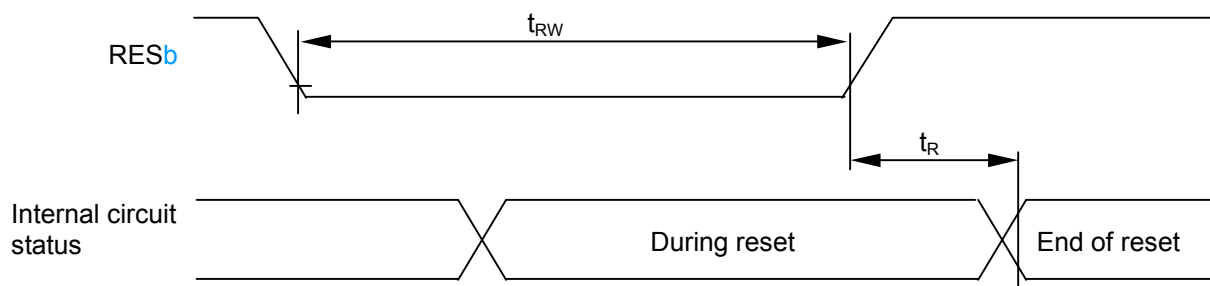
Note) Each timing is specified based on 20% and 80% of V_{DD}.

Note 1) Applied to the variable gradation / mode MON="0",PWM="0"

Note 2) Applied to the fixed gradation / mode MON="0",PWM="1"

Note 3) Applied to the B&W mode / MON="1"

- Reset input timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

Note) Each timing is specified based on 20% and 80% of V_{DD} .

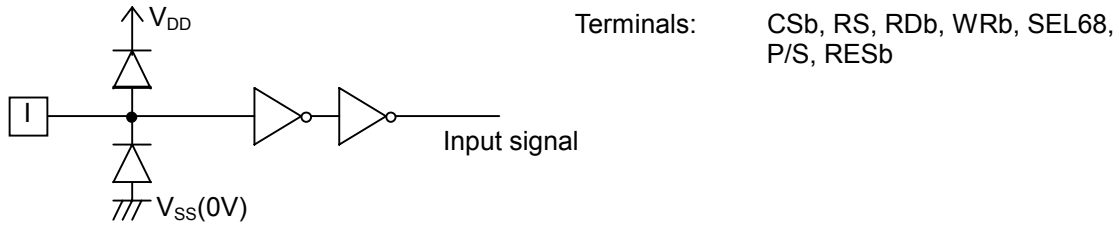
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- Typical characteristic

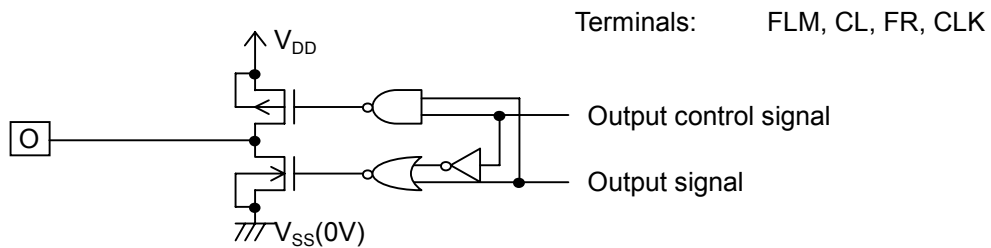
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	$T_a=+25^{\circ}\text{C}$, $V_{SS}=0\text{V}$, $V_{DD}=3.0\text{V}$		10		ns

- Input output terminal type

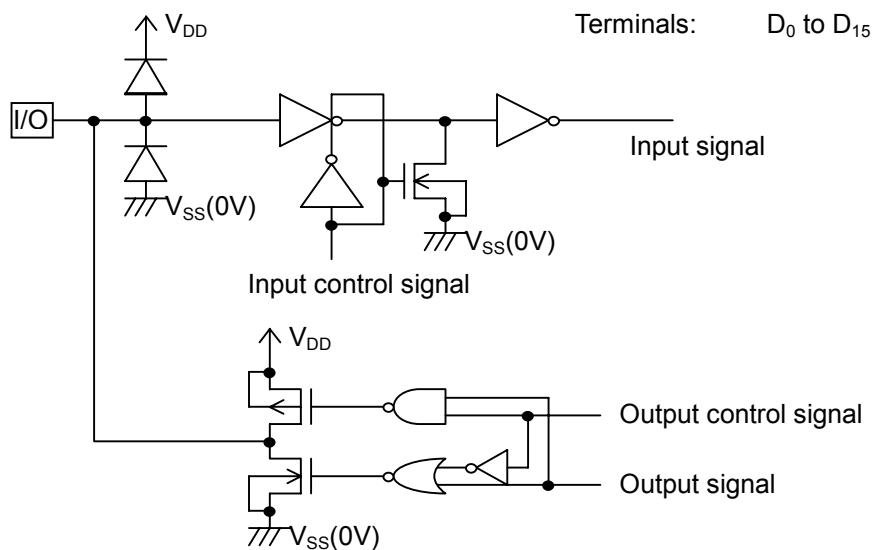
(a) Input circuit



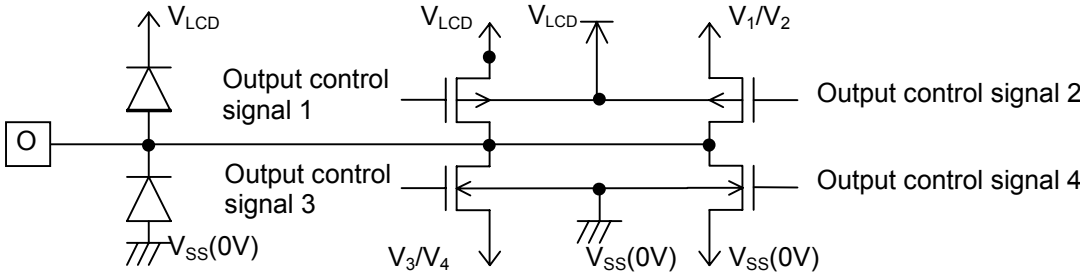
(b) Output circuit



(c) Input/Output circuit



(d) Display output circuit



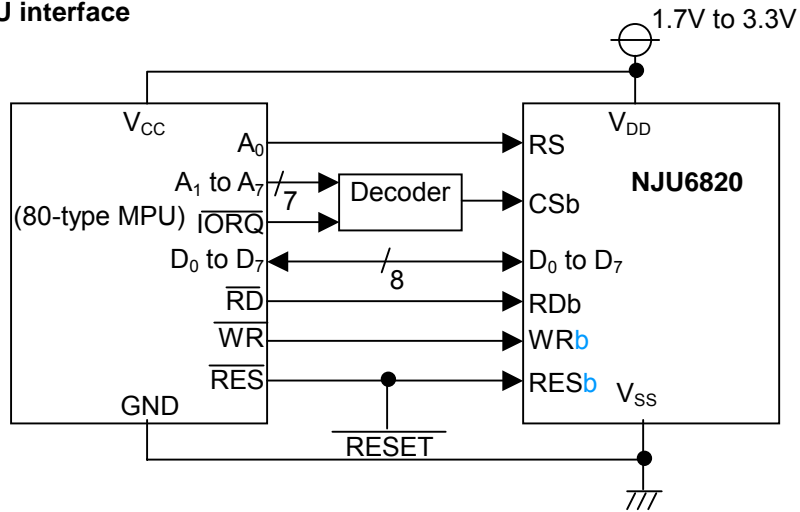
Terminals: SEGA₀ to SEGA₁₂₇
SEGB₀ to SEGB₁₂₇
SEGC₀ to SEGC₁₂₇
COM₀ to COM₃₉

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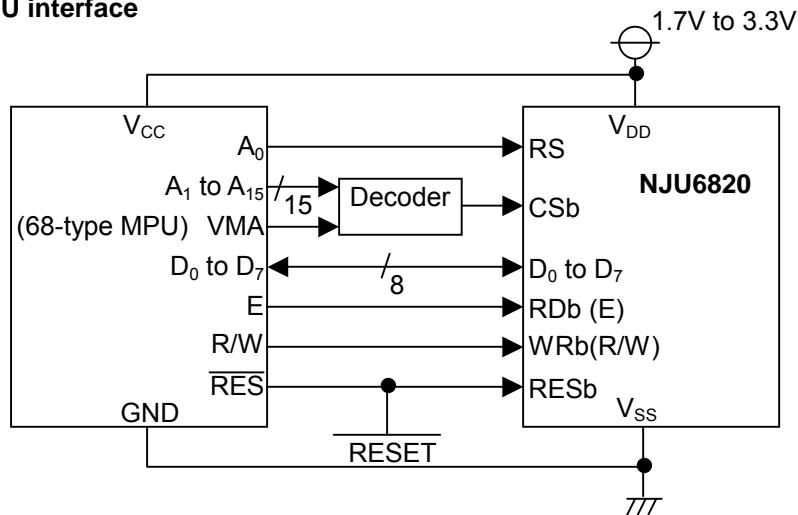
APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

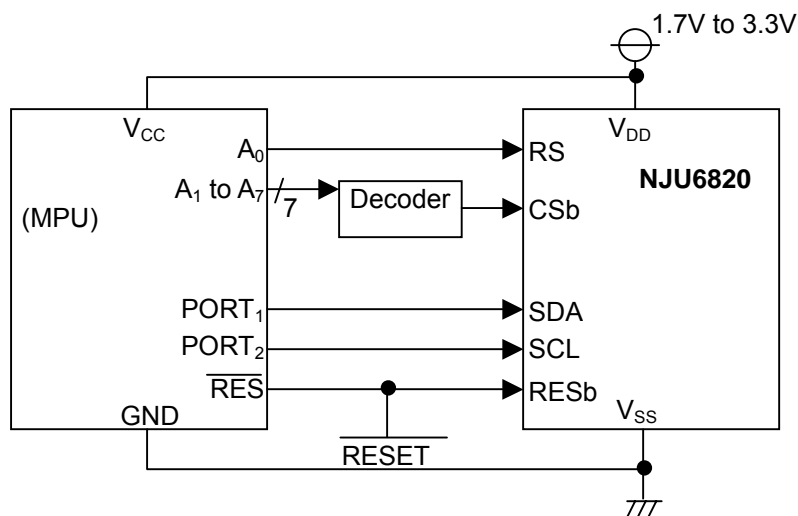
80-type MPU interface



68-type MPU interface



Serial interface



[CAUTION]

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