2Vrms Ground Referenced Stereo Line Amplifier with LPF

■ GENERAL DESCRIPTION

The **NJU72014** is an audio line Amplifier . It can swing 2Vrms (5.6V peak-to-peak) signal at 3.3V operating voltage.

Ground-referenced outputs eliminate output coupling capacitor. The pop noise suppression circuit removes a pop noise at the power-on and power-off.

It is suitable for audio line interface of audio equipment which does not have over 9V regulator.

■ PACKAGE OUTLINE

NJU72014RB2

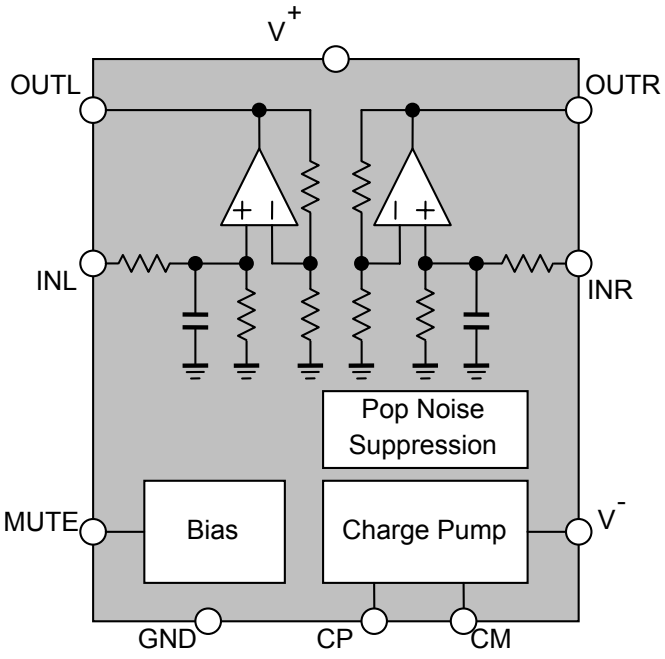
■ APPLICATIONS

- Audio applications requiring 2Vrms outputs

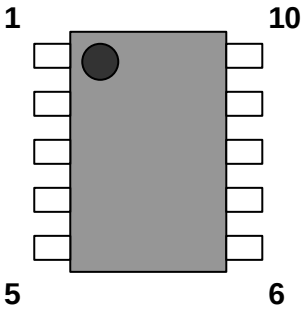
■ FEATURES

- Operating Voltage +2.7 to +3.6V
- Operating Current I_{DD}=4.5mA typ.at V^+=3.3V, R_L=47kΩ, No Signal
- Output Coupling Capacitor-less
- Pop Noise Suppression Circuit
- 2nd order LPF
- C-MOS Technology
- Package Outline MSOP10 (TVSP10)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Symbol	Function
1	INL	Lch Input
2	OUTL	Lch Output
3	V+	V+ Power Supply
4	CP	Flying Capacitor Positive Terminal
5	CN	Flying Capacitor Negative Terminal
6	V-	V- Power Supply
7	MUTE	Mute / Pop Noise Suppression
8	GND	Ground
9	OUTR	Rch Output
10	INR	Rch Input

■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	+4	V
Power Dissipation	P_D	530(Note1))	mW
Maximum Input Voltage	V_{IMAX}	$-V^+$ -0.3 ~ V^+ +0.3	V
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

■ **RECOMMENDED OPERATING CONDITIONS**

(Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		2.7	3.3	3.6	V

■ **ELECTRICAL CHARACTERISTICS**

(Ta=25°C, V^+=3.3V, f=1kHz, Vin=0.6Vrms, Mute=OFF, R_L=47kΩ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{DD}	No signal	-	4.5	10	mA
Output Gain	G_V		10	10.5	11	dB
Output Gain Error	ΔG_V		-0.5	0	0.5	dB
Maximum Output Voltage Level	V_{OMAX}	THD=1%	-	2.3	-	Vrms
Mute Level	V_{MUTE}	Rg=0Ω, Mute=ON	-	-110	-	dB
Equivalent Input Noise Voltage	V_{NO}	Rg=0Ω, BW:400Hz-22kHz	-	-106	-	dB
Total Harmonic Distortion	THD	BW:400Hz-22kHz	-	0.003	-	%
Channel Separation	CS	Rg=600Ω	80	-	-	dB
Cut-off Frequency	f_C	2^{nd} order LPF	100	150	200	kHz
Output Offset Voltage	V_{OS}	Rg=0Ω	-	1	5	mV
Power Supply Rejection Ratio	PSRR	Vripple=1kHz / 100mVrms	-	50	-	dB
Output Impedance	R_{OUT}		-	300	-	Ω

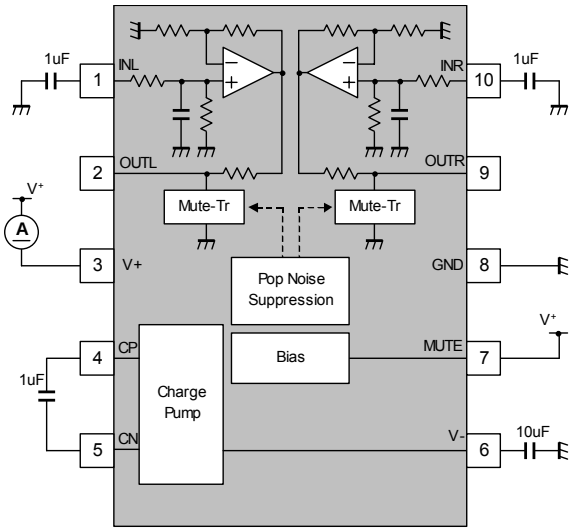
■ **CONTROL CHARACTERISTICS**

(Ta=25°C, V^+=3.3V, R_L=47kΩ unless otherwise specified)

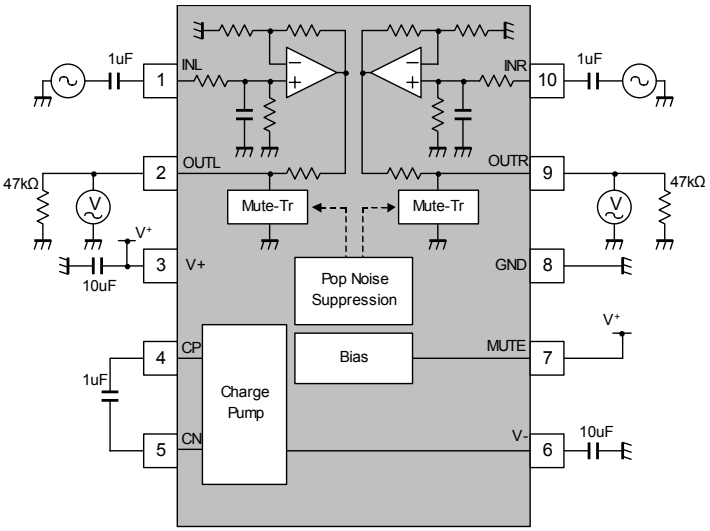
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Mute terminal High	MuteH	Mute=OFF	0.8V^+	-	V^+	V
Mute terminal Low	MuteL	Mute=ON	0	-	0.2V^+	V

■TEST CIRCUIT

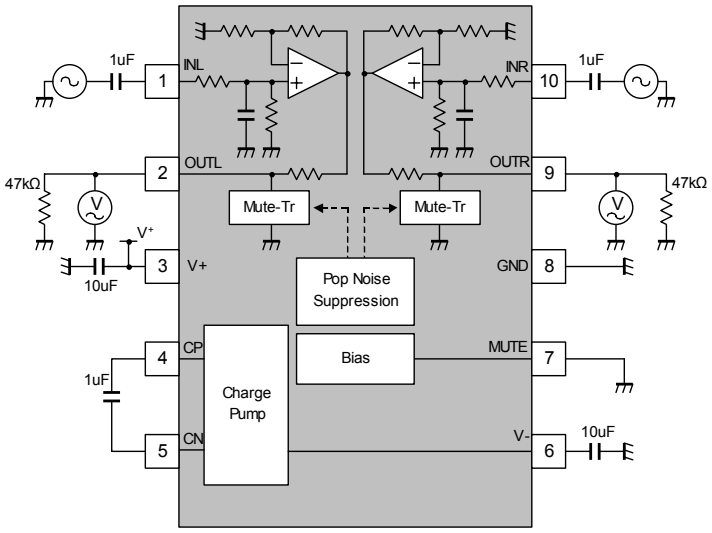
♦I_{DD}



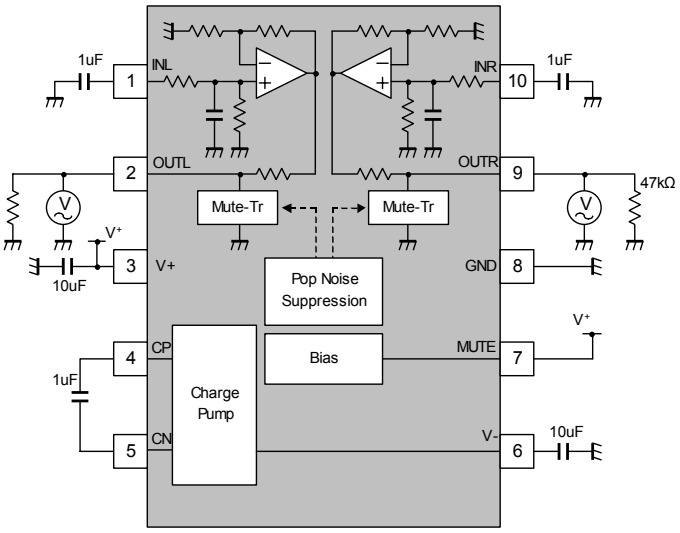
♦G_V, V_{OMAX}, THD



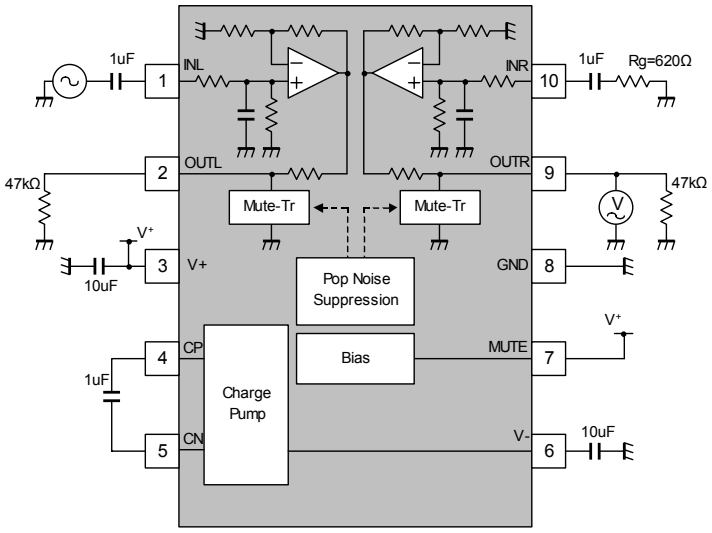
♦V_{MUTE}



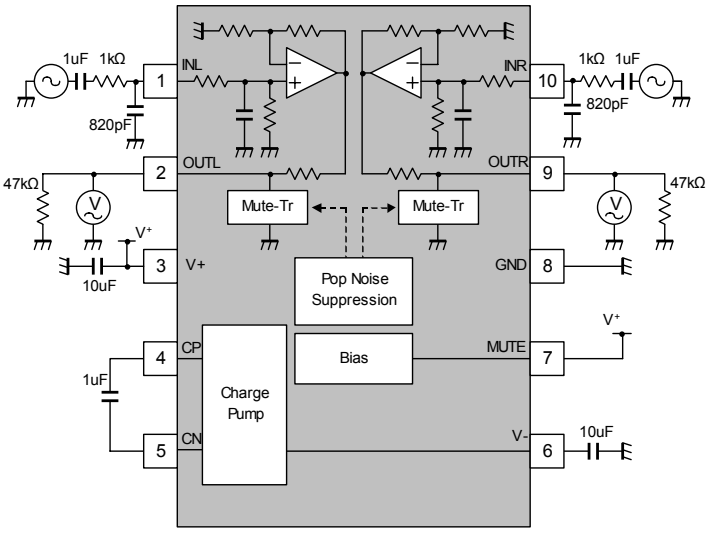
♦V_{NO} [V_{NO}=(measurement)-Gv1]



♦CS



♦f_C



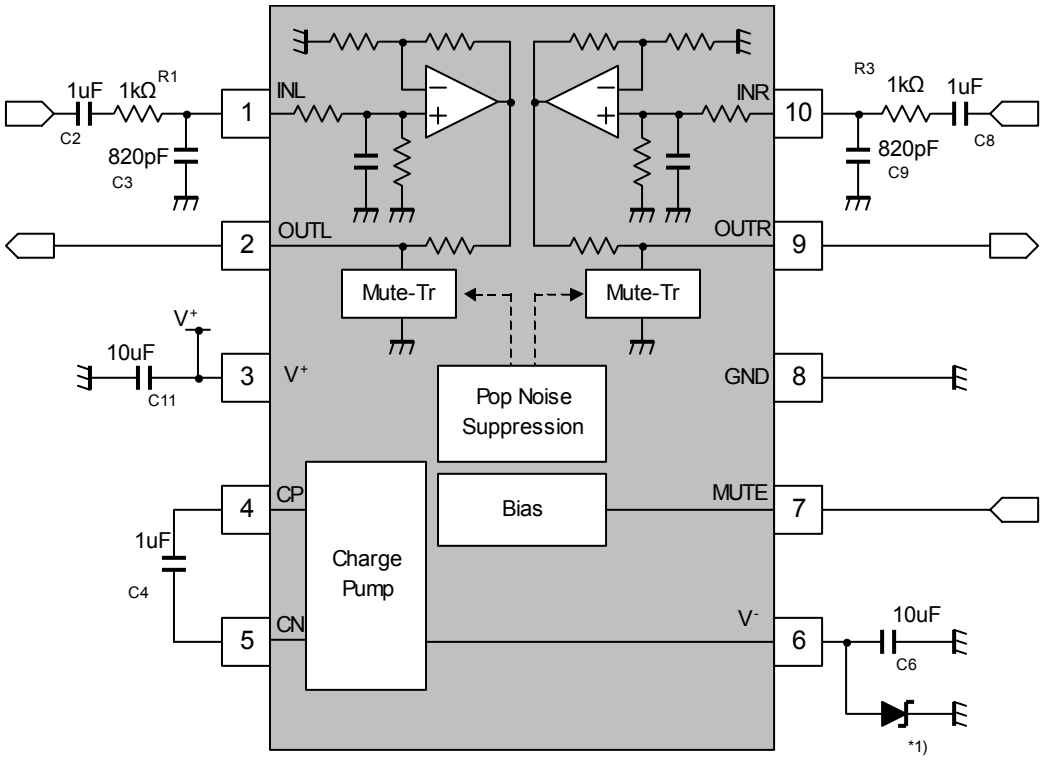
■ APPLICATION NOTE

The NJU72014 is an audio line amplifier that eliminates the need for external dc-blocking output capacitors. The NJU72014 has built-in pop suppression circuitry to eliminate disturbing pop noise during power-on, power-off and mute-control.

1. Operating Principle

The NJU72014 has the built-in non-inverted input operational amplifiers, voltage inverter, and pop noise suppression circuitry (Fig.1).

The voltage inverter for NJU72014 eliminates the need for external dc-blocking output capacitors. The pop suppression circuitry for NJU72014 eliminates the pop noise during power-on, power-off and mute-control.



*1) Connect a zener diode between V- terminal[6pin] and GND terminal[8pin] to prevent connecting V- terminal[6pin] and V+ terminal[3pin].

Fig.1 The NJU72014 functional block diagram

1.1 External parts

1.1.1 Input coupling capacitors C_i (C2, C8)

The input coupling capacitor (C_i) and the total of the external resistance (R1, R3) and the input resistance (R_{in}=218kΩ typ.) for the non-inverted terminal form a high-pass filter with the corner frequency determined in [fc=1/(2π x (R1+218kΩ) x C_i)). It is necessary to adjust 1uF or more.

1.1.2 Flying capacitor (C4)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between CP terminal (4pin), CN terminal (5pin), and the flying capacitor (C4).

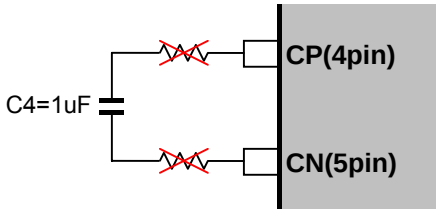


Fig.2 The NJU72014 block diagram (4pin, 5pin)

1.1.3 Hold capacitor (C6)

Use capacitors with a low-ESR (ex. ceramic capacitors) for optimum performance. Design to provide low impedance for the wiring between the hold capacitor (C6), V- terminal (6pin) and the GND on the PCB.

Separate the GND pattern connecting to the hold capacitor (C6) from that connecting to the GND terminal (8pin), thus suppressing the influence of switching noise by removing the common impedance of the GND wiring.

Design no short-circuits of V- terminal (6pin) and V+ terminal (3pin) on the PCB pattern.

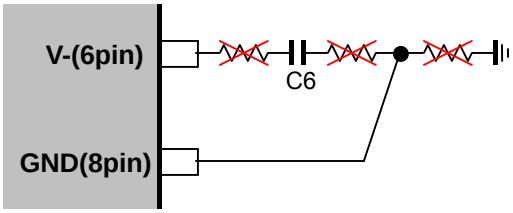


Fig.3 The NJU72014 block diagram (6pin, 8pin)

1.1.4 To reducing output signal level

Output Gain level(Gv) is adjustable by the value of the R1 and R2 connected to Input pin (Pin 1,10). Add ATT to input pin of NJU72014 as shown in Fig.4.

$$Gv = 11.25 + 20\log\frac{R_2 // (R_3 + R_4)}{R_1 + R_2 // (R_3 + R_4)} + 20\log\frac{R_4}{R_3 + R_4} \quad (1)$$

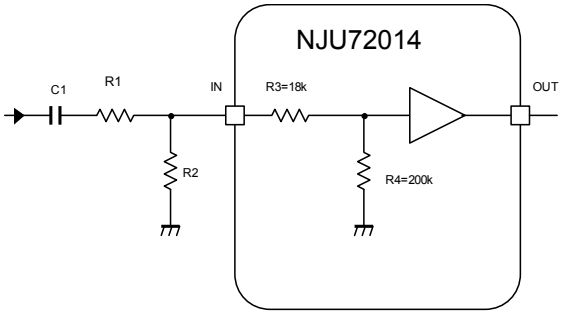


Fig.4 NJU72014 with ATT.

Ex) In the case of R1=1kΩ and R2=82kΩ

$$Gv = 11.25 + 20\log\frac{R_2 // (R_3 + R_4)}{R_1 + R_2 // (R_3 + R_4)} + 20\log\frac{R_4}{R_3 + R_4}$$

$$= 11.25 + 20\log\frac{82k // (18k + 200k)}{1k + 82k // (18k + 200k)} + 20\log\frac{200k}{18k + 200k}$$

$$= 10.36\,[dB]$$

1.2 Control of V+ terminal and Mute terminal

1.2.2 Power-on procedure

Turn on the V+ in the condition of MUTE terminal is “Low”. After 100msec from power on, change the control voltage of MUTE terminal (Vcnt) from "Low" to "High".

* It is necessary to stabilize an IC for 100msec.

1.2.3 Power-off procedure

Change the control voltage of MUTE terminal (Vcnt) from "High" to "Low".By the MUTE function, the output signals are stopped from output terminal.

Turn off the V+.

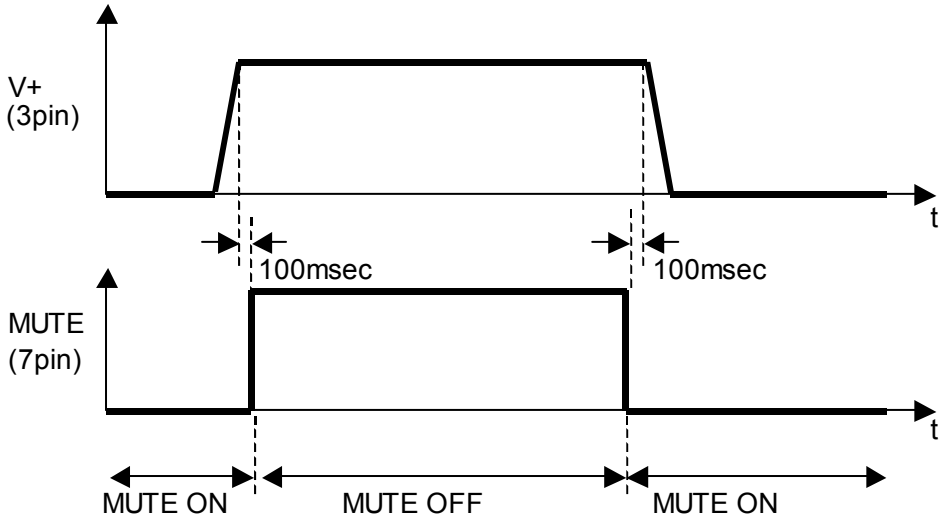
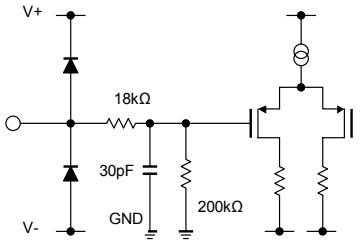
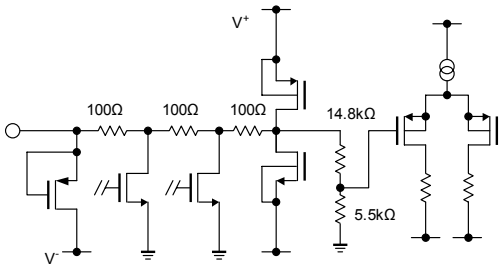
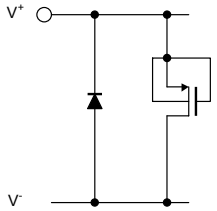
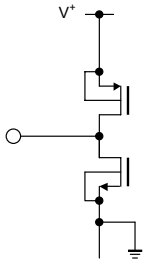
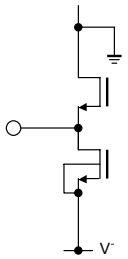
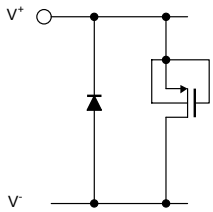
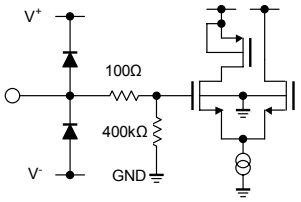


Fig.5 Power-on / Power-off timing chart

■TERMINAL DESCRIPTION

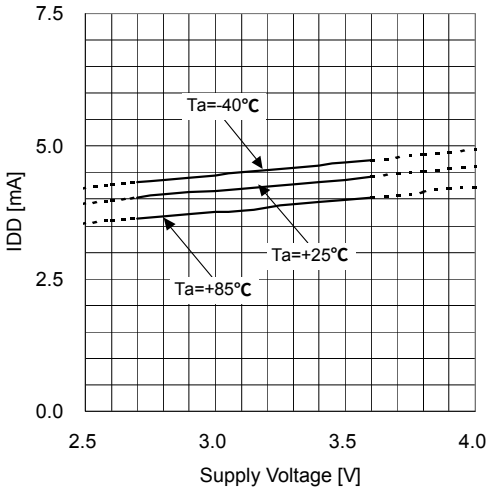
Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
1 10	INL INR	AC Input		0V
2 9	OUTL OUTR	AC Output		0V
3	V+	Supply Voltage		V+
4	CP	Flying Capacitor Positive Terminal		-

■TERMINAL DESCRIPTION

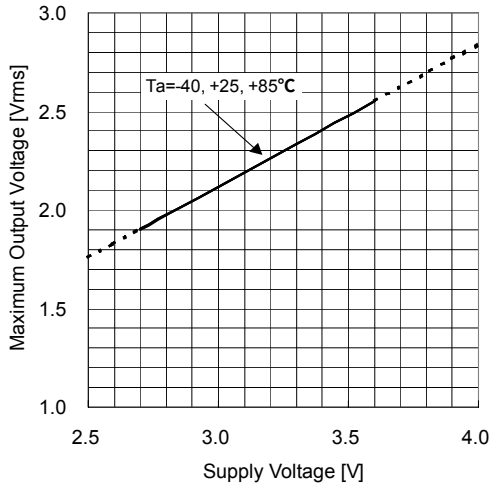
Terminal	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
5	CN	Flying Capacitor Negative Terminal		-
6	V-	V- Voltage		-[V+]
7	MUTE	MUTE/Pop Noise Suppression		0V

■TYPICAL CHARACTERISTICS

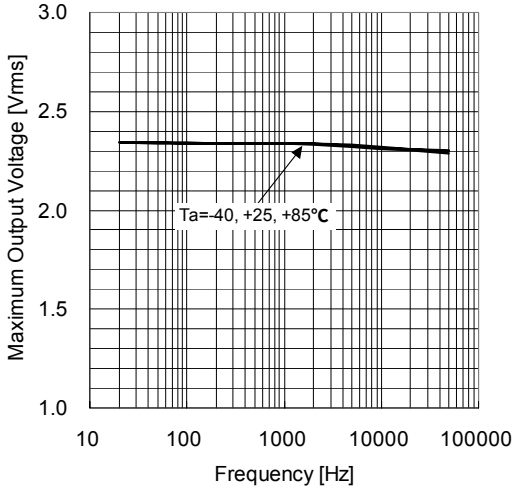
IDD vs Supply Voltage
No signal



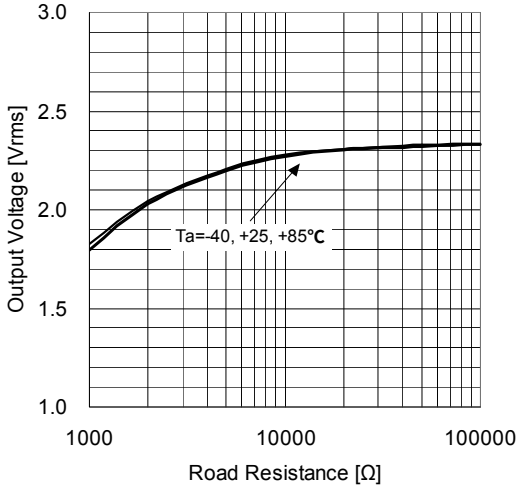
Maximum Output Voltage vs Supply Voltage
THD+N=1%, RL=47kohm, I/O=INL-OUTL



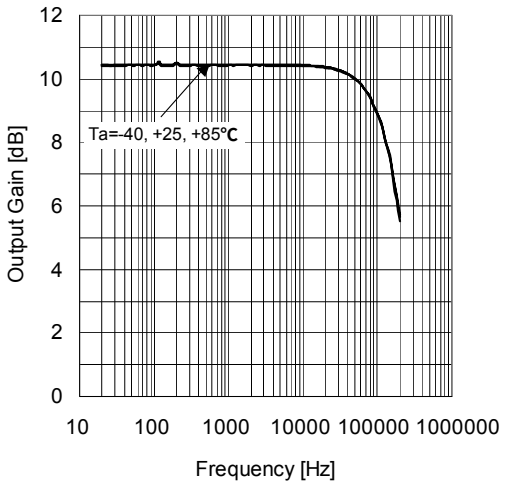
Maximum Output Voltage vs Frequency
V+=3.3V, THD+N=1%, RL=47kohm, I/O=INL-OUTL



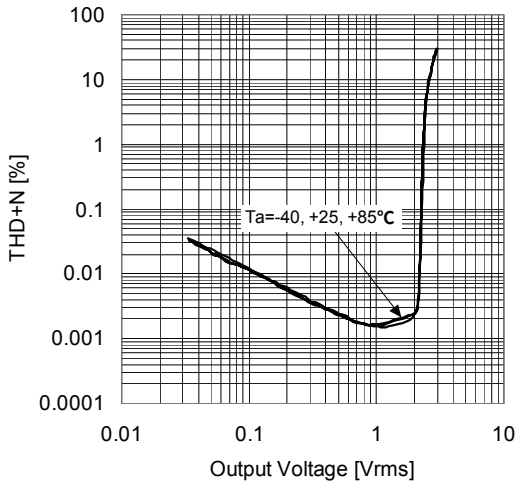
Output Voltage vs Road Resistance
V+=3.3V, Vin=0.7Vrms, f=1kHz,
I/O=INL-OUTL



Output Gain vs Frequency (2nd LPF)
V+=3.3V, Vin=0.6Vrms, RL=47kohm,
2nd LPF



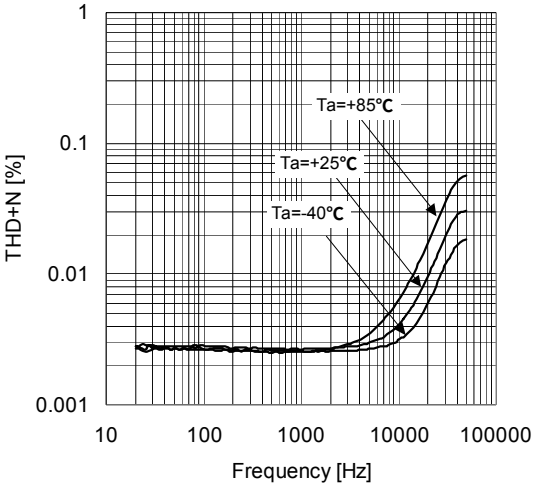
THD+N vs Output Voltage
V+=3.3V, f=1kHz, BW: 400-22kHz(f=1kHz),
I/O=INL-OUTL,



■TYPICAL CHARACTERISTICS

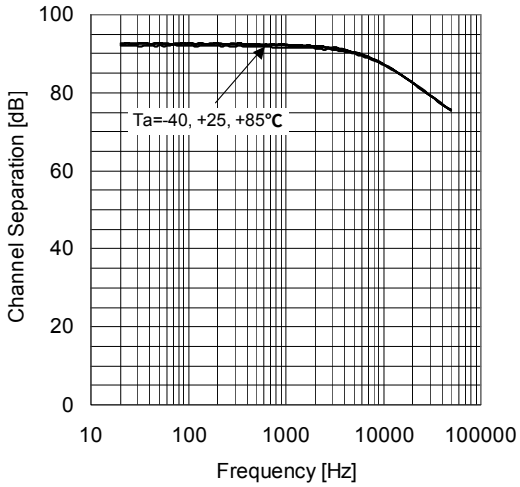
THD+N vs Frequency

V+=3.3V, Vin=0.6Vrms, RL=47kohm,
BW=10-80kHz, I/O:INL-OUTL



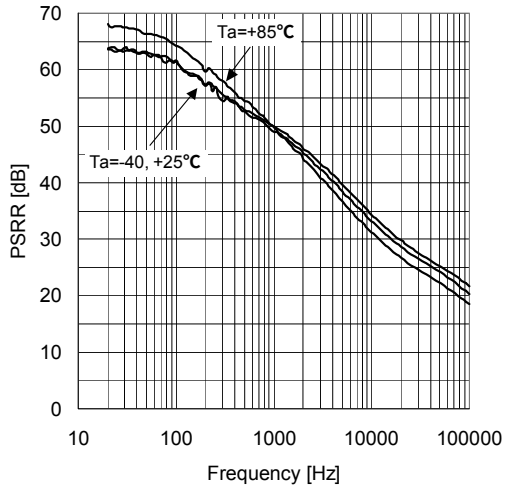
Channel Separation vs Frequency

V+=3.3V, RL=47kohm, Vin=0.6Vrms,
BW:10-80kHz, I/O: INR-OUTL



PSRR vs Frequency

V+=3.3V, Vripple=100mVrms, f=1kHz,
BW: Bandpass



Output Gain vs Mute Control Voltage

V+=3.3V, Vin=0.6Vrms, f=1kHz,
BW: 400-22kHz