Low Dropout Voltage Regulator with Reset

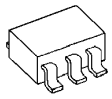
■ GENERAL DISCRIPTION

The NJU7271 is a low drop out voltage regulator with output-monitor reset function. Advanced CMOS technology achieves ultra low current consumption and high accuracy.

It delivers up to 5V/100mA output power with the maximum input voltage of 9V.

The NJU7270 is suitable for MPU applications.

■ PACKAGE OUTLINE

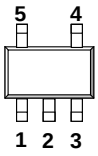


NJU7271F

■ FEATURES

- Ultra Low Quiescent Current Iq=3.0μA typ. (Io=0mA)
- Output Voltage Accuracy Vo = ±1.0%
- Reset Voltage Accuracy V_{RT} = ±1.0%
- Output Voltage Monitor type
- Output Current Io(max.)=100mA
- Output capacitor with 0.1uF ceramic capacitor
- Nch Open Drain Output
- Internal Short Circuit Current Limit
- CMOS Technology
- Package Outline SOT-23-5

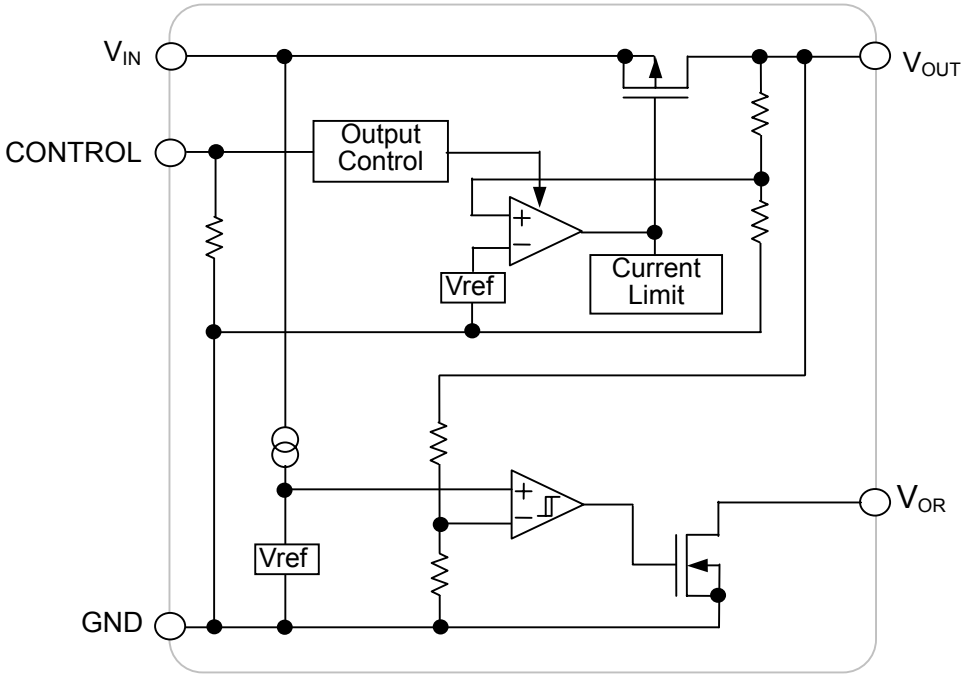
■ PIN CONFIGURATION



1.V_{IN}
2.GND
3.CONTROL
4.V_{OR}
5.V_{OUT}

NJU7271F

■ EQUIVALENT CIRCUIT



■ OUTPUT VOLTAGE/ DETECTION VOLTAGE

Device Name	Output Voltage	Detection Voltage
NJU7271F1813A	1.8V	1.3V
NJU7271F3328A	3.3V	2.8V
NJU7271F0543A	5.0V	4.3V

Output voltage options available : 1.8 ~ 5.0V (0.1V step)
Detection voltage options available : 1.3 ~ 4.5V (0.1V step)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	+11	V
Control Voltage	V_{CONT}	+11(*1)	V
V_{OR} Pin Output Voltage	V_{OR}	V_{SS} - 0.3 ~ +11	V
V_{OR} Pin Output Current	I_{OR}	50	mA
Power Dissipation	P_D	200(*2) 350(*3)	mW
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C

(*1): Device itself
(*2): Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

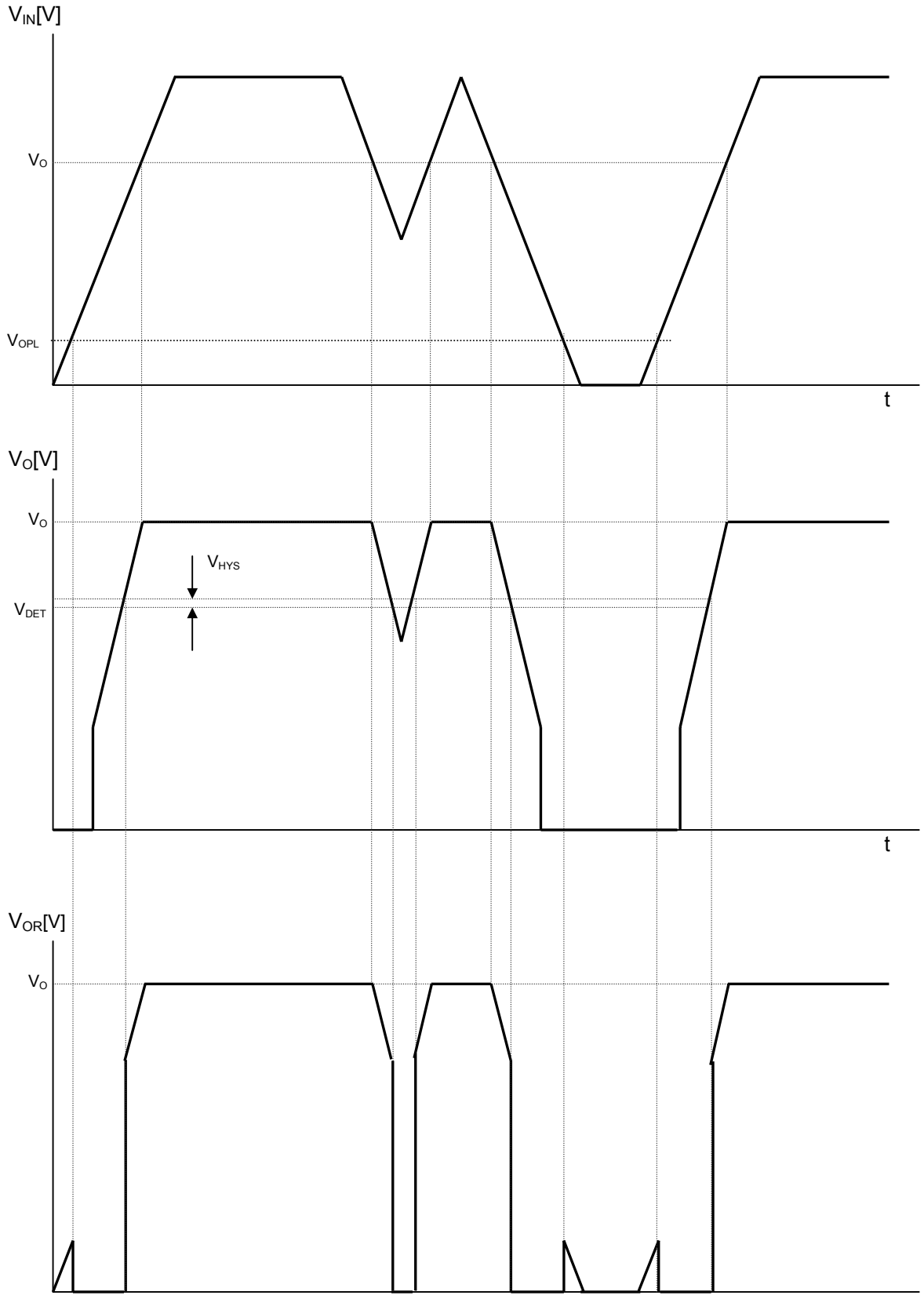
■ ELECTRICAL CHARACTERISTICS (V_{IN}=Vo+1, C_{IN}=0.1µF, C_O=0.1µF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
General Characteristics							
Quiescent Current	I_Q	V_{CONT}=V_{IN} , I_O=0mA		-	3.0	7.6	µA
Quiescent Current at Control OFF	$I_{Q(OFF)}$	V_{CONT}=0V , I_O=0mA		-	0.1	1.0	µA
Regulator Block							
Output Voltage	V_O	I_O=30mA		-1.0%	-	+1.0%	V
Output Current	I_O	V_O - 0.3V		100	-	-	mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN}=V_O+1V ~ V_O+6V(3.0 > V_O) V_{IN}=V_O+1V ~ 9.0V(3.0 ≤ V_O) I_O=30mA		-	-	0.30	%/V
Load Regulation	$\Delta V_O/\Delta I_O$	I_O=0 ~ 100mA		-	-	0.15	%/mA
Output Voltage Temperature Coefficient	$\Delta V_O/\Delta Ta$	Ta=0 ~ 85°C, I_O=10mA		-	±100	-	ppm/°C
Control Voltage for ON-State	$V_{CONT(ON)}$			1.6	-	V_{IN}	V
Control Voltage for OFF-State	$V_{CONT(OFF)}$			0	-	0.3	V
Pull-down Resistance	R_{CONT}			2.0	5	10	MΩ
Short Circuit Limit	I_{LIM}	V_O=0V		-	25	-	mA
Input Voltage	V_{IN}			-	-	9	V
Dropout Voltage	ΔV_{I-O}	I_O=40mA	1.5V ≤ V_O ≤ 2.0V	-	0.19	0.60	V
		I_O=60mA	2.1V ≤ V_O ≤ 2.4V	-	0.19	0.29	V
			2.5V ≤ V_O ≤ 2.7V	-	0.18	0.27	V
			2.8V ≤ V_O ≤ 3.3V	-	0.17	0.26	V
			3.4V ≤ V_O ≤ 5.0V	-	0.16	0.24	V
			5.1V ≤ V_O ≤ 6.0V	-	0.15	0.22	V

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Reset Block							
Detection Voltage	V_{DET}			-1.0%	-	+1.0%	V
Hysteresis Voltage	V_{HYS}			V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.08	V
V_{OR} Pin Output Current	I_{OR}	Nch,V_{DS}=0.5V V_{CONT}=0V	V_{IN}=1.2V	0.75	2.0	-	mA
			V_{IN}=2.4V (V_{DET} ≥ 2.7V Version)	4.5	7.0	-	mA
Output Leak Current	I_{LEAK}	V_{IN}=V_{OR}=V_{CONT}=9V		-	-	0.1	μA
Detection Voltage	$\Delta V_{DET}/\Delta Ta$	Ta=0 ~ 85°C		-	±100	-	ppm/°C
Operating Voltage(*4)	V_{OPL}	R_L=100kΩ		-	-	0.8	V

(*3): The value condition that V_{OR} become 10% or less of V_{IN}.

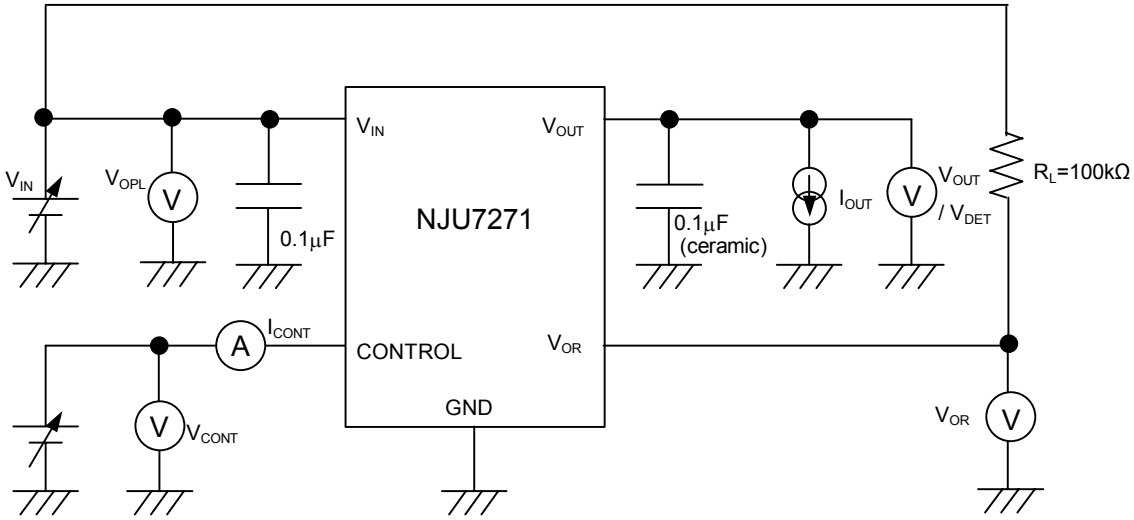
■ TIMING CHART



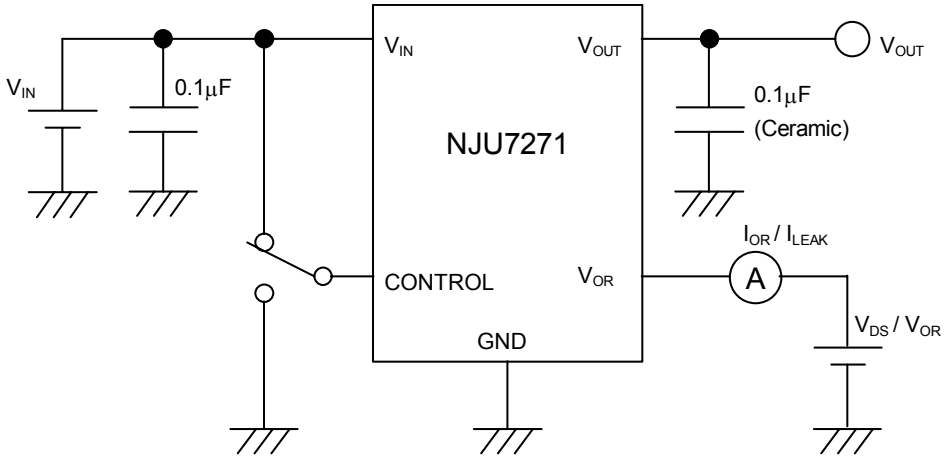
∗ V_{OR} is the case where a pull-up is carried out to V_{IN} through resistance.

■ TEST CIRCUIT

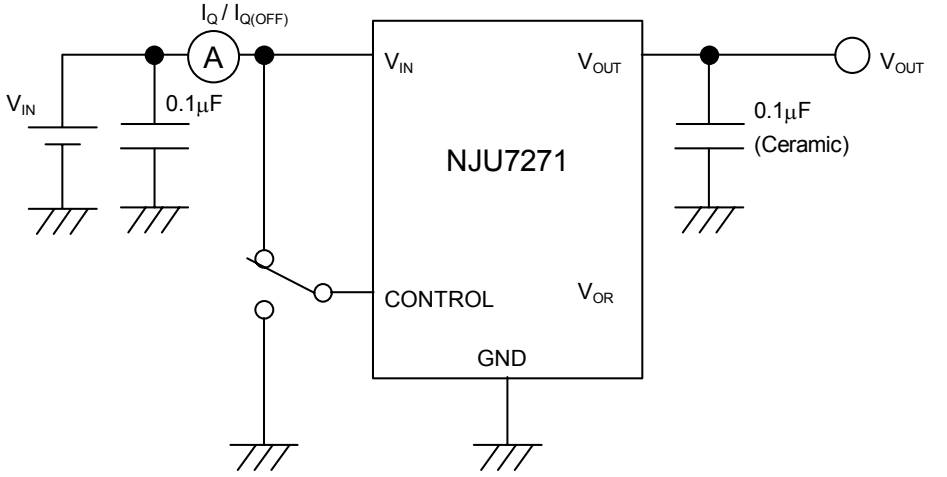
① COMMON TEST CIRCUIT



② OUTPUT CURRENT/OUTPUT LEAK CURRENT TEST CIRCUIT

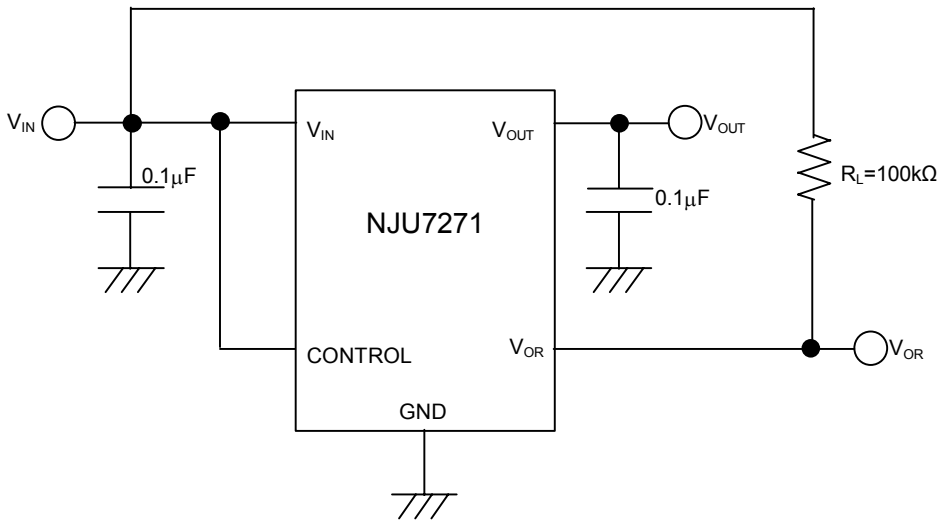


③ QUIESCENT CURRENT TEST CIRCUIT



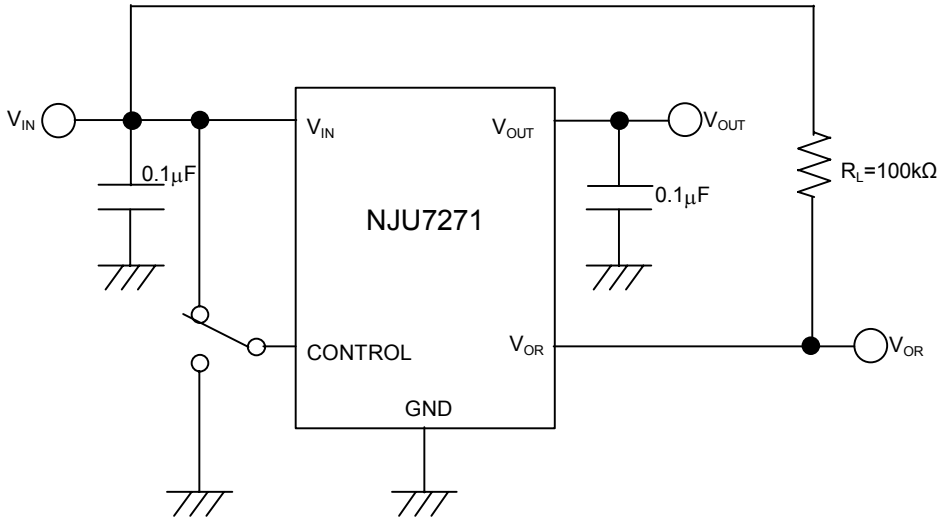
■ TYPICAL APPLICATION

① In case that ON/OFF Control is not required:



Connect control terminal to V_{IN} terminal.

② In use of ON/OFF Control:



State of control terminal:

- "H" → output is enabled.
- "L" or "open" → output is disabled.

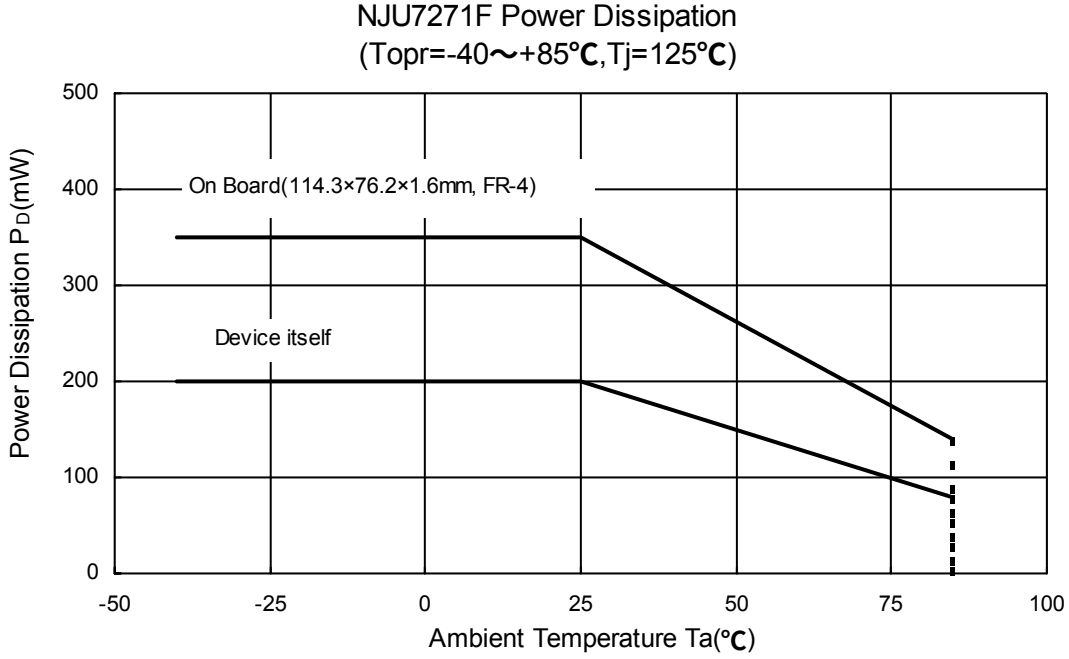
∗Input Capacitance C_{IN}

Input Capacitance C_{IN} is required to prevent oscillation and reduce power supply ripple for applications with high power supply impedance or a long power supply line.
Use the C_{IN} value of 0.1µF greater to avoid the problem.
C_{IN} should connect between GND and V_{IN} as short as possible.

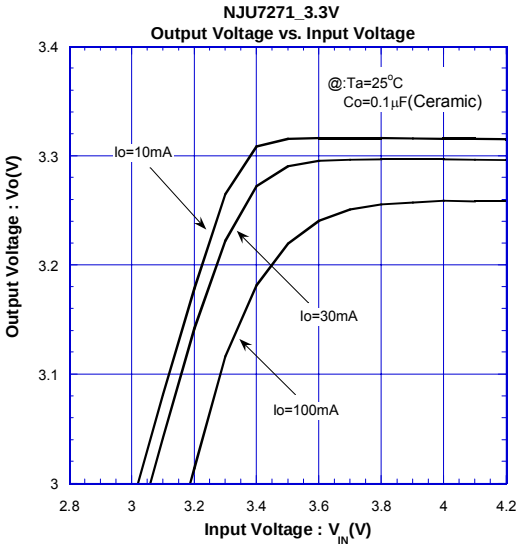
∗Output Capacitance Co

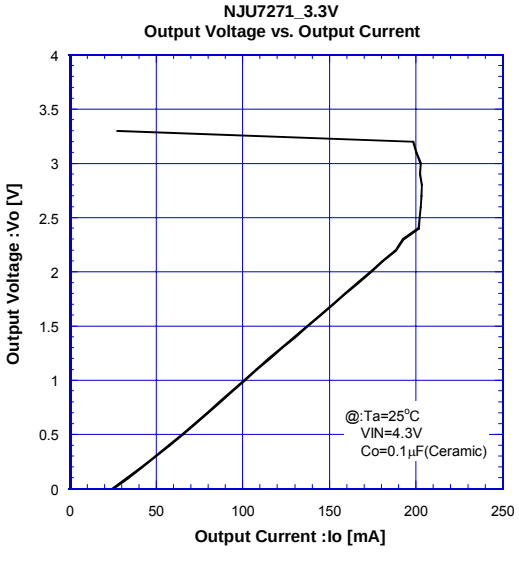
Output capacitor (Co) is required for a phase compensation of the internal error amplifier. The capacitance and the equivalent series resistance (ESR) influence stability of the regulator.
If use a smaller Co, it may cause excess output noise or oscillation of the regulator due to lack of the phase compensation. Therefore, use Co with the recommended capacitance or greater value and connect between Vo terminal and GND terminal with minimal wiring.
The recommended capacitance depends on the output voltage. Low voltage regulator requires greater value of the Co. Thus, check the recommended capacitance for each output voltage.
Use of a greater Co reduces output noise and ripple output, and also improves transient response of the output voltage against rapid load change.
This product is designed to work with any capacitor including a low ESR capacitor for the Co; however, refer "Equivalent Series Resistance vs. Output Current" and choose suitable capacitor.

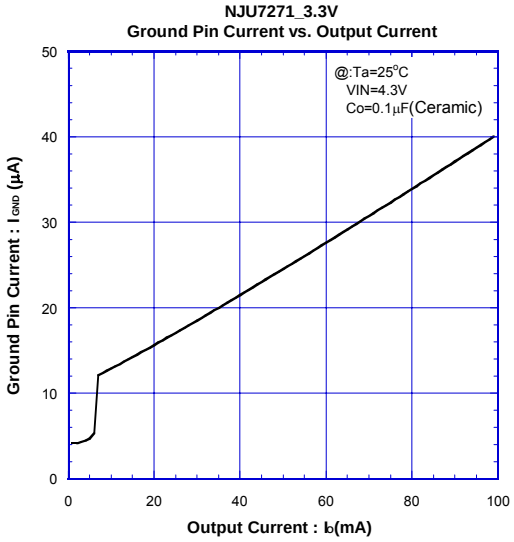
■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

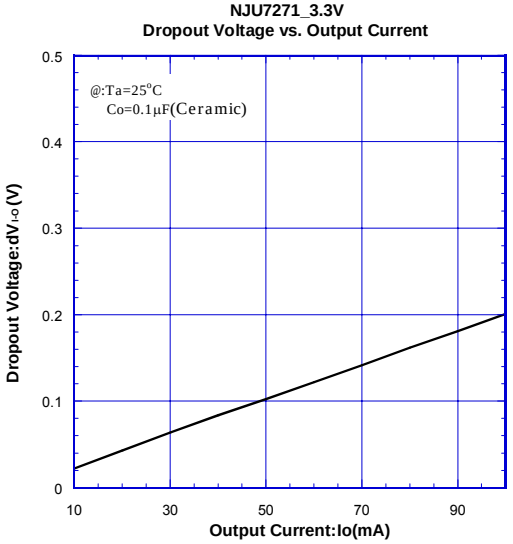


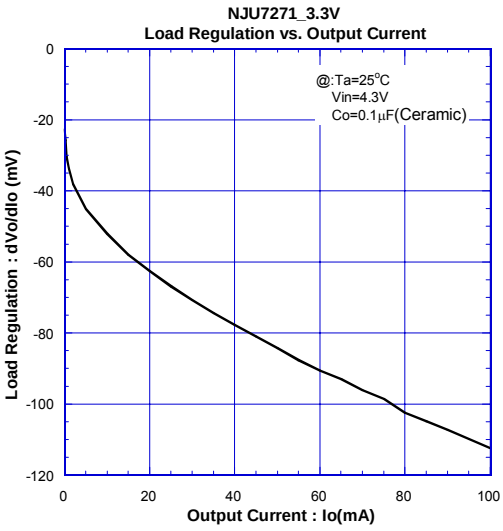
■ TYPICAL CHARACTERISTICS (LDO BLOCK)

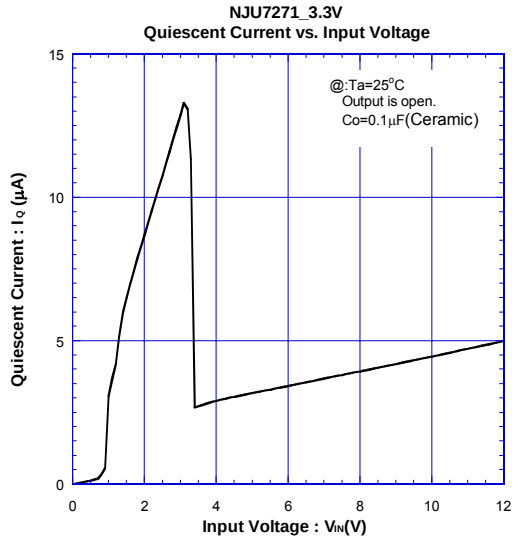












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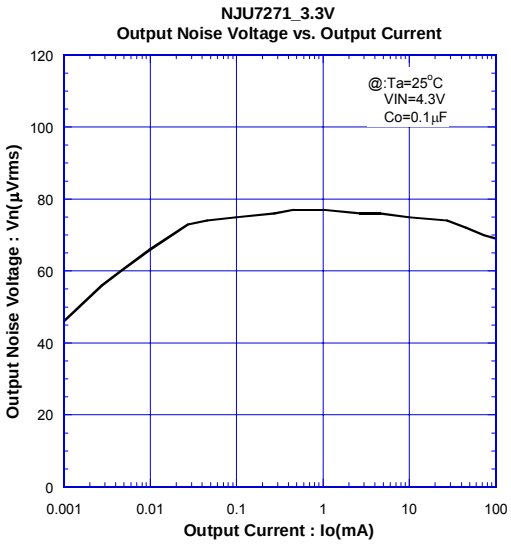
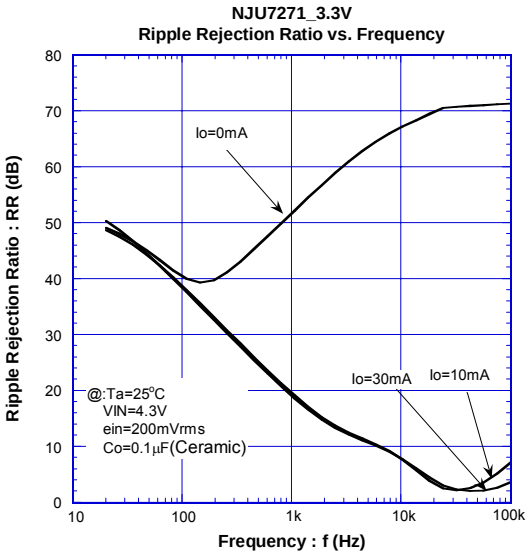
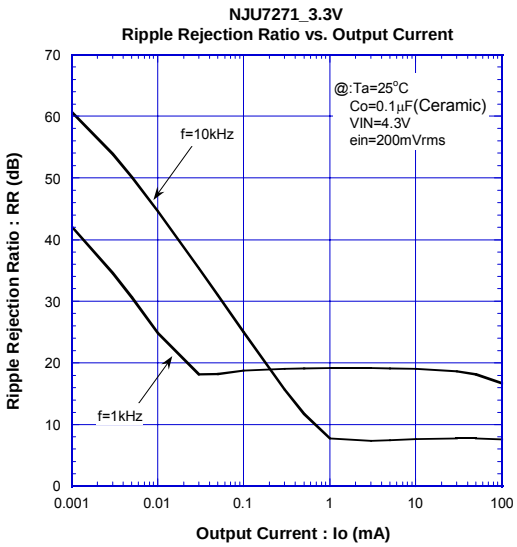
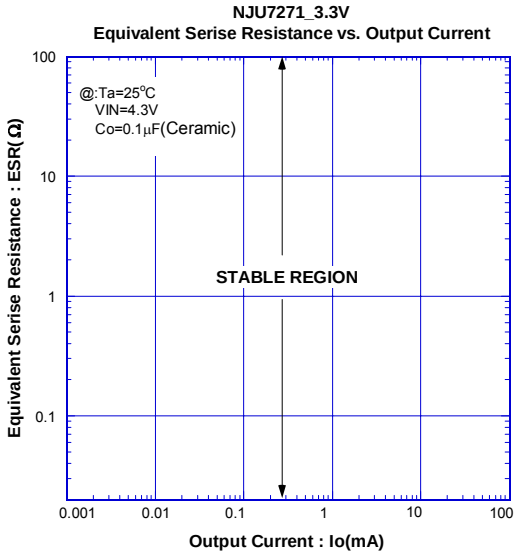


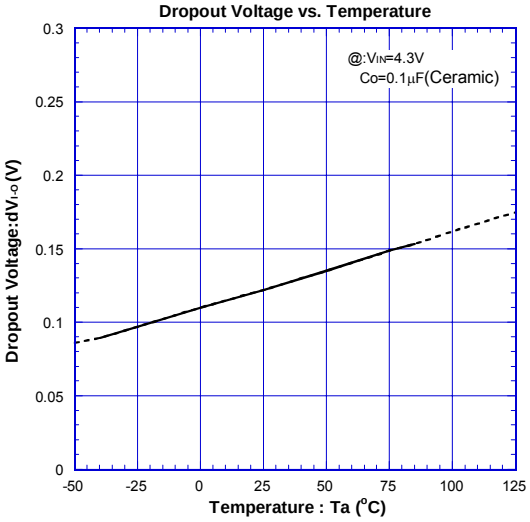




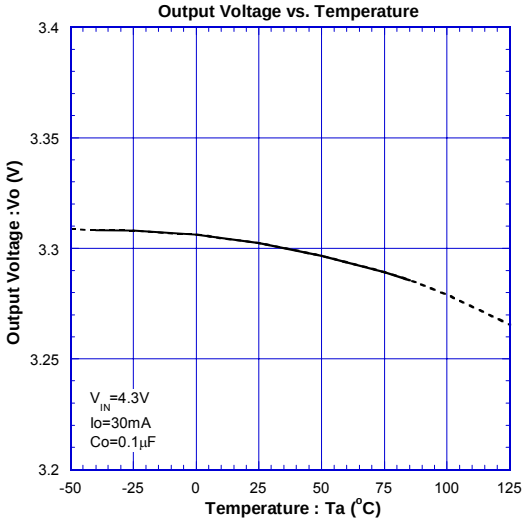


■ TYPICAL CHARACTERISTICS (LDO BLOCK)

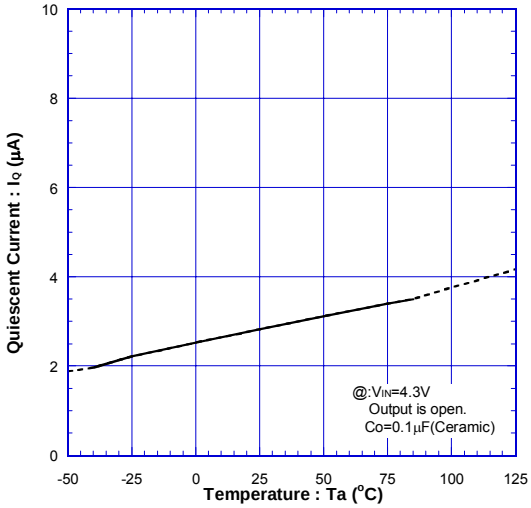
NJU7271_3.3V
Dropout Voltage vs. Temperature



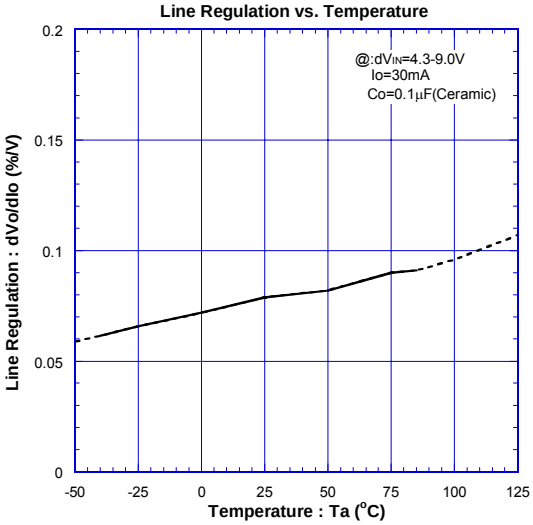
NJU7271_3.3V
Output Voltage vs. Temperature



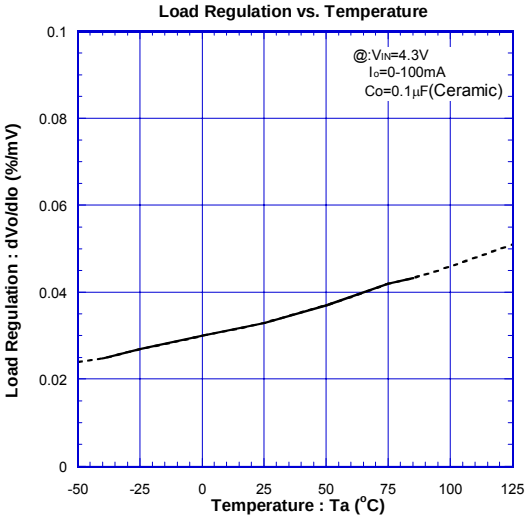
NJM7271_3.3V
Quiescent Current vs. Temperature



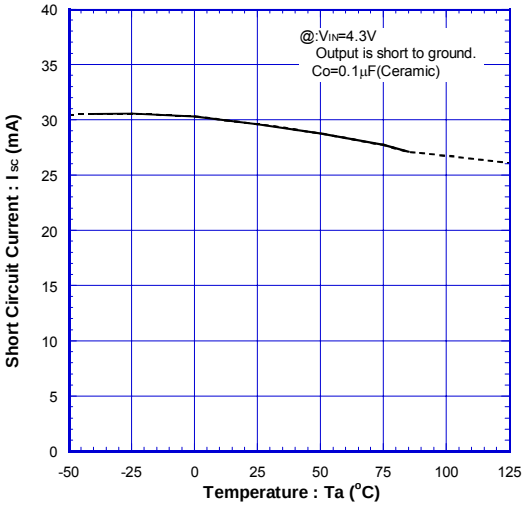
NJU7271_3.3V
Line Regulation vs. Temperature



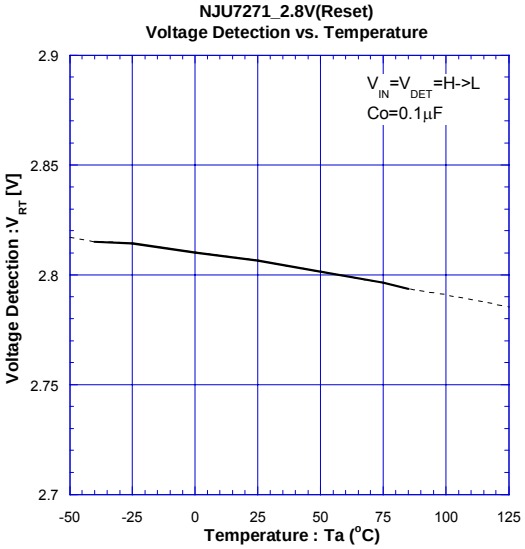
NJU7271_3.3V
Load Regulation vs. Temperature

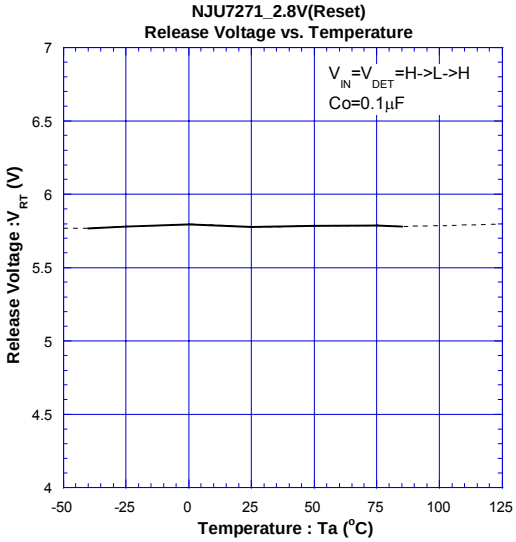


NJU7271_3.3V
Short Circuit Current vs. Temperature



■ TYPICAL CHARACTERISTICS (RESET BLOCK)





[CAUTION]
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