STEPPER MOTOR CONTROLLER

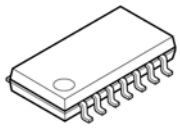
■ GENERAL DESCRIPTION

NJU7380 is a translator to convert the signal of the STEP&DIR input method into Phase signal.

It can control the stepping motor driver with STEP&DIR input signal to Phase input methods such as NJM3775, NJM3777.

NJU7380 is also including Auto Current Down(ACD) circuit witch is suitable for reducing power dissipation of power devices and motor.

■ PACKAGE OUTLINE

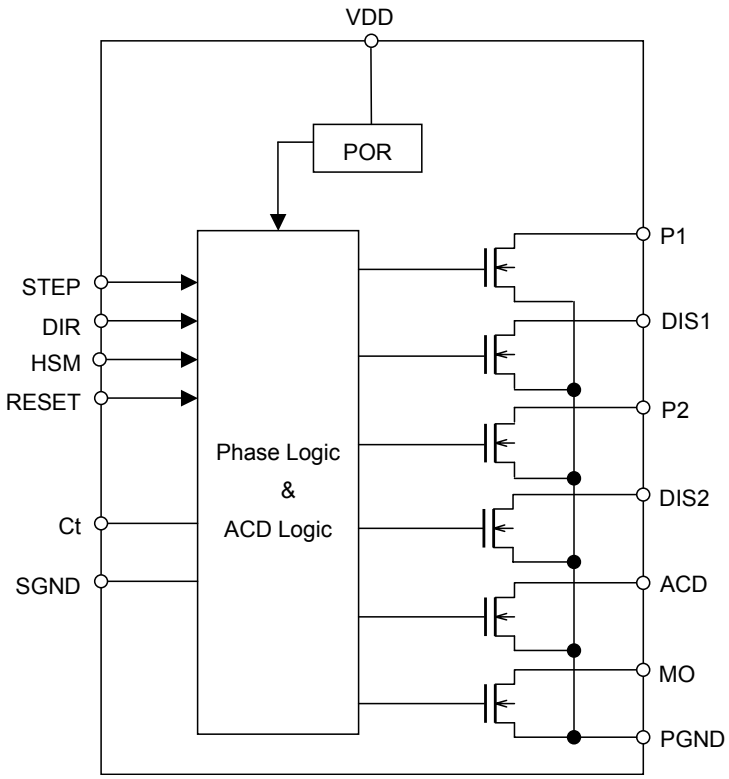


NJU7380M

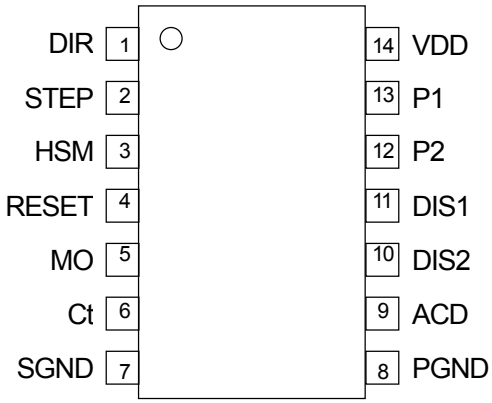
■ FEATURES

- Operating Voltage 4.75V to 5.25V
- Internal Phase Logic Circuit
- Phase Logic Reset Function (RESET)
- Motor Origin Monitor Function (MO)
- Half / Full Step Mode Select (HSM)
- Auto Current Down Function (ACD)
- Specially matched to NJM37XX series
- Package DMP14

■ BLOCK DIAGRAM



■ PIN CONNECTION



DMP14

■ PIN FUNCTION LIST

No.	Pin Name	Description
1	DIR	Direction command input for determining motor turning direction
2	STEP	Motor steeping pulse input, phase logic operation triggered by negative edge of STEP signal
3	HSM	Half / Full step mode select input "H" level in full step mode and "L" level in half step mode
4	RESET	Phase logic initial input
5	MO	Phase output initial status detection output
6	Ct	A value of connected capacitor determines lock detection time (t_{on}) and auto resume time (t_{OFF})
7	SGND	SGND (Logic GND) and PGND (Analog GND) is not connect in the IC
8	PGND	SGND and PGND pins should be connected ground respectively.
9	ACD	Auto Current Down output terminal L level in active
10	DIS2	Step sequence output terminals
11	DIS1	P1/DIS1(P2/DIS2) determine a sequence output on Phase1(2) for driver IC
12	P2	P1(P2) determine a motor current direction on Phase1(2) for driver IC
13	P1	DIS1(DIS2) determine a phase current OFF mode at the half-step
14	VDD	Logic power supply voltage terminal

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	V_{DD}	+7.0	V	
Input Voltage	V_{ID}	-0.3 ~ V_{DD}+0.3	V	
Output Current	I_O	10	mA	
Operating Temperature Range	T_{opr}	-40 ~ +85	ºC	
Storage Temperature Range	T_{stg}	-40 ~ +125	ºC	
Power Dissipation	P_D	300	mW	Device itself

■ RECOMMENDED OPERATING CONDITION

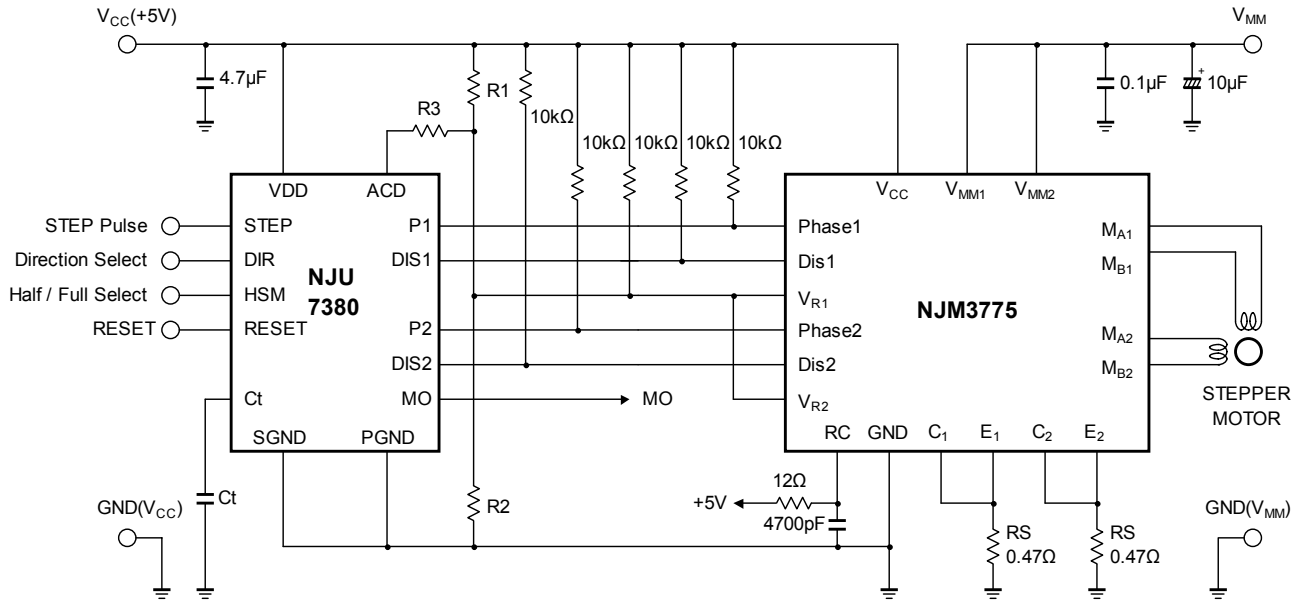
V_{DD}= 4.75V to 5.25V

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V, Ta=25ºC)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{DD}	No Signal	-	0.2	0.3	mA
H Level Input Voltage	V_{IH}	-	3.5	-	-	V
L Level Input Voltage	V_{IL}	-	-	-	1.5	V
H Level Input Current	I_{IH}	-	-	0.1	1.0	µA
L Level Input Current	I_{IL}	-	-	-50	-100	µA
Phase Output Saturation Voltage	V_P	I_P=5mA	-	-	0.5	V
DIS Output Saturation Voltage	V_{DIS}	I_{DIS}=5mA	-	-	0.5	V
ACD Output Saturation Voltage	V_{ACD}	I_{ACD}=5mA	-	-	0.5	V
MO Output Saturation Voltage	V_{MO}	I_{MO}=5mA	-	-	0.5	V
Output Leak Current	I_{LEAK}	V_{DD}=7V	-	-	1	µA
Auto Current Down ON Time	t_{ON}	C_T=0.068µF	-	200	-	ms
Turn ON Time	t_{dON}	R_L=1kΩ	-	0.1	-	µs
Set-up Time	t_S	-	400	-	-	ns
Step-pulse Continuation Time	t_p	-	800	-	-	ns

■ APPLACATION CIRCUIT



■ FUNCTION DESCRIPTION

NJU7380 is a controller for driver of 2-phase stepper motor.
It can control the stepping motor driver with STEP&DIR input signal to Phase input methods such as NJM3775, NJM3777.
NJU7380 is also including Auto Current Down(ACD) circuit witch is suitable for reducing power dissipation of power devices and motor.

■ LOGIC BLOCK

NJU7380 contains all phase logic necessary to control the motor in a proper way.
If any of the logic inputs are left open, the circuit will accept it as a HIGH level.
In order to make noise-proof nature into the maximum, it is necessary to connect an idle input terminal to V_{DD} level.

• STEP – Stepping pulse

The built-in phase logic sequencer counts up on every negative edge of the STEP signal (pulse).
In full step mode, the pulse turns the stepping motor at the basic step angle.
In half step mode, two pulses are required to turn the motor at the basic step angle.
The DIR (direction) signal and HSM (half/full mode) are latched to the STEP negative edge and must therefore be established before the start of the negative edge.

Note the setup time ts in Figure 1.

• DIR – Direction

The DIR signal determines the step direction.
The direction of the stepping motor depends on how the NJU7380 and the driver are connected to the motor.
Although DIR can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge.

• HSM – Half / Full step mode select

This signal determines whether the stepping motor turns at half step or full step mode.
The built-in phase logic is set to the half step mode when HSM is low level.
Although HSM can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge.

• RESET

A two-phase stepping motor repeats the same winding energizing sequence every angle that is a multiple of four of the basic step.
The phase logic sequence is repeated every four pulses in the full step mode and every eight pulses in the half step mode.
RESET forces to initialize the phase logic to sequence start mode.
When RESET is at L level, the phase logic is initialized and the energizing pattern of phase logic at sequence start is output.
At this time, the STEP input of phase logic will be ignored during the RESET is at L level.

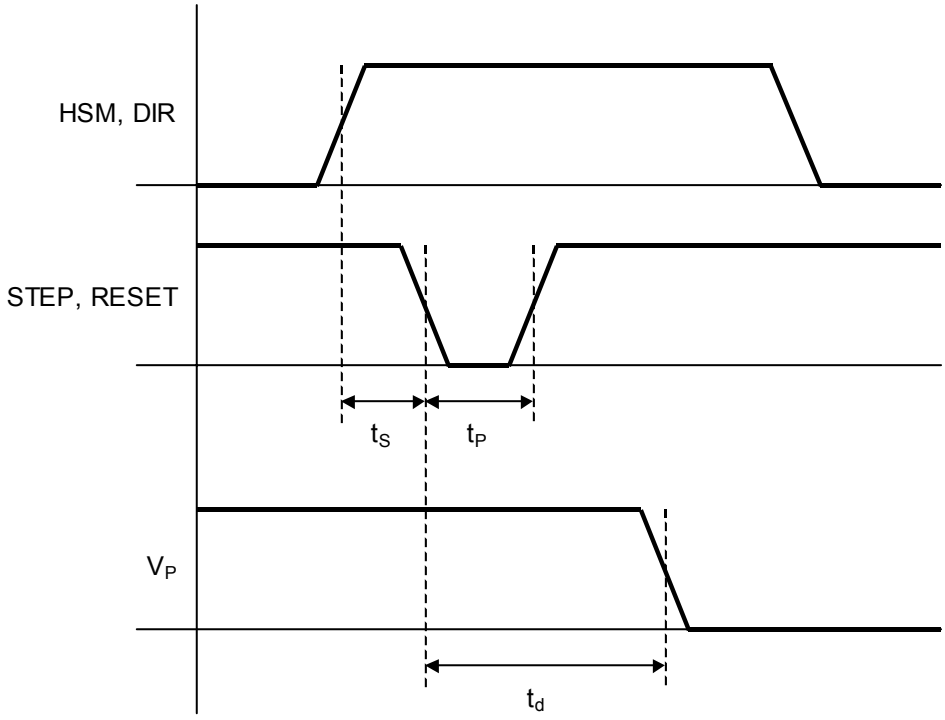


Fig 1 : Timing chart

• POR – Power on and reset function

The internal power-on and reset circuit, which is connected to V_{DD}, resets the phase logic and turns off phase output when the power is supplied to prevent missteps.
Each time the power is turned on, the energizing pattern of phase logic at sequence start is output.

• MO – Origin monitor

At sequence start of the phase logic or after POR or external RESET, an L level output is made to indicate to external devices that the energizing sequence is in initial status.
In a system using a stepping motor, the device sensor and the MO AND function enable a higher resolution detection of motor origin.

■ ACD – Auto Current Down function

The ACD monitors step signals and sets the ACD pin output to H when the negative edge of a STEP signal is input. It then sets the ACD output to L after a time (t_{ON}) that is fixed by the capacitor that is connected to the Ct pin.
By combining this pin with the VR pin that determines motor current for the motor, it is possible to reduce current when stopping the motor.
If the next negative edge of a STEP is input during the time t_{ON}, an internal retrigger will operate, maintaining the ACD pin's H output.
That is, after the final negative edge of a STEP is input, ACD H output is maintained during the time t_{ON}, after which it is set to L.
The time t_{ON} must be long enough to securely stop the stepping motor.
Approximately 100mS is usually sufficient for normal applications.
The following expression determines the time t_{ON}.

$$t_{ON}\ [ms] = 3 \times 10^9 \times Ct\ [F]$$

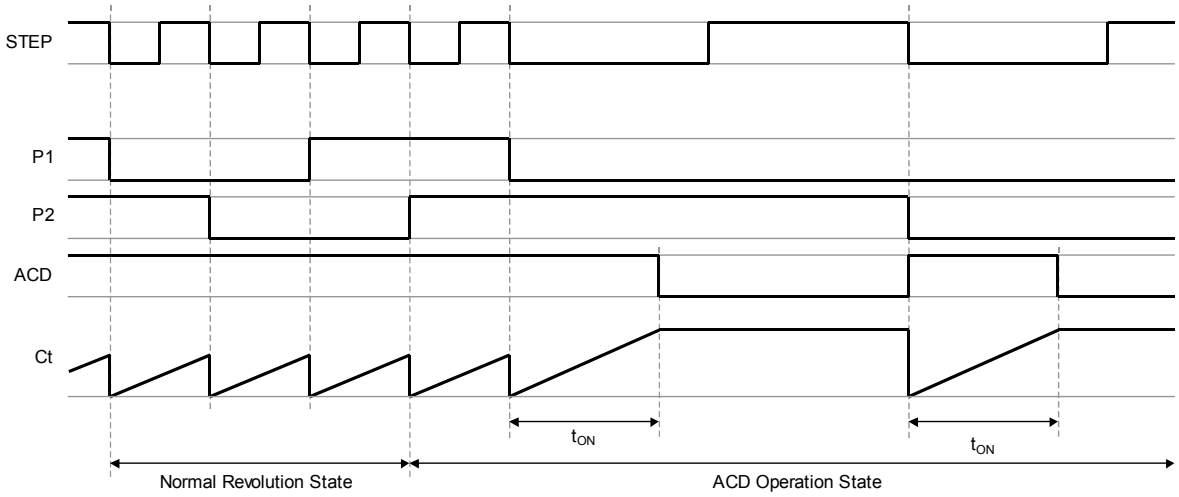
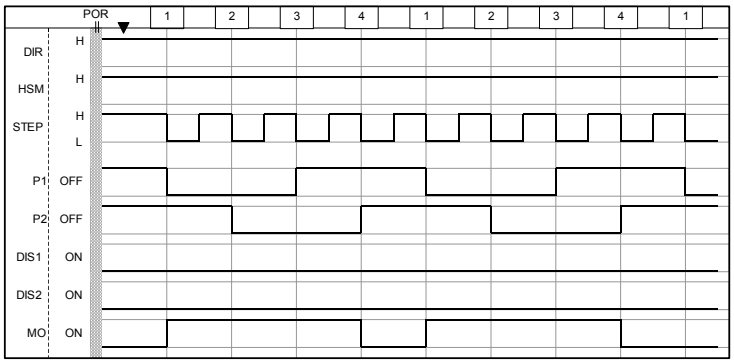


Fig2 : ACD Operation Timing Diagram

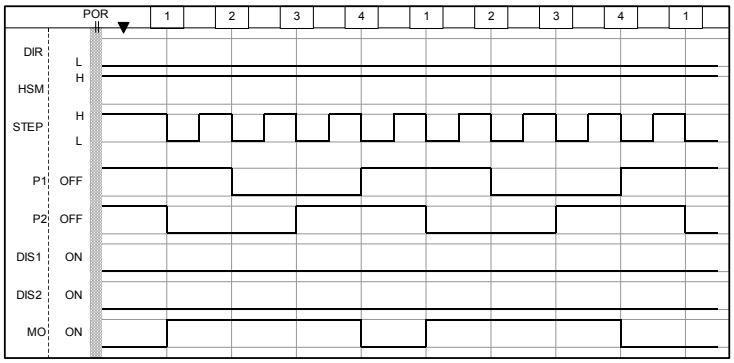
■ INPUT / OUTPUT SEQUENCE

It is timing chart of the input / output signal in each drive mode.
The state of the input / output signal after POR is shown in left side.

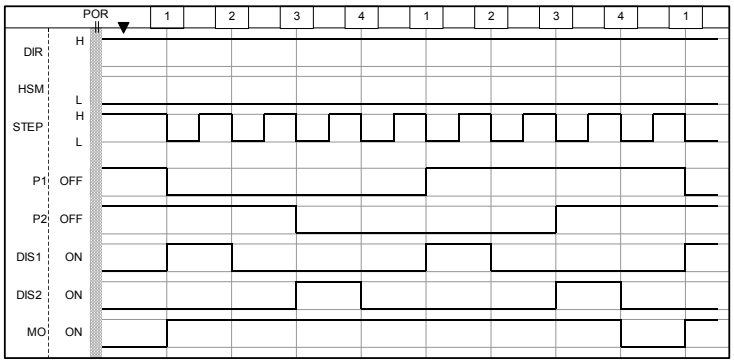
Full-step mode
Forward 4-step sequence



Full-step mode
Reverse 4-step sequence



Half-step mode
Forward 8-step sequence



Half-step mode
Reverse 8-step sequence