

## VOLTAGE DETECTOR

### ■ GENERAL DESCRIPTION

The NJU7704/05 is a low quiescent current voltage detector featuring high precision detection voltage.

The detection voltage is internally fixed with an accuracy of 1.0%.

The NJU7704/05 are useful for preventing malfunction of microcomputer or DSP etc. through detect a drop in voltage of battery or power supply.

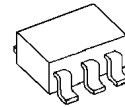
The delay function achieves set wait time when supply voltage is unstable. Moreover, the delay function can make a sequence that other devices in application work and stabilize before microcomputer or DSP works.

Delay time can be set by an external capacitor. Manual reset function can output reset signal irrespective of detection voltage.

NJU7704 is Nch. Open Drain and NJU7705 is a C-MOS output type.

Small packaging makes NJU7704 and NJU7705 suitable for space conscious applications.

### ■ PACKAGE OUTLINE



NJU7704/05F

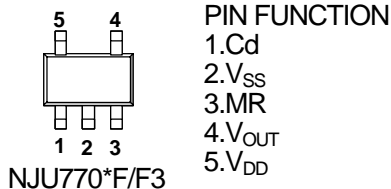


NJU7704/05F3

### ■ FEATURES

- High Precision Detection Voltage     $\pm 1.0\%$
- Low Quiescent Current                 $0.9\mu\text{A typ.}$
- Detection Voltage Range             $1.5\sim 6.0\text{V}(0.1\text{V Step})$
- Adjustable delay time with external capacitor
- Manual Reset                         Active "L" : NJU770\*\*\*\*A  
Active "H" : NJU770\*\*\*\*B
- Output Configuration                NJU7704: Nch. Open Drain type  
NJU7705: C-MOS Output type
- Package Outline                        SOT-23-5: NJU770\*F  
SC88A : NJU770\*F3

### ■ PIN CONFIGURATION

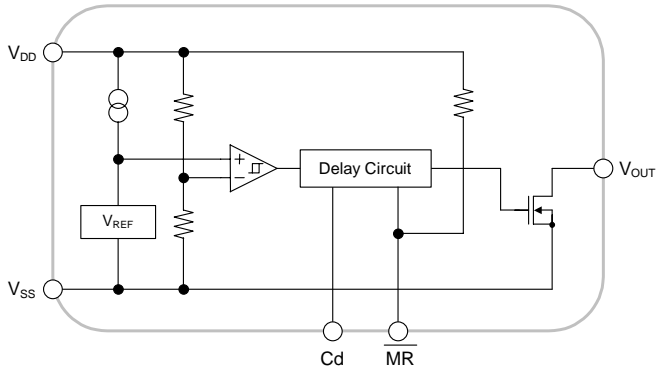


#### PIN FUNCTION

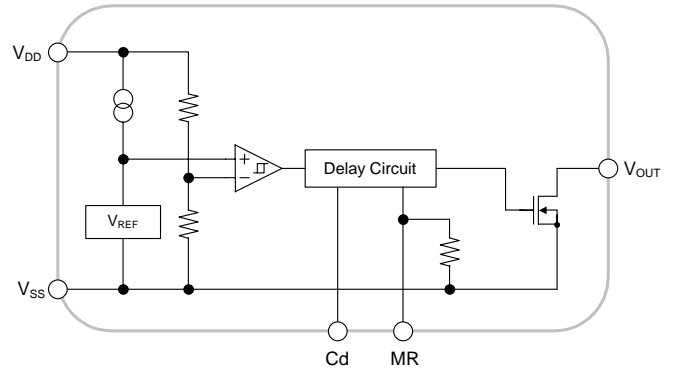
- 1.Cd
- 2.V<sub>SS</sub>
- 3.MR
- 4.V<sub>OUT</sub>
- 5.V<sub>DD</sub>

# NJU7704/05

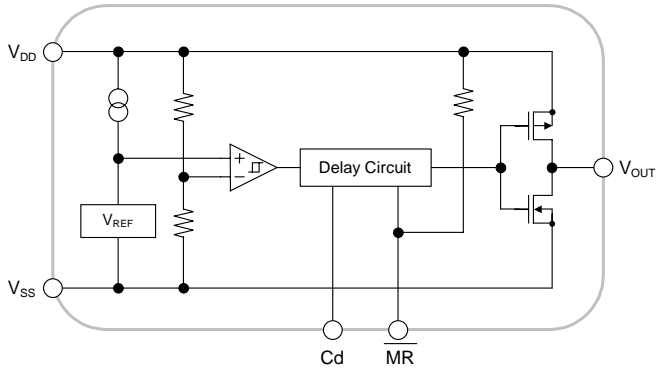
## ■ EQUIVALENT CIRCUIT



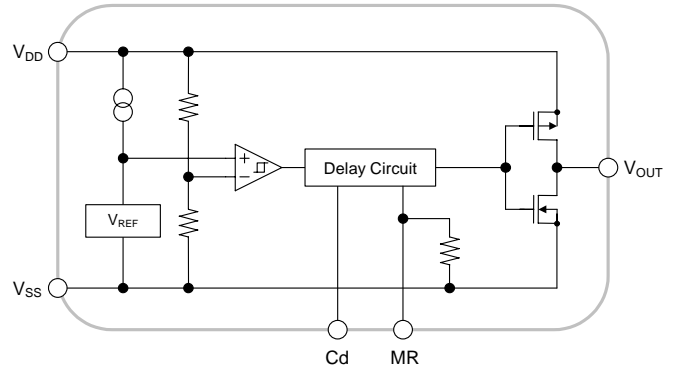
NJU7704\*\*\*A



NJU7704F\*\*B



NJU7705\*\*\*A



NJU7705\*\*\*B

■ DETECTION VOLTAGE RANK LIST

Device Name	V <sub>DET</sub>	MR Logic
NJU770*F3-/F15A	1.5V	Active "L"
NJU770*F3-/F19A	1.9V	
NJU770*F3-/F02A	2.0V	
NJU770*F3-/F21A	2.1V	
NJU770*F3-/F22A	2.2V	
NJU770*F3-/F23A	2.3V	
NJU770*F3-/F25A	2.5V	
NJU770*F3-/F27A	2.7V	
NJU770*F3-/F28A	2.8V	
NJU770*F3-/F29A	2.9V	
NJU770*F3-/F03A	3.0V	
NJU770*F3-/F32A	3.2V	
NJU770*F3-/F39A	3.9V	
NJU770*F3-/F42A	4.2V	
NJU770*F3-/F43A	4.3V	
NJU770*F3-/F44A	4.4V	
NJU770*F3-/F45A	4.5V	
NJU770*F3-/F48A	4.8V	
NJU770*F3-/F06A	6.0V	
NJU770*F3-/F19B	1.9V	Active "H"
NJU770*F3-/F27B	2.7V	
NJU770*F3-/F28B	2.8V	
NJU770*F3-/F03B	3.0V	
NJU770*F3-/F42B	4.2V	

# NJU7704/05

## ■ NJU7704

### ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	
Input Voltage	V <sub>DD</sub>	+10	V	
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.3~+10	V	
Input Voltage of Cd pin	V <sub>Cd</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V	
Input Voltage of MR pin	V <sub>MR</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V	
Output Current	I <sub>OUT</sub>	50	mA	
Power Dissipation	P <sub>D</sub>	SOT-23-5	350(*1)	mW
			200(*2)	
		SC88A	250(*1)	
Operating Temperature	Topr	-40 ~ +85	°C	
Storage Temperature	Tstg	-40 ~ +125	°C	

(\*1) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(\*2) : Device itself

### ■ ELECTRICAL CHARACTERISTICS

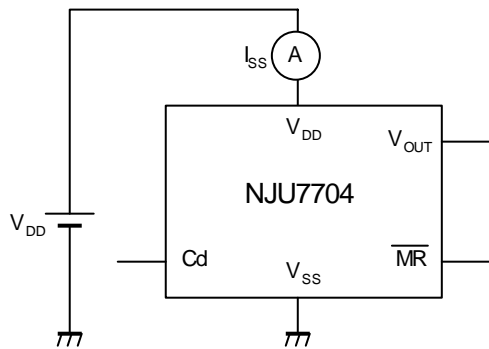
(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Detection Voltage	V <sub>DET</sub>		-1.0%	-	+1.0%	V	
Hysteresis Voltage	V <sub>HYS</sub>		70	90	130	mV	
Quiescent Current	I <sub>SS</sub>	V <sub>DD</sub> =V <sub>DET</sub> +1V	V <sub>DET</sub> =1.5V~1.9V Version	-	0.7	1.5	μA
			V <sub>DET</sub> =2.0V~6.0V Version	-	0.9	2.0	
Output Current	I <sub>OUT</sub>	Nch, V <sub>DS</sub> =0.5V	V <sub>DD</sub> =1.2V	0.75	2.0	-	mA
			V <sub>DD</sub> =2.4V (≥2.7V Version)	4.5	7.0	-	
Output Leak Current	I <sub>LEAK</sub>	V <sub>DD</sub> =V <sub>OUT</sub> =9V	-	-	0.1	μA	
Detection Voltage Temperature Coefficient	ΔV <sub>DET</sub> /ΔTa	Ta=0~+85°C	-	±100	-	ppm/°C	
Delay Time	t <sub>d</sub>	V <sub>DD</sub> =V <sub>DET</sub> +1V, Cd=4.7nF	8	10	12	ms	
Input Voltage of MR pin (Active "L")	V <sub>MR_H</sub>		1.5	-	V <sub>DD</sub>	V	
	V <sub>MR_L</sub>		0	-	0.3		
Input Voltage of MR pin (Active "H")	V <sub>MR_H</sub>		V <sub>DD</sub> -0.3	-	V <sub>DD</sub>	V	
	V <sub>MR_L</sub>		0	-	V <sub>DD</sub> -1.5		
Impedance of MR pin	R <sub>MR</sub>		1.0	2.0	3.0	MΩ	
Operating Voltage (*3)	V <sub>DD</sub>	R <sub>L</sub> =100kΩ	0.8	-	9	V	

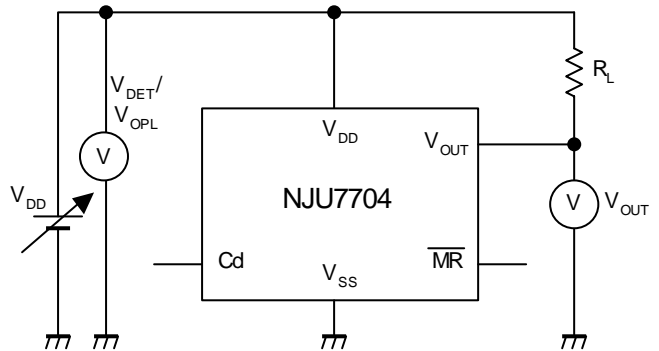
(\*3): The minimum operating voltage(V<sub>OPL</sub>) indicates the same value of the input voltage(V<sub>DD</sub>) on condition that V<sub>OUT</sub> becomes 10% or less of the input voltage(V<sub>DD</sub>).

## ■ TEST CIRCUIT

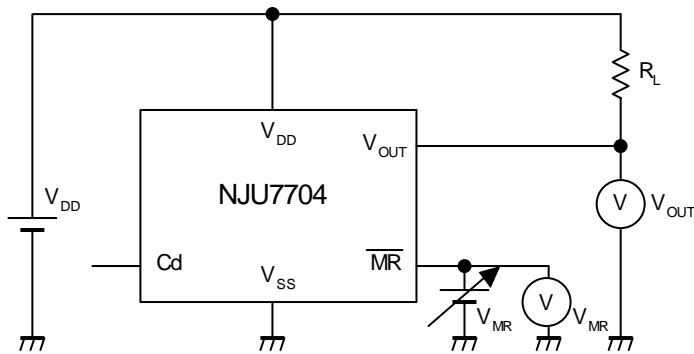
### ● Circuit Operating Current TEST CIRCUIT



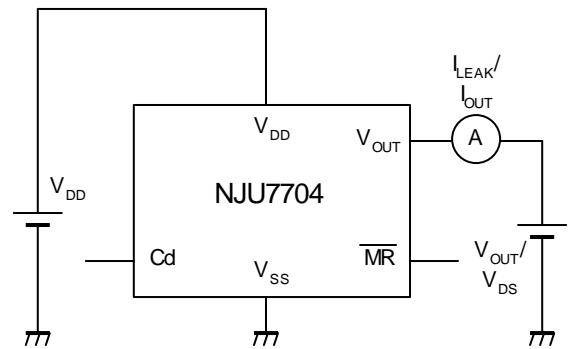
### ● Detection voltage/Minimum operating voltage



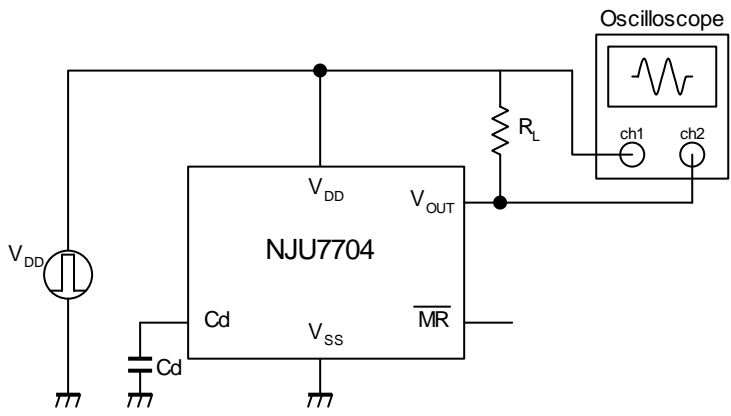
### ● MR pin Input voltage TEST CIRCUIT



### ● Leak current / Output current TEST CIRCUIT



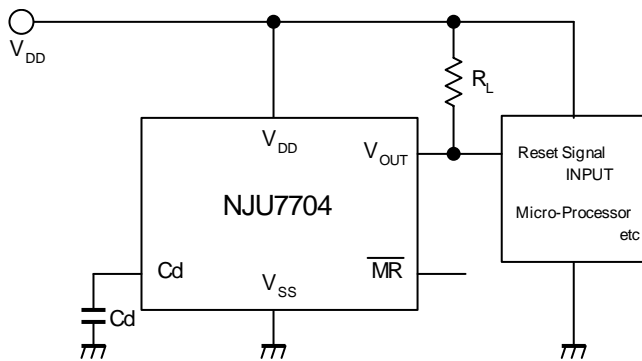
### ● Delay time TEST CIRCUIT



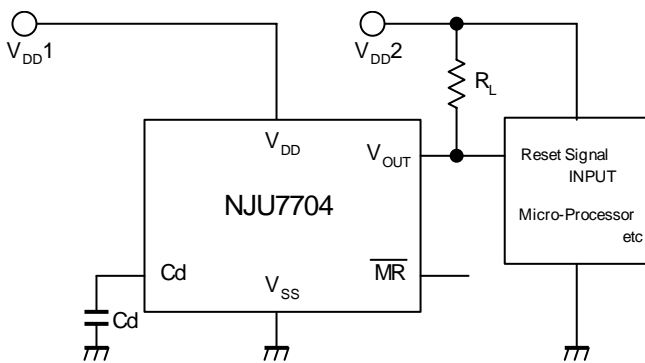
# NJU7704/05

## ■ TYPICAL APPLICATION

### ① Power Supply Monitor Circuit ( $V_{DD}$ line COMMON)



### ② Power Supply Monitor Circuit ( $V_{DD}$ line SEPARATE)



■ NJU7705

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	
Input Voltage	V <sub>DD</sub>	+10	V	
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.3~+10	V	
Input Voltage of Cd pin	V <sub>Cd</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V	
Input Voltage of MR pin	V <sub>MR</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V	
Output Current	I <sub>OUT</sub>	50	mA	
Power Dissipation	P <sub>D</sub>	SOT-23-5	350(*4)	mW
			200(*5)	
		SC88A	250(*4)	
Operating Temperature	Topr	-40~+85	°C	
Storage Temperature	Tstg	-40~+125	°C	

(\*4) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(\*5) : Device itself

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

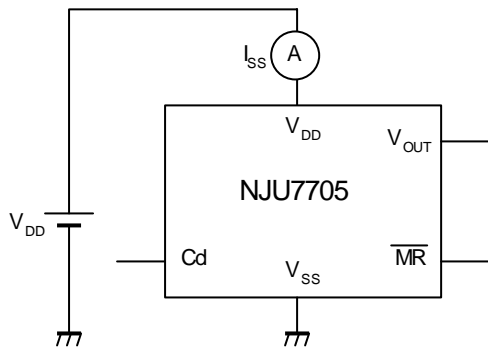
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Detection Voltage	V <sub>DET</sub>		-1.0%	-	+1.0%	V	
Hysteresis Voltage	V <sub>HYS</sub>		70	90	130	mV	
Quiescent Current	I <sub>SS</sub>	V <sub>DD</sub> =V <sub>DET</sub> +1V	V <sub>DET</sub> =1.5V~2.9V Version	-	0.7	1.5	μA
			V <sub>DET</sub> =2.6V~6.0V Version	-	0.9	2.0	
Output Current	I <sub>OUT</sub>	Nch, V <sub>DS</sub> =0.5V	V <sub>DD</sub> =1.2V	0.75	2.0	-	mA
			V <sub>DD</sub> =2.4V (≥2.7V Version)	4.5	7.0	-	
		Pch, V <sub>DS</sub> =0.5V	V <sub>DD</sub> =4.8V (≤3.9V Version)	2.0	3.5	-	
			V <sub>DD</sub> =6.0V (4.0~5.6V Version)	2.5	4.0	-	
			V <sub>DD</sub> =8.4V (≥5.7V Version)	3.0	5.0	-	
Detection Voltage Temperature Coefficient	Δ V <sub>DET</sub> / ΔTa	Ta=0~+85°C	-	±100	-	ppm/°C	
Delay Time	t <sub>d</sub>	V <sub>DD</sub> =V <sub>DET</sub> +1V, Cd=4.7nF	8	10	12	ms	
Input Voltage of MR pin (Active "L")	V <sub>MR_H</sub>		1.5	-	V <sub>DD</sub>	V	
	V <sub>MR_L</sub>		0	-	0.3		
Input Voltage of MR pin (Active "H")	V <sub>MR_H</sub>		V <sub>DD</sub> -0.3	-	V <sub>DD</sub>	V	
	V <sub>MR_L</sub>		0	-	V <sub>DD</sub> -1.5		
Impedance of MR pin	R <sub>MR</sub>		1.0	2.0	3.0	MΩ	
Operating Voltage (*6)	V <sub>DD</sub>	R <sub>L</sub> =100kΩ	0.8	-	9	V	

(\*6): The minimum operating voltage(V<sub>OPL</sub>) indicates the same value of the input voltage(V<sub>DD</sub>) on condition that V<sub>OUT</sub> becomes 10% or less of the input voltage(V<sub>DD</sub>).

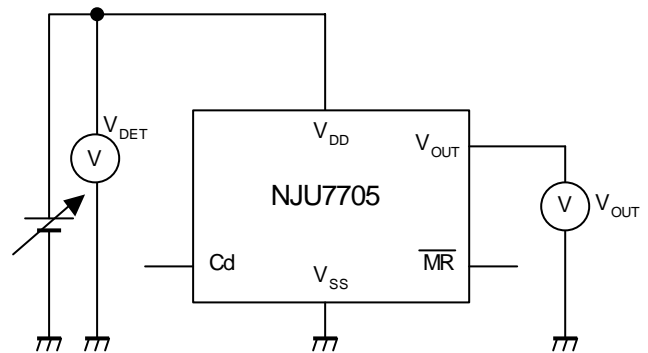
# NJU7704/05

## TEST CIRCUIT

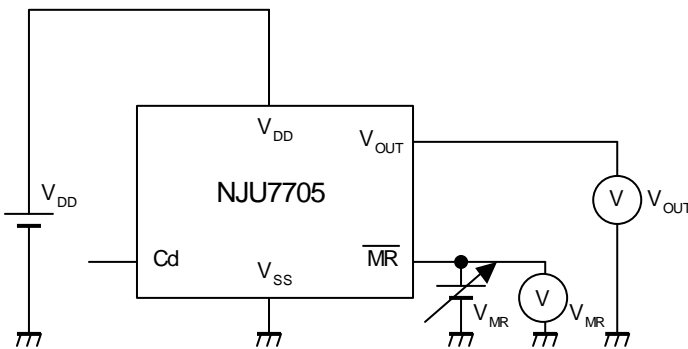
● Circuit Operating Current TEST CIRCUIT



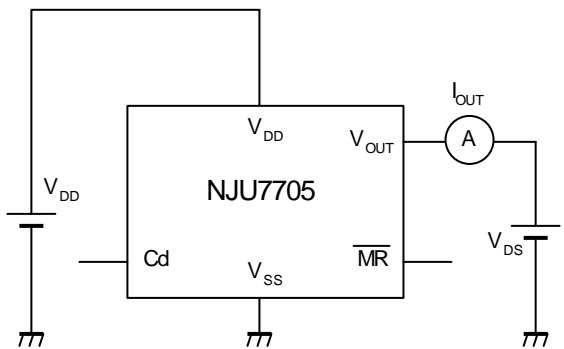
● Detection voltage TEST CIRCUIT



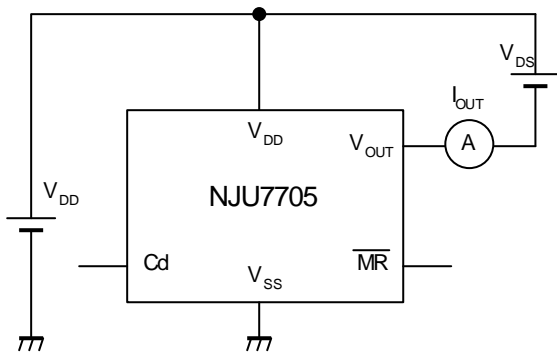
● MR pin Input voltage TEST CIRCUIT



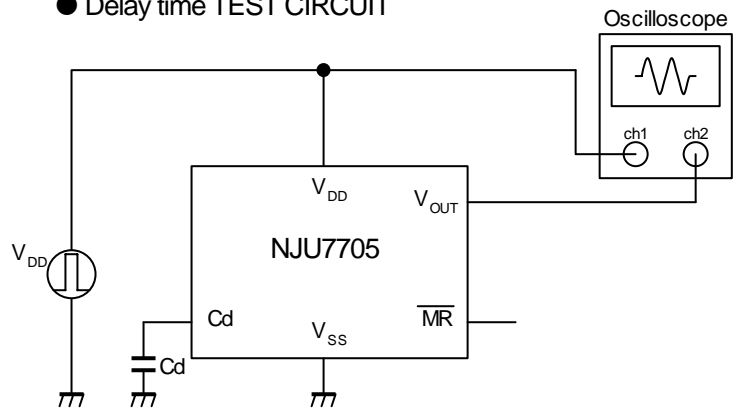
● Nch Output current TEST CIRCUIT



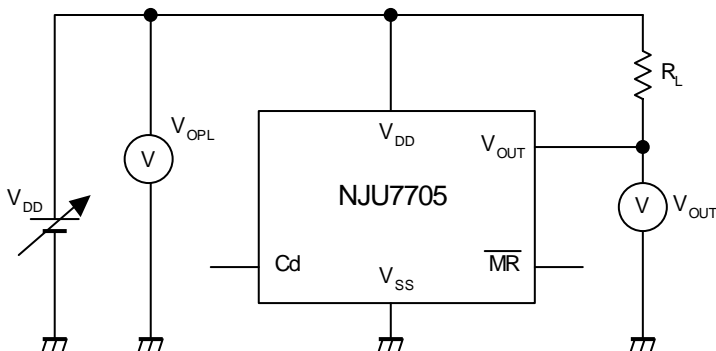
● Pch Output current TEST CIRCUIT



● Delay time TEST CIRCUIT



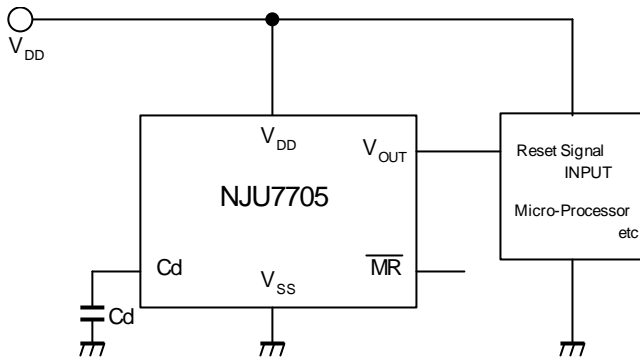
● Minimum operating voltage TEST CIRCUIT





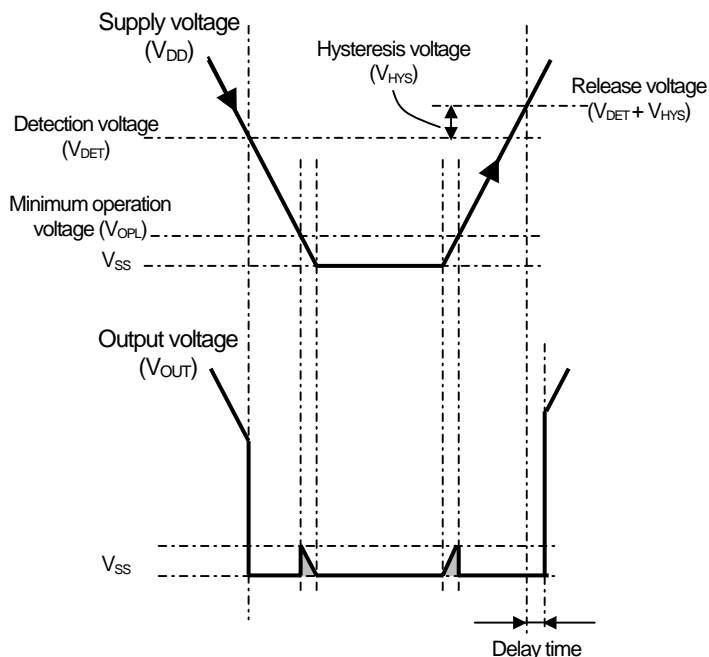
## ■ TYPICAL APPLICATION

### ① Power Supply Monitor Circuit ( $V_{DD}$ line COMMON)



## FUNCTIONAL DESCRIPTION

### (1) Basic Operation



- (1) When supply voltage ( $V_{DD}$ ) drops below detection voltage ( $V_{DET}$ ), Output voltage ( $V_{OUT}$ ) changes "H" to "L" to alert reset state.
- (2) The reset state is kept while  $V_{DD}$  is lower than release voltage. The release voltage is a sum of  $V_{DET}$  and Hysteresis voltage ( $V_{HYS}$ ). Please refer to the (\*7) below.
- (3) When  $V_{DD}$  becomes higher than the release voltage and reset release delay time set by the external capacitors is past, then  $V_{OUT}$  changes from "L" to "H" to resume normal state.

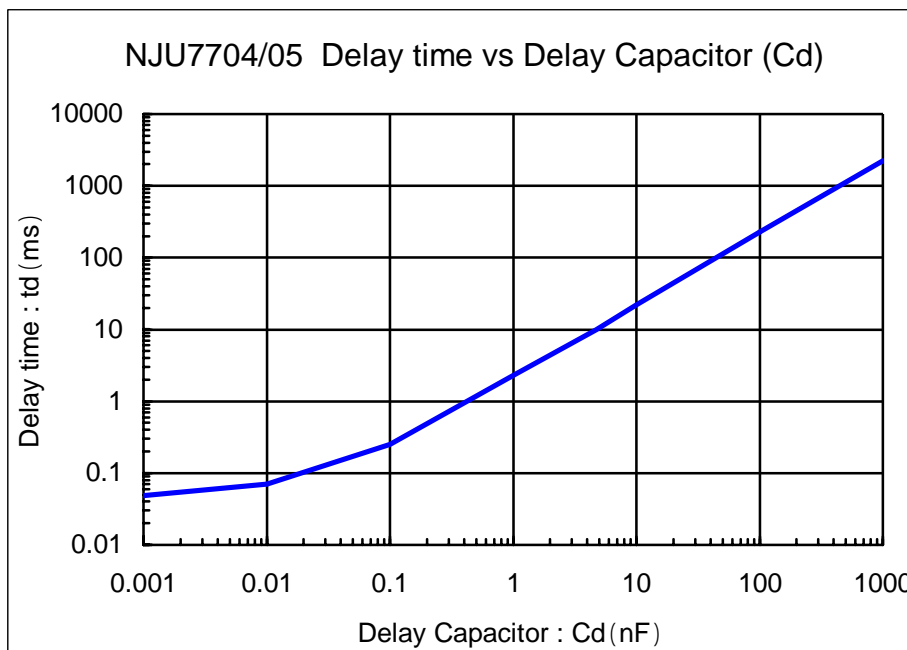
(\*7)  $V_{HYS}$  is to avoid unstable  $V_{OUT}$  state caused by rapid voltage change at nearby  $V_{DET}$ .

(\*8): C-MOS output product (NJU7705) : When  $V_{DD}$  less than  $V_{OPL}$ ,  $V_{OUT}$  is free of the shaded region.

### (2) Description of Delay Time

Delay time can be set by the external capacitor. The delay time is given by the following:

$$\text{External delay capacitor (nF)} = \text{Required delay time : } t_d(\text{ms}) / 10(\text{ms}) \times 4.7(\text{nF})$$



(3) Description of Manual Reset

Reset signal can output independently with MR.

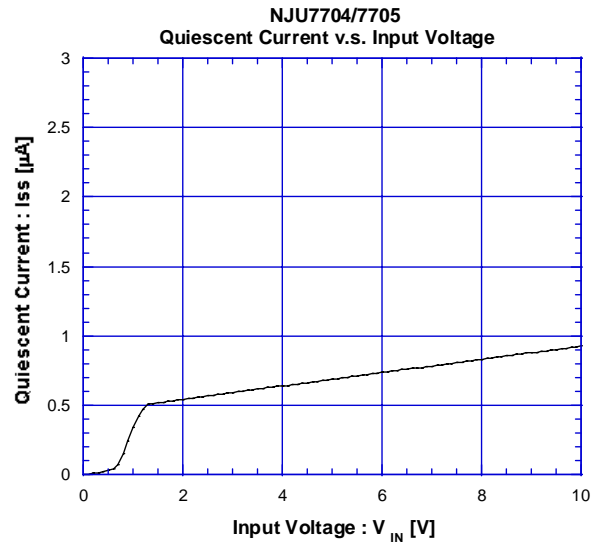
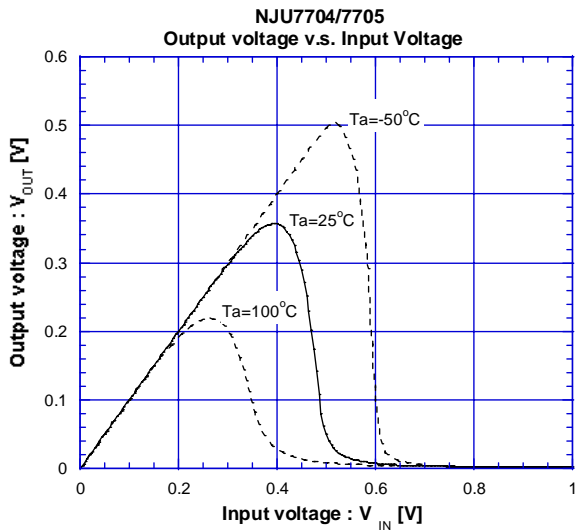
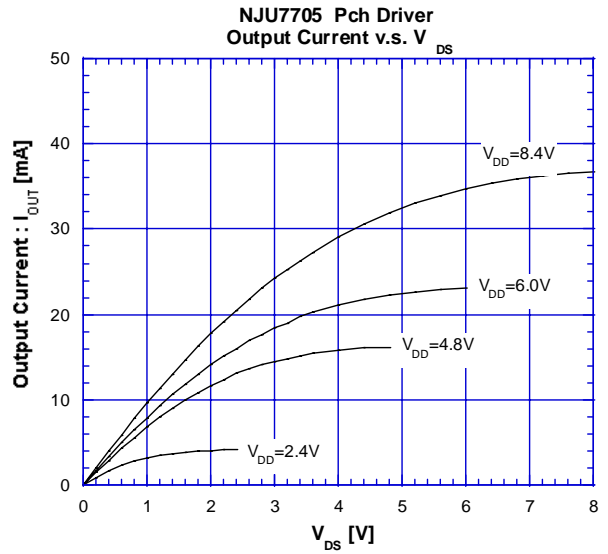
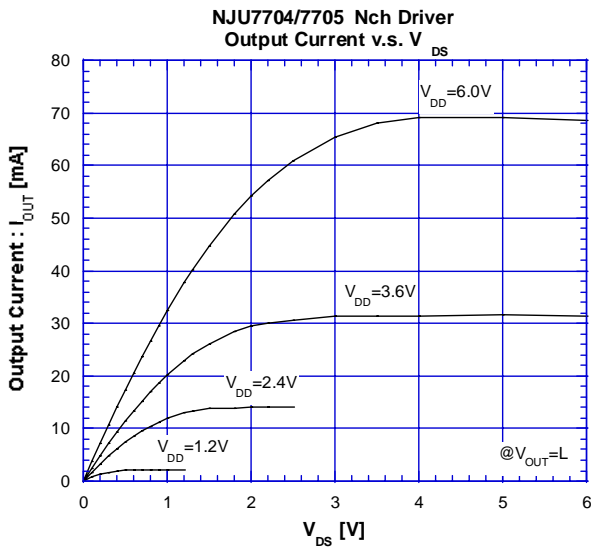
Logic of MR	Operation
Active "L"	$V_{MR} = "L" \Rightarrow$ Reset "ON"
Active "H"	$V_{MR} = "H" \Rightarrow$ Reset "ON"

If Manual Reset is not required, please connect MR terminal as following.

Logic of MR	Connection
Active "L"	Connect MR terminal to $V_{DD}$ or open
Active "H"	Connect MR terminal to GND or open

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## ■ TYPICAL CHARACTERISTICS



**[CAUTION]**

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