VOLTAGE DETECTOR

■ GENERAL DESCRIPTION

The NJU7706/07 is a high precision voltage detector with a built-in delay time generator of fixed time.

The NJU7706/07 is useful for preventing malfunction of microprocessor or DSP through monitoring power supply voltage.

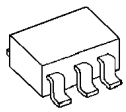
The delay function achieves set wait time when supply voltage is unstable. Moreover, the delay function can make a sequence that other devices in application work and stabilize before microcomputer or DSP works.

The detection voltage is internally fixed with an accuracy of 1.0%, and three fixed delay times 50ms, 100ms and 200ms are available. Manual reset function can output reset signal irrespective of detection voltage.

NJU7706 is Nch. Open Drain and NJU7707 is a C-MOS output type.

Small packaging makes NJU7706 and NJU7707 suitable for space conscious applications.

■ PACKAGE OUTLINE

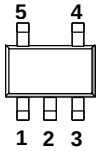


NJU7706/07F

■ FEATURES

● High Precision Detection Voltage	±1.0%
● Low Quiescent Current	1.3μA typ.
● Detection Voltage Range	1.5 ~ 6.0V(0.1V step)
● Delay Time(Built-in Fixed Type)	50ms /100ms /200ms(Built-in Fixed Type)
● ON/OFF switch of delay time(DSW pin)	
● Manual Reset	Active “L” : NJU770*F**A
	Active "H" : NJU770*F**B
● Output Configuration	NJU7706: Nch. Open Drain type
	NJU7707: C-MOS Output type
● Package Outline	SOT-23-5

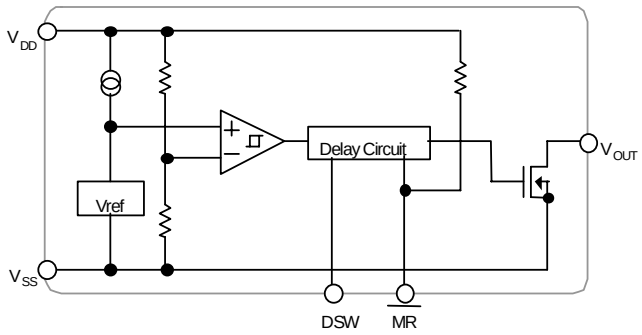
■ PIN CONFIGURATION



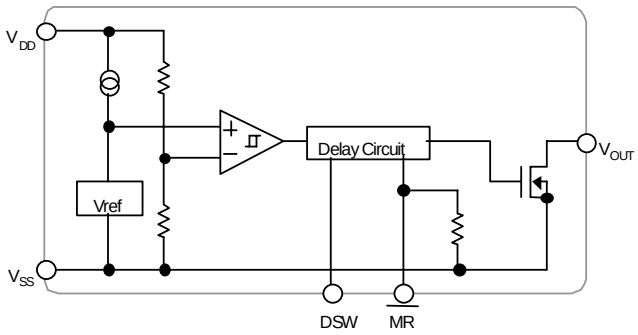
NJU7706/07F

PIN FUNCTION
1.DSW
2.V_{SS}
3.MR
4.V_{OUT}
5.V_{DD}

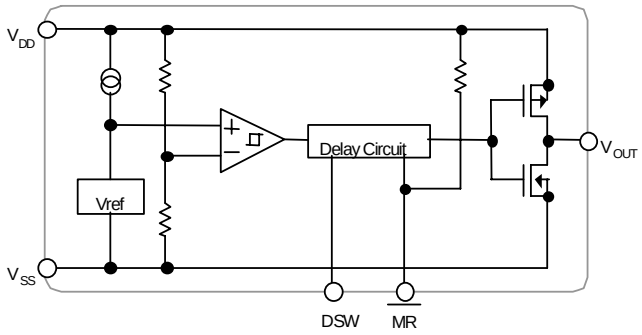
■ EQUIVALENT CIRCUIT



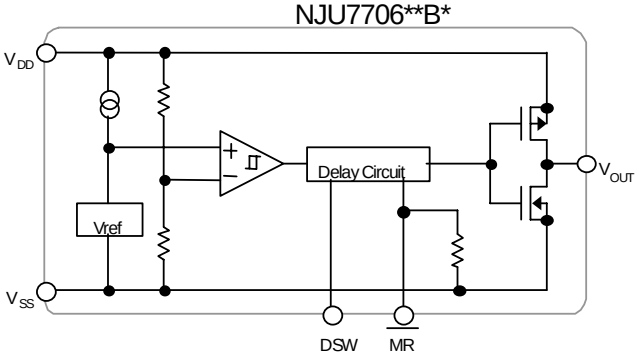
NJU7706**A*



NJU7706**B*



NJU7707**A*



NJU7707**B*

■ DETECTION VOLTAGE RANK LIST

Device Name	V_{DET}	MR Logic	Delay Time
NJU770*F25A1	2.5V	Active “L”	50ms
NJU770*F26A1	2.6V		
NJU770*F27A1	2.7V		
NJU770*F28A1	2.8V		
NJU770*F29A1	2.9V		
NJU770*F03A1	3.0V		
NJU770*F39A1	3.9V		
NJU770*F42A1	4.2V		
NJU770*F27B1	2.7V	Active “H”	
NJU770*F15A2	1.5V	Active “L”	100ms
NJU770*F18A2	1.8V		
NJU770*F19A2	1.9V		
NJU770*F21A2	2.1V		
NJU770*F22A2	2.2V		
NJU770*F25A2	2.5V		
NJU770*F27A2	2.7V		
NJU770*F28A2	2.8V		
NJU770*F29A2	2.9V		
NJU770*F03A2	3.0V		
NJU770*F31A2	3.1V		
NJU770*F39A2	3.9V		
NJU770*F04A2	4.0V		
NJU770*F42A2	4.2V		
NJU770*F43A2	4.3V		
NJU770*F45A2	4.5V		
NJU770*F46A2	4.6V		
NJU770*F06A2	6.0V		
NJU770*F25B2	2.5V	Active “H”	
NJU770*F27B2	2.7V		
NJU770*F42B2	4.2V		
NJU770*F27A3	2.7V	Active “L”	200ms
NJU770*F39A3	3.9V		
NJU770*F42A3	4.2V		
NJU770*F27B3	2.7V	Active “H”	

■ NJU7706

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS		UNIT
Input Voltage	V_{DD}	+10		V
Output Voltage	V_{OUT}	V_{SS}-0.3 ~ +10		V
Input Voltage of DSW pin	V_{DSW}	V_{SS}-0.3~V_{DD}+0.3		V
Input Voltage of MR pin	V_{MR}	V_{SS}-0.3~V_{DD}+0.3		V
Output Current	I_{OUT}	50		mA
Power Dissipation	P_D	SOT-23-5	350(*1)	mW
			200(*2)	
Operating Temperature	Topr	-40 ~ +85		°C
Storage Temperature	Tstg	-40 ~ +125		°C

(*1) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(*2) : Device itself

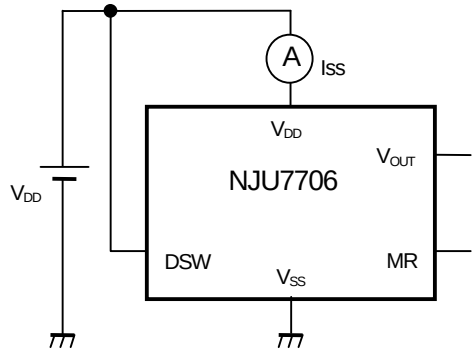
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Detection Voltage	V_{DET}			-1.0%	–	+1.0%	V
Hysteresis Voltage	V_{HYS}			70	90	130	mV
Quiescent Current	I_{SS}	V_{DD}=V_{DET}+1V	V_{DET}=1.5V ~ 1.9V Version	–	1.0	1.7	µA
			V_{DET}=2.0V ~ 6.0V Version	–	1.3	2.2	
Output Current	I_{OUT}	Nch,V_{DS}=0.5V	V_{DD}=1.2V	0.75	2.0	–	mA
			V_{DD}=2.4V (≥2.7V Version)	4.5	7.0	–	
Output Leak Current	I_{LEAK}	V_{DD}=V_{OUT}=9V		–	–	0.1	µA
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/\Delta Ta$	Ta=0 ~ +85°C		–	±100	–	ppm/°C
Delay Time 1	t_{d1}	V_{DD}=V_{DET}+1V, DSW="L Level"	NJU7706F***1	42.5	50	57.5	ms
			NJU7706F***2	85	100	115	ms
			NJU7706F***3	170	200	230	ms
Delay Time 2	t_{d2}	V_{DD}=V_{DET}+1V, DSW="H Level"		25	100	300	µs
Input Voltage of DSW pin	V_{DSW_H}			1.5	–	V_{DD}	V
	V_{DSW_L}			0	–	0.3	V
Input Voltage of MR pin (Active "L")	V_{MR_H}			1.5	–	V_{DD}	V
	V_{MR_L}			0	–	0.3	V
Input Voltage of MR pin (Active "H")	V_{MR_H}			V_{DD}-0.3	–	V_{DD}	V
	V_{MR_L}			0	–	V_{DD}-1.5	V
Impedance of MR pin	R_{MR}			1.0	2.0	3.0	MΩ
Operating Voltage (*3)	V_{DD}	R_L=100kΩ		0.8	–	9	V

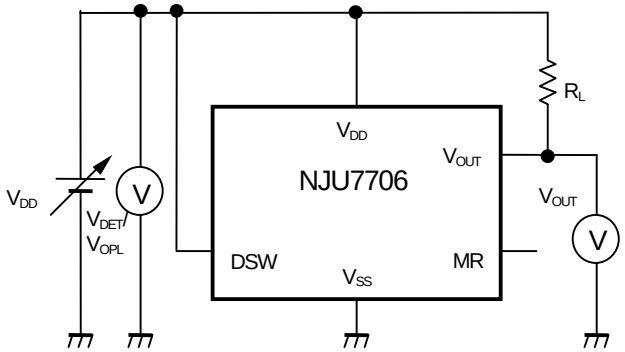
(*3): The minimum operating voltage(V_{OPL}) indicates the same value of the input voltage(V_{DD}) on condition that V_{OUT} becomes 10% or less of the input voltage(V_{DD}).

■ TEST CIRCUIT

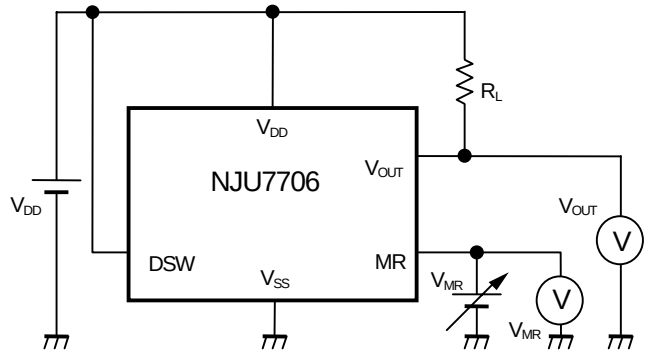
● Circuit Operating Current TEST CIRCUIT



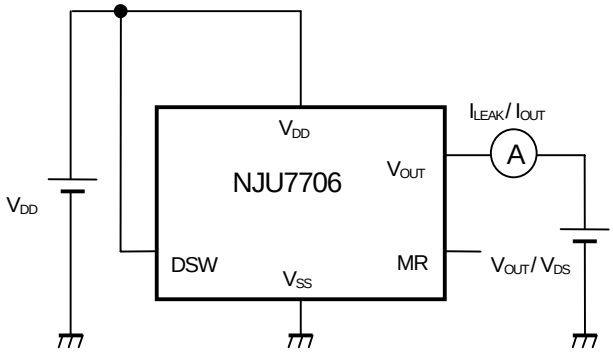
● Detection voltage / Minimum operating voltage TEST CIRCUIT



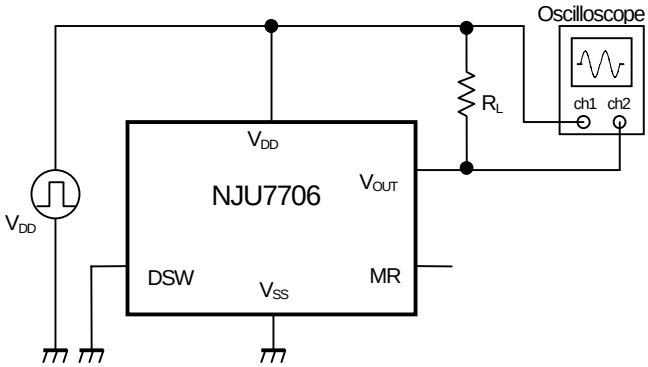
● MR pin Input voltage TEST CIRCUIT



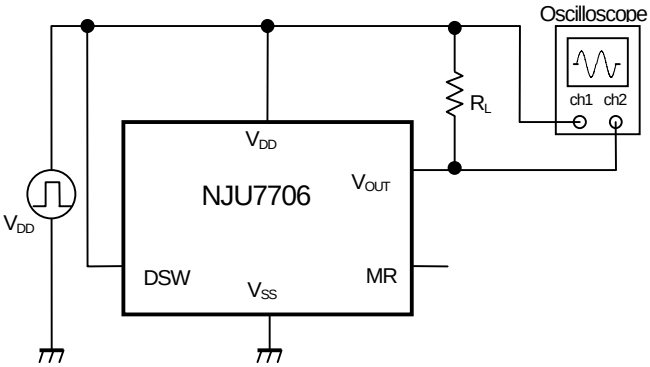
● Leak current / Output current TEST CIRCUIT



● Delay time1 TEST CIRCUIT

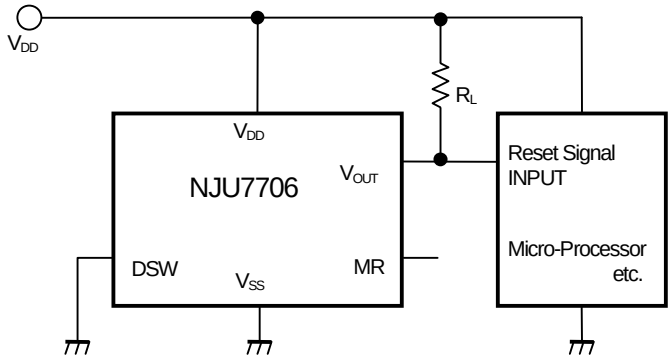


● Delay time2 TEST CIRCUIT

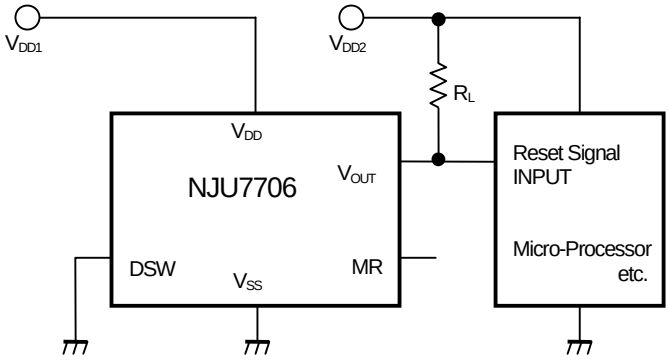


■ TYPICAL APPLICATION

① Power Supply Monitor Circuit (V_{DD} line COMMON)



② Power Supply Monitor Circuit (V_{DD} line SEPARATE)



■ NJU7707

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS		UNIT
Input Voltage	V_{DD}	+10		V
Output Voltage	V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3		V
Input Voltage of DSW pin	V_{DSW}	V_{SS}-0.3~V_{DD}+0.3		V
Input Voltage of MR pin	V_{MR}	V_{SS}-0.3~V_{DD}+0.3		V
Output Current	I_{OUT}	50		mA
Power Dissipation	P_D	SOT-23-5	350(*4)	mW
			200(*5)	
Operating Temperature	Topr	-40 ~ +85		°C
Storage Temperature	Tstg	-40 ~ +125		°C

(*4) : Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers)

(*5) : Device itself

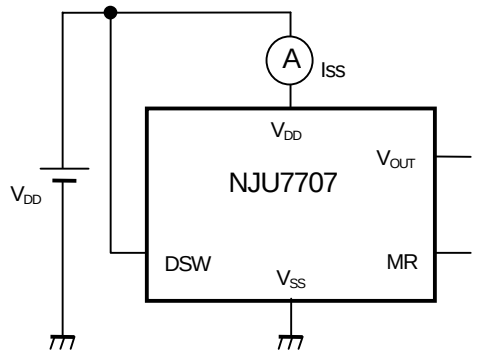
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Detection Voltage	V_{DET}			-1.0%	–	+1.0%	V
Hysteresis Voltage	V_{HYS}			70	90	130	mV
Quiescent Current	I_{SS}	V_{DD}=V_{DET}+1V	V_{DET}=1.5V ~ 1.9V Version	–	1.0	1.7	µA
			V_{DET}=2.0V~ 6.0V Version	–	1.3	2.2	
Output Current	I_{OUT}	Nch, V_{DS}=0.5V	V_{DD}=1.2V	0.75	2.0	–	mA
			V_{DD}=2.4V (≥2.7V Version)	4.5	7.0	–	
		Pch, V_{DS}=0.5V	V_{DD}=4.8V (≤3.9V Version)	2.0	3.5	–	
			V_{DD}=6.0V (4.0V ~ 5.6V Version)	2.5	4.0	–	
			V_{DD}=8.4V (≥5.7V Version)	3.0	5.0	–	
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/\Delta Ta$	Ta=0 ~ +85°C		–	±100	–	ppm/°C
Delay Time 1	t_{d1}	V_{DD}=V_{DET}+1V, DSW="L Level"	NJU7707F***1	42.5	50	57.5	ms
			NJU7707F***2	85	100	115	ms
			NJU7707F***3	170	200	230	ms
Delay Time 2	t_{d2}	V_{DD}=V_{DET}+1V, DSW="H Level"		25	50	300	µs
Input Voltage of DSW pin	V_{DSW_H}			1.5	–	V_{DD}	V
	V_{DSW_L}			0	–	0.3	V
Input Voltage of MR pin (Active "L")	V_{MR_H}			1.5	–	V_{DD}	V
	V_{MR_L}			0	–	0.3	V
Input Voltage of MR pin (Active "H")	V_{MR_H}			V_{DD}-0.3	–	V_{DD}	V
	V_{MR_L}			0	–	V_{DD}-1.5	V
Impedance of MR pin	R_{MR}			1.0	2.0	3.0	MΩ
Operating Voltage (*6)	V_{DD}	R_L=100kΩ		0.8	–	9	V

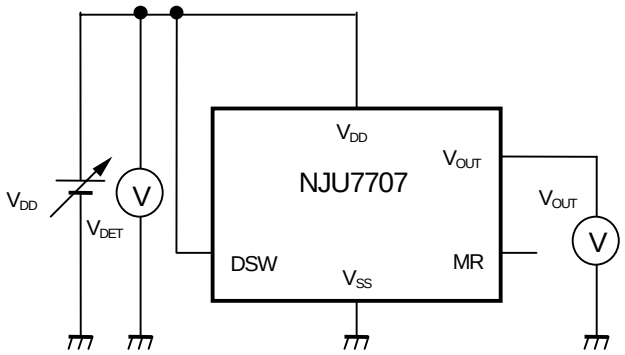
(*6): The minimum operating voltage(V_{OPL}) indicates the same value of the input voltage(V_{DD}) on condition that V_{OUT} becomes 10% or less of the input voltage(V_{DD}).

■ TEST CIRCUIT

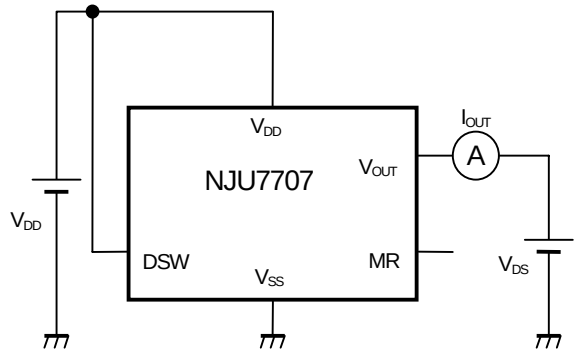
● Circuit Operating Current TEST CIRCUIT



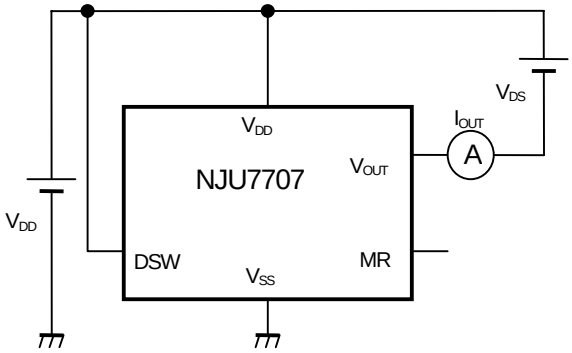
● Detection voltage TEST CIRCUIT



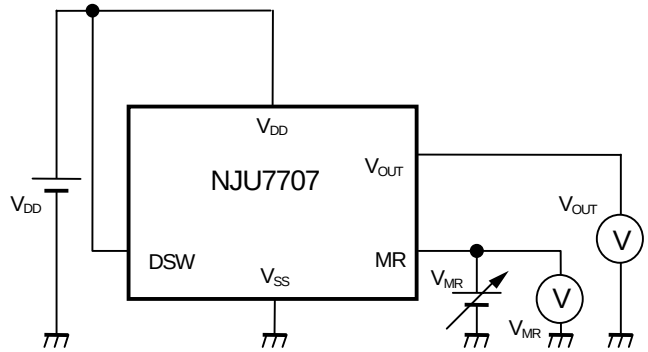
● Nch Output current TEST CIRCUIT



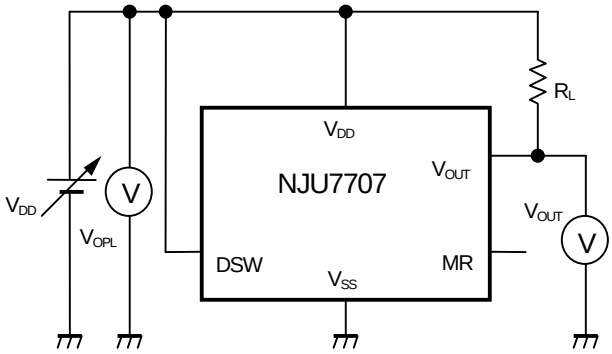
● Pch Output current TEST CIRCUIT



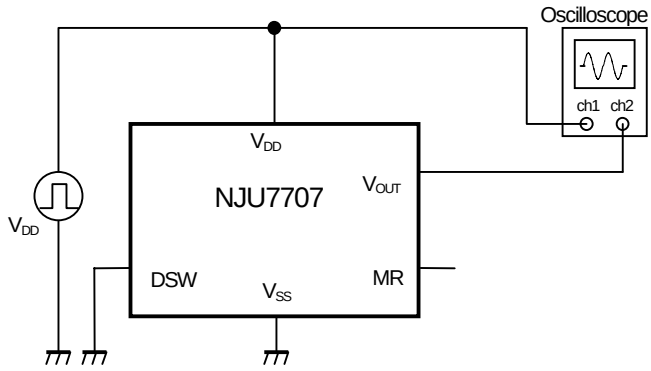
● MR pin Input voltage TEST CIRCUIT



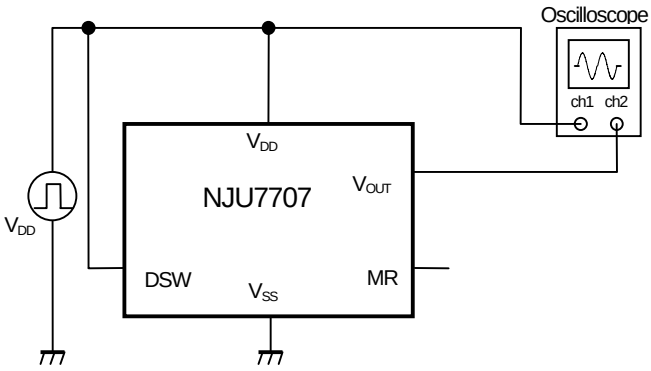
● Minimum operating voltage TEST CIRCUIT



● Delay time1 TEST CIRCUIT

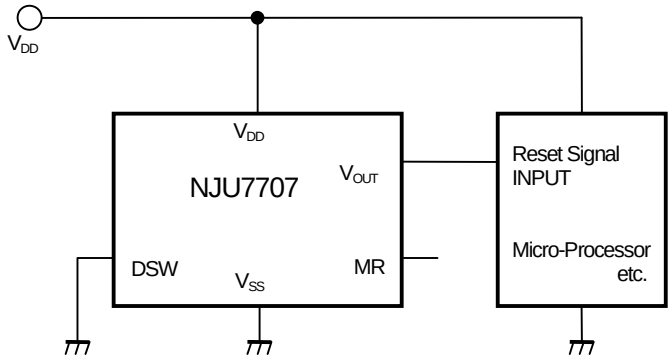


● Delay time2 TEST CIRCUIT



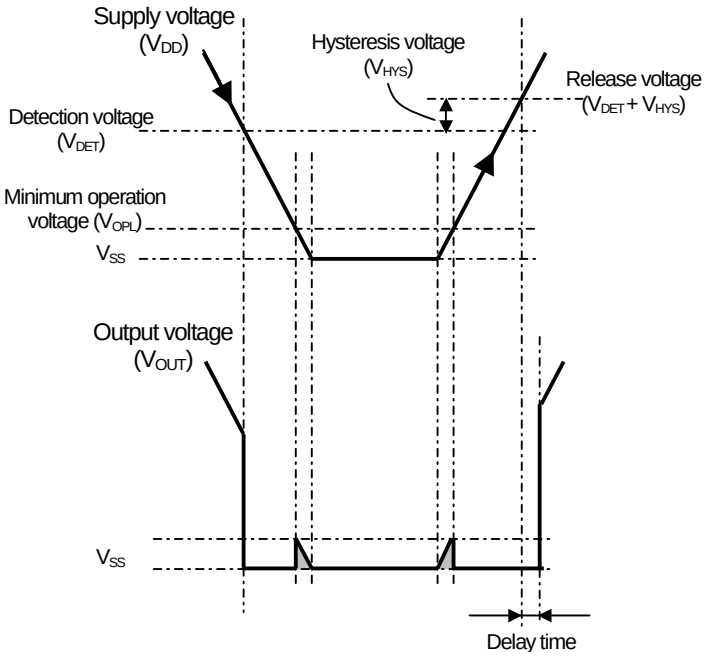
■ TYPICAL APPLICATION

① Power Supply Monitor Circuit (VDD line COMMON)



■ Functional Description

(1) Basic operation



(1) When supply voltage(V_{DD}) drops below detection voltage(V_{DET}), Output voltage(V_{OUT}) changes "H" to "L" to alert reset state.

(2) The reset state is kept while V_{DD} is lower than release voltage. The release voltage is a sum of V_{DET} and Hysterisis voltage (V_{HYS}). Please refer to the (*7) below.

(3) When V_{DD} becomes higher than the release voltage and reset release delay time fixed by internal is past, then V_{OUT} changes from "L" to "H" to resume normal state.

(*7) V_{HYS} is to avoid unstable V_{OUT} state caused by rapid voltage change at nearby V_{DET}.

(*8): C-MOS output product (NJU7707) : When V_{DD} less than V_{OPL}, V_{OUT} is free of the shaded region.

(2) Description of Manual Reset

Reset signal can output independently with MR.

Logic of MR	Operation
Active "L"	V_{MR}= "L" => Reset "ON"
Active "H"	V_{MR}= "H" => Reset "ON"

If Manual Reset is not required, please connect MR terminal as following.

Logic of MR	Connection
Active "L"	Connect MR terminal to V_{DD} or open
Active "H"	Connect MR terminal to GND or open