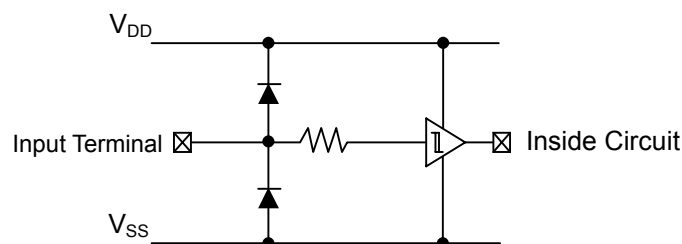




## ■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
13	$V_{DD}$	-	Operation Power Supply, $V_{DD}=2V$
2	$V_{SS}$	-	Operation Power GND, $V_{SS}=0V$
7 8	$V_{DDO}$	-	Driving Power Supply, $V_{DDO}=2V$ Terminal No.7 and No.8 should be connected to the same electric potential.
5 10	$V_{SSO}$	-	Driving Power GND, $V_{SSO}=0V$ Terminal No.5 and No.10 should be connected to the same electric potential.
1	MCK	I	Master Clock Input Terminal The condition of the data input terminal is fetched with the rising edge of this signal.
4 11	$EN_1$ $EN_2$	I	Output Control Terminal Output circuit is selected by the condition of this terminal.
3 12	$IN_1$ $IN_2$	I	Audio Signal Input Terminal 1-bit Audio Signal inputs into this terminal.
14	BEEP	I	Beep Signal Input Terminal Beep signal inputs into this terminal.
6 9	$OUT_1$ $OUT_2$	O	Output Terminal <ul style="list-style-type: none"> <li>When Output Terminal selects Audio Signal, <math>IN_1</math> terminal input data outputs from <math>OUT_1</math> terminal and <math>IN_2</math> terminal input data outputs from <math>OUT_2</math> terminal.</li> <li>When Output Terminal selects Beep Signal, BEEP terminal input data outputs from <math>OUT_1</math> and <math>OUT_2</math> terminals.</li> </ul>

## ■ INPUT TERMINAL STRUCTURE



## ■ FUNCTIONAL DESCRIPTION

### (1) Signal Output

PWM signals of L channel and R output from OUT<sub>1</sub> and OUT<sub>2</sub> terminals respectively. These signals are converted to analog signal by external 2nd-order or over LC filter. The output driver power supplied from V<sub>DDO</sub> and V<sub>SSO</sub> are required high response power supply against voltage fluctuation like as switching regulator because Output T.H.D is effected by power supply stability.

### (2) Master Clock

Master clock (MCK) synchronizes the Audio signal inputs (IN<sub>1</sub> and IN<sub>2</sub>). The setup time and the hold time should be kept in the AC characteristics because IN<sub>1</sub> and IN<sub>2</sub> are fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

OUT<sub>1</sub> and OUT<sub>2</sub> occur the pop noise when MCK is stopped in operation without standby mode. Therefore, the standby mode should be set before MCK stop.

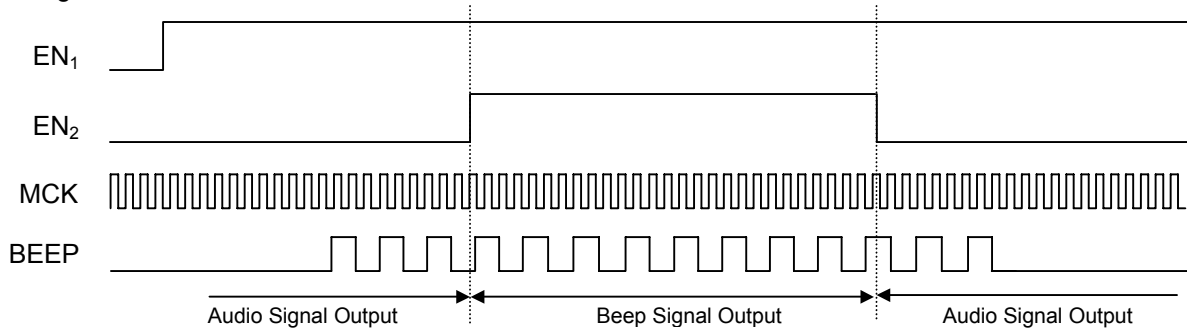
### (3) Output Control

Output circuit is selected by the conditions of EN<sub>1</sub> and EN<sub>2</sub> terminals.

EN <sub>2</sub>	EN <sub>1</sub>	Output State of OUT <sub>1</sub> & OUT <sub>2</sub>
0	0	Standby(High impedance)
0	1	Audio Signal Output
1	0	BPZ Output
1	1	Beep Signal Output

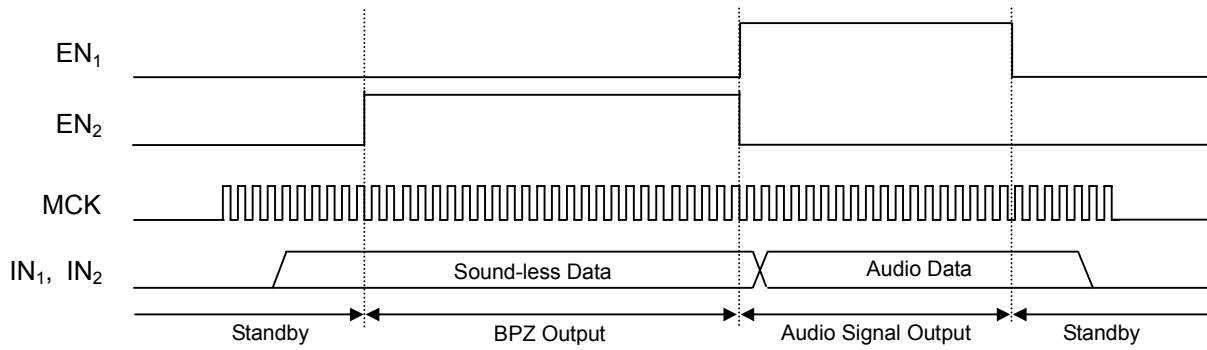
### (4) Beep Function

The beep signal must be input before the rising edge of EN<sub>2</sub> signal and must be stopped after the falling edge of EN<sub>2</sub> signal.



## (5) BPZ Function

BPZ Function operates to charge the external AC coupling capacitor for the BPZ level which is a point of the analog signal common. Be sure to input sound-less data to  $IN_1$  and  $IN_2$  in busy of the BPZ function. At this time, the sound-less signal must be input before the rising edge of  $EN_2$  signal and must be continue after the falling edge of  $EN_2$  signal. The charging time is in proportion to the capacity value of the external AC coupling capacitor.



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Operation Supply Voltage		V <sub>DD</sub>	-0.3 to +4.0	V
Driving Supply Voltage		V <sub>DDO</sub>	-0.3 to +2.7	V
Input Voltage		V <sub>in</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	SSOP14	P <sub>D</sub>	300	mW
Power Supply Voltage Condition		-	V <sub>DD</sub> ≥ V <sub>DDO</sub>	V

Note 1) All voltage values are specified as V<sub>SS</sub>=V<sub>SSO</sub>=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitors should be connected between V<sub>DD</sub>-V<sub>SS</sub> and V<sub>DDO</sub>-V<sub>SSO</sub> due to the stabilized operation.

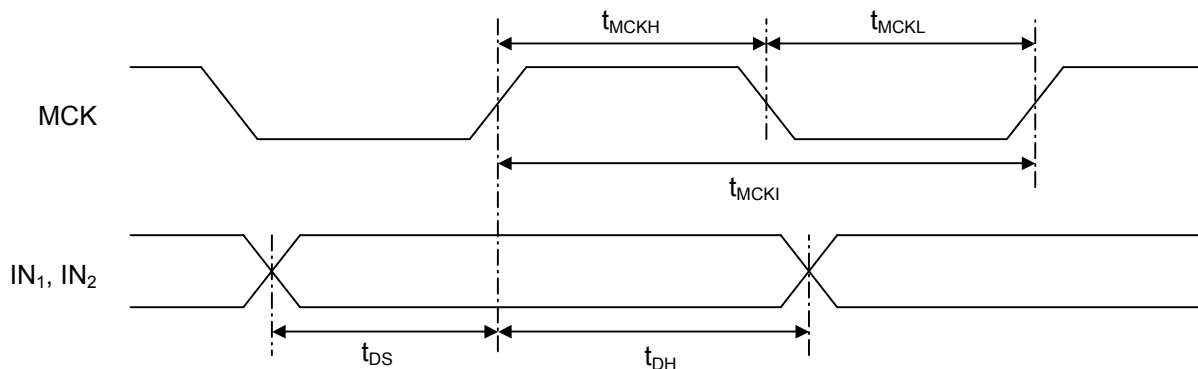
## ■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V<sub>DD</sub>=V<sub>DDO</sub>=2.0V, V<sub>SS</sub>=V<sub>SSO</sub>=0.0V, Load Impedance=32Ω, f<sub>s</sub>=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>		1.7	2.0	2.7	V
V <sub>DDO</sub> Supply Voltage	V <sub>DDO</sub>		1.7	2.0	V <sub>DD</sub>	V
BPZ Driving Voltage	V <sub>BPZ</sub>	load operating MCK=256f <sub>s</sub> IN <sub>1</sub> , IN <sub>2</sub> =32f <sub>s</sub> Duty50%	V <sub>DDO</sub> /2-0.2	V <sub>DDO</sub> /2	V <sub>DDO</sub> /2+0.2	V
Output Driver High side Resistance	R <sub>H</sub>	V <sub>OUT</sub> =V <sub>DDO</sub> -0.1V	-	1.5	2	Ω
Output Driver Low side Resistance	R <sub>L</sub>	V <sub>OUT</sub> =0.1V	-	1.5	2	Ω
Beep High side Current	I <sub>BH</sub>	V <sub>OUT</sub> =V <sub>DDO</sub> -1V	20	50	150	uA
Beep Low side Current	I <sub>BL</sub>	V <sub>OUT</sub> =1V	20	50	150	uA
Operating Current At Standby	I <sub>ST</sub>	Stopping MCK, IN <sub>1</sub> , IN <sub>2</sub> , BEEP	-	-	1	uA
Operating Current At no input signal	I <sub>DD</sub>	No-load operating IN <sub>1</sub> , IN <sub>2</sub> =32f <sub>s</sub> MCK=256f <sub>s</sub>	-	0.05	0.1	mA
	I <sub>DDO</sub>		-	0.6	1.2	
Input Voltage	V <sub>IH</sub>		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V
	V <sub>IL</sub>		0	-	0.3V <sub>DD</sub>	V
Input Leakage Current	I <sub>LK</sub>		-	-	±1	uA

## ■ TIMING CHARACTERISTICS

- Audio Signal Input

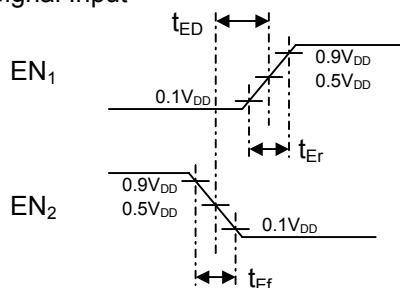


( $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=V_{DDO}=2.0\text{V}$ ,  $V_{SS}=V_{SSO}=0.0\text{V}$ , unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	$f_{MCKI}$		8	-	25	MHz
MCK Pulse Width (H)	$t_{MCKH}$		12	-	-	ns
MCK Pulse Width (L)	$t_{MCKL}$		12	-	-	ns
IN <sub>1</sub> ,IN <sub>2</sub> Setup Time	$t_{DS}$		20	-	-	ns
IN <sub>1</sub> ,IN <sub>2</sub> Hold Time	$t_{DH}$		20	-	-	ns
BEEP Frequency	$f_{BEEP}$		0.1	-	20	kHz

Note 4)  $t_{MCKI}$  shows the cycle of the MCK signal.

- Output Control Signal Input



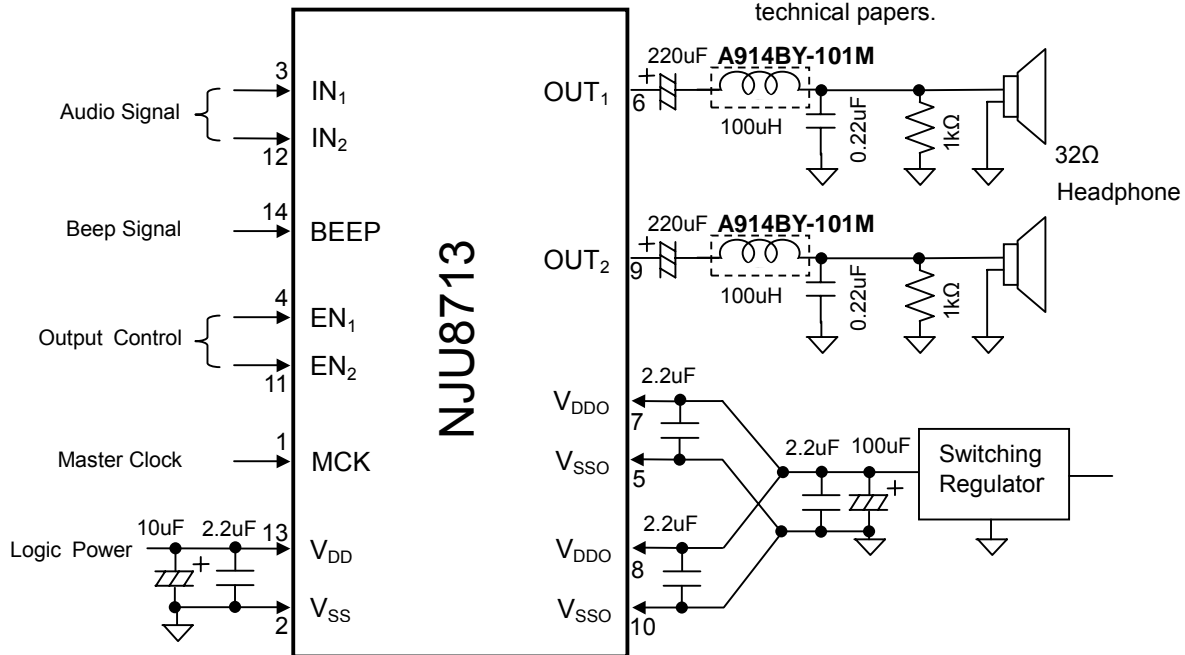
( $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=V_{DDO}=2.0\text{V}$ ,  $V_{SS}=V_{SSO}=0.0\text{V}$ , unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	$t_{Er}$		-	-	50	ns
Fall Time	$t_{Ef}$		-	-	50	ns
Switching Time	$t_{ED}$				100	ns

Note 5) All timings are based on 30% and 70% voltage level of  $V_{DD}$ .

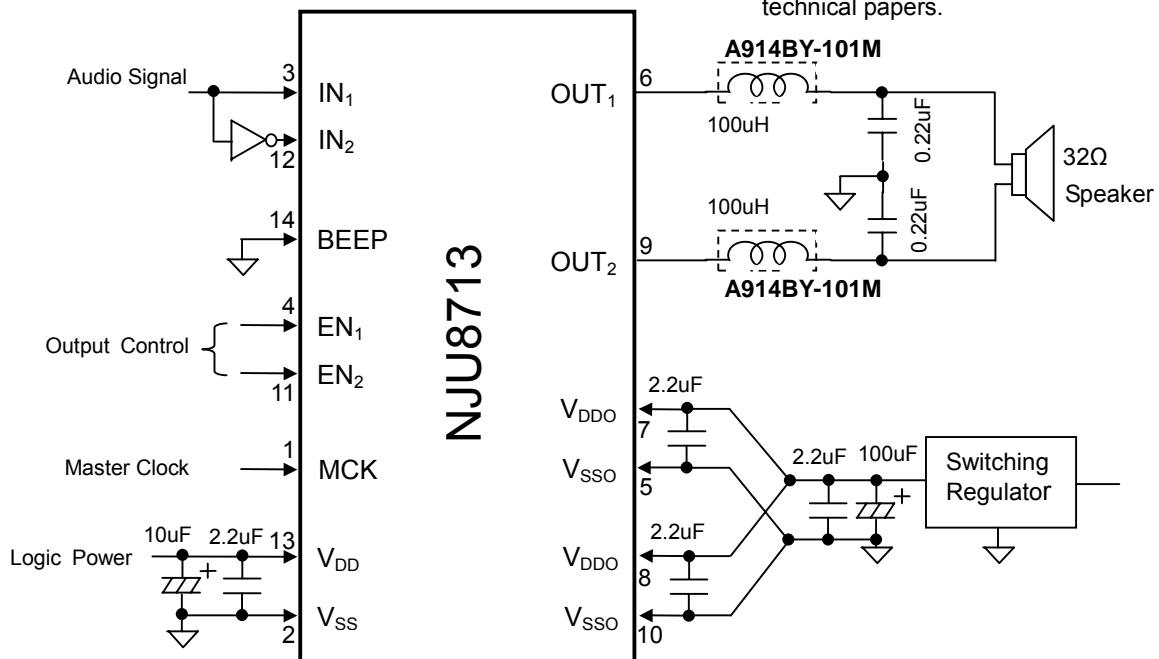
## APPLICATION CIRCUIT

### • Stereo OTL application example



•A914BY-101M is manufactured by TOKO, INC. For further information, please refer to its technical papers.

### • 1 channel BTL application example



•A914BY-101M is manufactured by TOKO, INC. For further information, please refer to its technical papers.

Note 6) De-coupling capacitors must be connected between each power supply pin and GND pin.

Note 7) The power supply for  $V_{DDO}$  requires fast driving response performance such as a switching regulator for T.H.D.

Note 8) The bigger capacitor value of external AC-coupling capacitors realize better low frequency response characteristics. In addition, ESR(Equivalent Series Resistance) should be low.

Note 9) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.

**[CAUTION]**

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