PRELIMINARY

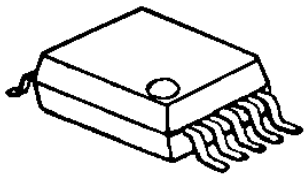
Monaural BTL Output Switching Driver for Class D Amplifier

■ GENERAL DESCRIPTION

The **NJU8719** is a monaural BTL output switching driver for class D amplifier. It converts 1bit digital signal input, such as PWM or PDM signal, to analog signal output with simple external LC low-pass filter.

The **NJU8719** realizes very high power-efficiency by class D operation. Therefore, It is suitable for portable set with speaker.

■ PACKAGE OUTLINE

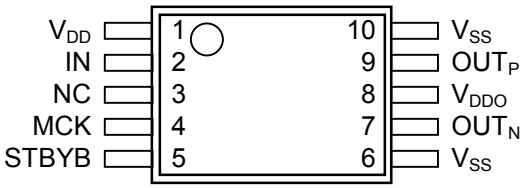


NJU8719V

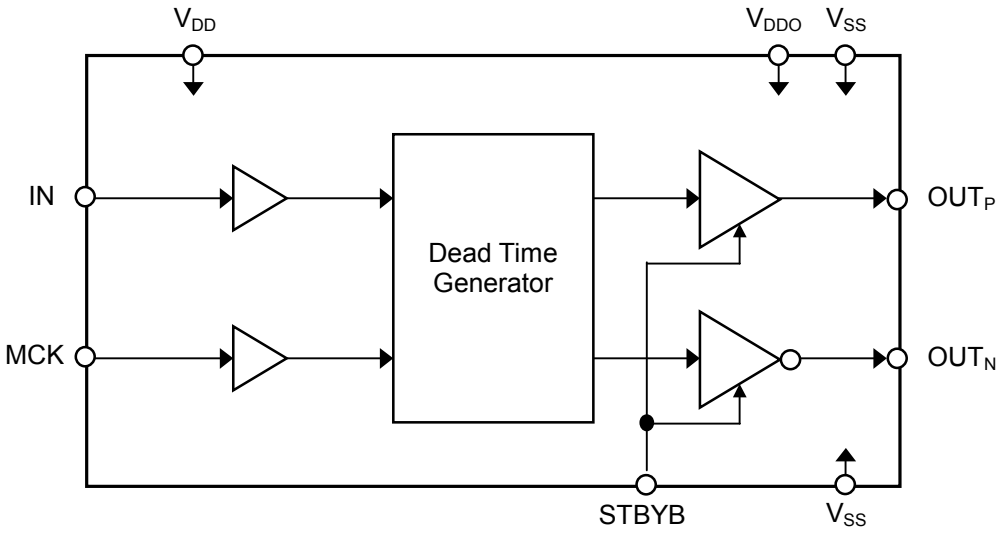
■ FEATURES

- 1-channel 1bit Audio Signal Input
- Monaural BTL Output
- Standby(Hi-Z) Control Function
- Operating Voltage : 2.4V to 5.25V
- CMOS Technology
- Package Outline : SSOP10

■ PIN CONFIGURATION



■ BLOCK DIAGRAM

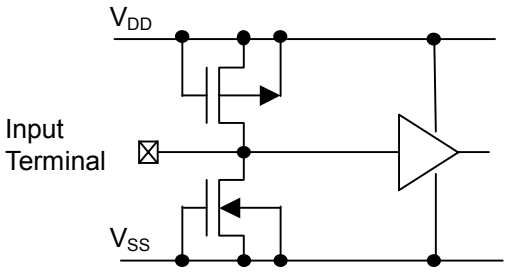


■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
1	V_{DD}	–	Power Supply, V_{DD}=5V
2	IN	I	1-bit Data Input Terminal
3	NC	–	Non connection
4	MCK	I	Master Clock Input Terminal The condition of the data input terminal is fetched with the rising edge of this signal.
5	STBYB	I	Standby Control Terminal (L:Standby)
6 10	V_{SS}	–	Power GND and Output GND terminal: V_{SS}=0V
7	OUT_N	O	Negative output
8	V_{DDO}	–	Output Power Supply, V_{DD}=5V
9	OUT_P	O	Positive output

*V_{SS}(Terminal No.6,10) should be connected at a nearest point to the IC.
*V_{DD}(Terminal No.1) and V_{DDO}(Terminal No.8) should be connected at a nearest point to the IC.
*STBYB(Terminal No.5) must be connected to V_{DD}, when this terminal is not used.

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output

The OUT_P and OUT_N generate PMW output signal, which is converted to analog signal via external 2nd-order or higher LC filter. The NJU8719 drives a speaker by the BTL output, and OUT_P is a positive output and OUT_N is a negative outputs.

A switching regulator with a high response against a voltage fluctuation is the best selection for the $V_{DDO,}$ which is the power supply for output drivers. To obtain better T.H.D. performance, the stabilization of the power is required.

(2) Standby Control Function

By setting the STBYB terminal to “L”, the **NJU8719** becomes standby condition. During standby condition, OUT_P and OUT_N are in Hi-Z.

(3) Master Clock

Master clock (MCK) synchronizes with the Audio signal input (IN). The setup time and the hold time should be kept in the AC characteristics because IN is fetched with the rising edge of MCK. MCK requires jitter-free or jitter as small as possible because the jitter downs S/N ratio.

OUT_P and OUT_N occur the pop noise when MCK is stopped in operation without standby mode. Therefore, the standby mode should be set before MCK stop.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	-0.3 to +5.5	V
		V_{DDO}	-0.3 to +5.5	
Input Voltage		Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	SSOP10	P_D	360*	mW

* : Mounted on two-layer board of based on the JEDEC.

Note 1) All voltage values are specified as V_{SS}=0V.
Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.
Note 3) De-coupling capacitors should be connected between V_{DD}-V_{SS} and V_{DDO}-V_{SS} due to the stabilized operation.

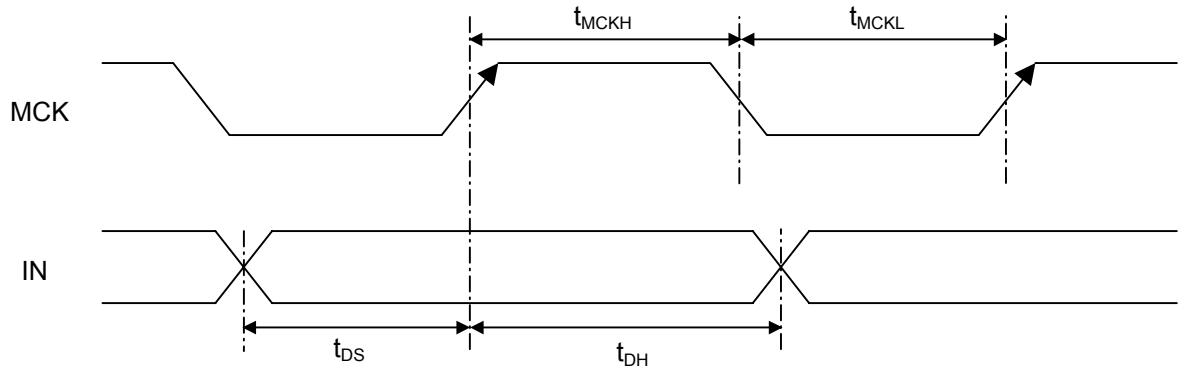
■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}= V_{DDO}=5.0V, V_{SS}=0V, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} ,V_{DDO} Supply Voltage	V_{DD}		2.4	5.0	5.25	V
Output Driver High side Resistance	R_H	V_{OUT}=V_{DDO}-0.1V	-	0.5	1.5	Ω
Output Driver Low side Resistance	R_L	V_{OUT}=0.1V	-	0.5	1.5	Ω
Operating Current at Standby	I_{ST}	IN, STBYB=0V No-load operating	-	-	1	μA
Operating Current at Operating (Mute signal input)	I_{DD}	IN=32f_S MCK=256f_S No-load operating	-	3.8	5.7	mA
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
Input Leakage Current	I_{LK}		-	-	±1	μA

■ TIMING CHARACTERISTICS

- Audio Signal Input



(Ta=25°C, V_{DD}= V_{DDO}=5.0V, V_{SS}=0V, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	f_{MCKI}		-	-	25	MHz
MCK Pulse Width (H)	t_{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		12	-	-	ns
IN Setup Time	t_{DS}		20	-	-	ns
IN Hold Time	t_{DH}		20	-	-	ns

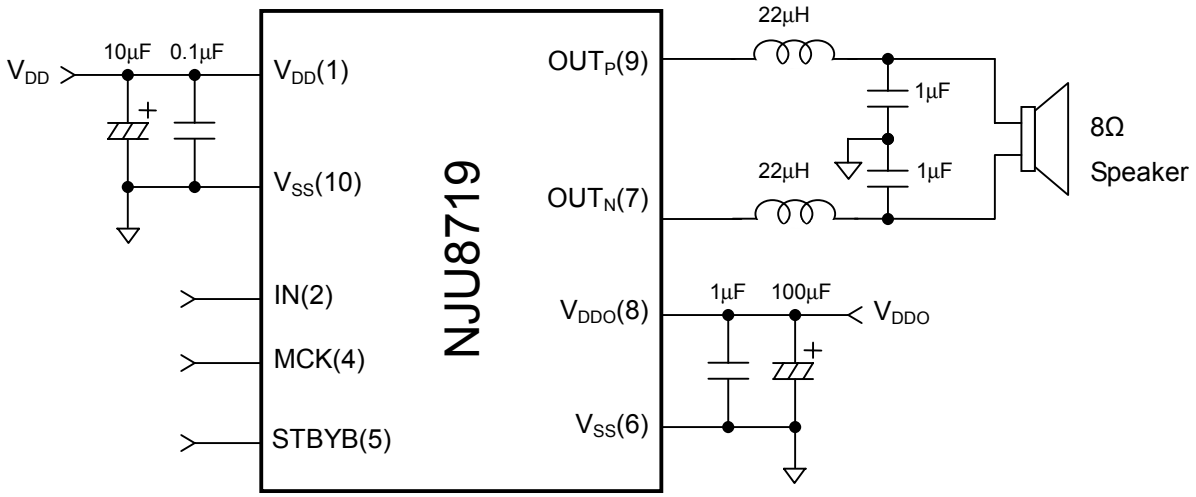
- Output Control Signal Input

(Ta=25°C, V_{DD}= V_{DDO}=5.0V, V_{SS}=0V, f_S=44.1kHz, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t_{UP}		-	-	50	ns
Fall Time	t_{DN}		-	-	50	ns

Note 4) All timings are based on 30% and 70% voltage level of V_{DD}.

■ APPLICATION CIRCUIT



Note 5) De-coupling capacitors must be connected between each power supply terminal and GND terminal.
Note 6) The power supply for V_{DDO} requires fast driving response performance such as a switching regulator for T.H.D..
Note 7) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.