

# Analog Signal Input Monaural Class-D Power Amplifier for Piezo Speaker

## ■ GENERAL DESCRIPTION

The **NJU8761** is an analog signal input monaural class-D amplifier for Piezo speaker.

The NJU8761 incorporates BTL amplifiers, which eliminate AC coupling capacitor. The input block operates on 2.6V(Min.) as power supply and the output block operates up to 12V, therefore it can output close to 17.5V<sub>P-P</sub> amplified signal and drive Piezo speaker with louder sound and high efficiency.

Class-D operation achieves lower power operation for Piezo speaker, thus the **NJU8761** is suited for battery-powered applications such as cellular phone and PDA.

## ■ PACKAGE OUTLINE

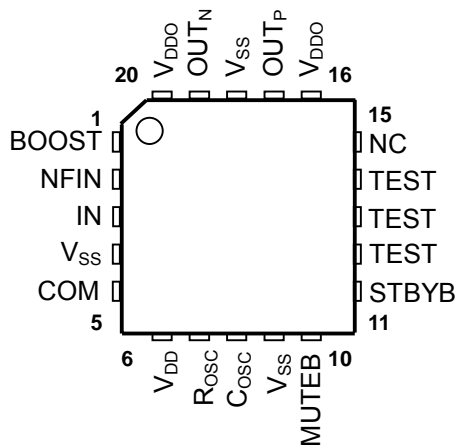


**NJU8761KM1**

## ■ FEATURES

- Piezo Speaker Driving
- Output voltage 6.2 Vrms (Typ.) @V<sub>DDO</sub>=10 V, THD+N=10%
- Analog input, Monaural BTL output
- Standby(Hi-Z), Mute control
- Built-in Low Voltage Detector for V<sub>DD</sub> & V<sub>DDO</sub>
- Operating Voltage   Input Block: 2.6~3.6V(V<sub>DD</sub>)  
                                  Output Block: 8.0~12.0V(V<sub>DDO</sub>)
- CMOS Technology
- Package Outline    QFN20-M1

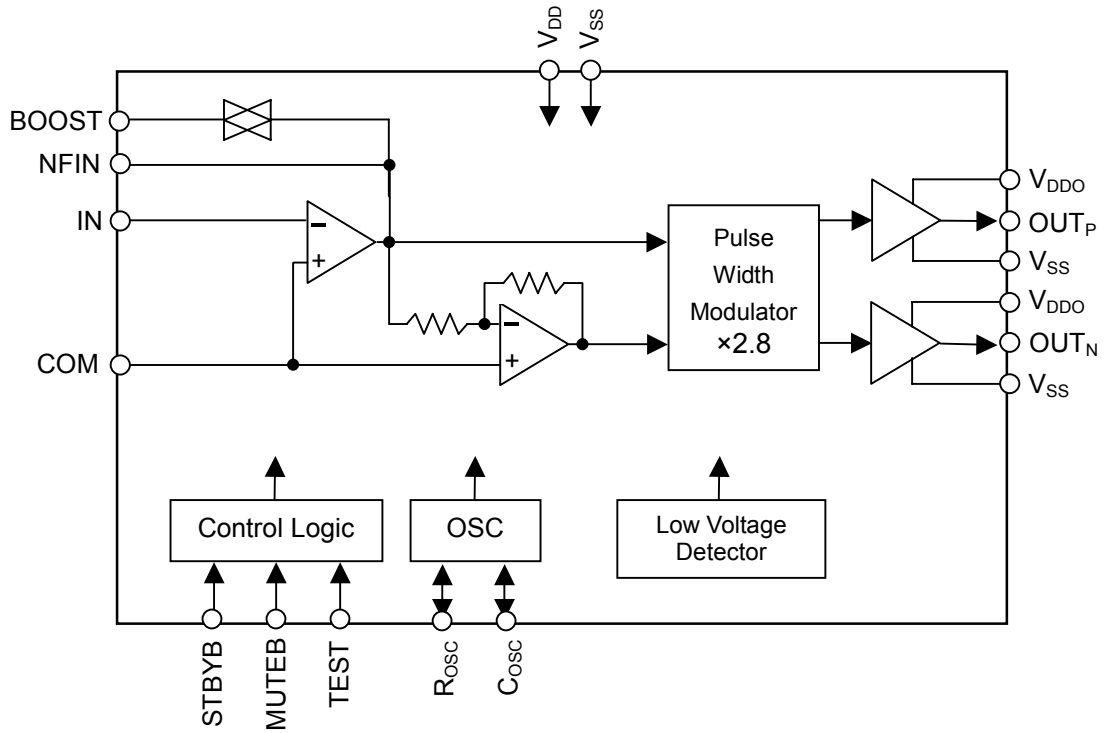
## ■ PIN CONFIGURATION



# NJU8761

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## ■ BLOCK DIAGRAM



## ■ PIN DESCRIPTION

No.	SYMBOL	I/O	Function
1	BOOST	I/O	Input capacitor charge terminal
2	NFIN	I/O	Input amplifier gain setting terminal
3	IN	I	Signal input terminal
4,9,18	V <sub>SS</sub>	-	Power GND: V <sub>SS</sub> =0V
5	COM	-	Analog common
6	V <sub>DD</sub>	-	Power Supply
7	R <sub>OSC</sub>	I	Resistor connection terminal for oscillator
8	C <sub>OSC</sub>	I	Capacitor connection terminal for oscillator
10	MUTEB	I	Mute Control H: Normal operation, L: Mute ON
11	STBYB	I	Standby Control H: Normal operation, L: Standby ON
12,13,14	TEST	I	Maker test terminal L: Normal operation
15	NC	-	Non connection
16,20	V <sub>DDO</sub>	-	Output Power Supply: V <sub>DDO</sub> =MAX.12V
17	OUT <sub>P</sub>	O	Positive signal output terminal
19	OUT <sub>N</sub>	O	Negative signal output terminal

Note 1) Pin No. 4,9,18(V<sub>SS</sub>) should be connected at the nearest point of the IC on the PCB.

Note 2) Pin No.16, 20(V<sub>DDO</sub>) should be connected at the nearest point of the IC on the PCB.

## ■ FUNCTION DESCRIPTION

### (1) Power supply

- $V_{DD}$  : Power supply for input amplifier in power amplifier block and PWM(Pulse Width Modulator)circuit block.
- $V_{DDO}$  : Power supply for output drivers in power amplifier block.

### (2) Standby control

By setting the STBYB pin to "L" level, it switches the NJU8761 into standby condition. During the standby condition, output pins ( $OUT_P$ ,  $OUT_N$ ) become high impedance. Keep the STBYB pin to "L" level at least 41ms once switched into the standby condition. For normal operation, the STBYB pin requires "H" level.

Note 3) The STBYB pin must be required into "L" level at power-on.

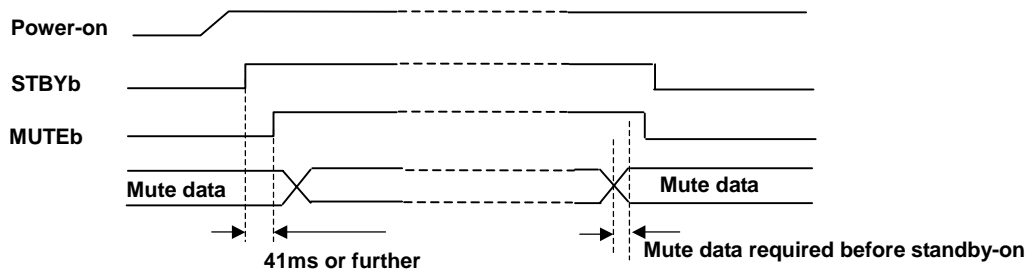
### (3) Boost function

The boost function provides the pop-noise reduction on startup by charging the input capacitor( $C_C$ ) to the same voltage of the COM pin. The charging needs 41ms since the STBYB pin has been changed to "H" level from "L" level.

### (4) Mute control

By setting the MUTEb pin to "L" level, it switches the NJU8761 into mute condition. During the mute condition, output pins ( $OUT_P$ ,  $OUT_N$ ) output the PWM waves (Duty 50%).

Note 4) The **NJU8761** has a built-in circuit for the pop-noise reduction at power-on. However the control with the following sequence can realize more effective the pop-noise reduction.



### (5) Power supply voltage detection circuit

To prevent an irregular oscillation in the internal circuit, the **NJU8761** ceases operating when power supply voltage reaches the detection voltage as shown below.

	$V_{DD}$	$V_{DDO}$
Operating Start-voltage	Around 1.8V	Around 5.5V
Operating Halt-voltage	Around 1.6V	Around 5.0V

Detection circuits in  $V_{DD}$  and  $V_{DDO}$  blocks work individually and each operation is as shown below.

Note 5) Output blocks become high-impedance during halts.

When  $V_{DD} > \text{Approx } 1.8V$  and  $V_{DDO} < \text{Approx } 5.0V$ , only output block is halted.

When  $V_{DD} > \text{Approx } 1.6V$ , the whole circuits are halted.(If  $V_{DD}$  is recovered, the **NJU8761** restarts after 41ms as same as the Standby-off.

## (6) Power Amplifier

### (6-1) Input signal

The amount of current passing through a capacitive load increases proportionately with frequency of audio signal. Input filters should be put in the input line to reduce load current at high frequency-band.

The input filters are composed of 1st-order RC LPF(Low Pass Filter) and 1st-order RC HPF(High Pass Filter).

$f_{CH1}$ (Cut-off frequency of HPF) and  $f_{CL1}$ (Cut-off frequency of LPF) are determined by input resistance( $R_{IN}$ ), resistor for LPF( $R_{LPF}$ ), capacitor for LPF( $C_{LPF}$ ) and AC coupling capacitor( $C_C$ ).

When  $R_{IN}=10k\Omega$ ,  $R_{LPF}=3k\Omega$  and  $C_{LPF}=0.01\mu F$ ,  $C_C=2.2\mu F$ ,  $f_{CH1}$  and  $f_{CL1}$  are roughly calculated as following expressions.

$$f_{CH1} = \frac{1}{2\pi (R_{IN} + R_{LPF})C_C} = \frac{1}{2 \times 3.14 \times (10 \times 10^3 + 3 \times 10^3) \times 2.2 \times 10^{-6}} \cong 5.6[\text{Hz}]$$

$$f_{CL1} = \frac{1}{2\pi (R_{IN} // R_{LPF})C_{LPF}} = \frac{1}{2 \times 3.14 \times (10 \times 10^3 // 3 \times 10^3) \times 0.01 \times 10^{-6}} \cong 6.9[\text{kHz}]$$

### (6-2) Output signal

The output signals are PWM signals, which will be converted to analog signal via external 2nd-order or higher LC filter. To reduce the current consumption with signal-input close to cutoff-frequency of LPF( $f_c$ ). Damping resistor should be connected between  $OUT_P$  pin and coil, and between  $OUT_N$  pin and coil.

Note 6) Q(The gain of LPF at  $f_c$ ) should be within 1 with settings of L, C and  $R_{DAMP}$ .

When  $L=22\mu F$ ,  $CL=1.1\mu F$ ,  $R_{DAMP}=4.3\Omega$  and equivalent series resistance( $R_{DCR}$ )= $0.21\Omega$ , cut-off frequency of LPF( $f_c$ ) and Q are roughly calculated as following expressions.

$$f_c = \frac{1}{2\pi \sqrt{2LC_L}} = \frac{1}{2 \times 3.14 \times \sqrt{2 \times 22 \times 10^{-6} \times 1.1 \times 10^{-6}}} \cong 23[\text{kHz}]$$

$$Q = \frac{1}{(R_{DAMP} + R_{DCR})\sqrt{2C_L}} = \frac{1}{(4.3 + 0.21) \times \sqrt{2 \times 1.1 \times 10^{-6}}} \cong 0.70$$

### (6-3) Voltage gain

The voltage gain is estimated by multiplying the voltage gain of input amplifier by the gain of PWM circuit and the gain of BTL output stages. The gain of PWM circuit is 2.8 times and the gain of BTL output stage is twofold. The voltage gain of input amplifier is determined by the ratio of negative feedback resistor (RFB connected with NFIN pin) versus external input resistor ( $R_{IN}$  connected with IN pin).

Note 7) The negative feedback resistor ( $R_{FB}$ ) must be set  $10k\Omega$  or further. In addition, due to the limitation of phase-margin, the gain of input amplifier must be one time or further.

When input resistor is  $10k\Omega$  and negative feedback resistor is  $39k\Omega$ , total voltage gain is roughly calculated as following.

$$\text{Voltage gain} = 39k\Omega / 10k\Omega \times 2.8 \times 2 = 21.8 \text{ times} \cong 26\text{dB}$$

Note 8) The maximum output amplitude is approx " $V_{DD} \times 0.7 [V_{PP}]$ ". When the gain of input amplifier is one time, maximum input amplitude is " $V_{DD} \times 0.7 / 1 [V_{PP}]$ ". If input signal exceeds maximum input amplitude, output waveform must be distorted.

### (6-4) Oscillation frequency

The oscillation frequency is determined by  $R_{OSC}$  (connected with  $R_{OSC}$  pin),  $C_{OSC}$  (connected with  $C_{OSC}$  pin) and power supply ( $V_{DD}$ ).

Note 9)  $250\text{kHz} \pm 20\text{kHz}$  is recommended for oscillation frequency. The following conditions would be suitable at this frequency. ( $V_{DD}$  is  $2.85\text{V}$ ,  $R_{OSC}$  is  $180k\Omega$  and  $C_{OSC}$  is  $390\text{pF}$ )

$$f_{osc} = \frac{3.3 \times V_{DD} + 8.5}{C_{OSC} \times R_{OSC}} = \frac{3.3 \times 2.85 + 8.5}{390 \times 10^{-12} \times 180 \times 10^3} \cong 255[\text{kHz}]$$

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3 ~ +4.0	V
	V <sub>DDOL</sub> V <sub>DDOR</sub>	-0.3 ~ +18.0	V
	Input Voltage	V <sub>in</sub>	-0.3 ~ V <sub>DD</sub> +0.3
Operating Temperature	T <sub>opr</sub>	-40 ~ +85	°C
Storage Temperature	T <sub>stg</sub>	-40 ~ +125	°C
Power Dissipation	P <sub>D</sub>	620	mW

\* : Mounted on two-layer board based on JEDEC

Note10) All voltage are relative to “V<sub>SS</sub> =0V” reference. The LSI must be used within the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

Note11) De-coupling capacitors for V<sub>DD</sub>-V<sub>SS</sub> and V<sub>DDO</sub>-V<sub>SS</sub> should be connected for stable operation.

Note12) Mounted on PCB (50mm x 50mm x 1.6mm)

## ■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V<sub>DD</sub>=2.85V, V<sub>DDO</sub>=10.0V, V<sub>SS</sub>=0V, TEST=0V  
 STBYB=MUTE B=2.85V, Input Signal=1kHz, Input Signal Level=250mVrms,  
 Frequency Band=20Hz~20kHz, Load Impedance=1.1μF, 2nd-order 23kHz LC Filter(Q=0.70))  
 R<sub>OSC</sub>=180kΩ, C<sub>OSC</sub>=390pF, R<sub>IN</sub>=10kΩ, R<sub>FB</sub>=39KΩ

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>		2.6	2.85	3.6	V
V <sub>DDO</sub> Supply Voltage	V <sub>DDO</sub>		8.0	10.0	12.0	V
Voltage Gain	A <sub>V</sub>		-	26	-	dB
THD+N	THD	Input Signal Level =250mVrms	-	0.3	0.8	%
Output Voltage	V <sub>o</sub>	Output THD=10%	-	6.2	-	Vrms
Operating Current(Stanby)	I <sub>ST</sub>	STBYB=0V	-	-	1	μA
Operating Current (No signal input)	I <sub>DD</sub>	No-load operating	-	1.5	3	mA
	I <sub>DDO</sub>	No Signal Input	-	1	2	
Input Voltage	V <sub>IH</sub>	MUTE B, STBYB pins	1.5	-	V <sub>DD</sub>	V
	V <sub>IL</sub>	MUTE B, STBYB pins	0	-	0.3	V
Input Leakage Current	I <sub>LK</sub>	EN, MODE pins	-	-	±1.0	μA

Note13) Test system of the output THD+N

The output THD+N is tested in the system shown in Figure 1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

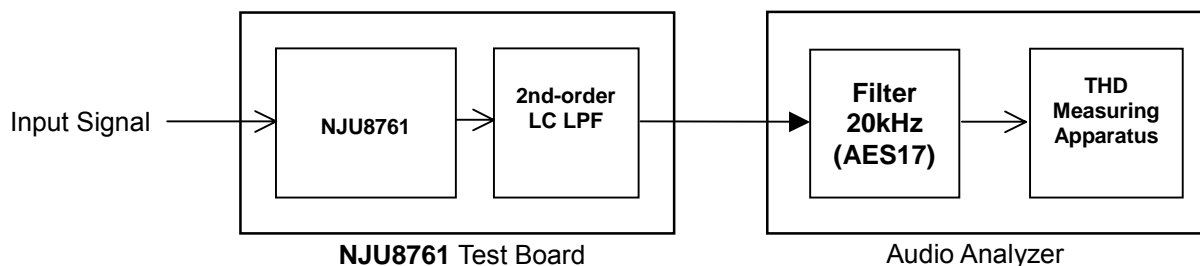
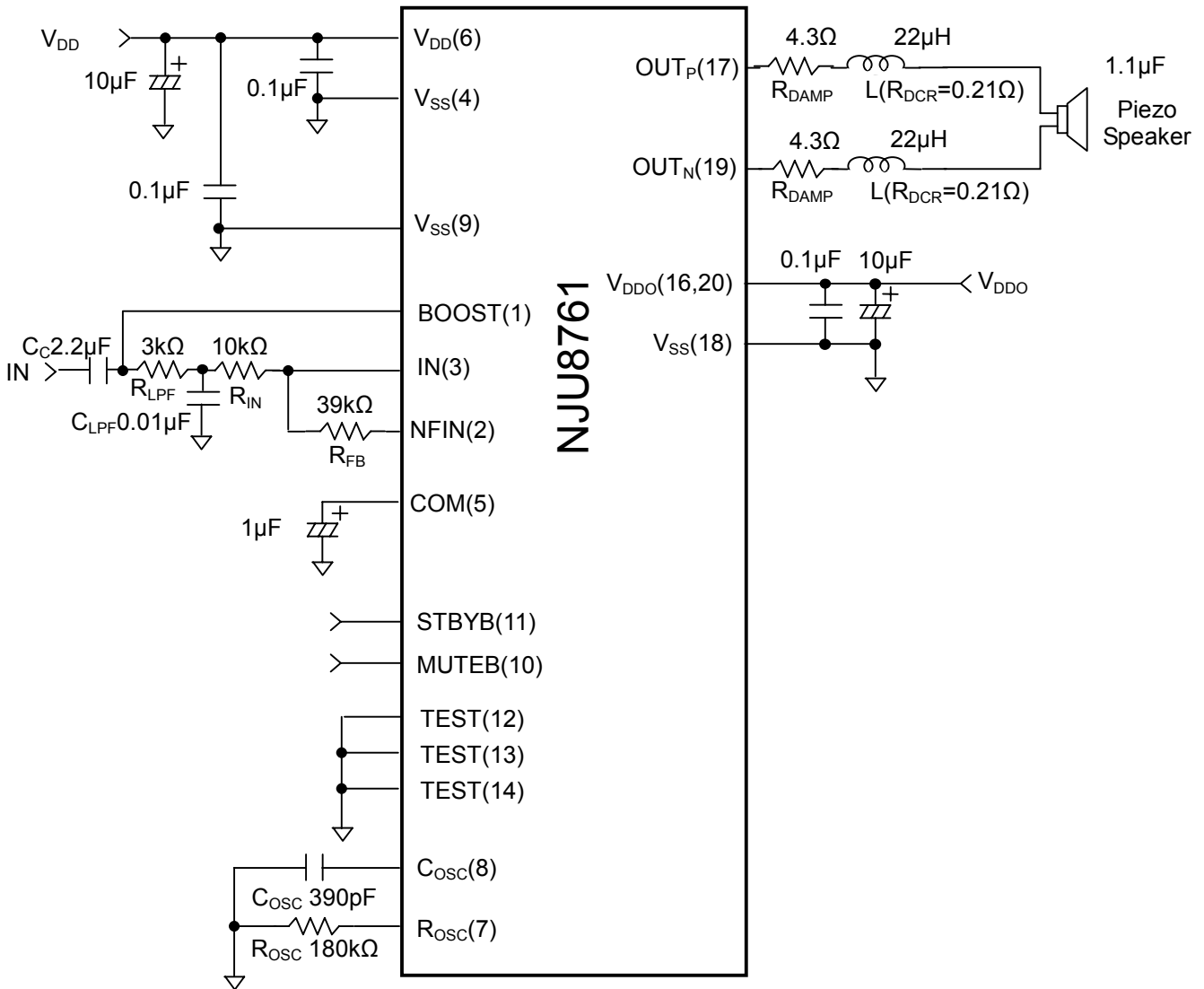


Figure 1. THD+N Test System

2nd-order LPF : Refer to “Typical Application Circuit”.  
 Filters : 22Hz HPF + 20kHz LPF(AES17)

## ■ TYPICAL APPLICATION CIRCUIT



Note 13) VDD power-on must be applied before V<sub>DDO</sub> power-on.

Note 14) (1) to (20) indicates pin numbers.

Note 15) De-coupling capacitors must be connected between each power-supply pin and GND. The capacitance should be adjusted on the application circuit and the operation temperature. It may malfunction if capacitance is small.

Note 16) The transition time for STBYB and MUTE signals must be less than 100µs. Otherwise, a multifunction may be caused.

Note 17) External coils, diodes, capacitors and resistors should be connected at the nearest point to the IC.

Note 18) The above circuit shows only application example and does not guarantee any electrical characteristic. Cut-off frequency of the LC filter influences the quality of sound. Therefore, please test the circuit carefully to fit your application.

**[CAUTION]**

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