8input-2output Video Driver
with Isolation Amplifier & 47μF AC-Coupling Capacitor

■FEATURES

- ●Operating Voltage 4.5 to 9.5V
- ●Small output coupling capacitor 47μF(VOUT2)
- ●Isolation Amplifiers (VIN1,2)
- ●8in-2out Video Switch
- ●Common Mode Rejection Ratio -50dB typ
- ●I²C BUS interface
- ●Bi-CMOS Technology
- ●Package Outline SSOP20-C3

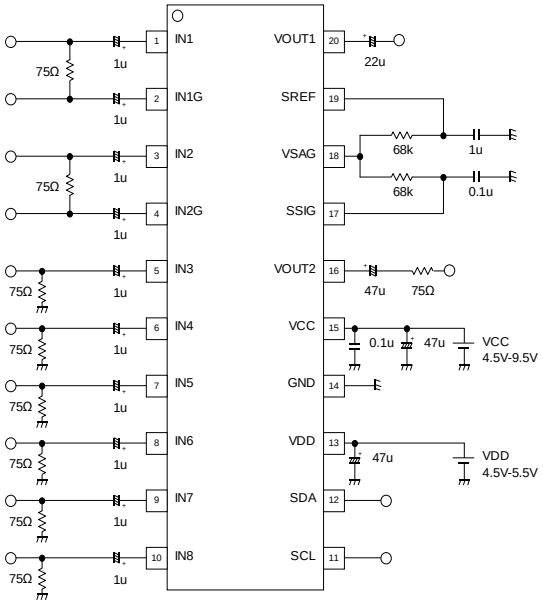
■GENERAL DESCRIPTION

NJW1341 is 8-Input, 2-Output Video Switch. It consists of switch and isolation amplifiers (2input) and Video Driver which features 47μF AC-coupled(1output). All of functions are controlled by I2C Bus.

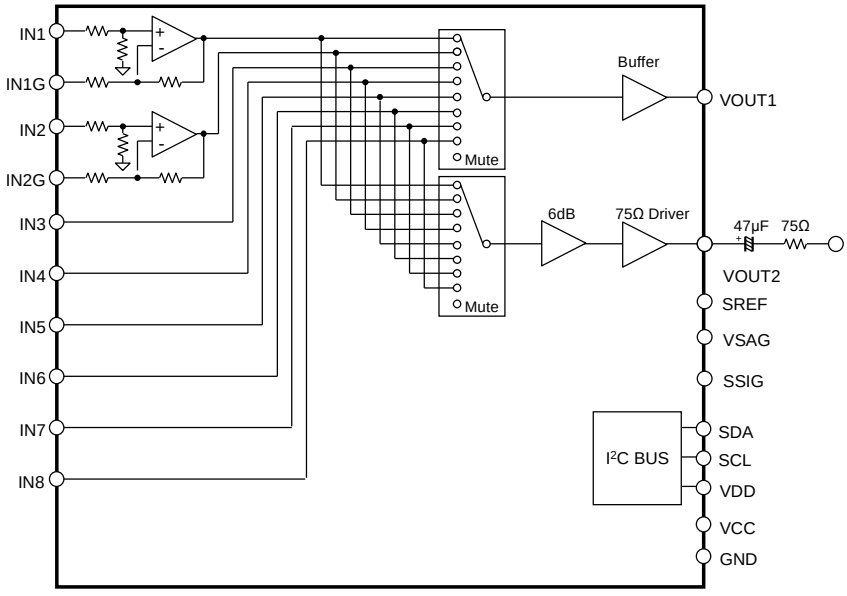
■APPLICATION

- ●Car Navigation

■APPLICATION CIRCUIT



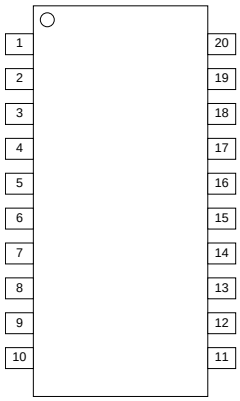
■EQUIVALENT CIRCUIT・BLOCK DIAGRAM



■47μF Output Capacitor Series

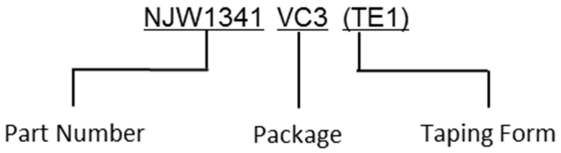
Input-Output	Part No.
3in-1out	NJM41050
4in-2out	NJW1342

■PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	IN1	Video Signal Input Terminal
2	IN1G	GND Input Terminal (from souse side)
3	IN2	Video Signal Input Terminal
4	IN2G	GND Input Terminal (from souse side)
5	IN3	Video Signal Input Terminal
6	IN4	Video Signal Input Terminal
7	IN5	Video Signal Input Terminal
8	IN6	Video Signal Input Terminal
9	IN7	Video Signal Input Terminal
10	IN8	Video Signal Input Terminal
11	SCL	I^2C Clock Input Terminal
12	SDA	I^2C Data Input Terminal
13	VDD	Power Supply Terminal
14	GND	GND Terminal
15	VCC	Power Supply Terminal
16	VOUT2	Video Signal Output Terminal
17	SSIG	SAG Correction Terminal
18	VSAG	SAG Correction Terminal
19	SREF	SAG Correction Terminal
20	VOUT1	Video Signal Output Terminal

■MARK INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJW1341VC3	SSOP20-C3	Yes	Yes	Sn-2Bi	1341	89	2,000

■ABSOLUTE MAXIMUM RATINGS

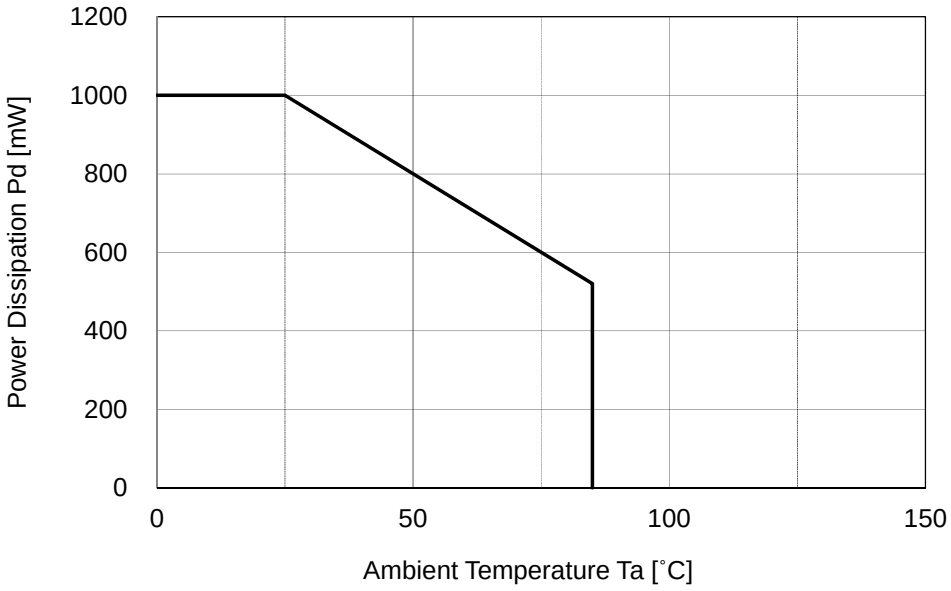
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage 1	VCC	13.0	V
Supply Voltage 2	VDD	7.0	V
Power Dissipation (Ta=25°C)	P_D	1,000(1)	mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(1) At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm Two layers, FR-4)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Voltage 1	VCC	4.5 to 9.5	V
Operating Voltage 2	VDD	4.5 to 5.5	V

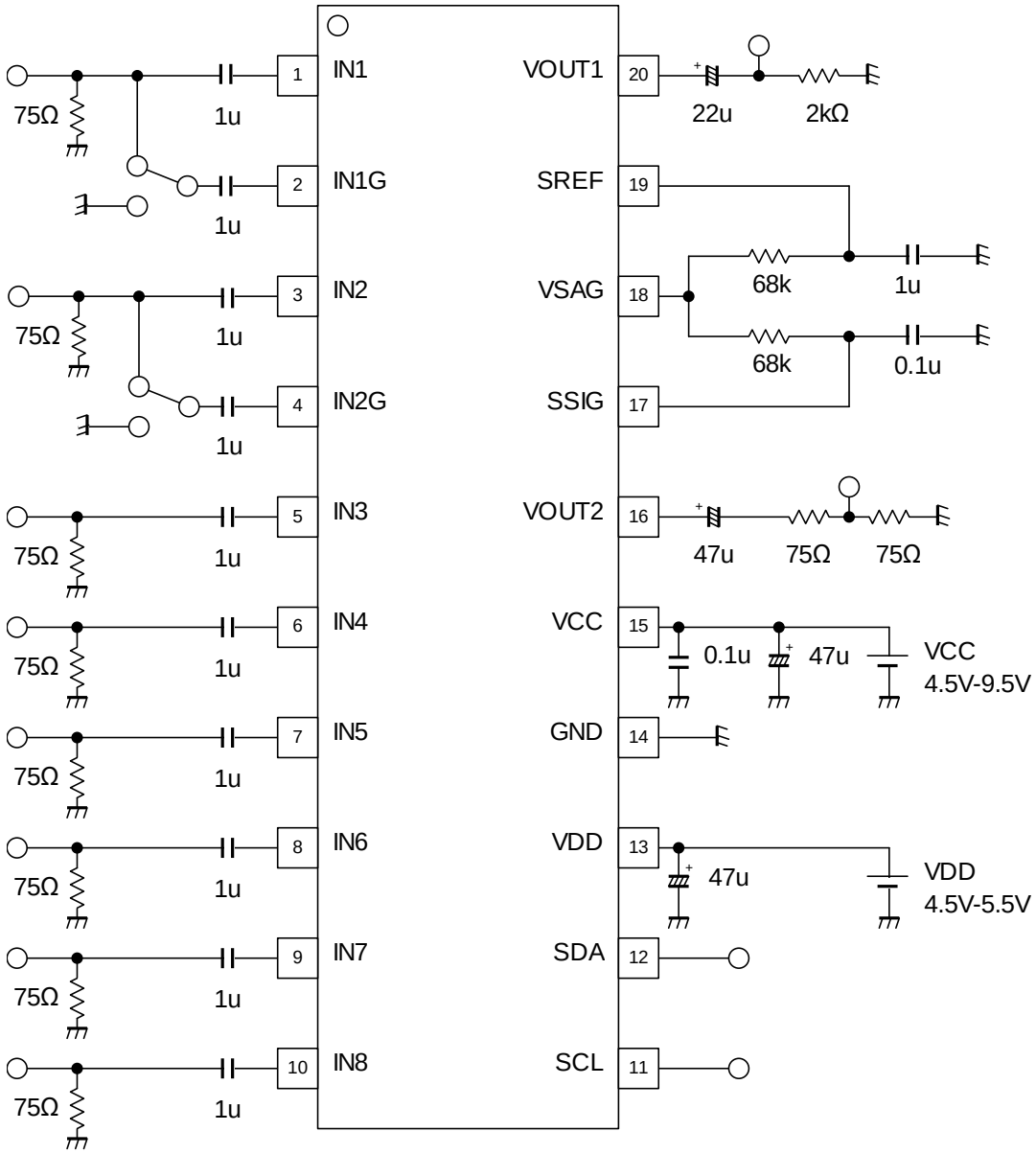
■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■**ELECTRICAL CHARACTERISTICS** (Ta=25°C, VCC=VDD=5V, unless otherwise specified)

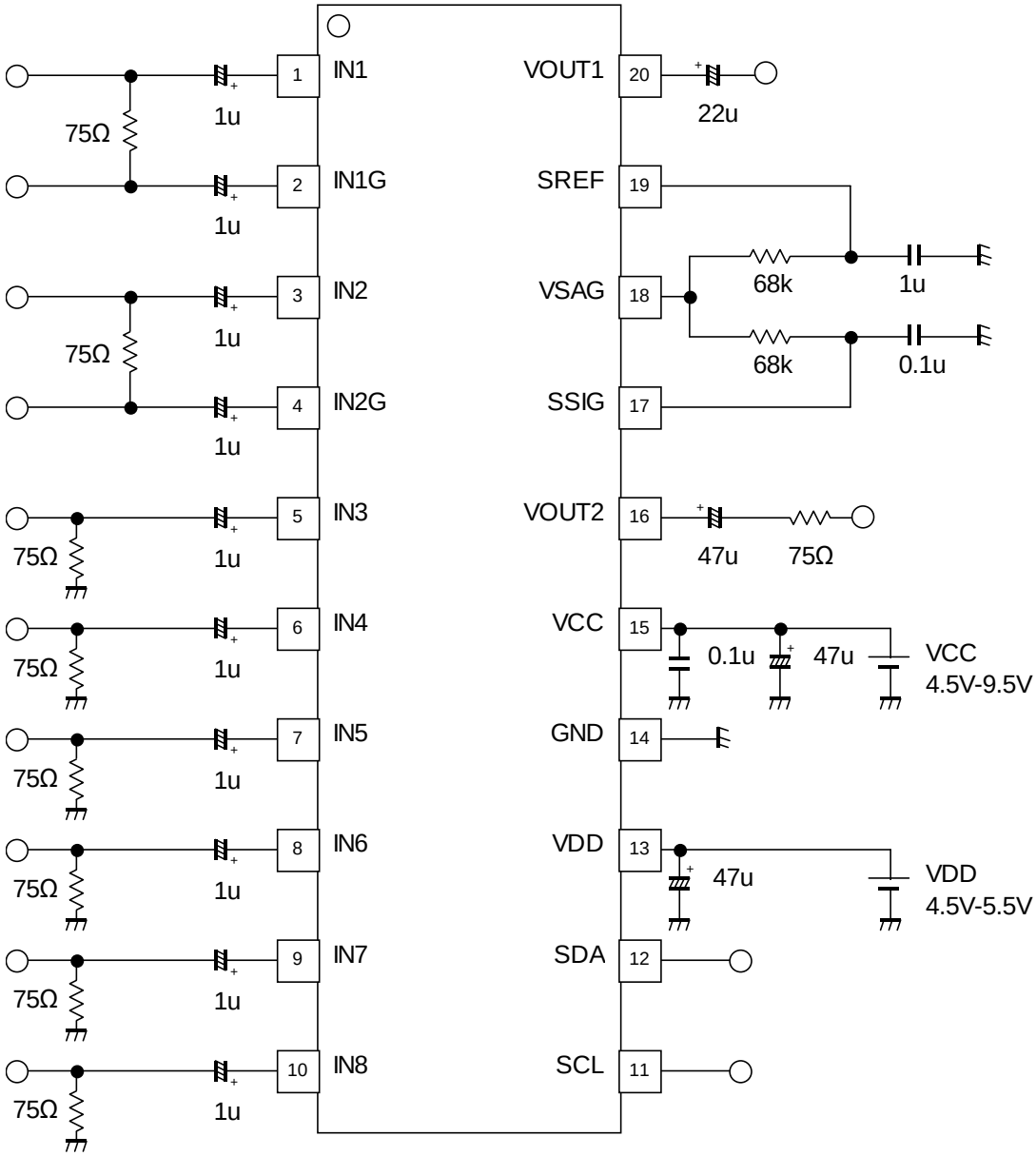
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current 1	I_{CC1}	No, signal	-	25	40	mA
Supply Current 2	I_{CC2}	OUT2 power save, OUT1 active	-	10	15	mA
Supply Current 3	I_{CC3}	OUT1power save, OUT2 active	-	20	35	mA
Supply Current at Power Save Mode	Isave	OUT1,OUT2 power save		2	4	mA
Maximum Output Level	Vom	f=100kHz,THD=1%	2.4	-	-	Vp-p
Frequency Characteristics	Gf	Vin=10MHz /1MHz, 1.0Vp-p Sine Signal	-1.0	0	1.0	dB
Voltage Gain 1	Gv1	OUT1,Vin=1MHz,1.0Vp-p,Sine Signal	-1.0	0	1.0	dB
Voltage Gain 2	Gv2	OUT2,Vin=1MHz,1.0Vp-p,Sine Signal	5.5	6.0	6.5	dB
Differential Gain	DG	Vin=1.0Vp-p 10step video signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step video signal	-	0.5	-	deg
S/N Ratio	SN	Vin=1.0Vp-p, 100% White video signal, RL=75Ω, 100KHz to 6MHz	-	60	-	dB
Common mode Rejection Ratio	CMR	Vin=20kHz, 1.0Vp-p Sine Signal	-	-55	-	dB
CrossTalk	CT	Vin=4.43MHz, 1.0Vp-p Sine Signal		-60		dB

■TEST CIRCUIT



Note) NJW1341 has possibilities that decrease in the capacitance in low-frequency band when the ceramic capacitor is used (pin16). It is a possibility that the sag is generated when the ceramic capacitor decreases capacity. Please verify it in consideration of the capacity drop of the ceramic capacitor.

■APPLICATION CIRCUIT



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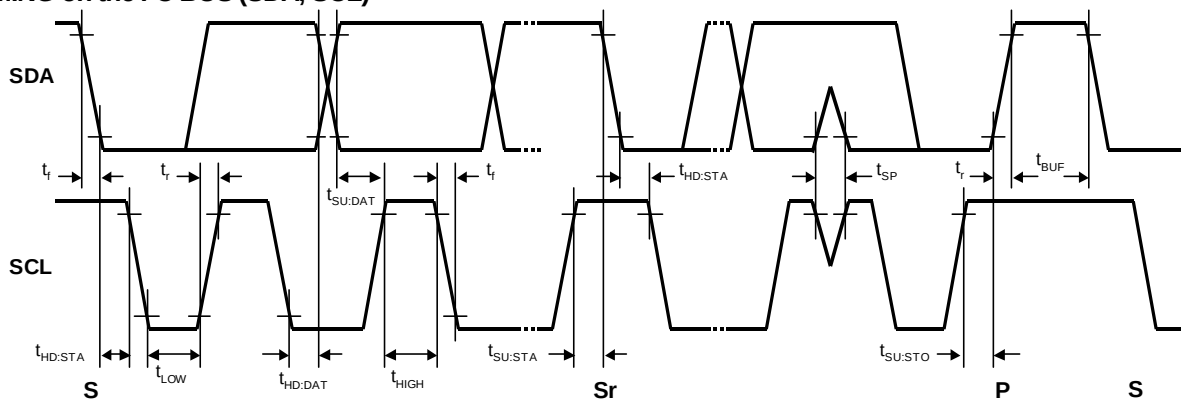
■TIMING on the I²C BUS (SDA, SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

STANDARD MODE: Pull up resistance 4kΩ (Connected to +5.0V), Load capacitance 200pF (Connected to GND)

FAST MODE: Pull up resistance 4kΩ (Connected to +5.0V), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	2.7	-	5.0	2.7	-	5.0	V
Low level Output Voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	0	-	0.4	V
Input Current each I/O pin with an Input Voltage between 0.1 and 0.9V_{DDmax}	I_i	-10	-	10	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C BUS DEVICES

PARAMETER	SYMBOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL Clock Frequency	f_{SCL}	-	-	100	-	-	400	kHz
Data Transfer Start Minimum Waiting Time	$t_{HD:STA}$	4.0	-	-	0.6	-	-	µs
Low Level Clock Pulse Width	t_{LOW}	4.7	-	-	1.3	-	-	µs
High Level Clock Pulse Width	t_{HIGH}	4.0	-	-	0.6	-	-	µs
Minimum Start Preparation Waiting Time	$t_{SU:STA}$	4.7	-	-	0.6	-	-	µs
Minimum Data Hold Time NOTE)	$t_{HD:DAT}$	0.0	-	-	0.0	-	-	µs
Minimum Data Preparation Time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise Time	t_r	-	-	1000	-	-	300	ns
Fall Time	t_f	-	-	300	-	-	300	ns
Minimum Stop Preparation Waiting Time	$t_{SU:STO}$	4.0	-	-	0.6	-	-	µs
Data Change Minimum Waiting Time	t_{BUF}	4.7	-	-	1.3	-	-	µs
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise Margin at the Low Level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise Margin at the High Level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF.

NOTE). Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

■DEFINITION OF I²C REGISTER

I²C BUS FORMAT

MSB		LSB	MSB		LSB	
S	Slave Address	A	Data		A	P
1bit	8bit	1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

SLAVE ADDRESS

MSB							LSB
0	0	1	0	0	0	0	0

R/W=0: Receive Only
R/W=1: Data is not transmitted.

■CONTROL REGISTER DEFAULT VALUE

Control register default values are as follows :

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	0	0	0	0	0	0	0	0

■INSTRUCTION CODE

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	OUT1 MUTE	OUT1 Select			OUT2 MUTE	OUT2 Select		

■MUTE TABLE

MUTE D7	OUT1
0	MUTE OFF
1	MUTE ON

MUTE D3	OUT2
0	MUTE OFF
1	MUTE ON

MUTE OFF: Active mode
MUTE ON: Power save mode

■VOUT SELECT TABLE

OUT1 Select			OUT1
D6	D5	D4	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8

OUT2 Select			OUT2
D2	D1	D0	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8

■About the ASC(Advanced SAG Correction) circuit

Advanced SAG Correction circuit is our own sag correction technology (patent). It can reduce the output coupling capacitor than conventional sag correction circuit. You can use the ASC circuit, it will contribute to space saving. Also, because it is not in the output capacitor-less, does not have any anxiety which the output is short-circuited.

This section describes the following four items.

1) Overview of the ASC circuit
2) How to set up an external circuit
3) Circuit example of when the two systems drive
4) Notes on Using

1) Overview of the ASC circuit

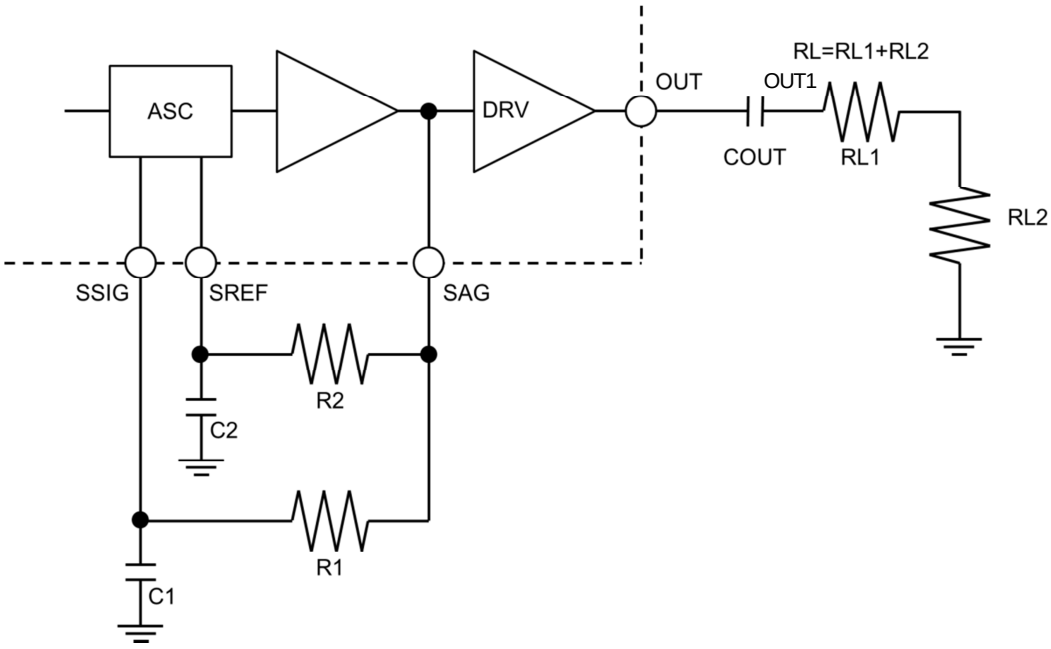
A high-pass filter in the load resistance and output coupling capacitor is configured. Sag occurs because the low-frequency component of the signal is attenuated by this high-pass filter. ASC circuit amplifies the low-frequency component of the signal, corrects for attenuation of the low-frequency component.

The figure below shows ASC around circuit.

SAG terminal is a signal output terminal for correcting the sag. Low pass filter of the resistor R1 and the capacitor C1 will cancel the high-pass filter of the load resistor RL and an output coupling capacitor which is connected to the OUT terminal. And, it is connected to the SSIG terminal. The signal input to the SSIG terminal by processing inside the IC, and generates a signal for correcting the sag.

ASC circuit for amplification the low frequency components of the signal, require a wide dynamic range. The low-pass filter of the resistor R2 and the capacitor C2, to generate a signal of APL (Average Picture Level) voltage. And input to the VREF terminal. Use this voltage of SREF terminal it has to optimize the voltage of the internal IC. ASC circuit generates a sag correction waveform by processing the signal of SSIG terminal and SREF terminal. If sag correction component is large, it may exceed the dynamic range of IC. ASC circuit will stop the operation of the sag correction function if it exceeds the dynamic range by sag correction circuit. Therefore, and preventing that the signal is clipped to fit within the dynamic range.

< ASC around circuit >



2) How to set up an external circuit

This section describes the constant setting steps of the ASC around circuit.

1: First, determine the cut-off frequency: fcout of the high-pass filter to resistance: RL and the output capacitor: COUT of the OUT terminal is configured.

The output capacitor: COUT, please be more than 47uF.

$$fcout = \frac{1}{2\pi \cdot COUT \cdot RL}$$

2: The low-pass filter with a resistor R1 (> 10kΩ) and capacitor C1 is configured. Please refer to the cut-off frequency fc1 the same as fcout.

$$fc1 = \frac{1}{2\pi \cdot C1 \cdot R1} = fcout$$

3: The low-pass filter with a resistor R2 (> 10kΩ) and capacitor C2 is configured. Please do cut-off frequency fc2 is less than or equal to 3Hz.

$$fc2 = \frac{1}{2\pi \cdot C2 \cdot R2} \le 3$$

4: Please make sure that the combined resistance R1 // R2 of the resistors R1 and R2 is equal to or more than 5kΩ. And please check the sag characteristics.

Parameter Set example

Set the constant in the case where the output capacitor COUT = 47uF, and a resistor RL = 150Ω.

1. Calculate the cut-off frequency of the high-pass filter formed by capacitor 47uF and resistance 150Ω of OUT terminal.

$$fcout = \frac{1}{2\pi \cdot COUT \cdot RL} = \frac{1}{2\pi \cdot 47u \cdot 150} = 22.6[Hz]$$

2. LPF is configured by a resistor R1 (> 10kΩ) and capacitor C1, and so the cut-off frequency fc1 is the same as fcout.

$$fc1 = \frac{1}{2\pi \cdot C1 \cdot R1} = \frac{1}{2\pi \cdot 0.1u \cdot R1} = 22.6$$

$$R1 = \frac{1}{2\pi \cdot 0.1u \cdot 22.6} = 70.4[k\Omega] \cong 68[k\Omega]$$

Calculation results of the resistor R1 is 70.4kΩ. Here are the 68kΩ available at E6 series.

3. LPF is configured by a resistor R2 (> 10kΩ) and capacitor C2, and cut-off frequency fc2 is set to be less t than 3Hz. When the capacitor C2 to 1uF, and will be as follows.

$$fc2 = \frac{1}{2\pi \cdot C2 \cdot R2} = \frac{1}{2\pi \cdot 1u \cdot R2} < 3$$

$$R2 > \frac{1}{2\pi \cdot 1u \cdot 3} = 53[k\Omega] \Rightarrow 68[k\Omega]$$

Calculation results of the resistor R2 must be more than or equal to 53kΩ. Therefore, it is the resistor R1 and the same 68kΩ.

4. Make sure that the combined resistance of R1 and R2 is equal to or more than 5kΩ

$$R1 // R2 = 68k // 68k = 34k$$

After constant determination, each characteristic is please makes sure that there is no problem.

This setting example is the same as the test circuit diagram of the data sheet.

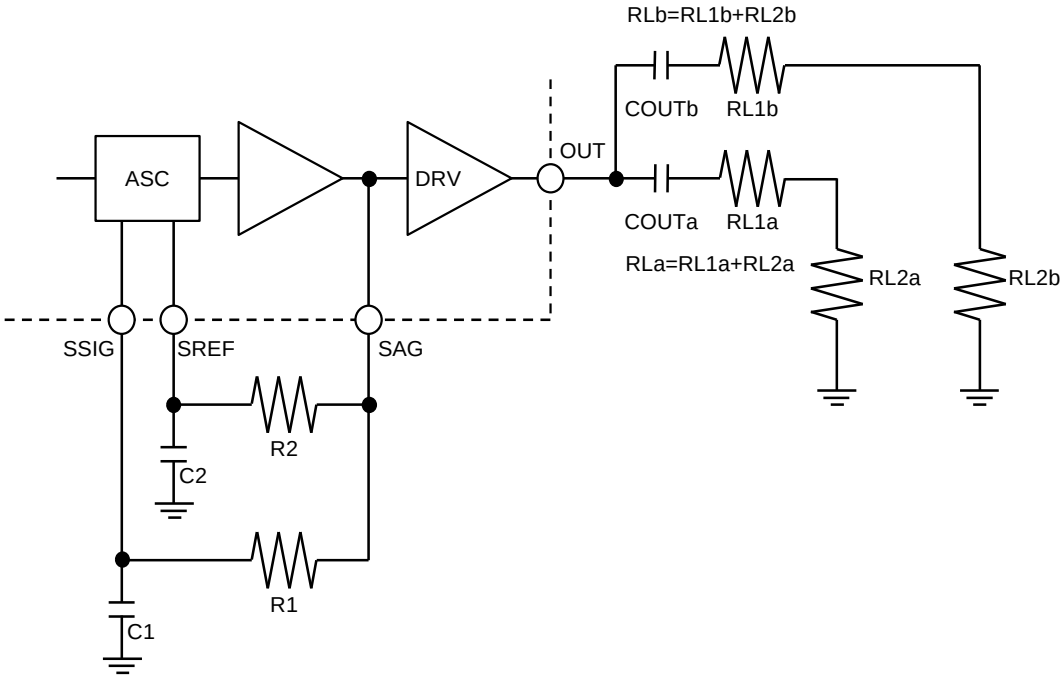
3) Circuit example of two systems drive

An example of a circuit of the two systems drive is shown in the following figure. In the case of a two-system drive, the output capacitor requires COUTa and COUTb. As the cut-off frequency of the high-pass filter is the same, the output capacitor (COUTa, COUTb) and resistance (RLa, RLb) please set.

$$fcout = \frac{1}{2\pi \cdot COUTa \cdot RLa} = \frac{1}{2\pi \cdot COUTb \cdot RLb}$$

Element constant of SAG terminal and SSIG terminal and SREF terminal, please set according to the previous section on how to set up.

< Two system drive circuit >



4) Usage note

Resistance value of SAG terminal R (= R1 // R2), please be more than 5kΩ.

If the resistance is small, the signal to output to the OUT terminal may be distorted.

Wiring of SAG terminal and SREF terminal and SSIG terminal please do as much as possible short.

If the noise is mixed to these terminals, the noise is mixed in signals output to the OUT terminal.

If you want to use a ceramic capacitor, please use a capacitor with good DC bias characteristics.

Ceramic capacitors, capacitance value will vary depending on the DC voltage to be applied. This characteristic is referred to as the DC bias characteristics. There is the actual capacitance value and the desired capacitance value is shifted by this DC bias characteristics. Thereby, it may sag correction function does not work well.

You may also set the constants of external elements does not work sag correction function.

If sag correction component is large, it becomes a waveform signal exceeds the dynamic range of the IC.

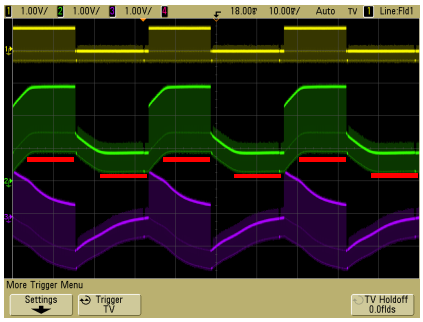
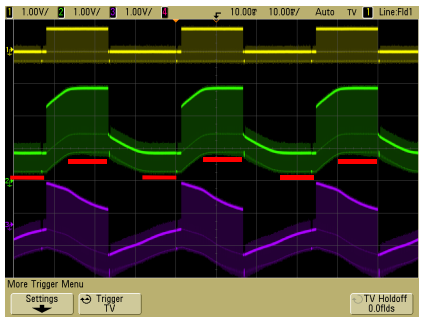
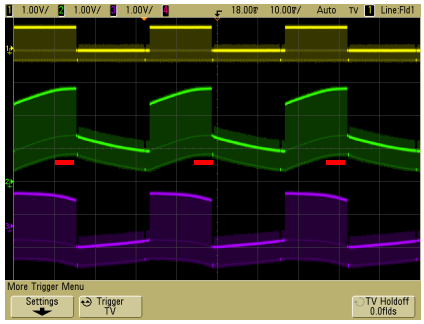
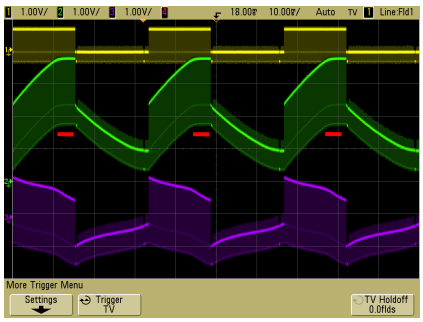
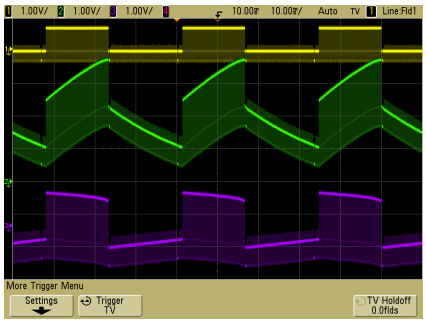
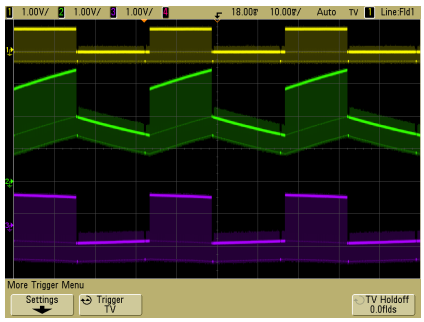
In order to prevent that the signal exceeds the dynamic range is to clip, ASC circuit will stop the sag correction function.

In this case, whether to enhance the power supply voltage, or change each element constant by increasing the output capacitor

■**Waveform example**

Input: Bounce signal (IRE0%, IRE100%, 30Hz), RL=150Ω

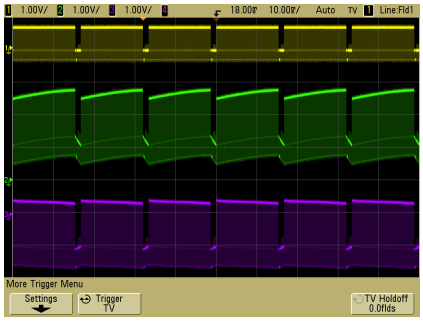
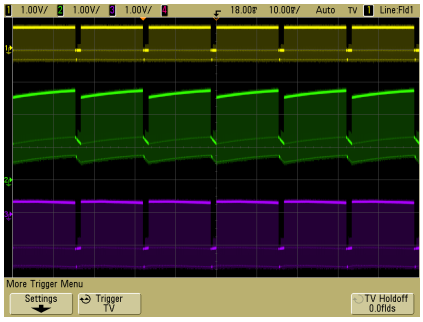
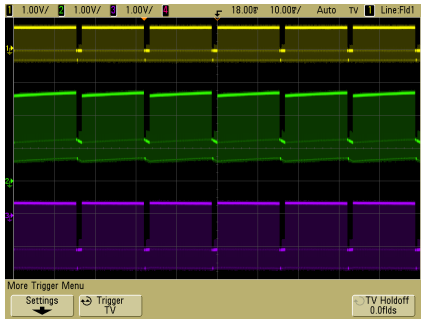
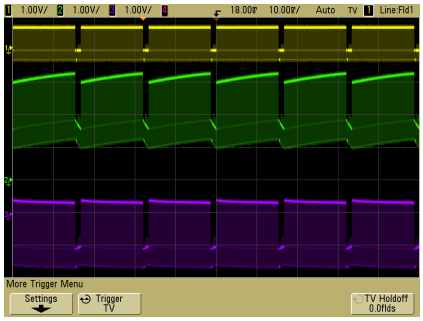
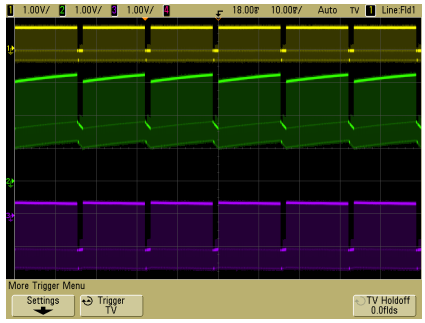
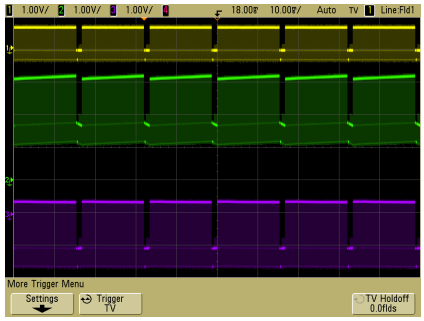
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal, red = Sag correction stop period

	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	**Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF**	**Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF**
Vcc=3.0V			
Vcc=5.0V			

If the power supply voltage is low, if the output capacitor is small, to prevent signal clipping beyond the dynamic range of the OUT terminal, sag correction function stops.

Input: White 100%, RL=150Ω

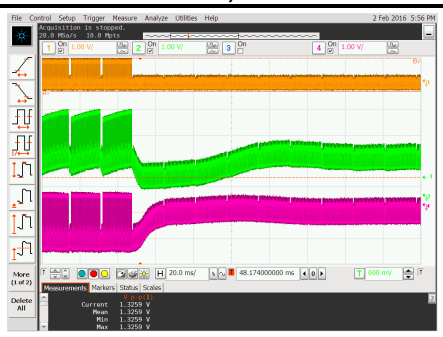
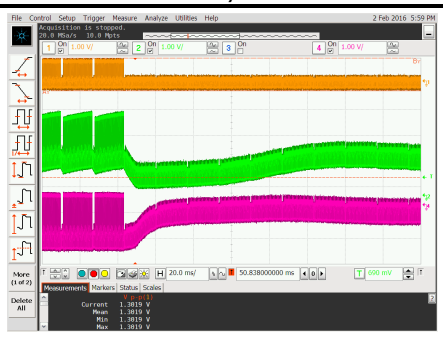
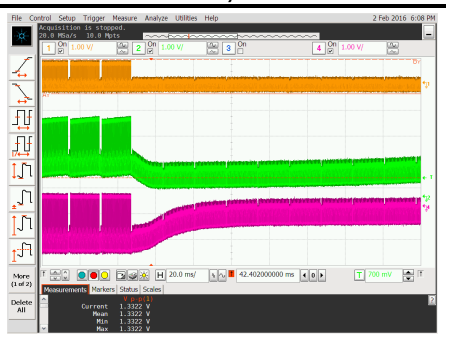
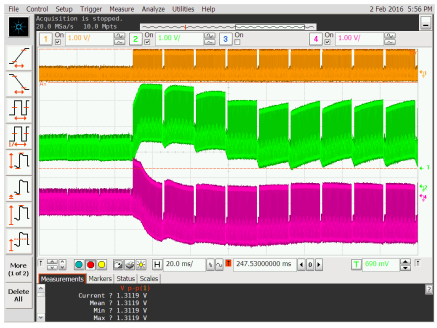
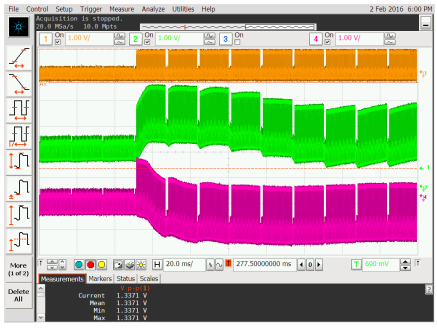
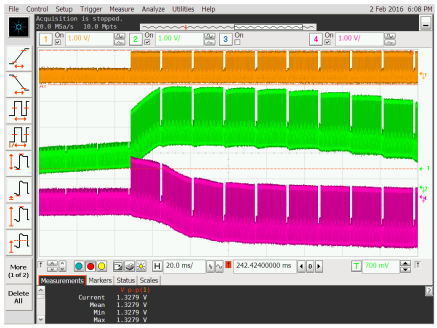
Waveform: yellow = Input signal, green = Output signal, purple = OUT1 signal

	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	**Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF**	**Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF**
Vcc=3.0V			
Vcc=5.0V			

■**Waveform example at Black-and-White change**

Input: Black-and-White change signal, RL=150Ω

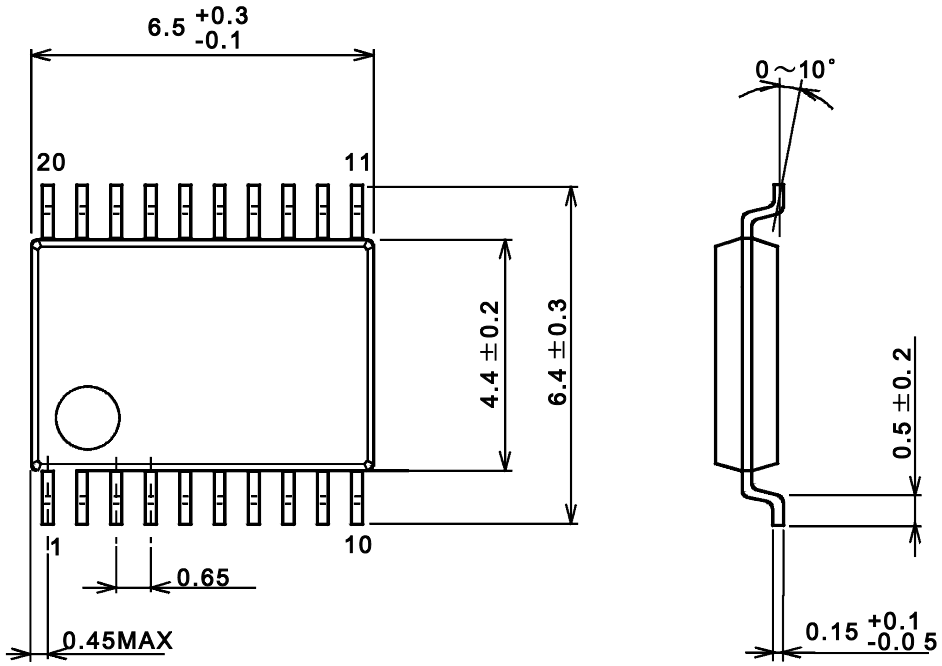
Waveform: yellow = Input signal, green = Output signal, red = OUT1 signal

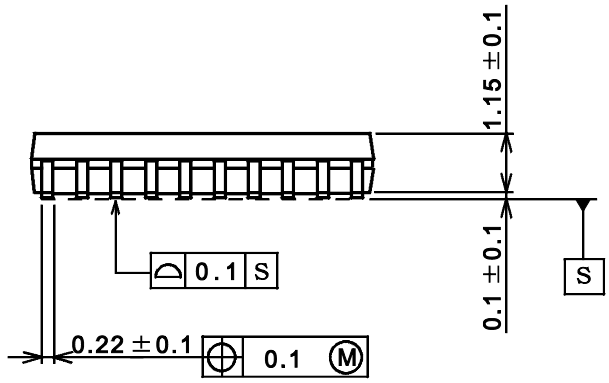
	Cout=33uF,R1=R2=51kΩ, C1=0.1uF,C2=1uF	**Cout=47uF,R1=R2=68kΩ, C1=0.1uF,C2=1uF**	**Cout=100uF,R1=R2=150kΩ, C1=0.1uF,C2=1uF**
Vcc=5.0V 白黒			
Vcc=5.0V 黒白			

DC level will change by APL fluctuation at the black-and-white change. The rate of change of the DC level is dependent on the capacitance value of Cout.

■PACKAGE OUTLINE

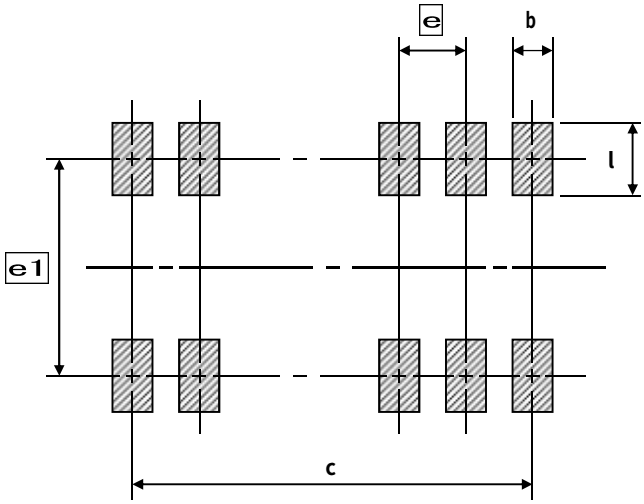
SSOP20-C3





■SOLDER FOOT PRINT

PKG	b	l	c	e1	e
SSOP20-C3	0.35	1.00	5.85	5.90	0.65



Note : These solder foot print dimensions are just examples.
When designing PCB, please estimate the pattern carefully.

Unit : mm

■PACKING SPECIFICATION

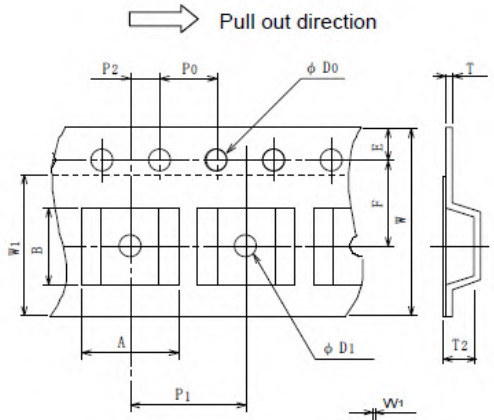
General Description

NJRC delivers ICs in 4 methods, plastic tube container, two kinds of Taping, tray and vinyl bag packing. Except adhesive tape treated anti electrostatic and contain carbon are using as the ESD (Electrostatic Discharge Damage) protection.

SSOP Emboss Taping(TE1)

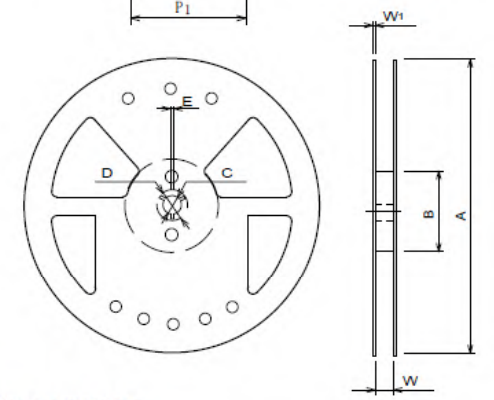
Symbol	SSOP20-C3	Remark
A	6.7	Bottom size
B	6.9	Bottom size
D_0	1.55±0.05	
D_1	1.55±0.1	
E	1.75±0.1	
F	5.5±0.05	
P_0	4.0±0.1	
P_1	8.0±0.1	
P_2	2.0±0.05	
T	0.3±0.05	
T_2	1.9	
W	12.0±0.3	
W_1	9.5	Thickness 0.1MAX

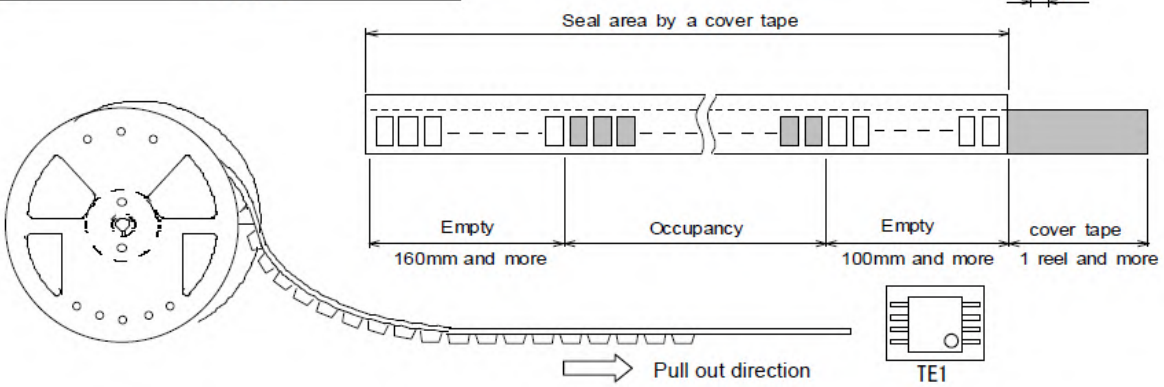
Unit : mm

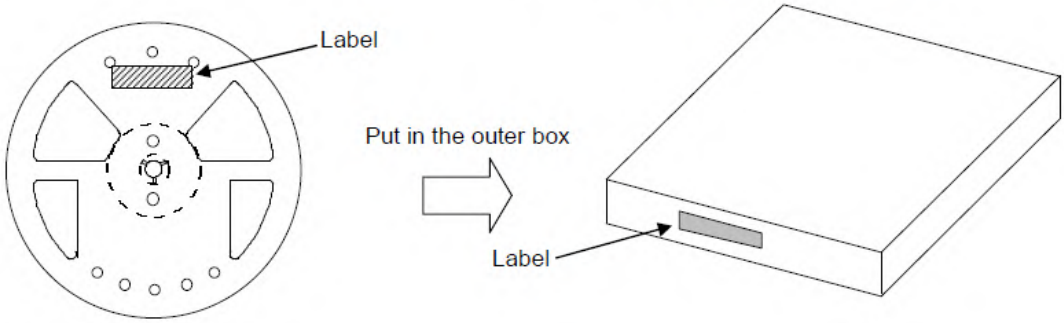


Symbol	SSOP20-C3
A	Ø254±2
B	Ø100±1
C	Ø13±0.2
D	Ø21±0.8
E	2±0.5
W	13.5±0.5
W_1	2±0.2
Contents	2,000 pcs

Unit : mm

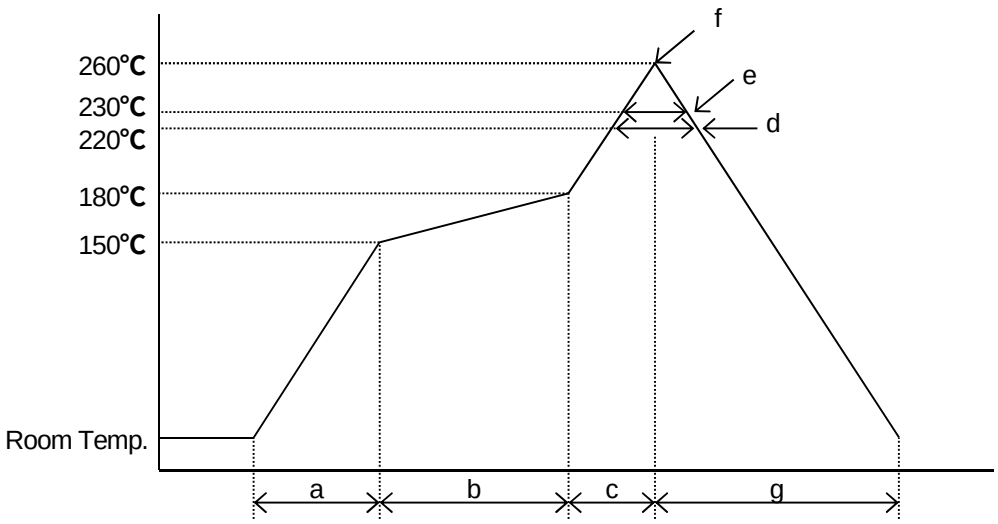






■RECOMMENDED MOUNTING METHOD

∗Recommended reflow soldering procedure



a：Temperature ramping rate	: 1 to 4℃/s
b：Pre-heating temperature	: 150 to 180℃
time	: 60 to 120s
c：Temperature ramp rate	: 1 to 4℃/s
d：220℃ or higher time	: Shorter than 60s
e：230℃ or higher time	: Shorter than 40s
f：Peak temperature	: Lower than 260℃
g：Temperature ramping rate	: 1 to 6℃/s

The temperature indicates at the surface of mold package.

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