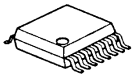
PLL Synthesizer with I²C Bus for TV Tuner

■ DESCRIPTION

The NJW1504/1508 are a PLL frequency synthesizer especially designed for TV and VCR tuning systems and consists of PLL circuit and a prescaler which operates up to 1.0GHz, built into one chip.

The NJW1504/1508 are controlled through an I²C-bus.

■ PACKAGE OUTLINE

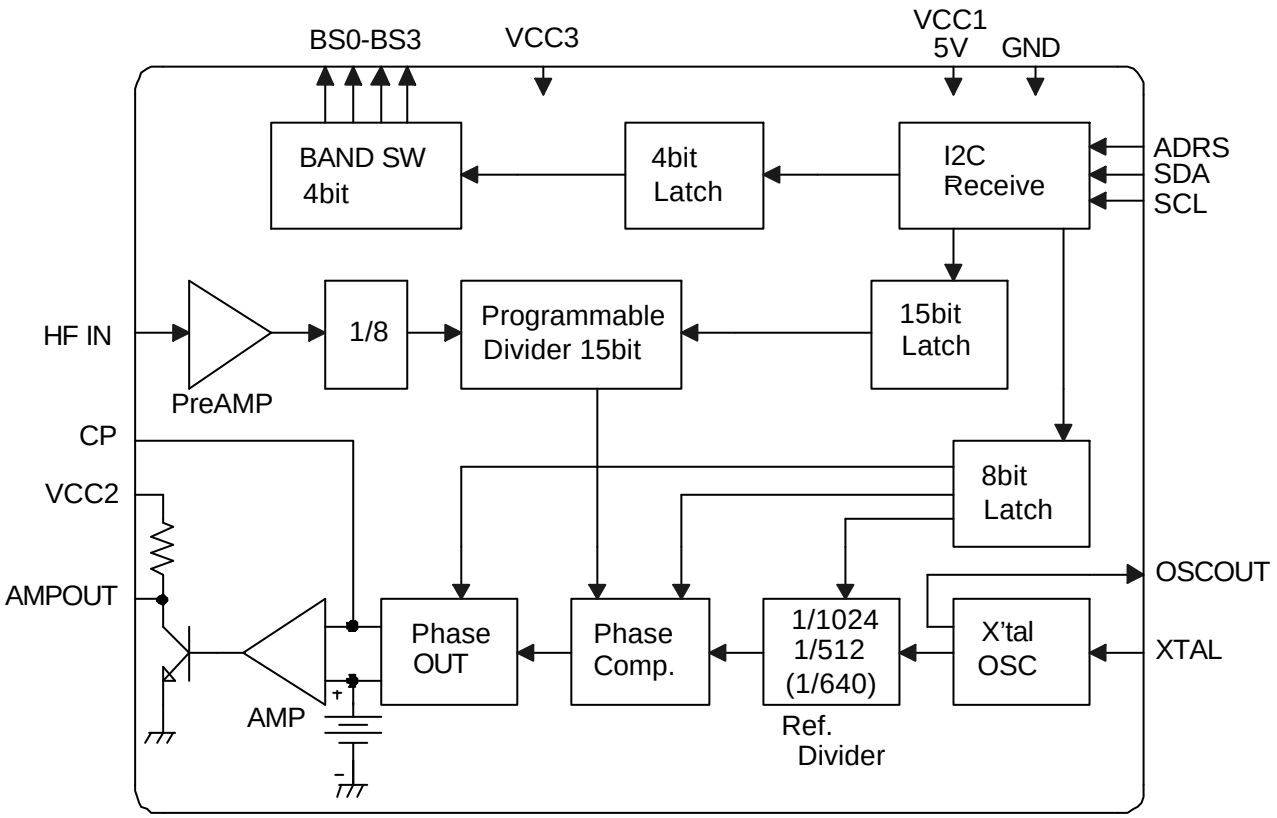


NJW1504V/NJW1508V

■ FEATURES

- Operating Voltage 5V
- Low Operating Current : 15mA typ. @Vcc=5V
- Prescaler accepts frequencies up to 1GHz on chip
- Reference Signal :
  NJW1504: Reference Signal Oscillator with peripheral of Xtal on chip
  NJW1508: Buffer Amplifier for External Reference Signal on chip
- 34V max. tuning voltage output
- Package Outline: SSOP16

■ BLOCK DIAGRAM



(Note)

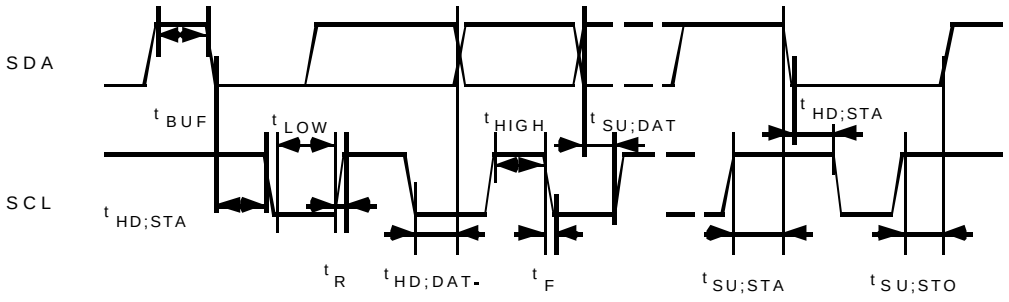
Purchase of I²C components of New Japan RadioCo.,Ltd or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C standard specification as definedby by Philips.

■ **ABSOLUTE MAXIMUM RATINGS** (T_A=25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage (Vcc1, 3)	Vcc1, Vcc3	-0.3 to +6.5	V
Supply Voltage (Vcc2)	Vcc2	-0.3 to +36	V
Input Voltage (except I^2C bus)	Vi	-0.3 to Vcc+0.3	V
Output Voltage (except I^2C bus)	Vo	-0.3 to Vcc+0.3	V
I^2C bus Input Voltage	V_{iiic}	-0.3 to 6.5	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	-20 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C

■ **RECOMMENDED OPERATING CONDITION** (T_A=25°C)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage	Vcc1, Vcc3	Vcc1, Vcc3	4.5	5	5.5	V
Operating Voltage	Vcc2	Vcc2	0	-	34	V
X'tal Operating Range		f_{xtal}	3.15	4	4.05	MHz
HF Input Frequency	Input= -20dBm	f_{hf}	80	-	1000	MHz
Clock Frequency	Refer to I^2C bus Timing Chart	f_{SCL}	0	-	100	KHz
Bus Free Time		t_{BUF}	4.7	-	-	uS
Data Hold Time		t_{HDSTA}	2	-	-	uS
SCL Low Hold Time		t_{LOW}	4.7	-	-	uS
SCL High Hold Time		t_{HIGH}	2	-	-	uS
Set-up Time		t_{SUSTA}	2	-	-	uS
Data Hold Time		t_{HDDAT}	0	-	-	uS
Data Set-up Time		t_{SUDAT}	250	-	-	nS
Rise Time		t_R	-	-	1000	nS
Fall Time		t_F	-	-	300	nS
Data Set-up Time		t_{SUSTO}	4	-	-	uS



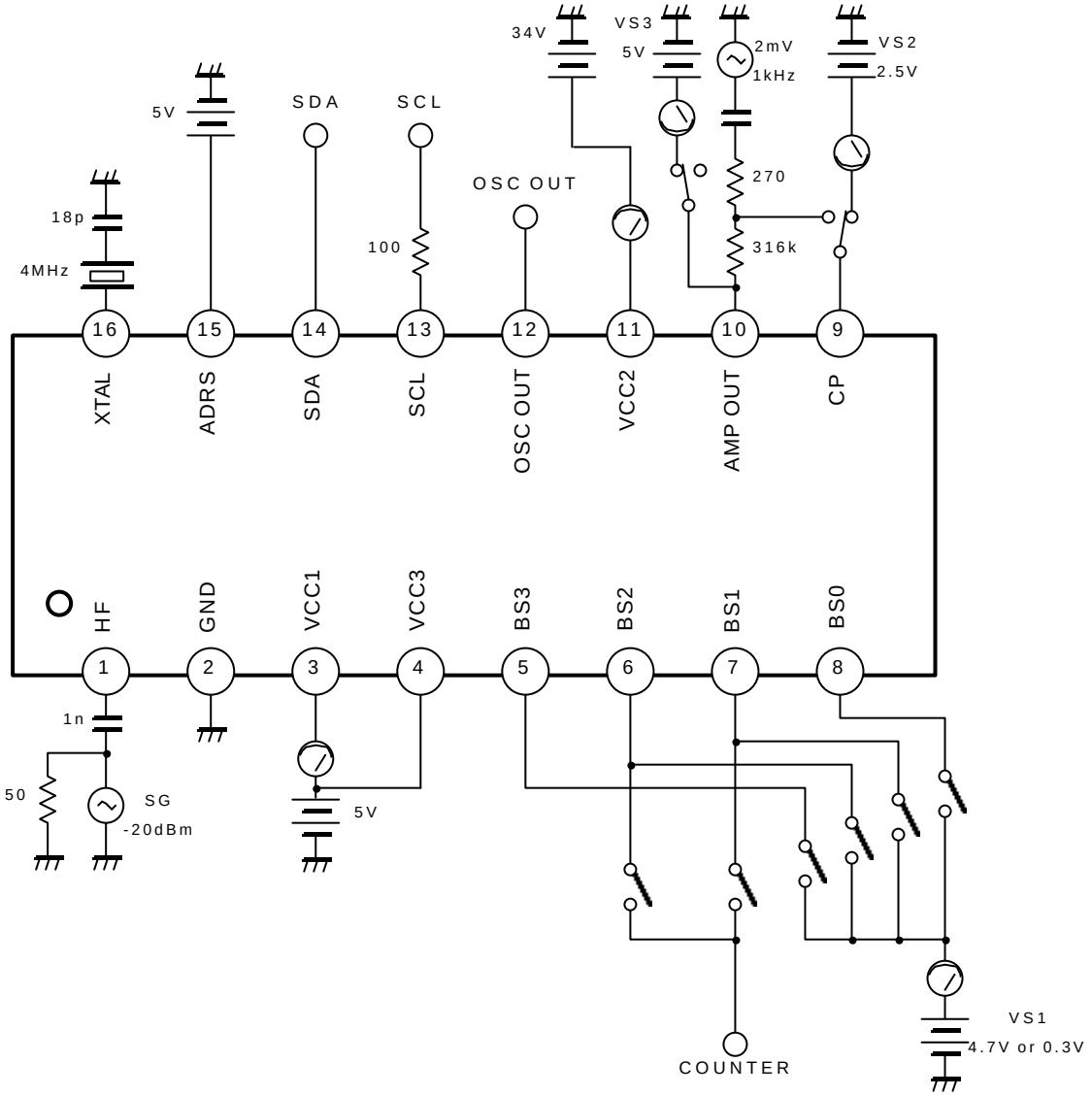
I^2C bus Timing Chart

V_{IH}min(0.7 Vcc1) and V_{IL}max(0.3 Vcc1)

■ **ELECTRICAL CHARACTERISTICS** (Vcc1,3=5V,Vcc2=34V,T_A=25°C)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating Current 1	f_{HF}=100MHz	I_{CC}	12	15	21	mA
Operating Current 2	AMPOUT: Low Level	$I_{CC}2$	-	1.6	-	mA
AMP Input Current	Phase OUT: High Imp (2.5V)	I_{IN}	(-50)	0.1	(50)	nA
AMP Output Current	ANP OUT: Low Level AMPOUT Input=5V	I_{OUT}	-	-	-2	mA
AMP Gain	f=1KHz	AV	40	50	60	dB
Phase Comparator Output Current	Current Source	I_{sourse}	190	280	400	uA
Phase Comparator Output Current	Current Sink	I_{sink}	-400	-280	-190	uA
Band Switch						
"L" Output Current	BS0=BS1=0.3V	$I_{OBS0-1L}$	-2.0	-1	0	mA
"H" Output Current	BS0=BS1=4.7V	$I_{OBS0-1H}$	11.0	15.0	-	mA
"L" Output Current	BS2=BS3=0.3V	$I_{OBS2-3L}$	-2.0	-1.0	0	mA
"H" Output Current	BS2=BS3=4.7V	$I_{OBS2-3H}$	5.5	7.5	-	mA
I^2C bus						
"H" Input Current	SCL, SDA Terminal	$I_{IN}H$	-5	0	5	uA
"L" Input Current	SCL, SDA Terminal	$I_{IN}L$	-5	0	5	uA
"H" Input Voltage Range	SCL, SDA Terminal	V_{IH}	3.5	-	5.3	V
"L" Input Voltage Range	SCL, SDA Terminal	V_{IL}	0	-	1.5	V
ACK Sink Current	ACK Output, SDA=0.4V	V_{ACK}	3	-	-	mA

■ **TEST CIRCUIT**



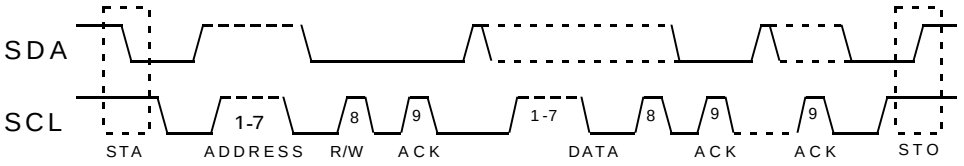
■ **I²C bus Protocols**

The input information, which consists of chip address and next two or four byte data, is received by I²C bus receiver. The allowable I²C bus protocols are as follows.

(1) STA CA CB BB STO
(2) STA CA D1 D2 STO
(3) STA CA CB BB D1 D2 STO
(4) STA CA D1 D2 CB BB STO

STA: Start Condition
STO: Stop Condition
CA: Chip Address
CB: Control Byte
BB: Band switch Byte
D1: Divider Byte 1
D2: Divider Byte 2

For suitable circuit operation,5-byte data should have chip address, 2-byte control data, band data, and 2-byte divider byte. Following chip address. 2-byte data is received. For distinction of each data, first and third data byte has a function bit. As function bit, divider byte has "1" and control/band data has "0".



■ **Data Format**

Parameter	Symbol	MSB								LSB
Chip Address	CA	1	1	0	0	0	CA1	CA0	0	A
Divider Byte 1	D1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider Byte 2	D2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte	CB	1	CP	T2	T1	T0	RD1	RD0	×	A
Band switch Byte	BB	×	×	×	×	BS3	BS2	BS1	BS0	A

· Data specifications

× : don't care ;0 or 1

CA1, CA0 : Programmable address bits

ADRS Voltage	CA1	CA0
Always valid	0	1
0 to 0.1 Vcc1	0	0
0.4 Vcc1 to 0.6 Vcc1	1	0
0.9 Vcc1 to Vcc1	1	1

BS0 to BS3 : Band switch buffers Control bits, BSn=1 then "ON"

N0 to N14 : Control of Programmable divider bits, N14=MSB N0=LSB

Dividing ratio : $N=2^{14}\times N14+2^{13}\times N13+\cdots\cdots+2^{1}\times N1+N0$

Maximum division ratio 32767

Minimum division ratio 256

CP : Charge Pump Current

CP	Charge Pump Current	Conditions
1	280µA	Normal, Default
0	60µA	Test

T0 to T2 :Test mode bits

T0,T1,T2 :Phase Comparator Output bits

T2	T1	T0	Phase Comparator, Band Switch	Conditions
0	0	×	Normal Output	Normal, Default
1	0	1	Phase Comparator (High Impedance)	Test
1	1	0	Phase Comparator (Sink)	Test
1	1	1	Phase Comparator (Source)	Test

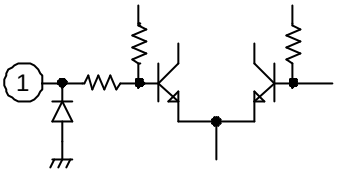
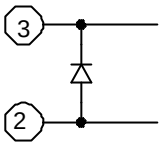
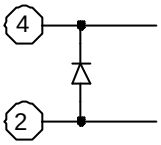
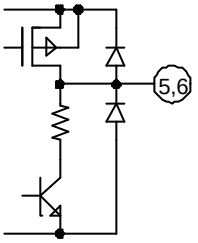
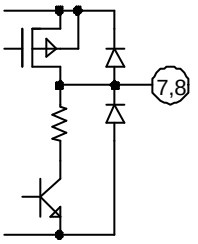
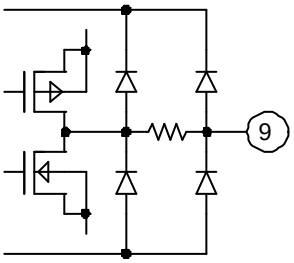
RD1,RD0 : Reference Divider bits

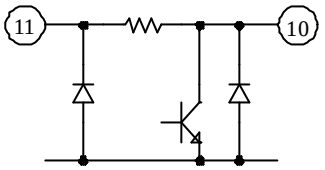
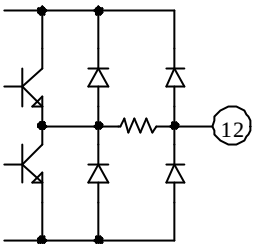
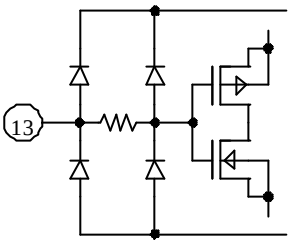
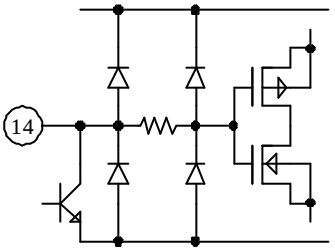
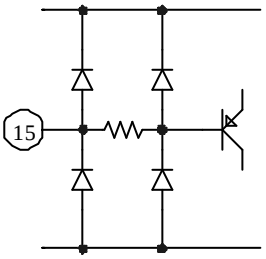
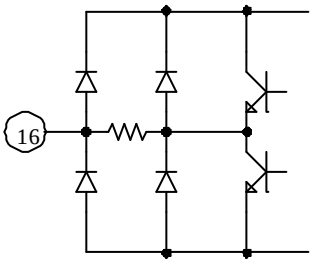
RD1	RD2	Reference Divider	Conditions
×	0	640	
1	1	512	Default
0	1	1024	

(Note)

Default : Power on reset

■ **TERMINAL CHARACTERISTICS**

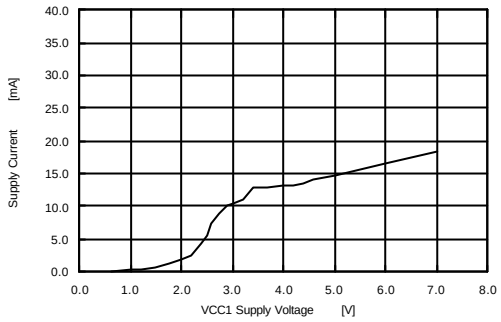
No.	Symbol	Typ.DC Voltage (V)	Equivalent Circuit	Function
1	HF	3.2		High Frequency Signal Input
2	GND	0		GND
3	VCC1	5		Power Supply
4	VCC3	5		Band Switch Power Supply
5 6	BS3 BS2	0		Band Switch (Typ: 7.5mA)
7 8	BS1 BS0	0		Band Switch (Typ: 15mA)
9	CP	-		Charge Pump Output

No.	Symbol	Typ.DC Voltage (V)	Equivalent Circuit	Function
10	AMPOUT	-		Amplifier Output
11	VCC2	34		Amplifier Power Supply
12	OSCOUT	4.1		Reference Oscillator Output
13	SCL	-		SCL Input (I^2C bus)
14	SDA	-		SCL Input (I^2C bus)
15	ADRS	-		ADRS Input (I^2C bus)
16	XTAL	3.3		Crystal Input

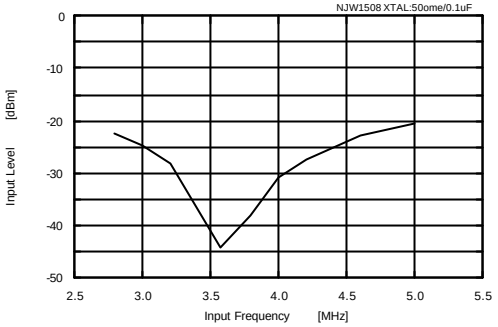
■ TYPICAL CHARACTERISTICS

T_A=25°C

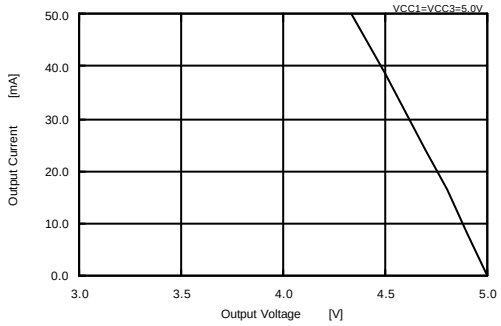
VCC1 Supply Current Curve



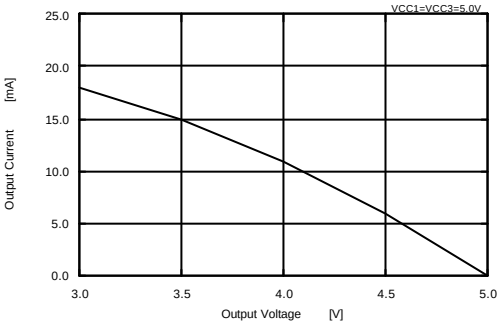
XTAL Input Sensitivity Curve



BS0-BS1 Output Current Curve



BS3 Output Current Curve



MEMO

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