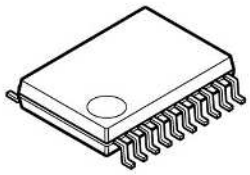
FM Modulation/Demodulation with PLL

■ GENERAL DESCRIPTION

NJW2307 is a FM modulation / demodulation IC for audio signal in full duplex communication that operates from 3.8V.
In addition to audio signal, it can also be used in data pulse.
By the parallel interface, set the carrier frequency (2.3MHz / 2.8MHz), and allows independently power-down control the Modulation / Demodulation circuit.
The NJW2307 includes FM Modulation / Demodulation, VCO, PLL and AFC, will contribute to the adjustment-free.

■ PACKAGE OUTLINE



NJW2307VC3

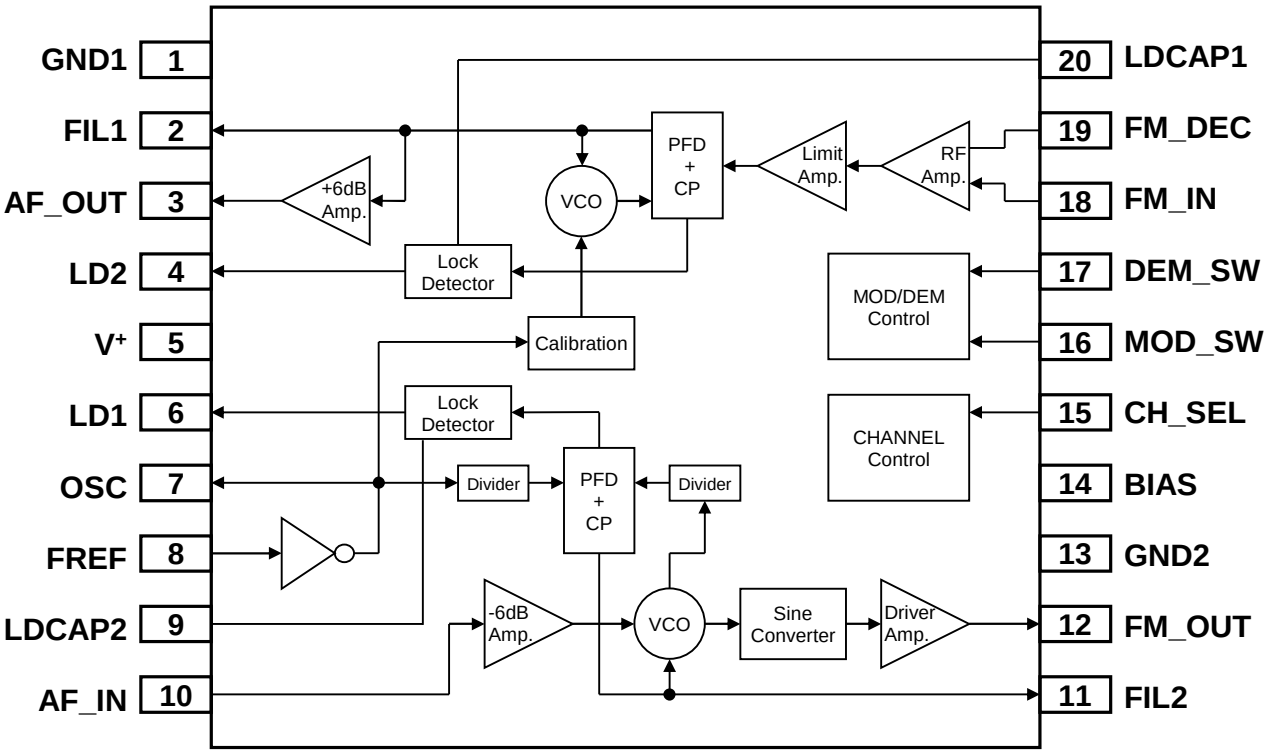
■ APPLICATIONS

Interphone, Voice for Hot water supply system , Wireless and Wired Communication Systems

■ FEATURES

- Operating Voltage 3.8 to 5.5V
- Low operating Current Mod : 9mA typ.
  Demod : 9.5mA typ.
  Power-Down : 1uA Max
- Deviation (AF_IN = 0.5Vpp) ±15kHz (standard)
  FM Modulation output 1Vpp(standard)
  AF Demodulation output 0.5Vpp(standard)
- BiCMOS
- Package SSOP20-C3

■ Block Diagram



■ Truth Table

● Carrier frequency selection

BIAS	CH_SEL	Modulation	Demodulation
H	L	2.8MHz	2.3MHz
H	H	2.3MHz	2.8MHz

※ H = $V_{SW}1$ or V_{BIAS}、 L = $V_{SW}2$
※ Set the CH_SEL state while Inactive (power-down)

● FM modulation / demodulation circuit operation control

Measurement Circuit 1

MOD_SW	DEM_SW	Modulation	Demodulation	FREF
L	L	OFF	OFF	OFF
L	H	OFF	ON	ON
H	L	ON	OFF	ON
H	H	ON	ON	ON

※ ON: circuit is active (power-on), OFF: circuit is inactive (power-down)
※ Set the DEM_SW and MOD_SW after V^+ become recommended operating voltage range

● Status of each pin of the stop / operation

Measurement Circuit 1

Pin No.	SYMBOL	Inactive (Power-down)	Active (Power-on)
1	GND1	-	-
2	FIL1	Hi-Z	-
3	AF_OUT	Hi-Z	-
4	LD2	V^+	PLL Unlock : V^+ PLL Lock : GND
5	V^+	V^+	V^+
6	LD1	V^+	PLL Unlock : V^+ PLL Lock : GND
7	OSC	V^+	-
8	FREF	Hi-Z	-
9	LDCAP2	GND	-
10	AF_IN	Hi-Z	PLL Unlock : Hi-Z PLL Lock : 1.8V
11	FIL2	Hi-Z	-
12	FM_OUT	Hi-Z	V^+-1.2V
13	GND2	-	-
14	BIAS	-	-
15	CH_SEL	-	-
16	MOD_SW	-	-
17	DEM_SW	-	-
18	FM_IN	-	V^+-1.0V
19	FMDEC	-	V^+-1.0V
20	LDCAP1	GND	-

※ Hi-Z means more than 3MΩ,but omly AF_OUT terminal is 34kΩ(standard).

■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	6	V
Control terminal voltage	V IN	-0.3 to 6	V
Power Dissipation	P_D	890 (note1)	mW
		1200 (note2)	mW
Operating Temperature	T o p r	- 40 to + 85	°C
Storage Temperature	T s t g	- 50 to +125	°C

(note1) EIJ/JEDEC standard test board (114.3x76.2x1.6mm, 2 layers, FR-4) mounting.
(note2) EIJ/JEDEC standard test board (114.3x76.2x1.6mm, 4 layers, FR-4) mounting.

■ RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+		3.8	5.0	5.5	V
Control Terminal Voltage	$V_{SW}1$	MOD_SW, DEM_SW, CH_SEL	0.75 × V^+	-	5.5	V
	$V_{SW}2$	MOD_SW, DEM_SW, CH_SEL	0	-	0.25 × V^+	V
	V_{BIAS}	BIAS	V^+ - 0.6	-	5.5	V

■ RECOMMENDED EXTERNAL REFERENCE INPUT SIGNAL (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Frequency	F_{FREF}		3	4	5	MHz
Voltage Range	V_{FREF}	F_{FREF}=4MHz V^+/2 bias	1.4	V^+	-	Vpp
Duty Ratio	DUTY	F_{FREF}=4MHz V^+/2 bias	-	50	-	%

■ ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V^+ = 5.0V, F_{Fref} = 4.0MHz, V_{Fref} = 2.5V(DC) + 5Vpp(AC), V_{FMIN} = 1Vpp, fdev = ±15kHz, fmod = 1kHz, F_{AFIN} = 1kHz, V_{AFIN} = 0.5Vpp, FM_OUT = 10kΩ, AF_OUT = 10kΩ, MOD_SW = H or L, DEM_SW = H or L, BIAS = H, CH_SEL = H or L, unless otherwise noted.)

Operating Current Characteristic (Test Circuit 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-Down Operating Current	I_{PD}	MOD_SW = L, DEM_SW = L, No Signal	-	0.1	1	uA
Modulation Operating Current	I_{MOD}	MOD_SW = H, DEM_SW = L, No Signal	-	9	12	mA
Demodulation Operating Current	I_{DEMOD}	MOD_SW = L, DEM_SW = H, No Signal	-	9.5	12.5	mA
Mod-Demod Operating Current	I_{MODEM}	MOD_SW= H, DEM_SW = H, No Signal	-	18	22	mA

Control Terminal Characteristic (Test Circuit 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
LD Output Terminal High Level Voltage	V_{LDH}	PLL Unlock	$0.75 \times V^+$	-	5.5	V
LD Output Terminal Low Level Voltage	I_{LDL}	PLL Lock	0	-	$0.25 \times V^+$	V
Control Terminal Input Current	I_{IN}	MOD_SW , DEM_SW , BIAS, CH_SEL	- 1	0	1	uA

Modulation Characteristic (Test Circuit 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Carrier Output Frequency1	$F_{FM\ OUT}1$	MOD_SW = H, CH_SEL =H, No Signal	2.28	2.30	2.32	MHz
Carrier Output Frequency2	$F_{FM\ OUT}2$	MOD_SW = H, CH_SEL = L, No Signal	2.78	2.80	2.82	MHz
Carrier Output Level1	$V_{FM\ OUT}1$	MOD_SW = H, No Signal	0.75	1.0	1.25	Vpp
Carrier Output Harmonics Level 1	$P_{HW}1$	MOD_SW = H, Unmodulated, 2^{nd} Harmonics	-	90	-	mVpp
Carrier Output Harmonics Level 2	$P_{HW}2$	MOD_SW = H, Unmodulated, 3^{rd} Harmonics	-	5	-	mVpp
Modulation depth	F_{DEV}	MOD_SW = H, $V_{AF\ IN}$ = 0.5Vpp	±11	±15	±19	kHz
Modulation S/N	MOD_SN	MOD_SW = H	29	40	-	dB
AFIN Input Frequency	$F_{AF\ IN}$	MOD_SW = H, F_{AFIN} = 300Hz, F_{AFIN} = 1kHz ⇒ 300Hz	- 3	- 2	1	dB
AFIN Maximum Input Level	$V_{AF\ IN}$	MOD_SW = H, -3dB Deviation	3	-	-	Vpp
AFIN Impedance	$Z_{AF\ IN}$	MOD_SW = H	7.5	10	12.5	kΩ
FMOUT Load capability	$Z_{FM\ OUT}$	MOD_SW = H, FM_OUT Load resistance = 10kΩ ⇒ 1kΩ	- 3	- 2	1	dB
LD1 Lock-up Time	$T_{LD}1$	MOD_SW = H, Test Circuit 3	-	1	1.6	msec

Demodulation Characteristic (Test Circuit 2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulation Output Frequency	$F_{AF\ OUT}$	DEM_SW = H, fmod = 1kHz ⇒ 5kHz	- 3	- 2	1	dB
Demodulation Level	$V_{AF\ OUT}$	DEM_SW = H	0.37	0.5	0.63	Vpp
Demodulation S/N1	SN1	DEM_SW = H	30	40	-	dB
Demodulation S/N2	SN2	DEM_SW = H, $V_{FM\ IN}$ = 2.0mVpp	-	12	-	dB
Demodulation Output Distortion Level	THD	DEM_SW = H	-	1	-	%
FMIN Impedance	$Z_{FM\ IN}$	DEM_SW = H	-	10	-	kΩ
AFOUT Load Capability	$Z_{AF\ OUT}$	DEM_SW = H, AF_OUT Load resistance = 10kΩ ⇒ 1kΩ	- 3	- 2	1	dB
LD2 Lock-up Time	$T_{LD}2$	MOD_SW = H	-	1	-	msec

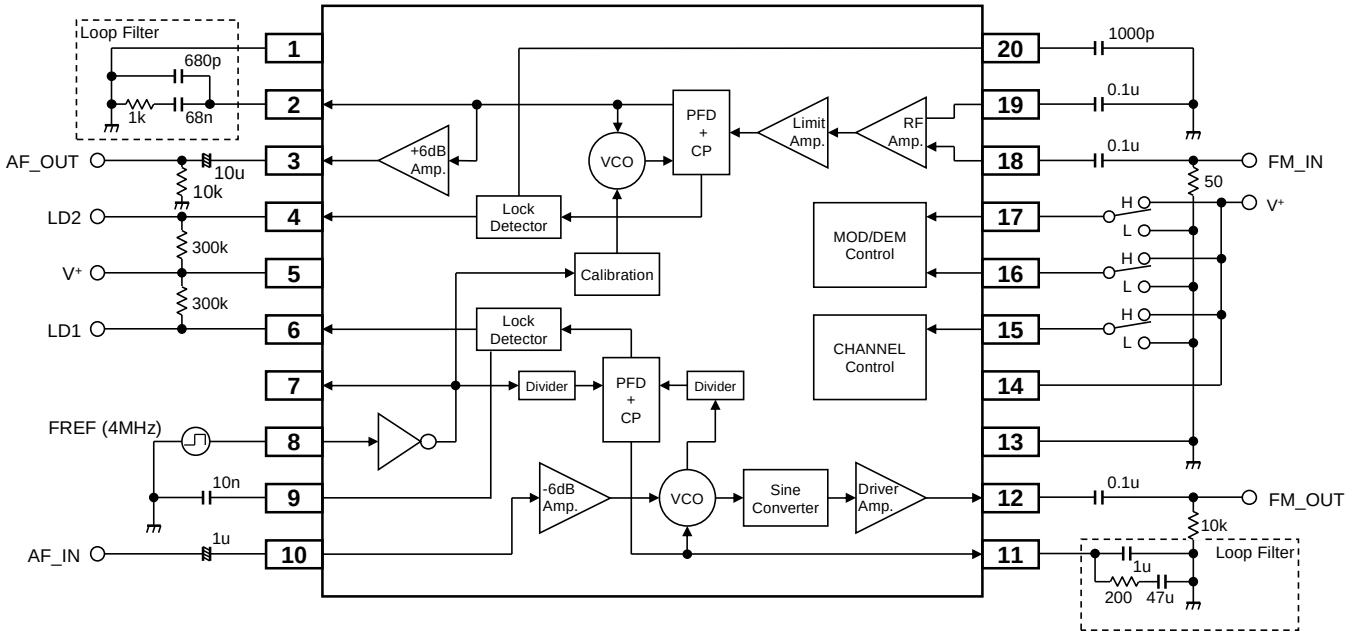
Reference Signal Oscillator Circuit Characteristic (Test Circuit 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillatory Frequency Range	F_{OSC}	OSC-GND = 47pF FREF-GND = 47pF OSC-FREF = 510kΩ	-	4	-	MHz
Negative resistance	- R	OSC-GND = 47pF FREF-GND = 47pF OSC-FREF = 510kΩ	-	- 5	-	kΩ
Oscillator Startup Time	$T_{OSCS}1$	OSC-GND = 47pF FREF-GND = 47pF OSC-FREF = 510kΩ	-	0.1	1.6	msec
Oscillation Detection Time	$T_{OSCS}2$	OSC-GND = 47pF FREF-GND = 47pF OSC-FREF = 510kΩ	-	50	-	usec

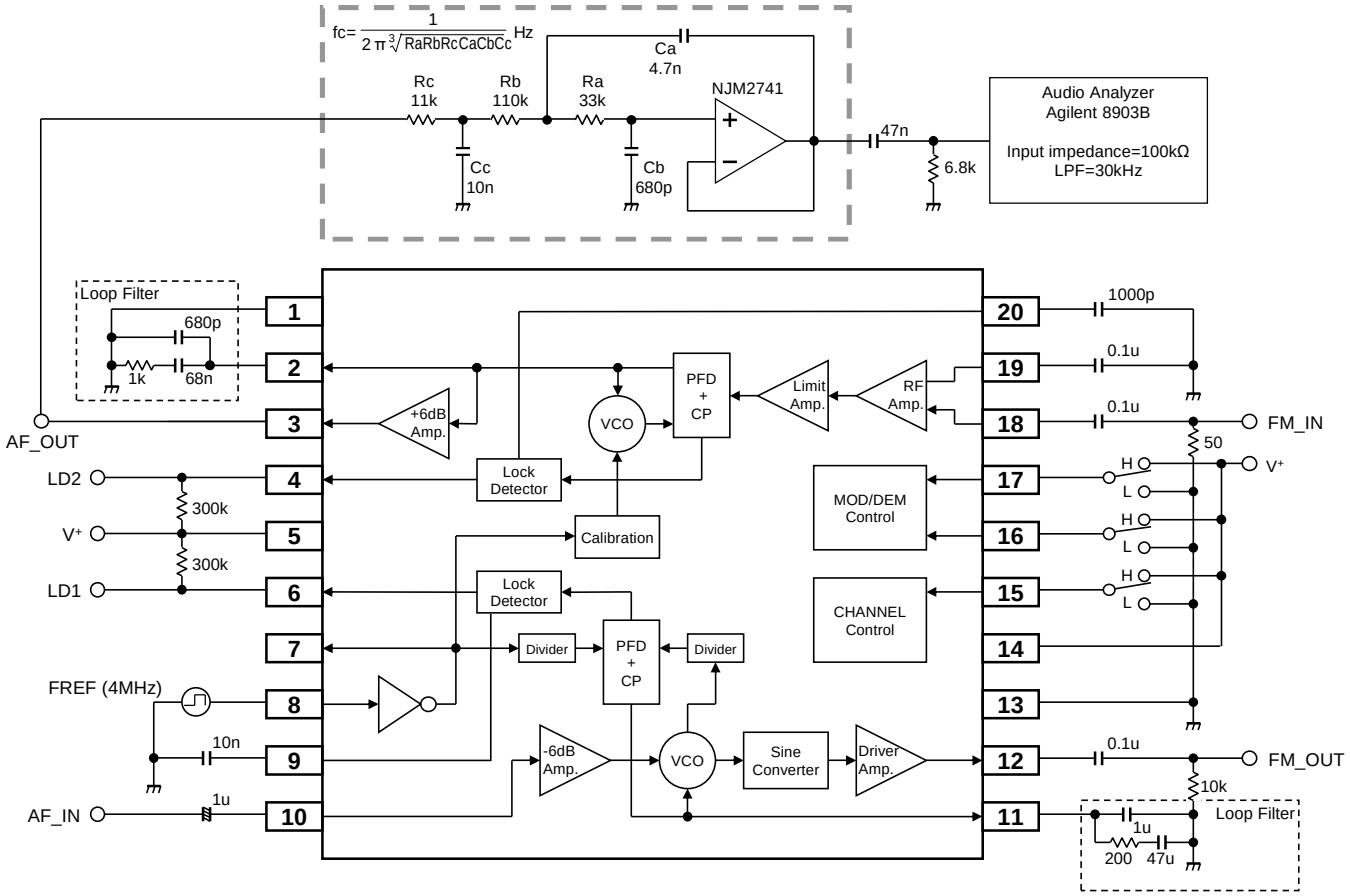
■ TEST CIRCUIT

These test circuits allow the measurement of all parameters described in “ELECTRICAL CHARACTERISTICS”.

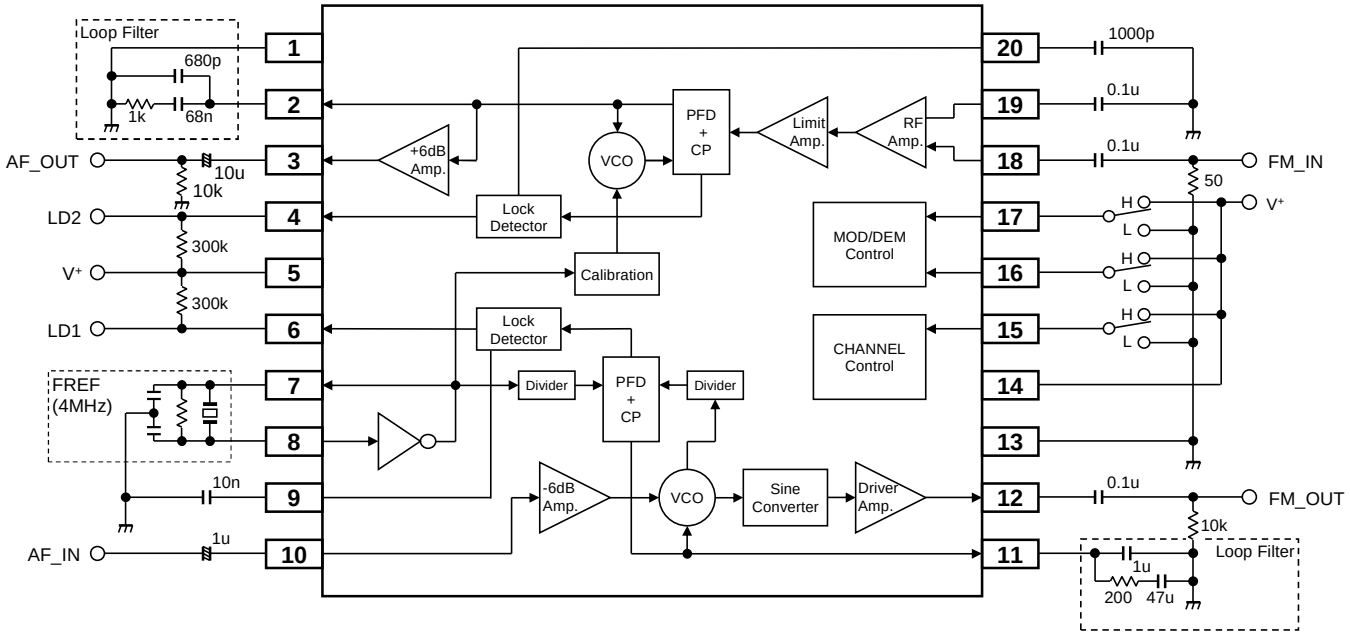
- **Test Circuit 1:External reference signal input**



- **Test Circuit 2:Oscillation device input (Crystal oscillator or Ceramic oscillator)**

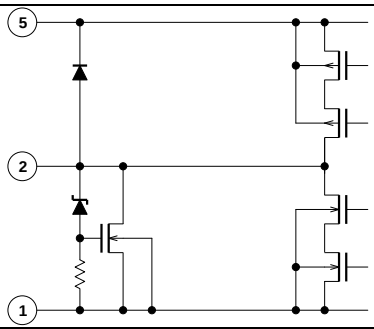
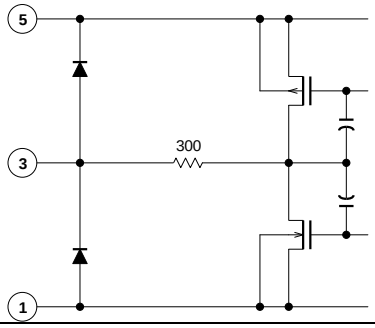
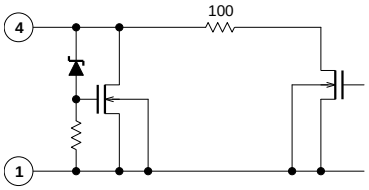
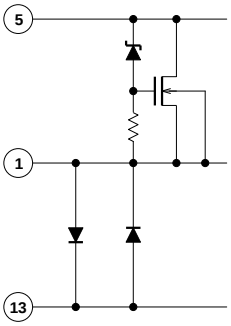
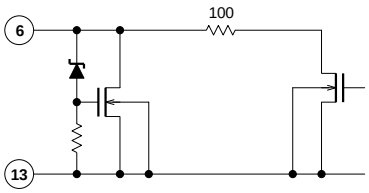


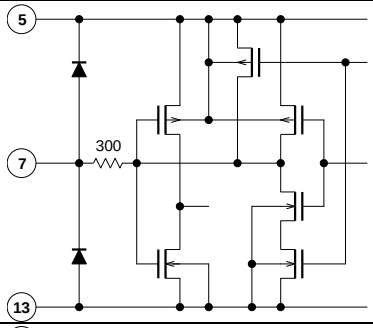
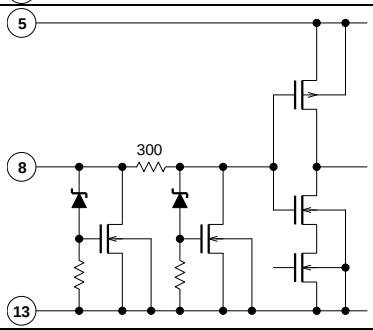
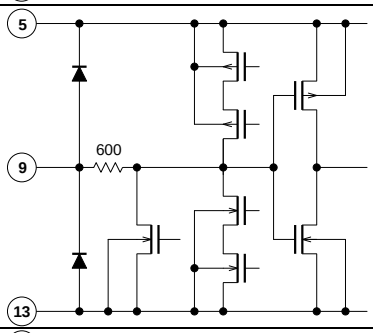
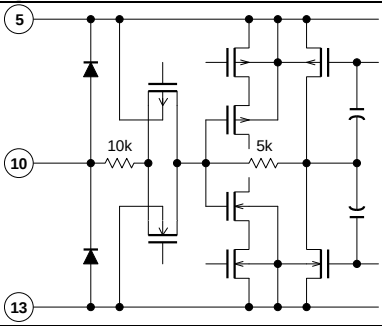
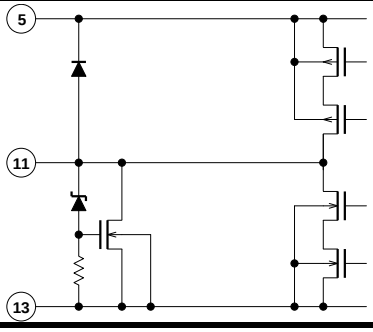
- **Test Circuit3**

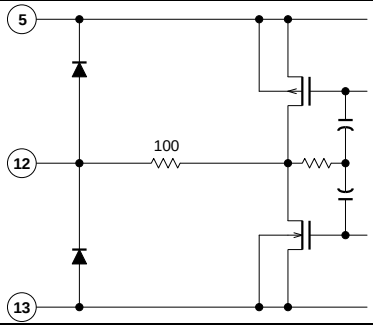
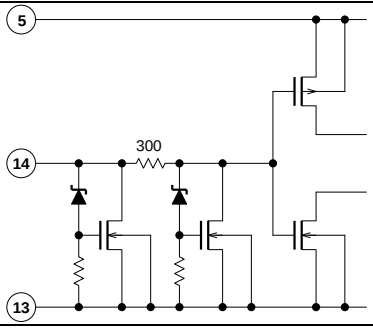
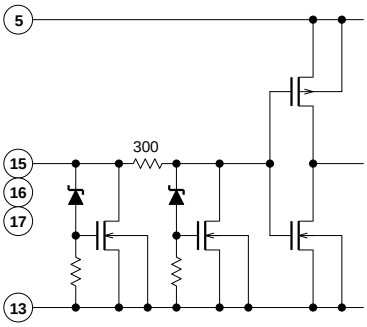
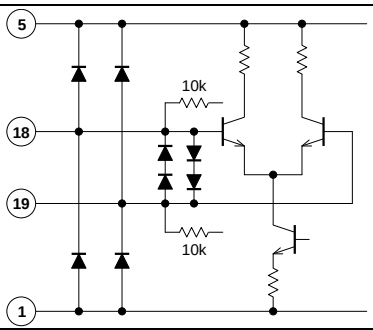
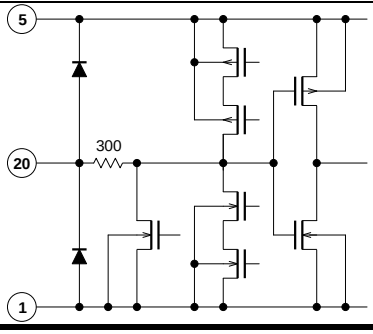


■ TERMINAL FUNCTION

(Ta = 25°C, V^+ = 5V, No signal)

Pin No.	SYMBOL	EQUIVARENT CIRCUIT	VOLTAGE	FUNCTION
1	GND1	--	--	**Ground** This is the ground terminal of the internal demodulator.
2	FIL1		--	**Demodulator PLL Filter** An external PLL loop filter for demodulator is connected to fix the upper limited demodulation frequency established by a cutoff frequency of a connected filter.
3	AF_OUT		--	**Demodulated Signal Output** The swing of signal level is double of pin 2 (FIL1).
4	LD2		Unlock : V^+ Lock : GND	**Demodulator Lock Detector** An output signal of the lock detection of the internal demodulator. Since this port is the open drain, a pull-up resister (is) may be required.
5	V^+		V^+	**Supply Voltage**
6	LD1		Unlock : V^+ Lock : GND	**Modulator Lock Detector** An output signal of the lock detection of the internal modulator. Since the port is the open drain, a pull-up resister (is) may be required.

Pin No.	SYMBOL	EQUIVARENT CIRCUIT	VOLTAGE	FUNCTION
7	OSC		--	**Oscillator** An oscillation device is placed between pin 7 and 8 for reference frequency.
8	FREF		--	**Reference Frequency** An external reference frequency is input, or an oscillation device is placed between pin 7 and 8.
9	LDCAP2		--	**Modulator Lock Detect Capacitor** An external decoupling capacitor for the lock detector of PLL of modulator is connected to enhance stability the output signal of pin 6.
10	AF_IN		Lock:1.8V Unlock: Hi-Z	**Audio Input for modulation**
11	FIL2		--	**Modulator PLL Filter** An external PLL loop filter for modulator is connected to fix the lower limited modulation frequency established by a cutoff frequency of a connected filter.

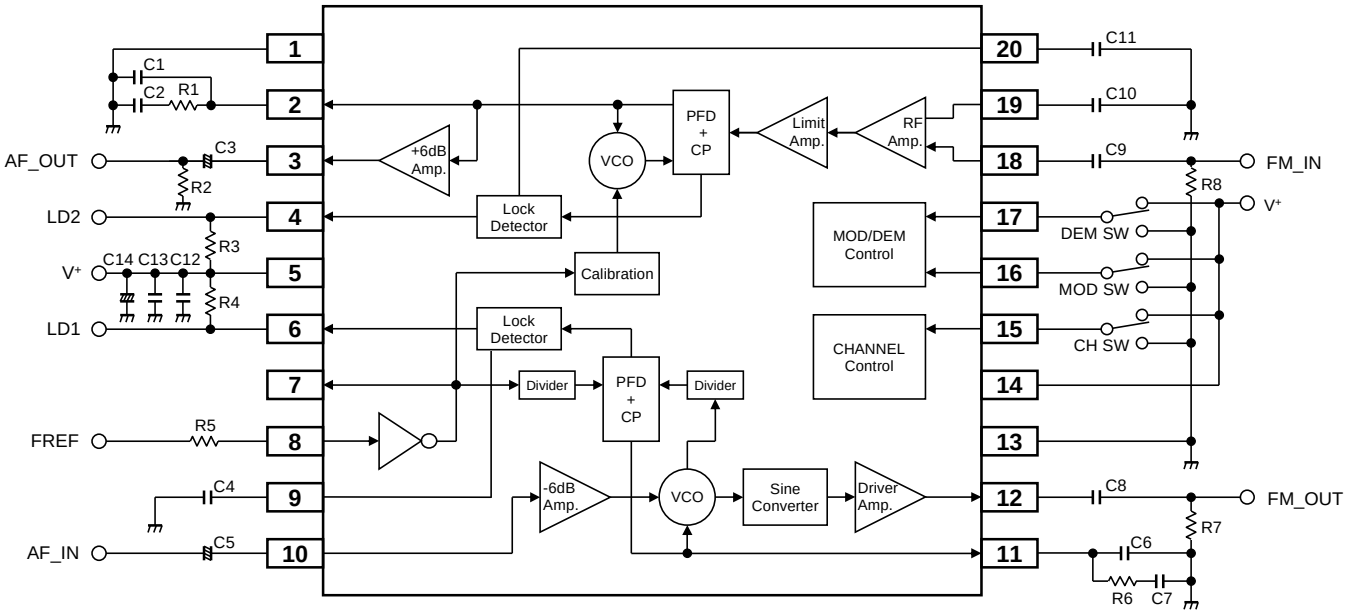
Pin No.	SYMBOL	EQUIVARENT CIRCUIT	VOLTAGE	FUNCTION
12	FM_OUT		V^+ - 1.2V	**FM Modulation Output** An input signal of pin 10 modulates to FM signal which carrier frequency is 2.3 or 2.8MHz.
13	GND2	--	--	**Ground** This is the ground terminal of the internal modulator.
14	BIAS		--	**Bias** Always keep a logical high level.
15 16 17	CH_SEL MOD_SW DEM_SW		--	**Pin 15: Selection of Carrier Frequency** The carrier frequency can be selected 2.3 or 2.8MHz. **Pin 16: Modulation Enable** **Pin 17: Demodulation Enable** Logical L sets inactive. Logical H sets active.
18 19	FM_IN FM_DEC		V^+ - 1.0V	**Pin 18: Modulation Input** Since the terminal is biased, input signal must pass through a capacitor. **Pin 19: Decoupling of Modulator Input**
20	LDCAP1		--	**Demodulator Lock Detect Capacitor** An external decoupling capacitor for the lock detector of PLL of demodulator is connected to enhance stability the output signal of pin 4.

■ EVALUATION PC BOARD

The evaluation board is useful for your design and to have more understanding of the usage and performance of this device.

Note that this board is not prepared to show the recommendation of pattern and parts layout.

- **Circuit Diagram**

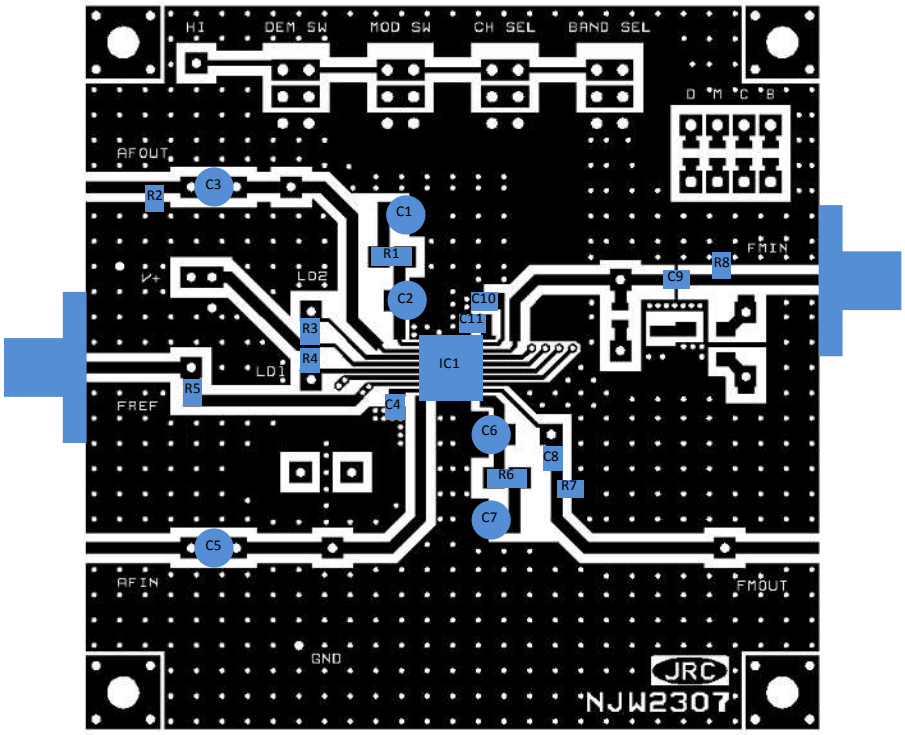


- **List of Component**

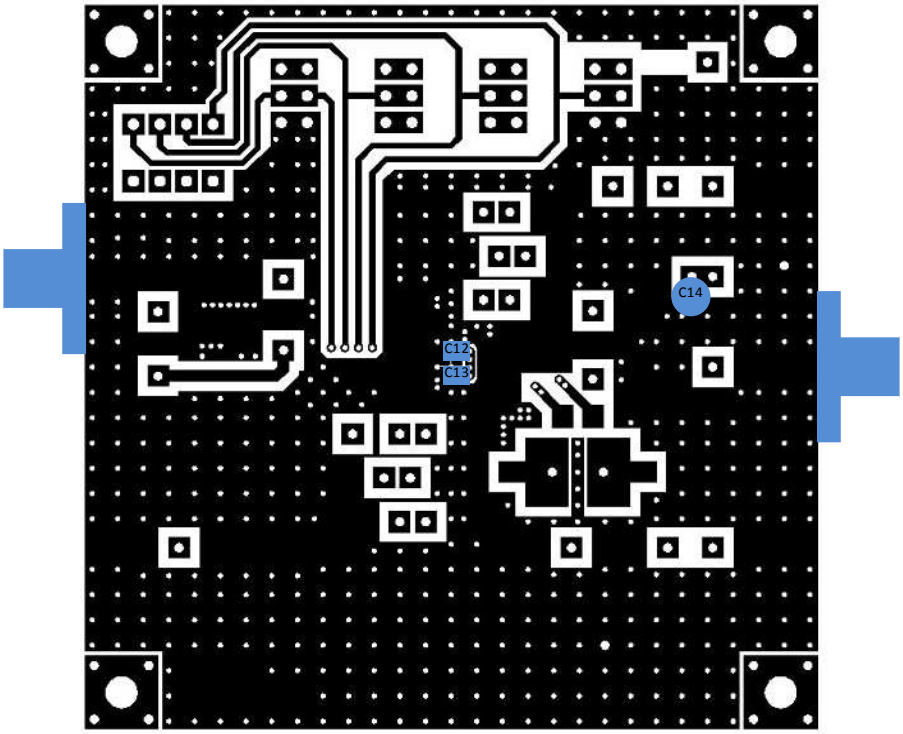
Designation	Value	Items	Designation	Value	Items
C1	680pF	Capacitor	R1	1kΩ	Resistor
C2	68nF	Capacitor	R2	10kΩ	Resistor
C3	10uF	Capacitor	R3	300kΩ	Resistor
C4	10nF	Capacitor	R4	300kΩ	Resistor
C5	1uF	Capacitor	R5	0Ω	Resistor
C6	1uF	Capacitor	R6	200Ω	Resistor
C7	47uF	Capacitor	R7	10kΩ	Resistor
C8	0.1uF	Capacitor	R8	50Ω	Resistor
C9	0.1uF	Capacitor			
C10	0.1uF	Capacitor			
C11	1000pF	Capacitor			
C12	0.1uF	Capacitor			
C13	1uF	Capacitor			
C14	10uF	Capacitor	IC1	NJW2307VC3	IC

- **PC Board**

Top View

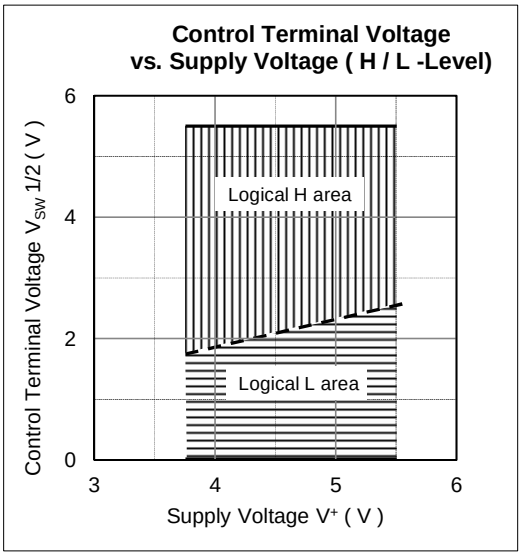


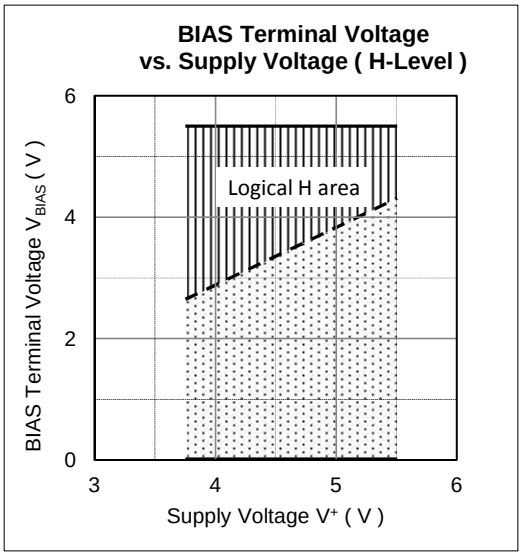
Bottom View

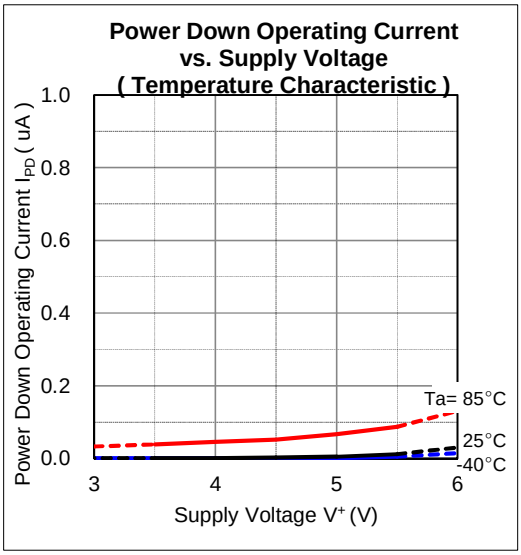


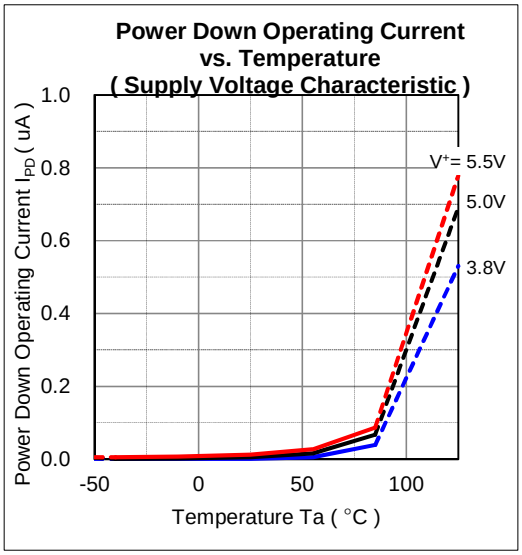
■ TYPICAL CHARACTERISTICS

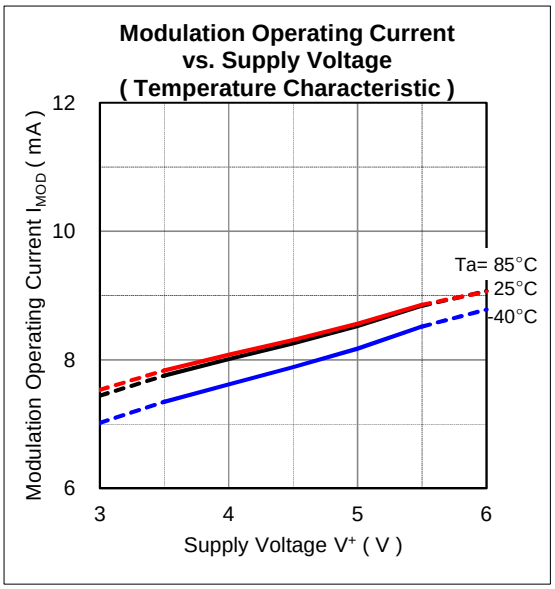
(Ta = 25°C, V^+ = 5.0V, fref = 4.0MHz, FM IN = 1Vpp, fdev = ±15kHz, fmod = 1kHz, AF IN = 0.5Vpp, AFfreq = 1kHz, FMOUT = 10kΩ, AFOUT = 10kΩ, unless otherwise noted.)

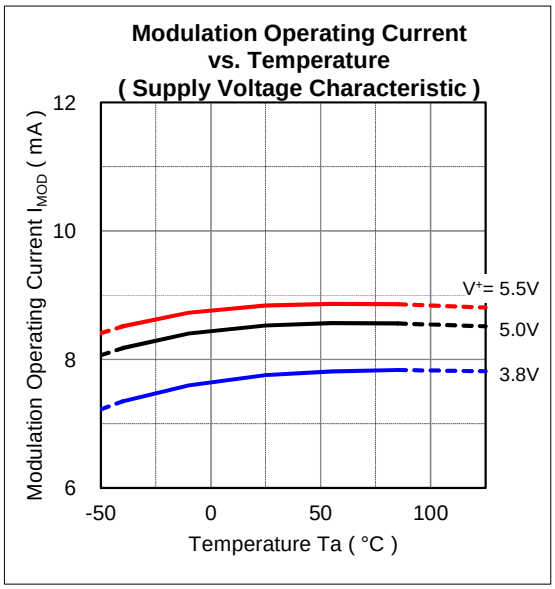


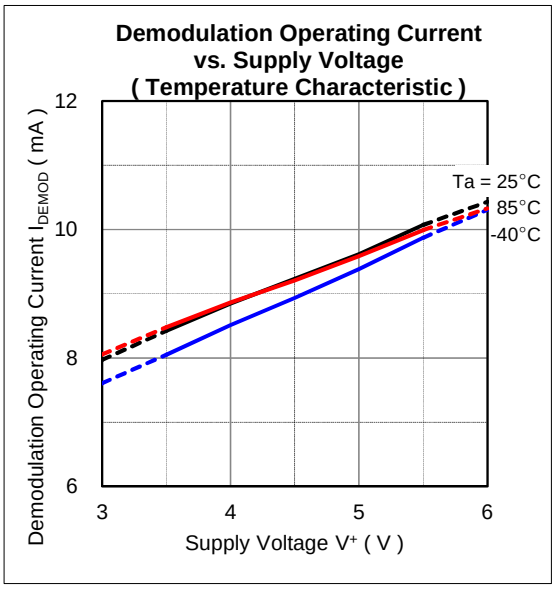


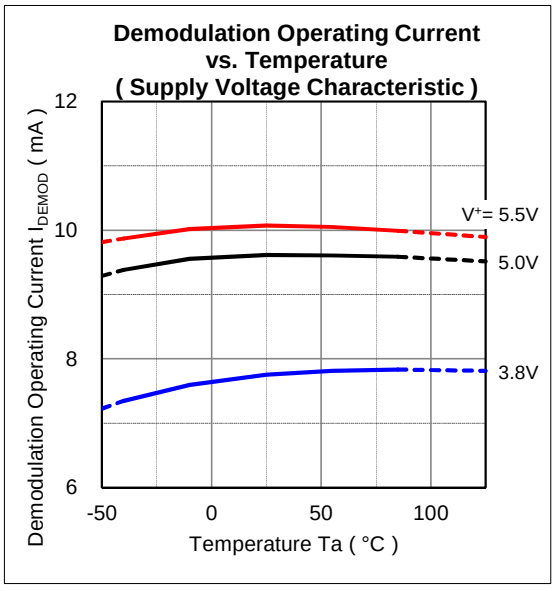


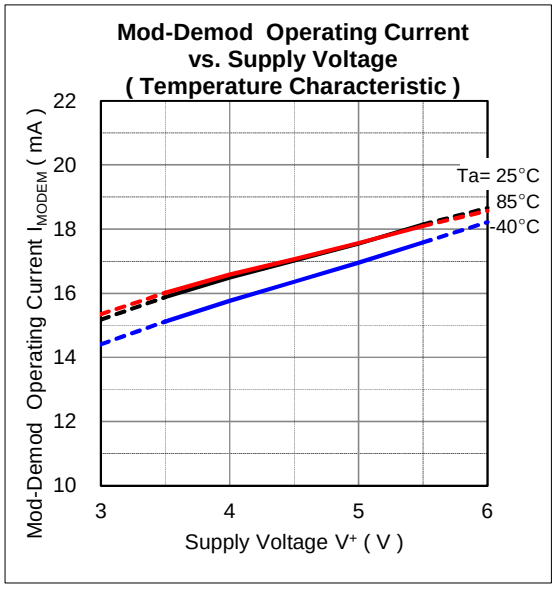


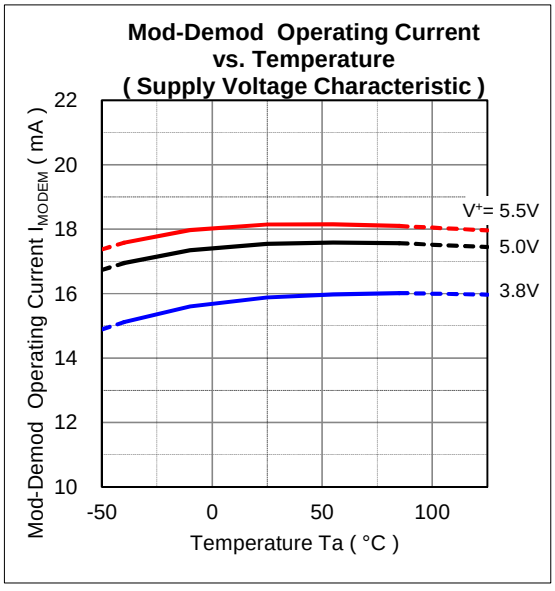

Modulation Operating Current
vs. Supply Voltage
(Temperature Characteristic)
Modulation Operating Current I_{MOD} (mA)
12
10
8
6
3
4
5
6
Supply Voltage V+ (V)
Ta= 85°C
25°C
-40°C

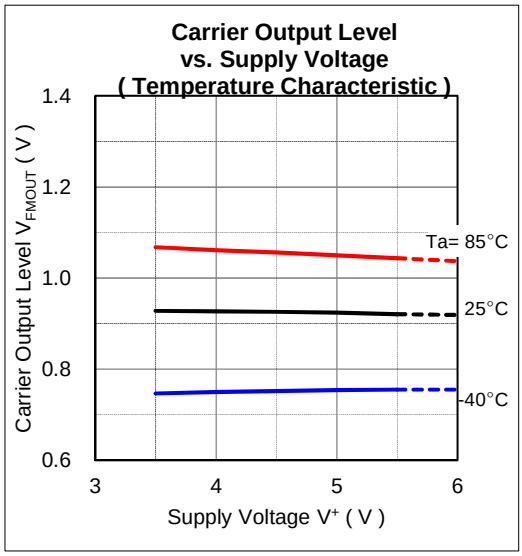

Modulation Operating Current
vs. Temperature
(Supply Voltage Characteristic)
Modulation Operating Current I_{MOD} (mA)
12
10
8
6
-50
0
50
100
Temperature Ta (°C)
V+= 5.5V
5.0V
3.8V

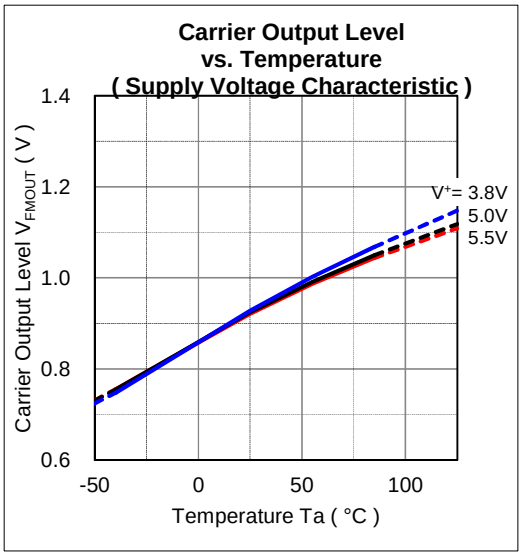

Demodulation Operating Current
vs. Supply Voltage
(Temperature Characteristic)
Demodulation Operating Current I_{DEMOD} (mA)
12
10
8
6
3
4
5
6
Supply Voltage V+ (V)
Ta = 25°C
85°C
-40°C

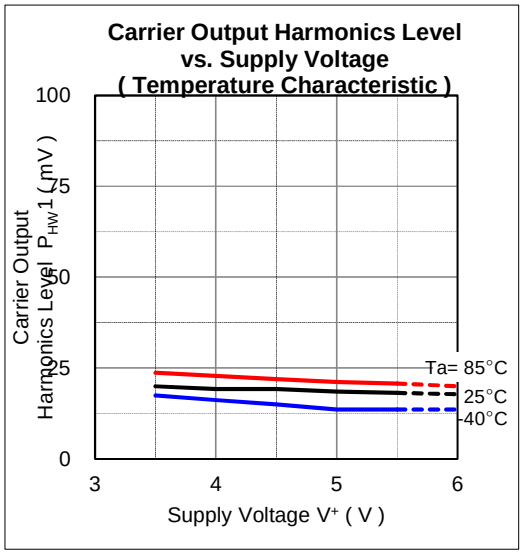

Demodulation Operating Current
vs. Temperature
(Supply Voltage Characteristic)
Demodulation Operating Current I_{DEMOD} (mA)
12
10
8
6
-50
0
50
100
Temperature Ta (°C)
V+= 5.5V
5.0V
3.8V

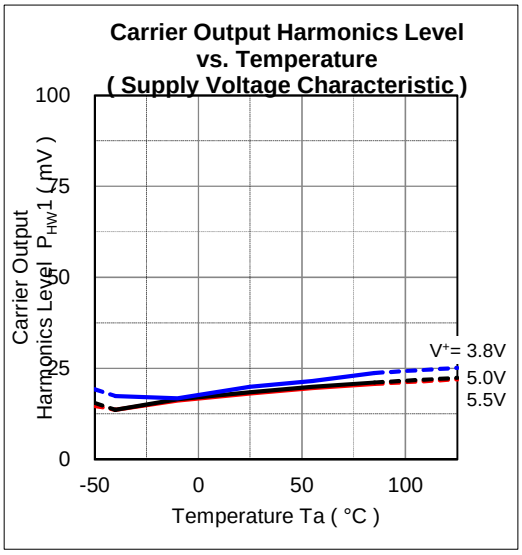

Mod-Demod Operating Current
vs. Supply Voltage
(Temperature Characteristic)
Mod-Demod Operating Current I_{MODEM} (mA)
22
20
18
16
14
12
10
3
4
5
6
Supply Voltage V+ (V)
Ta= 25°C
85°C
-40°C

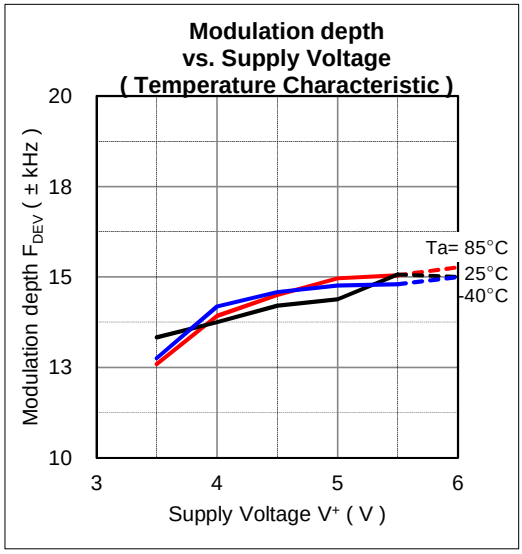

Mod-Demod Operating Current
vs. Temperature
(Supply Voltage Characteristic)
Mod-Demod Operating Current I_{MODEM} (mA)
22
20
18
16
14
12
10
-50
0
50
100
Temperature Ta (°C)
V+= 5.5V
5.0V
3.8V

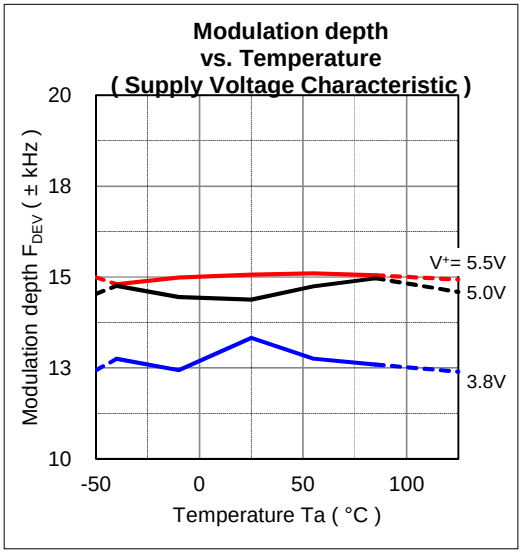

Carrier Output Level
vs. Supply Voltage
(Temperature Characteristic)
Carrier Output Level V_{FMOUT} (V)
1.4
1.2
1.0
0.8
0.6
3
4
5
6
Supply Voltage V+ (V)
Ta= 85°C
25°C
-40°C

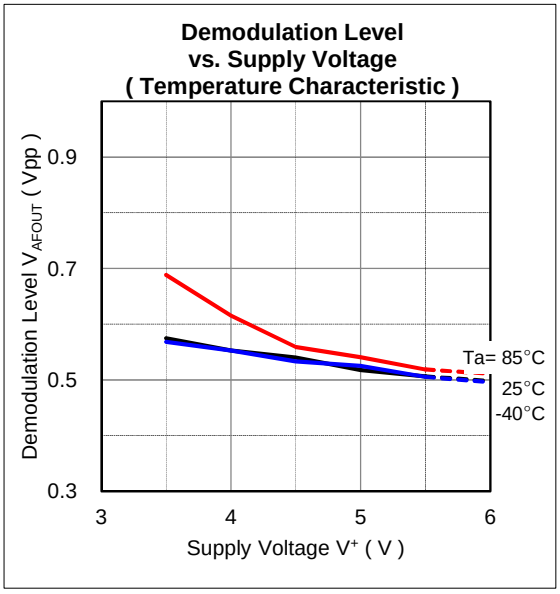

Carrier Output Level
vs. Temperature
(Supply Voltage Characteristic)
Carrier Output Level V_{FMOUT} (V)
1.4
1.2
1.0
0.8
0.6
-50
0
50
100
Temperature Ta (°C)
V+= 3.8V
5.0V
5.5V

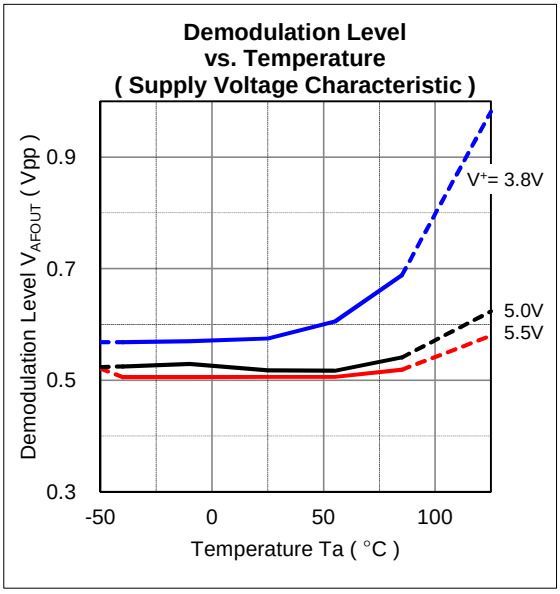

Carrier Output Harmonics Level
vs. Supply Voltage
(Temperature Characteristic)
Carrier Output Harmonics Level $P_{HW}1$ (mV)
100
75
50
25
0
3
4
5
6
Supply Voltage V+ (V)
Ta= 85°C
25°C
-40°C

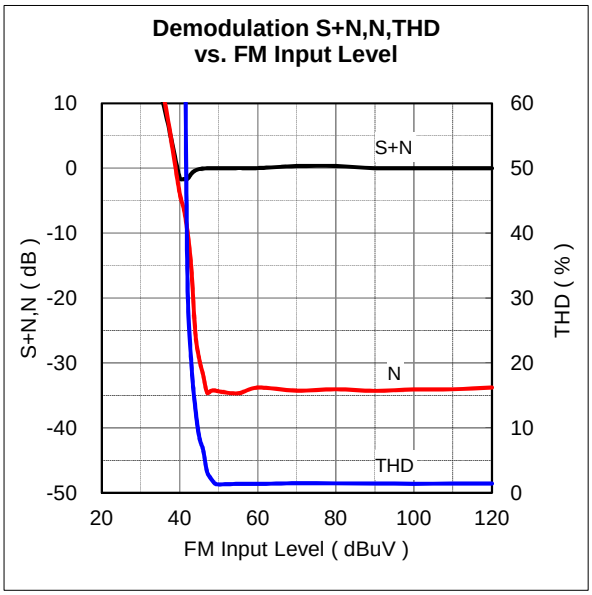

Carrier Output Harmonics Level
vs. Temperature
(Supply Voltage Characteristic)
Carrier Output Harmonics Level $P_{HW}1$ (mV)
100
75
50
25
0
-50
0
50
100
Temperature Ta (°C)
V+= 3.8V
5.0V
5.5V

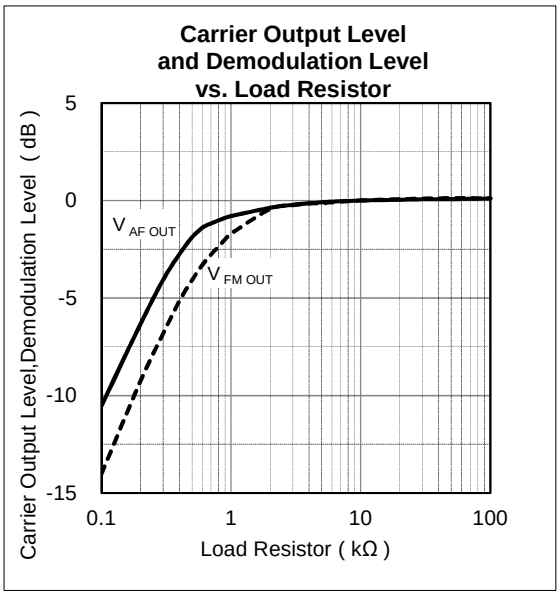

Modulation depth
vs. Supply Voltage
(Temperature Characteristic)
Modulation depth F_{DEV} (± kHz)
20
18
15
13
10
3
4
5
6
Supply Voltage V+ (V)
Ta= 85°C
25°C
-40°C

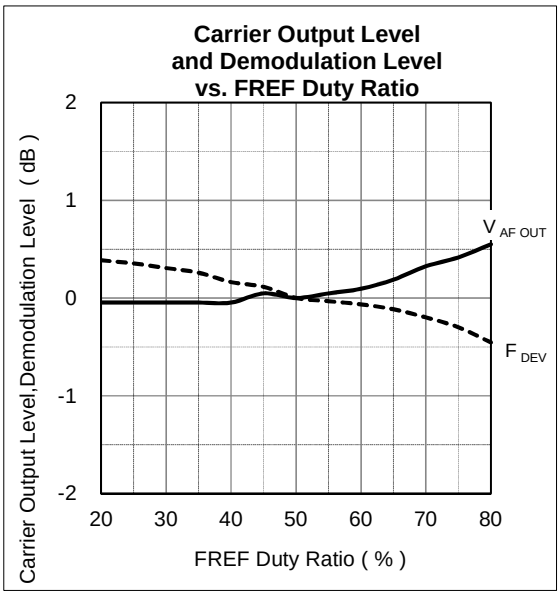

Modulation depth
vs. Temperature
(Supply Voltage Characteristic)
Modulation depth F_{DEV} (± kHz)
20
18
15
13
10
-50
0
50
100
Temperature Ta (°C)
V+= 5.5V
5.0V
3.8V

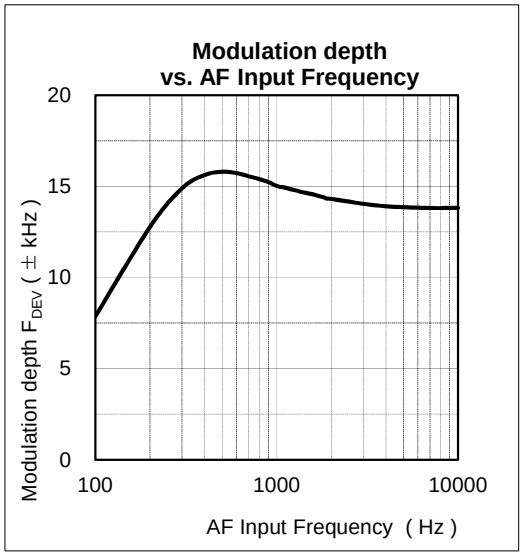

Demodulation Level
vs. Supply Voltage
(Temperature Characteristic)
Demodulation Level V_{AFOUT} (Vpp)
0.9
0.7
0.5
0.3
3
4
5
6
Supply Voltage V+ (V)
Ta= 85°C
25°C
-40°C

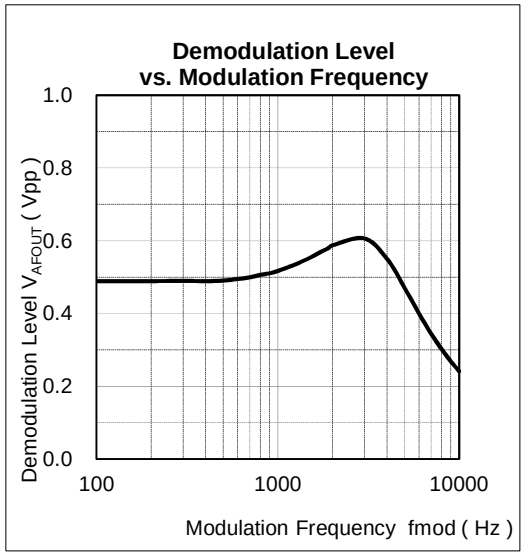

Demodulation Level
vs. Temperature
(Supply Voltage Characteristic)
Demodulation Level V_{AFOUT} (Vpp)
0.9
0.7
0.5
0.3
-50
0
50
100
Temperature Ta (°C)
V+= 3.8V
5.0V
5.5V


Demodulation S+N,N,THD
vs. FM Input Level
S+N,N (dB)
10
0
-10
-20
-30
-40
-50
THD (%)
60
50
40
30
20
10
0
20
40
60
80
100
120
FM Input Level (dBuV)
S+N
N
THD


Carrier Output Level
and Demodulation Level
vs. Load Resistor
Carrier Output Level,Demodulation Level (dB)
5
0
-5
-10
-15
0.1
1
10
100
Load Resistor (kΩ)
V AF OUT
V FM OUT


Carrier Output Level
and Demodulation Level
vs. FREF Duty Ratio
Carrier Output Level,Demodulation Level (dB)
2
1
0
-1
-2
20
30
40
50
60
70
80
FREF Duty Ratio (%)
V AF OUT
F DEV


Modulation depth
vs. AF Input Frequency
20
15
10
5
0
Modulation depth F_{DEV} (± kHz)
100
1000
10000
AF Input Frequency (Hz)


Demodulation Level
vs. Modulation Frequency
1.0
0.8
0.6
0.4
0.2
0.0
Demodulation Level V_{AFOUT} (Vpp)
100
1000
10000
Modulation Frequency fmod (Hz)

■ Product Outline

NJW2307 consists from some blocks such as a FM modulator, a FM demodulator, a reference oscillator and a parallel logic control interface. It's possible by a logical interface that the power of the FM modulator and demodulator can be controlled independently, and setting of a carrier frequency.

1. FM Modulation Block

The speech signal gets into the AF_IN terminal (pin 10) and becomes FM modulated signal at VCO of FM modulation through a buffer amplifier (-6dB Amp). The FM modulated signal becomes a sine wave at the Sine Converter, and it is output through a driver amplifier. The FM modulator is using PLL, and consists of PFD (Phase/Frequency detector), a CP (Charge Pump), Divider and VCO. The loop filter connected to FIL2 terminal (pin 11) can establish modulation bandwidth.

2. FM Demodulation Block

The FM signal fed into the FM_IN terminal (pin 18) is demodulated in the PFD (Phase/Frequency detector), passing through the internal RF amplifier and the limiter amplifier. The FM demodulated signal outputs from a driver amplifier (+6dB Amp). The FM demodulator is using PLL, and consists of PFD (Phase/Frequency detector), a CP (Charge Pump), Divider and VCO. The loop filter connected to FIL1 terminal (pin 2) can establish demodulation bandwidth.

3. Reference Frequency Oscillator

There is an internal inverter amplifier between the OSC (pin 7) and the FREF (pin 8), a resonator connection between 2 pins makes the reference oscillator of PLL. In case of using an external PLL reference frequency signal, please input it to the FREF terminal (8pin), and leave the OSC terminal (7pin) open (no connection).

4. Parallel logic control Interface

The input of an interface circuit is 3 terminals such as CH_SEL terminal (pin 15), MOD_SW terminal (pin 16) and DEM_SW terminal (pin 17). The carrier frequency of FM modulation and demodulation can be set to 2.3MHz or 2.8MHz by the CH_SEL terminal (15pin). Further, please always set the BIAS terminal (pin 14) to a logical high level.

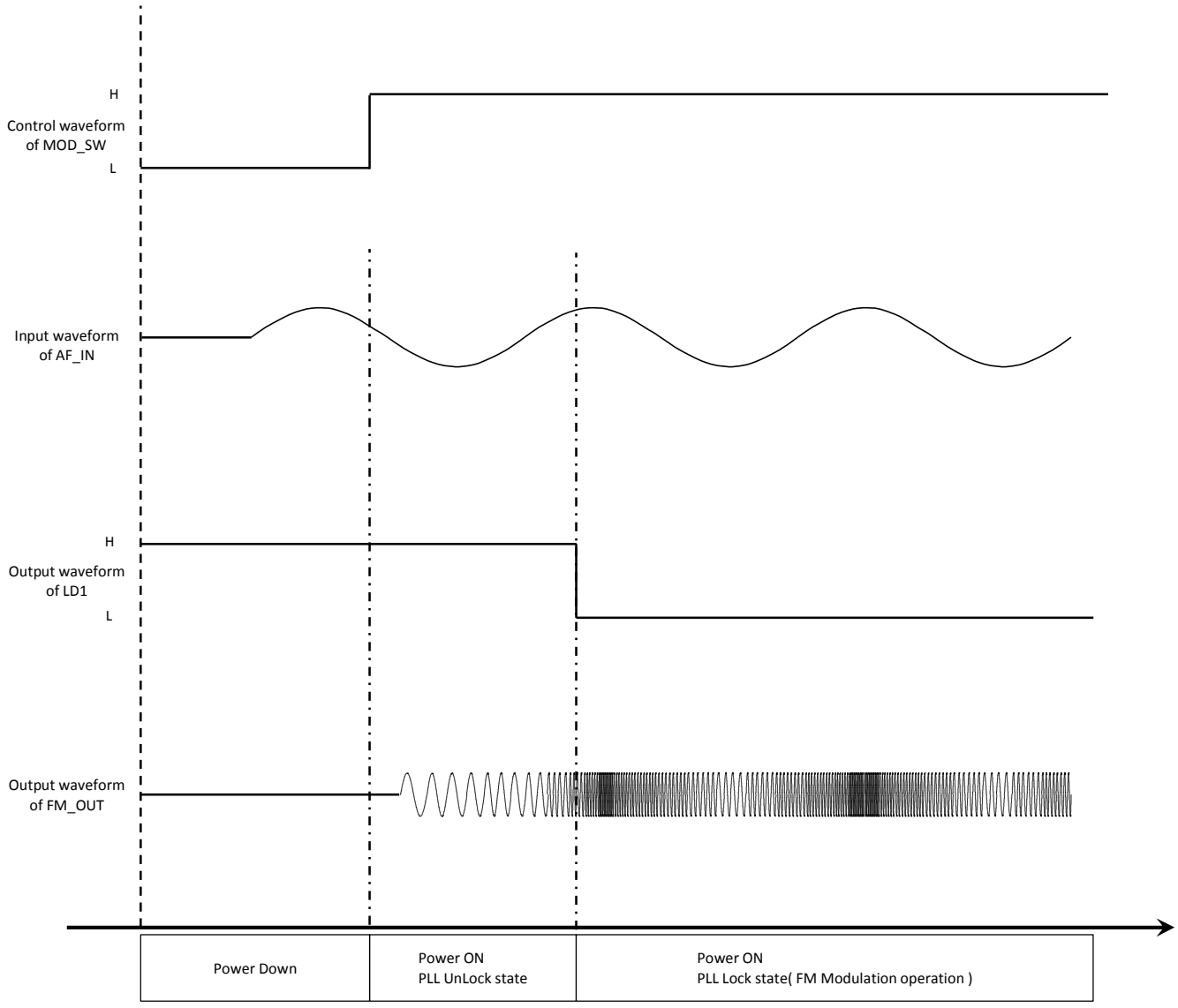
Setting of MOD_SW terminal (pin 16) can control the power-down function in the FM modulation block.

Setting of DEM_SW terminal (pin 17) can control the power-down function in the FM demodulation block.

- **Example and explanation in the FM modulation block**

When MOD_SW terminal (pin 16) is set to a logical high level, the FM modulation block will be the power-on state, and a PLL works for FM modulation, and the desired carrier signal is out from FM_OUT terminal (pin 12).

LD1 terminal (pin 6) will indicate the lock status of the PLL for FM modulation, and it becomes a logical low level when the carrier frequency becomes the set frequency. The input signal of AF_IN terminal (pin 10) becomes FM modulated signal after LD1 terminal (pin 6) becomes a logical low level. The input signal of AF_IN terminal (pin 10) doesn't become FM modulated signal while LD1 terminal (pin 6) is a logical high level. Therefore it recommends inputting a signal to AF_IN terminal after LD1 terminal (6pin) will be a logical low level. But, there is no problem with inputting a signal to AF_IN terminal (pin 10), even if LD1 terminal (pin 6) is a logical high level (PLL is unlocked status) or MOD_SW terminal (pin 16) is a logical low level (in power-down state).



- **Example and explanation in the FM demodulation block**

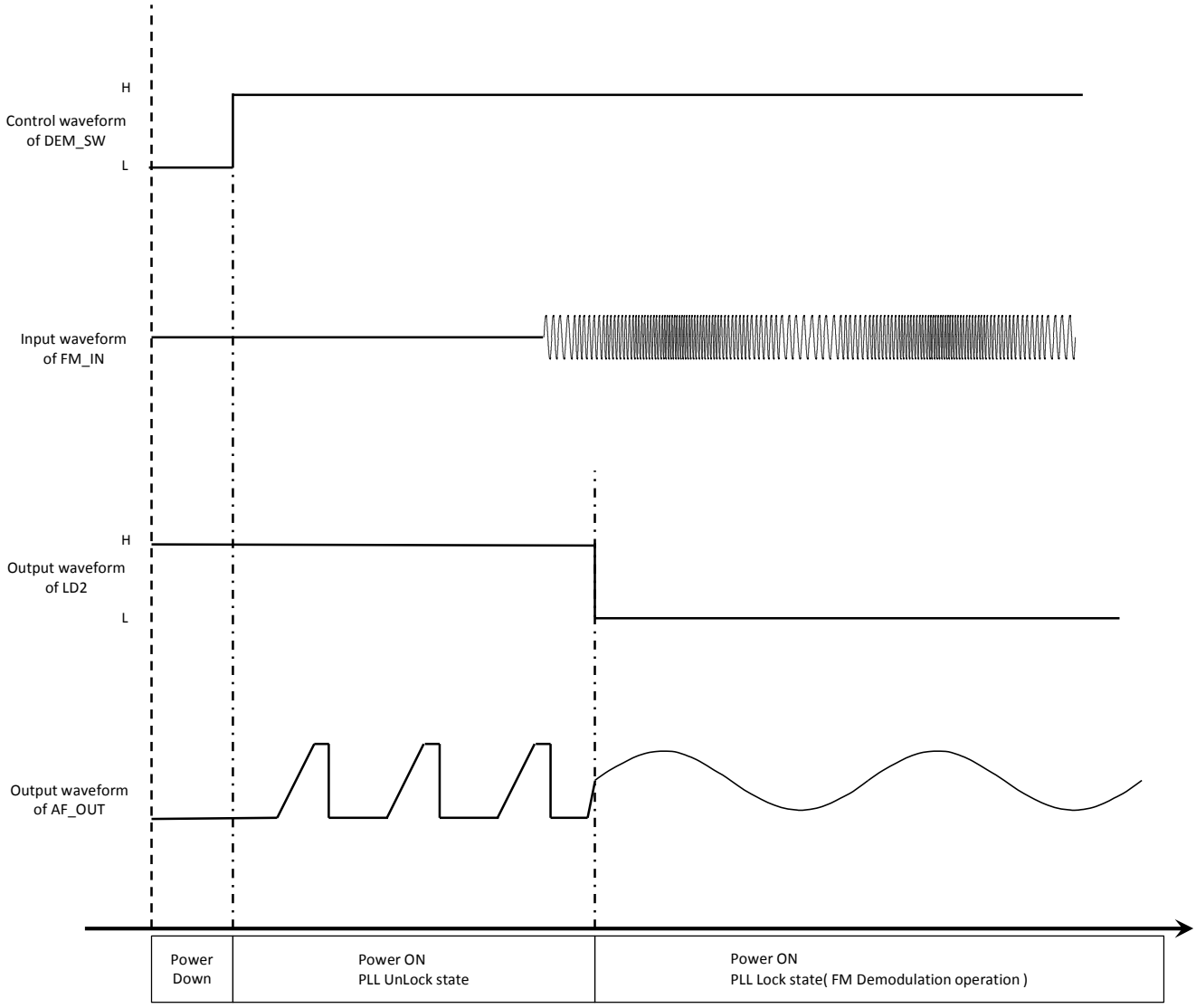
When DEM_SW terminal (pin 17) is set to a logical high level, an FM demodulator block is the power-on state, and a PLL works for FM demodulation, and a demodulated signal is output from AF_OUT terminal (pin 3).

LD2 terminal (pin 4) will indicate the lock status of the PLL for FM demodulation, and it becomes a logical low level when the carrier frequency into the FM_IN terminal (pin 18) becomes the same frequency of the internal VCO. The input signal of FM_IN terminal (pin 18) becomes FM demodulated signal after LD2 terminal (pin 4) becomes a logical low level. If the LD2 terminal (pin 4) is a logical high level (PLL is unlocked status), a correct demodulation signal doesn't come out because of the influence of the calibration which controls VCO for demodulation, and there is a possibility that a noise of speech bandwidth is output. Therefore when an improper FM input signal (*1) keeps being input to FM_IN terminal, it is undergoing influence of the calibration which controls VCO for demodulation, so please pay attention to this matter.

(*1): An improper FM input signal

(1) Different frequency from the set frequency by CH_SEL terminal

(2) In case of low input level or low SN ratio



The above AF_OUT output waveform is a reference diagram, an amplitude level and a frequency will change caused by signal condition into the FM_IN terminal (pin 18) and environment noise.

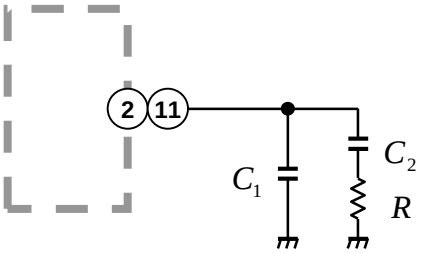
● About loop filter

The loop filter which is connected to FIL1 (pin 2) or FIL2 (pin 11) terminal is needed to let PLL work stably. And it's possible to change the frequency response of the modulation factor or demodulation level respectively by constant components of the loop filter. PLL works stably with phase margin which is generally setting of the constant component of the loop filter as more than 45 deg. When it's lacking in phase margin, the unusual situations occur, such as the PLL doesn't lock, PLL takes time to lock, or the output signal is unstable. Therefore please design the loop filter constant component to get the desired characteristics with having reserved enough phase margins.

The following is the loop filter design method connected to FIL1 (pin 2) or FIL2 (pin 11) terminal of the NJW2307. And we have an excel sheet to easily calculate the following formula, so please contact us.

● Design method of loop filter

The following is the way to calculate the loop filter constant component value from the condition of the cutoff frequency f_c (the frequency by which open-loop gain will be 0dB) and the phase margin ϕ_c. And it shows that how to confirm the frequency characteristic with calculated component value.



$$C_1 = T_1 - \frac{T_2}{R}$$

$$C_2 = \frac{T_2}{R}$$

$$R = \frac{T_2^2}{T_1 T_2 - T_1 T_3}$$

Time constant of a filter such as T_1, T_2 and T_3 are computable by the following formula under condition of $K = K_v K_p$ and $\omega_c = 2\pi f_c$.

$$T_1 = \frac{K}{N}\left|\frac{1 + j\omega_c T_2}{-\omega_c^2(1 + j\omega_c T_3)}\right|$$

$$T_2 = \frac{1}{\omega_c}\tan\left(\frac{90 + \phi_c}{2}\right)$$

$$T_3 = \frac{1}{\omega_c^2 T_2}$$

Each parameter is the following table. f_c and ϕ_c are given, the above calculation is performed and the loop filter constant parameters are obtained.

Symbol	Modulation		Demodulation		Unit
	2.3	2.8	2.3	2.8	MHz
N	115	140	1		-
Kv	$3.6\times10^{6}\times2\pi$		$0.12\times10^{6}\times2\pi$		rad/s/V
Kp	$\frac{250\times10^{-6}}{2\pi}$				A/rad

T_1, T_2 and T_3 are regarded as the following formulas with component parameters obtained of loop filter.

$$T_1 = C_1 + C_2$$

$$T_2 = RC_2$$

$$T_3 = \frac{RC_1C_2}{C_1 + C_2}$$

About each transfer function, their frequency characteristics are computable under condition of $s = j\omega$.

- Open loop transfer function $G_{open}(s)$

$$G_{open}(s) = \frac{sKT_2 + K}{s^3NT_1T_3 + s^2NT_1}$$

- Phase shift characteristic ϕ

The imaginal part of $G_{open}(s)$ is defined as $\mathrm{Im}\,G_{open}(s)$, and the real part of $G_{open}(s)$ is defined as $\mathrm{Re}\,G_{open}(s)$.

$$\phi = \frac{180}{\pi}\tan^{-1}\frac{\mathrm{Im}\,G_{open}(s)}{\mathrm{Re}\,G_{open}(s)}$$

- Modulation transfer function $G_{\mathrm{mod}}(s)$

$$G_{\mathrm{mod}}(s) = \frac{s^3NT_1T_3 + s^2NT_1}{s^3NT_1T_3 + s^2NT_1 + sKT_2 + K}$$

- Demodulation transfer function $G_{de\,\mathrm{mod}}(s)$

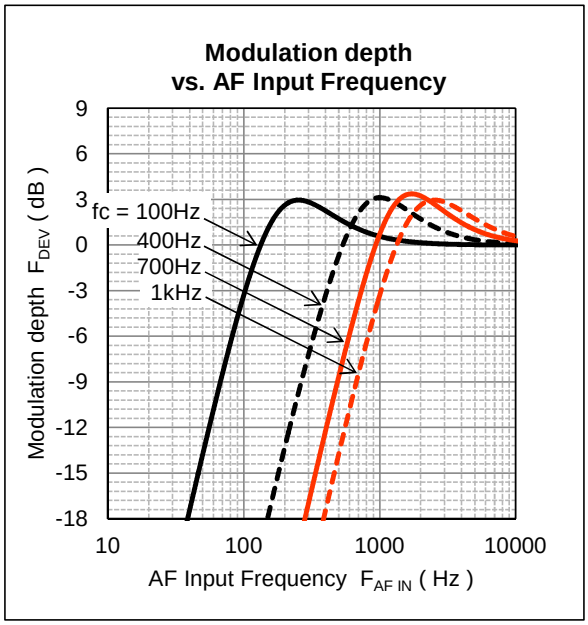
$$G_{de\,\mathrm{mod}}(s) = \frac{sKNT_2 + KN}{s^3NT_1T_3 + s^2NT_1 + sKT_2 + K}$$

Loop filter must be designed to work stably in a desired frequency response from the above calculation.

● Calculation example of loop filter

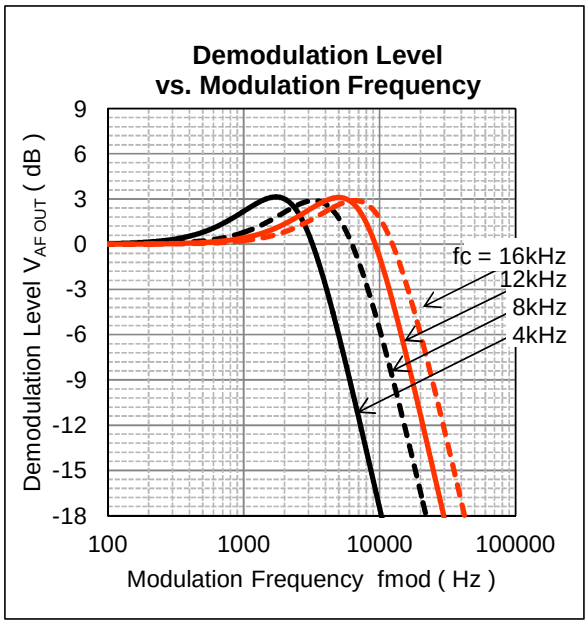
The following is the constant parameters and frequency characteristic as result of above calculation. The phase margin is 45 deg as the condition. S/N and harmonic distortion characteristics, etc. are strongly related to bandwidth.

- Modulation depth of AF input frequency (at carrier frequency 2.8MHz)



Cutoff frequency f_c [Hz]	C_1 [nF]	C_2 [nF]	R [kΩ]
100	2200	12000	0.20
400	150	820	0.82
700	47	220	1.50
1000	22	120	2.00

- Demodulation level of modulation frequency



Cutoff frequency f_c [kHz]	C_1 [nF]	C_2 [nF]	R [kΩ]
4	56	270	0.62
8	12	68	1.2
12	6.8	33	1.8
16	3.3	18	2.4