NJW4109

45 V, I_O = 500 mA LDO WITH POWER-GOOD

■ FEATURES

- Fast transient response
- Wide operating voltage 4.0 V to 40 V
- Wide operating temperature T_a = −40°C to 125°C
- Output voltage accuracy V_O ±1.0%
  (V_{IN} = V_O + 1 V to 40 V, I_O = 0 mA to 500 mA, T_a = 25°C)
- Output current 500 mA (min)
- ON/OFF control
- Ceramic capacitor compatible
- Power-good output
- Undervoltage lockout (UVLO)
- Thermal shutdown
- Overcurrent protection
- Package TO-252-5-L5

■ APPLICATIONS

- Car infotainment
- Active antenna power supplies
- Automotive camera power supplies
- External power supplies for industrial equipment

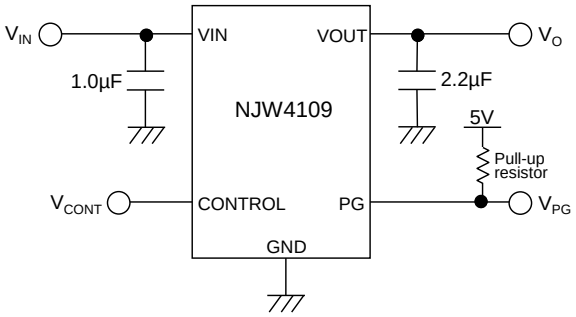
■ DESCRIPTION

The NJW4109 is a 45 V, I_O = 500 mA low dropout regulator with power-good. Power-good outputs whether the output voltage is within the normal range as a flag and notifies the MCU of the abnormal state. This device achieves fast transient response and offers stable output voltage even at line or load fluctuations.

The NJW4109 provides outstanding high output voltage accuracy that guaranteed ±1.0% under the conditions of V_{IN} = V_O + 1 V to 40 V, I_O = 0 mA to 500 mA.

Moreover, wide operating voltage, wide operating temperature, and power-good output make the NJW4109 ideal for automotive equipment or applications that require high reliability.

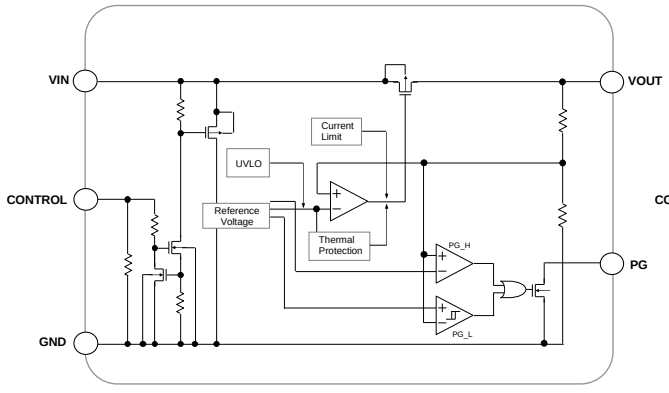
■ TYPICAL APPLICATION



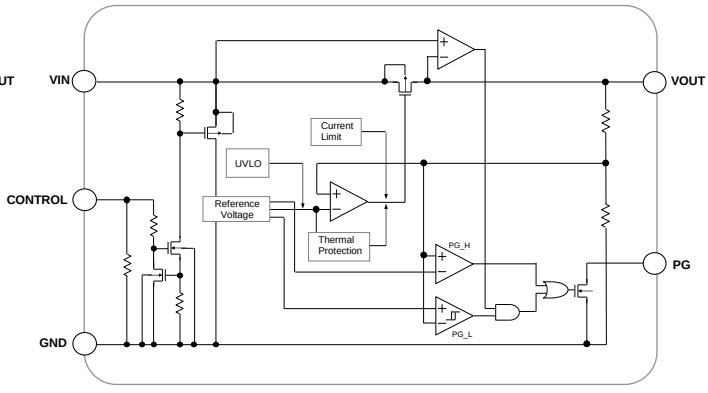
■ PRODUCT INFORMATION

PRODUCT NAME	FUNCTION
NJW4109DL5-A	PG detection of V_O due to V_{IN} drop is valid
NJW4109DL5-B	PG detection of V_O due to V_{IN} drop is invalid

■ BLOCK DIAGRAM



A-Version



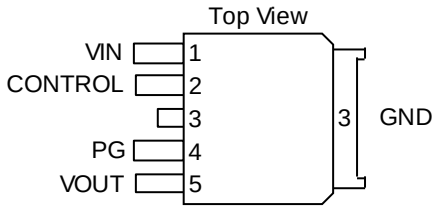
B-Version

■ OUTPUT VOLTAGE RANK

PRODUCT NAME	OUTPUT VOLTAGE
NJW4109DL5-08A	8.0V
NJW4109DL5-08B	8.0V

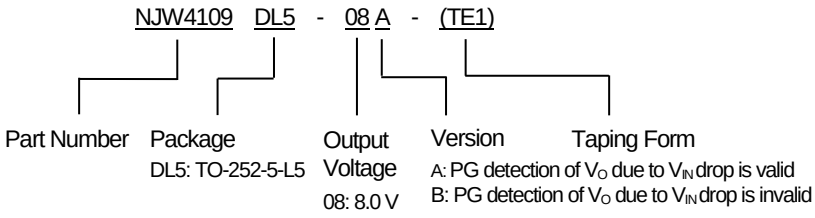
■ PIN CONFIGURATION

TO-252-5-L5



PIN NO.	NAME	FUNCTION
1	VIN	Input pin
2	CONTROL	ON/OFF control pin (active high)
3	GND	Ground pin
4	PG	Power-good pin (N-channel open-drain)
5	VOUT	Output pin

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4109DL5-08A (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	109A08	301	3000
NJW4109DL5-08B (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	109B08	301	3000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage	V_{IN}	−0.3 to 45	V
Control Pin Voltage	V_{CONT}	−0.3 to 45	V
Output Voltage	V_O	−0.3 to $V_{IN} \leq +17$ (1)	V
Power-Good Pin Voltage	V_{PG}	−0.3 to 45	V
Power Dissipation (T_a = 25°C) TO-252-5-L5	P_D	2-Layer / 4-Layer / High Power 4-Layer 890 (2) / 3200 (3) / 5200 (4)	mW
Junction Temperature	T_j	−40 to 150	°C
Storage Temperature	T_{stg}	−50 to 150	°C

(1) When the input voltage is less than 17 V, the absolute maximum output voltage is equal to the input voltage. If the input voltage is below 17 V, the maximum output voltage is 17 V.
(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(3) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
(4) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
*For the specifications of each board, see the BOARD SPECIFICATIONS.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage	V_{IN}	4.0 to 40	V
Control Voltage	V_{CONT}	0 to 40	V
Output Current	I_O	0 to 500	mA
Power-Good Pin Voltage	V_{PG}	0 to 40	V
Operating Temperature	T_{opr}	−40 to 125	°C

■ **ELECTRICAL CHARACTERISTICS** V_{IN} = V_O + 1 V, C_{IN} = 1.0 µF, C_O =2.2 µF, T_a = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
LDO REGULATOR							
Output Voltage	V_O	V_{IN} = V_O + 1 V to 40 V, I_O = 0 mA to 500 mA		−1.0%	-	+1.0%	V
Quiescent Current	I_Q	I_O = 0 mA, except I_{CONT}		-	90	130	µA
Quiescent Current at Control OFF	$I_{Q\,(OFF)}$	V_{CONT} = 0 V		-	-	3	µA
Output Current	I_O	V_O × 0.9		500	-	-	mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = V_O + 1 V to 40 V, I_O = 30 mA	V_O = 8 V	-	-	52.5	mV
Load Regulation	$\Delta V_O/\Delta I_O$	I_O = 0 mA to 500 mA	V_O = 8 V	-	-	36.0	mV
Ripple Rejection	RR	V_{IN} = V_O + 1 V, ein = 200 mVrms, f = 1 kHz, I_O = 10 mA	V_O = 8 V	-	50	-	dB
Dropout Voltage 1	ΔV_{IO1}	I_O = 300 mA		-	0.24	0.42	V
Dropout Voltage 2	ΔV_{IO2}	I_O = 500 mA		-	0.40	0.70	V
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T_a$	T_a = −40°C to 125°C, I_O = 30 mA		-	±50	-	ppm/°C
CONTROL							
Control Current	I_{CONT}	V_{CONT} = 1.6 V		-	0.5	2.0	µA
Output ON Control Voltage	$V_{CONT\,(ON)}$			1.6	-	-	V
Output OFF Control Voltage	$V_{CONT\,(OFF)}$			-	-	0.6	V
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Release Voltage	V_{UVLO}	V_{IN} = Sweep Up		2.3	2.7	3.1	V
UVLO Hysteresis Voltage	V_{UVLO_HYS}	V_{IN} = Sweep Down		200	500	-	mV
POWER-GOOD							
High-Level Detection Voltage	V_{THH_PG}	V_O = Sweep Up		105	110	115	%
Low-Level Detection Voltage	V_{THL_PG}	V_O = Sweep Down		85	90	95	%
Low-Level Release Hysteresis Voltage	V_{HYS_PG}	V_O = Sweep Up		1	2	-	%
Leakage Current at OFF	I_{LEAK_PG}	V_{PG} = 5 V		-	-	0.3	µA
Power-Good ON-Resistance	R_{ON_PG}	I_{PG} = 4 mA		-	220	280	Ω

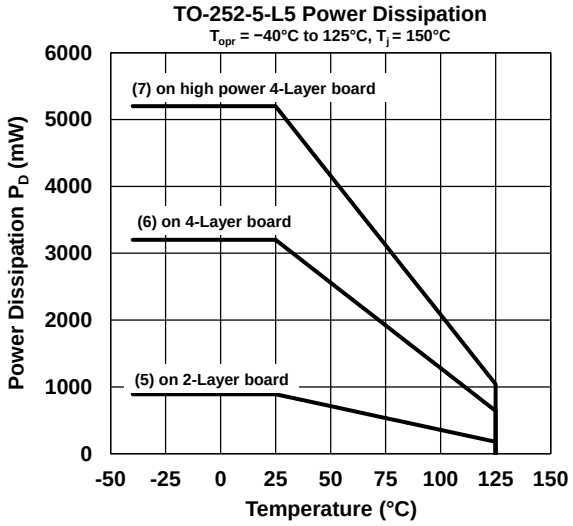
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-To-Ambient Thermal Resistance TO-252-5-L5	θ_{ja}	2-Layer / 4-Layer / High Power 4-Layer 140 (5) / 39 (6) / 24 (7)	°C/W
Junction-To-Top of Package Characterization Parameter TO-252-5-L5	Ψ_{jt}	2-Layer / 4-Layer / High Power 4-Layer 27 (5) / 12 (6) / 9 (7)	°C/W

■ BOARD SPECIFICATIONS

BOARD		JEDEC 2-LAYER BOARD	JEDEC 4-LAYER BOARD	HIGH POWER 4-LAYER BOARD
Dimension		76.2 mm × 114.3 mm, t = 1.6 mm		
Material		FR-4		
Cu Area	Surface Layer (Thickness: 70 µm)	Recommended land pattern + Measurement wiring	Recommended land pattern + Measurement wiring	Recommended land pattern + Heat dissipation pattern (50 mm × 50 mm) + Measurement wiring
	2nd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm	74.2 mm × 74.2 mm
	3rd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm	74.2 mm × 74.2 mm
	Back Layer (Thickness: 70 µm)	-	-	74.2 mm × 74.2 mm
Thermal Vias		-	Connected from surface layer to 2nd layer	All layers are connected

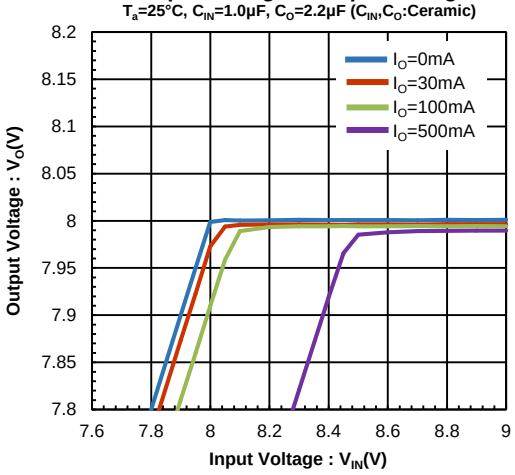
■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



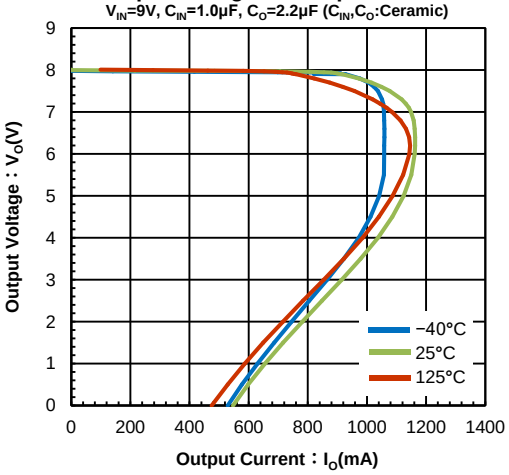
(5) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(6) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
(7) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ TYPICAL CHARACTERISTICS

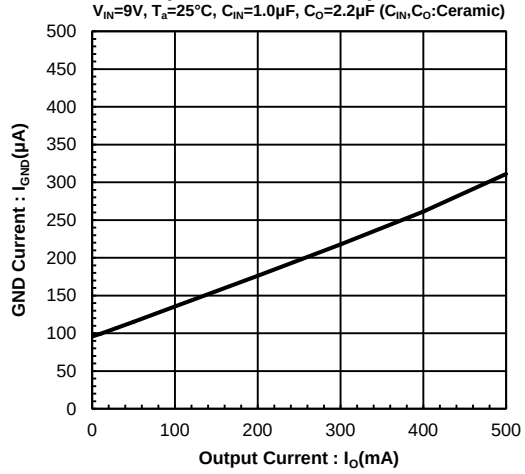
NJW4109
Output Voltage vs. Input Voltage
T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



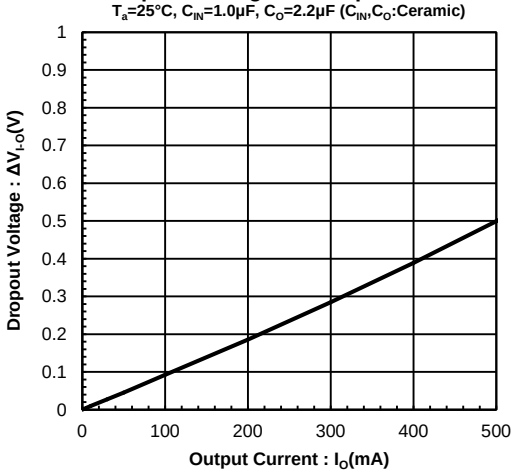
NJW4109
Output Voltage vs. Output Current
V_{IN}=9V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



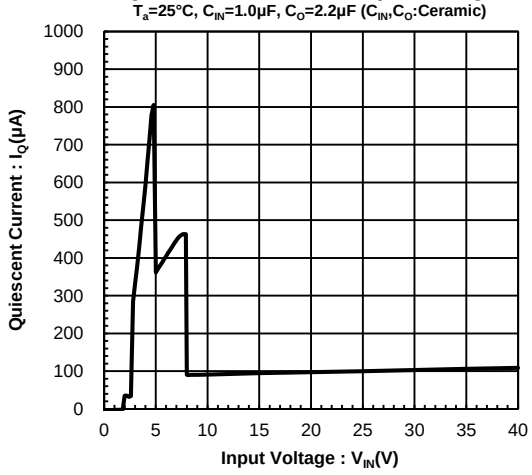
NJW4109
GND pin Current vs. Output Current
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



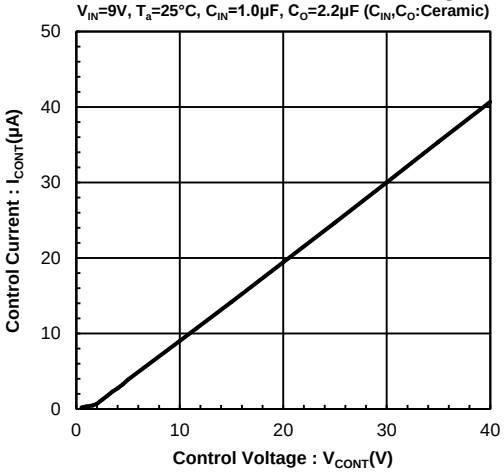
NJW4109
Dropout Voltage vs. Output Current
T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



NJW4109
Quiescent Current vs. Input Voltage
T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

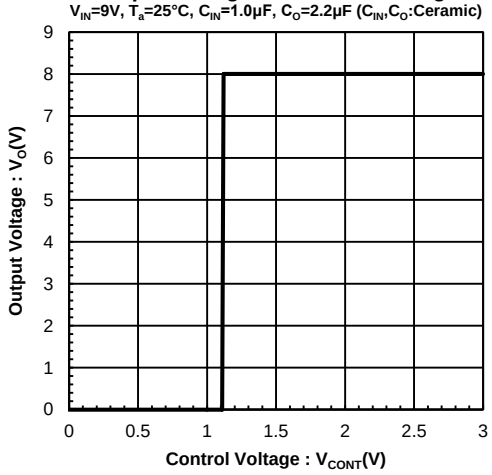


NJW4109
Control Current vs. Control Voltage
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

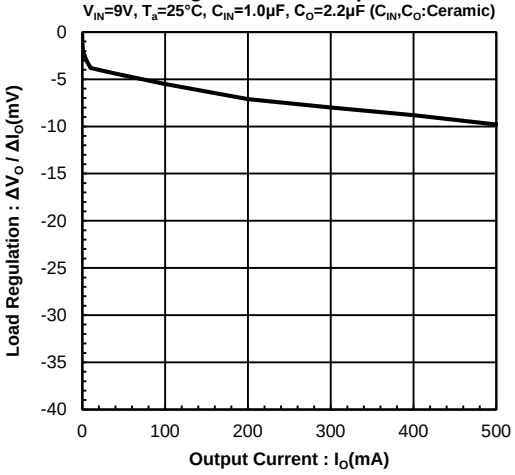


■ TYPICAL CHARACTERISTICS

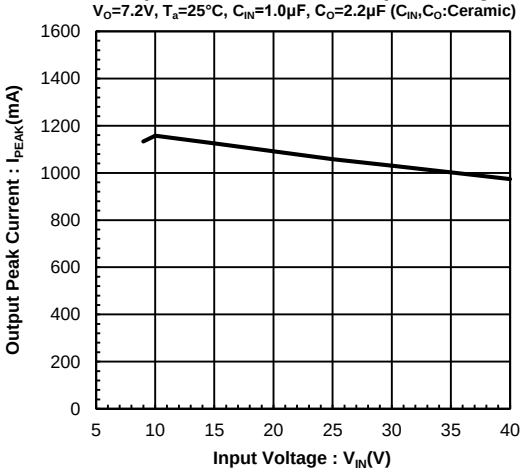
NJW4109
Output Voltage vs. Control Voltage
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



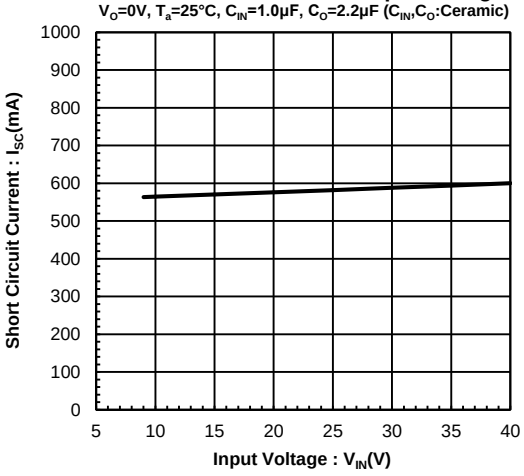
NJW4109
Load Regulation vs. Output Current
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



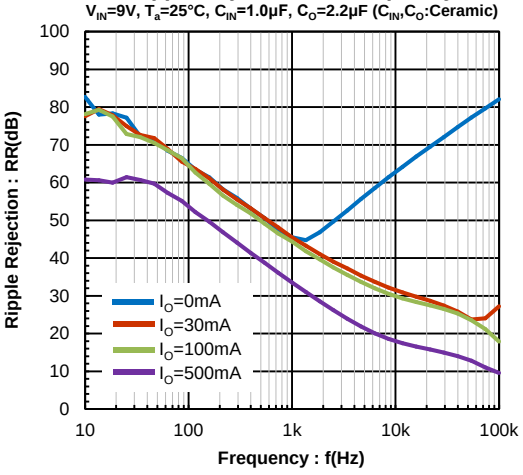
NJW4109
Output Peak Current vs. Input Voltage
V_O=7.2V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



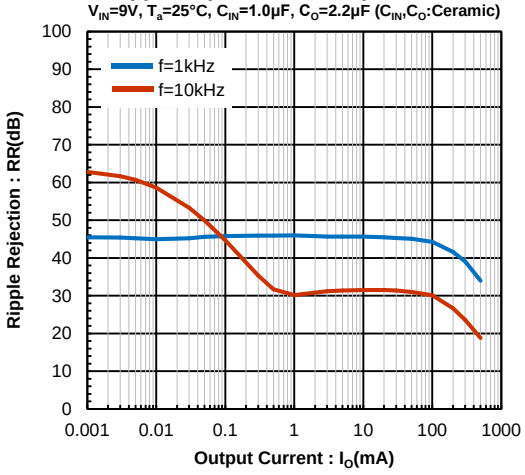
NJW4109
Short Circuit Current vs. Input Voltage
V_O=0V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



NJW4109
Ripple Rejection vs. Frequency
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

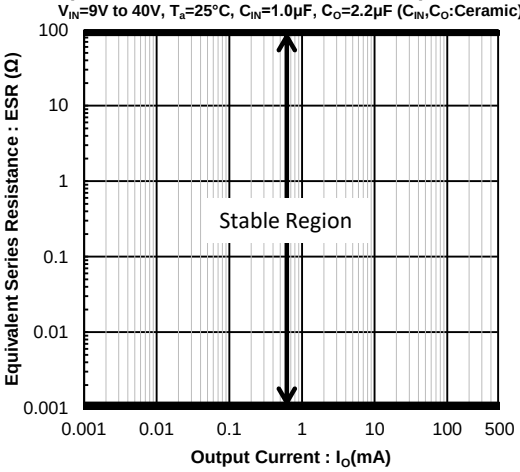


NJW4109
Ripple Rejection vs. Output Current
V_{IN}=9V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

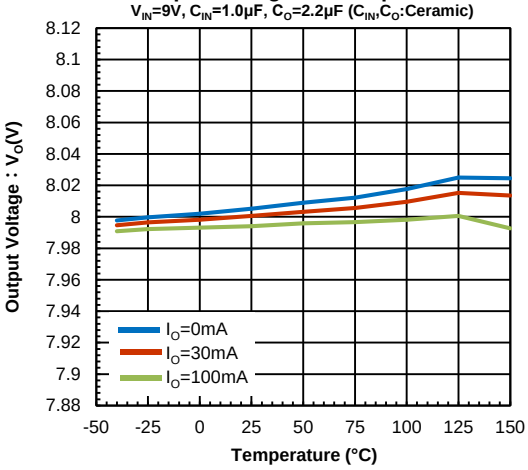


■ TYPICAL CHARACTERISTICS

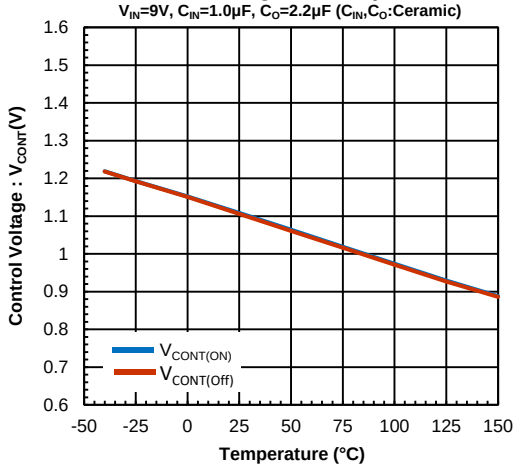
NJW4109
Equivalent Series Resistance vs. Output Current
V_{IN}=9V to 40V, T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



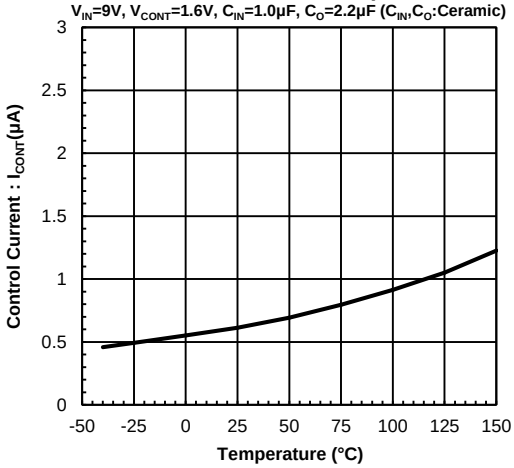
NJW4109
Output Voltage vs. Temperature
V_{IN}=9V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



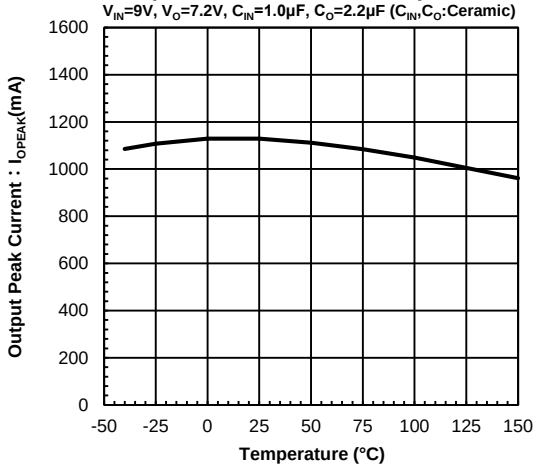
NJW4109
Control Voltage vs. Temperature
V_{IN}=9V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



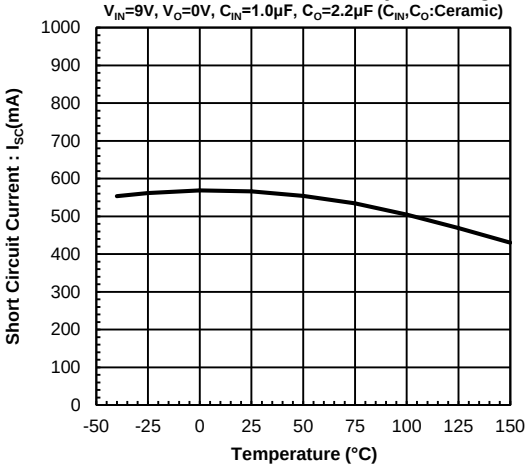
NJW4109
Control Current vs. Temperature
V_{IN}=9V, V_{CONT}=1.6V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



NJW4109
Output Peak Current vs. Temperature
V_{IN}=9V, V_O=7.2V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

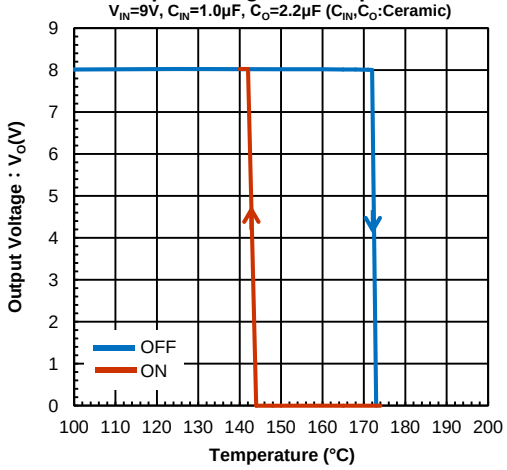


NJW4109
Short Circuit Current vs. Input Voltage
V_{IN}=9V, V_O=0V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)

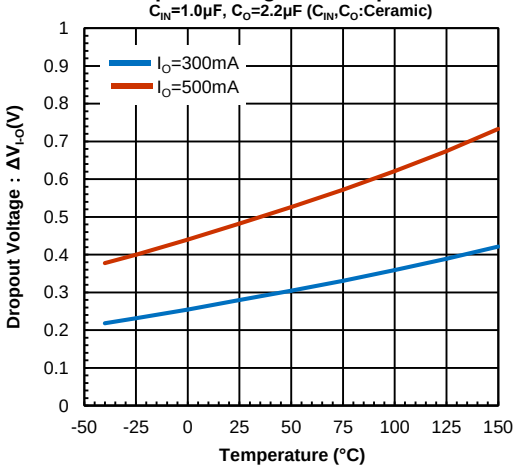


■ TYPICAL CHARACTERISTICS

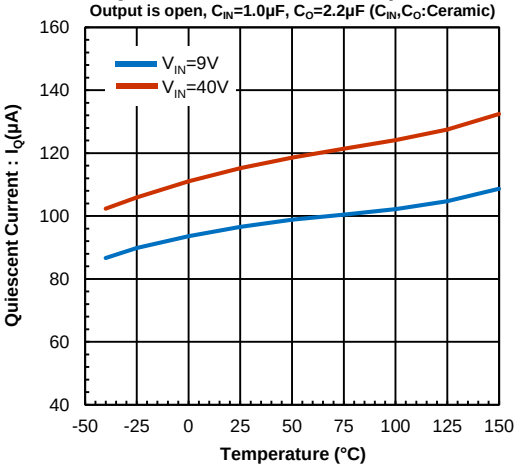
NJW4109
Output Voltage vs. Temperature
V_{IN}=9V, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



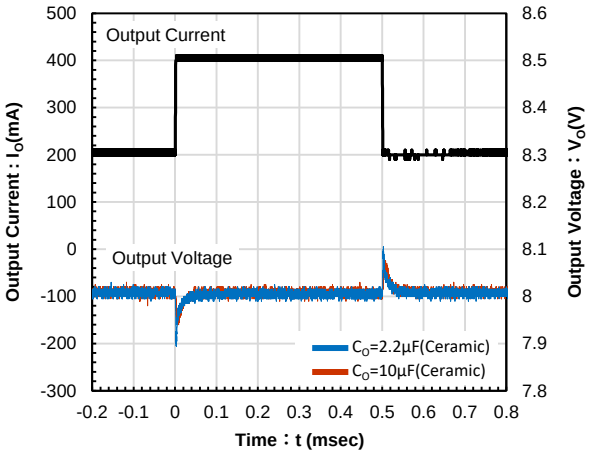
NJW4109
Dropout Voltage vs. Temperature
C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



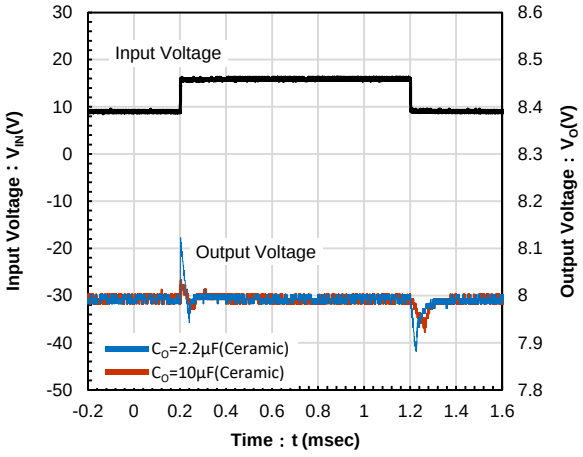
NJW4109
Quiescent Current vs. Temperature
Output is open, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



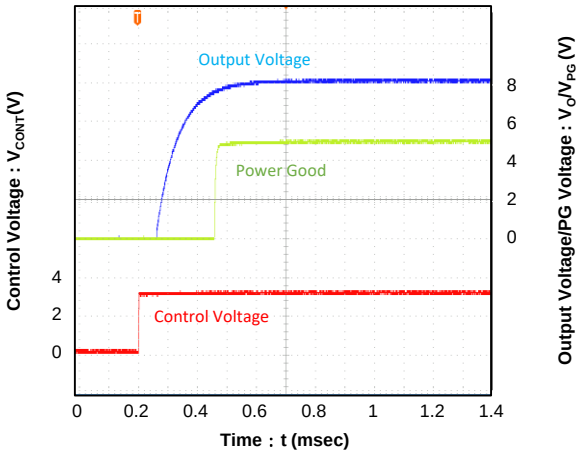
NJW4109
Load Transient Responce
V_{IN}=13.5V, I_O=200mA to 400mA, T_a=25°C



NJW4109
Line Transient Responce
V_{IN}=9V to 16V, I_O=10mA, T_a=25°C

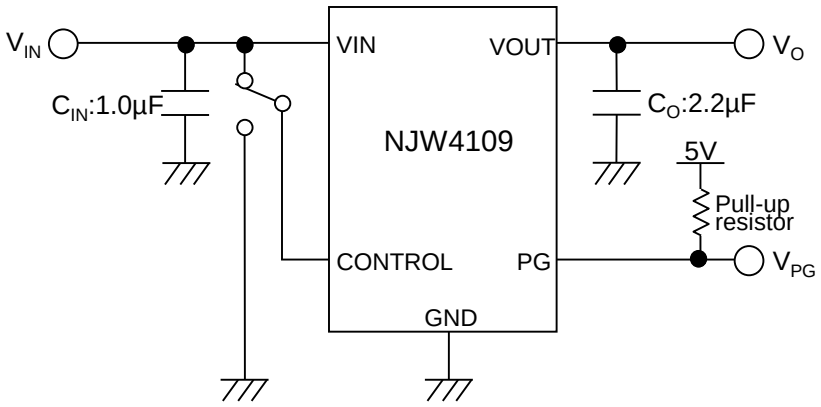


NJW4109
ON/OFF Transient Response
V_{IN}=9V, I_O=30mA, PG pull up to 5.0V(100kΩ)
T_a=25°C, C_{IN}=1.0µF, C_O=2.2µF (C_{IN},C_O:Ceramic)



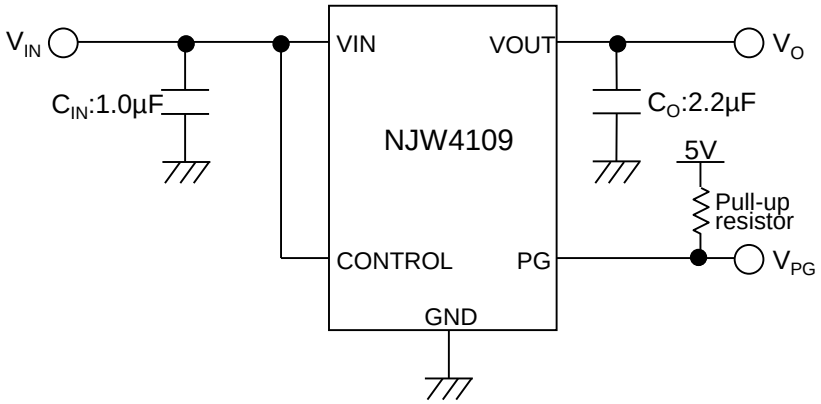
■ TYPICAL APPLICATION

① When ON/OFF control is used.



The CONTROL pin is turned on at high level and turned off at open or GND level.

② When ON/OFF control is not used.



Connect the CONTROL pin to the V_{IN}.

■ APPLICATION NOTE

Input Capacitor (C_{IN})

The C_{IN} prevents oscillations and reduce power supply ripple of applications when the power supply impedance is high or power supply line is long. Connecting a 1.0 µF or larger C_{IN} between VIN and GND pins as short path as possible.

Output Capacitor (C_O)

C_O is necessary for phase compensation of the internal error amplifier in the regulator, and the capacitance value and ESR affect the stability of the circuit. If a capacitor less than 2.2 µF is used, output noise and/or regulator oscillation may occur due to lack of the phase compensation. For stable operation, connect a 2.2 µF or larger C_O within the stable operation region (0.001 Ω ≤ ESR ≤ 100 Ω) between the VOUT and GND pins as short path as possible. The recommended capacitance value varies depending on the output voltage, and a low output voltage may require a large capacitance value; therefore, confirm the recommended capacitance of the required output voltage. As the capacitance value of C_O increases, output noise and ripple decrease, and the response to output load fluctuations also improves.

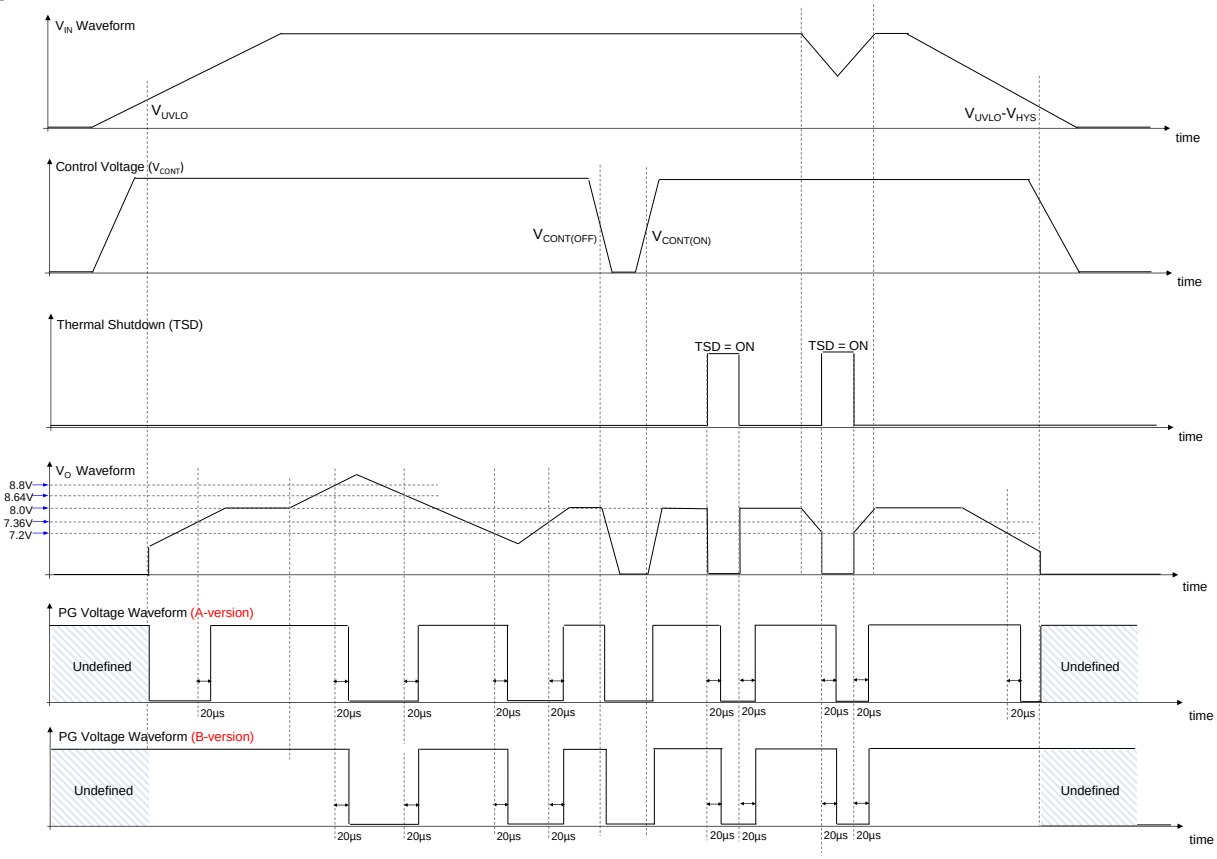
Select the output capacitor considering various characteristics such as frequency characteristics, temperature characteristics, and DC bias characteristics. For the C_O, a capacitor with excellent temperature characteristics and sufficient margin for output voltage is recommended.

Power-Good Output (PG)

The PG monitors the output status and outputs a signal from the open-drain PG pin. When the VOUT pin is stable at 90% (typ) < V_O < 110% (typ), the power-good output becomes high impedance. The power-good output goes low when V_O ≤ 90% or V_O ≥ 110%.

The NJW4109 is available in two versions, and can select whether to monitor the output voltage fluctuations caused by a drop in V_{IN}. The A-version outputs a PG signal when the V_O falls below the set value due to a drop in V_{IN}. The B-version does not output a PG signal even when the V_O falls below the set value due to a drop in V_{IN}. The following timing chart shows the difference between the operation of the A and B versions. To prevent malfunction of power-good output, a delay time of approximately 20 µs and 2% (typ) hysteresis for release from undervoltage detection are provided.

Timing Chart



■ REVISION HISTORY

DATE	REVISION	CHANGES
May 19, 2022	Ver.1.0	Initial Release

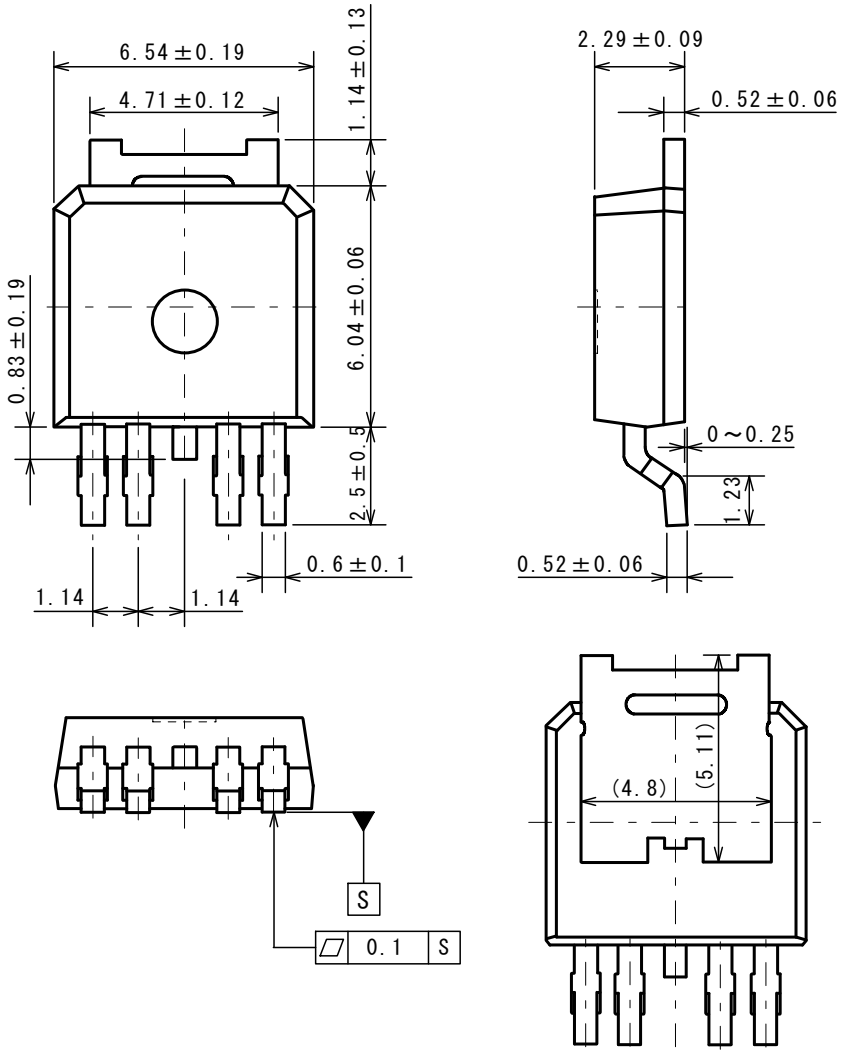
Nisshinbo Micro Devices Inc.

TO-252-5-L5

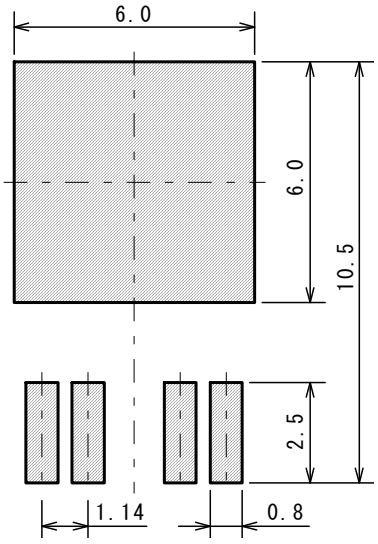
PI-TO-252-5-L5-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nisshinbo Micro Devices Inc.

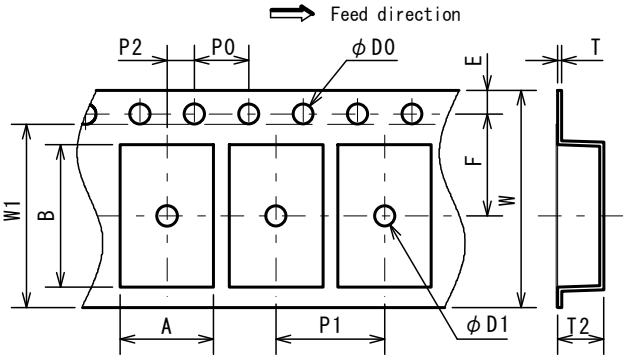
TO-252-5-L5

PI-TO-252-5-L5-E-A

■ PACKING SPEC

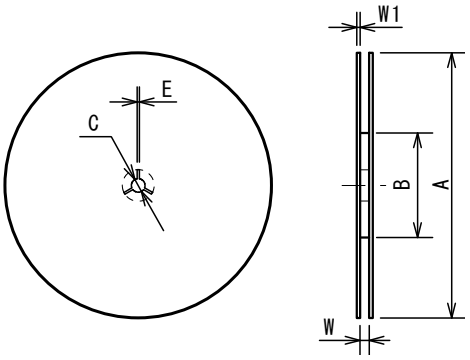
UNIT: mm

TAPING DIMENSIONS



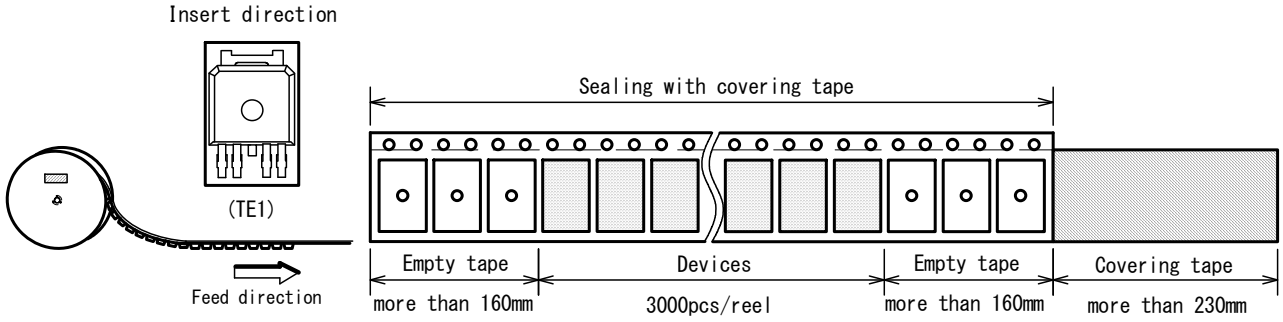
SYMBOL	DIMENSION	REMARKS
A	6.9±0.1	BOTTOM DIMENSION
B	10.5±0.1	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	7.5±0.1	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.1	
T	0.3±0.1	
T2	3.4 max	
W	16.0±0.3	
W1	13.5	THICKNESS 0.1max

REEL DIMENSIONS

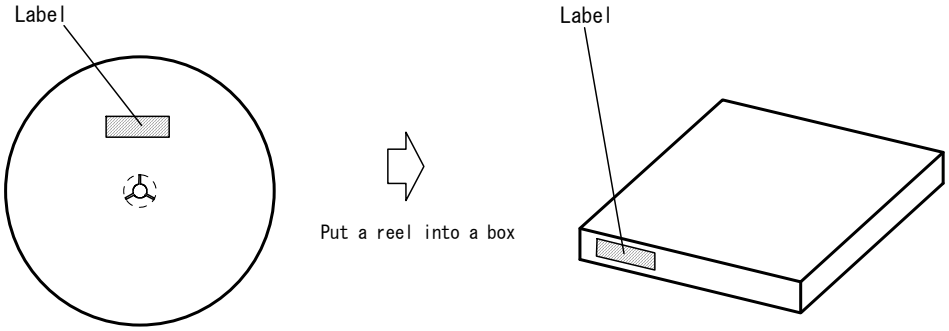


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.5
E	2
W	17.5±0.5
W1	2±0.5

TAPING STATE



PACKING STATE



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