

Io=500mA LDO with Watchdog Timer

■ GENERAL DESCRIPTION

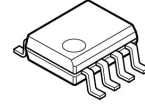
The NJW4113 is a 500mA output low dropout voltage regulator with watchdog timer(WDT).

It has a detecting circuit to monitor output voltage and a watchdog timer function for clock monitor. Detecting voltage is adjustable with external resistor.

Low consumption current characteristic contributes to reduce burden on automotive battery in full-time operating application.

Because of operating wide temperature range from -40°C to +125°C, the NJW4113 suits for high reliability application such as automotive application.

■ PACKAGE OUTLINE

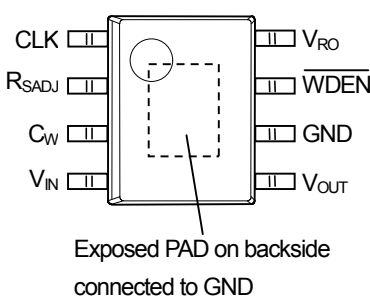


NJW4113GM1

■ FEATURES

- Wide Operating Voltage Range 4.0V to 40V max.
- Low Current Consumption 37μA typ.
- High Precision Output Voltage $V_o \pm 1.0\%$ ($T_a=25^\circ\text{C}$)
 $V_o \pm 1.5\%$ ($T_a=-40^\circ\text{C}$ to 125°C)
- High Precision Detection Voltage $V_{DET} \pm 1.0\%$ ($T_a=25^\circ\text{C}$)
 $V_{DET} \pm 2.0\%$ ($T_a=-40^\circ\text{C}$ to 125°C)
- Output Current $I_o(\text{min.})=500\text{mA}$
- Adjustable Detection Voltage with external resistor
- Setting WDT Monitor Time, WDT Reset Time and Output Delay Hold Time with external capacitor
- Watchdog Timer Enable Function
- Correspond to Low ESR capacitor (MLCC)
- Thermal shutdown circuit
- Over Current Protection
- Package Outline HSOP8

■ PIN CONFIGURATION



1. CLK Clock Input Pin
2. RSADJ External Resistor Pin for Adjusting Detection Voltage
3. CW External Capacitor Pin for Setting WDT Monitor Time/ Output delay hold Time
4. VIN Input Voltage Pin
5. VOUT Output Voltage Pin
6. GND Ground Pin
7. WDEN Watchdog Timer Disable Pin
8. VRO Reset Output Pin

■ PRODUCT CLASSIFICATION

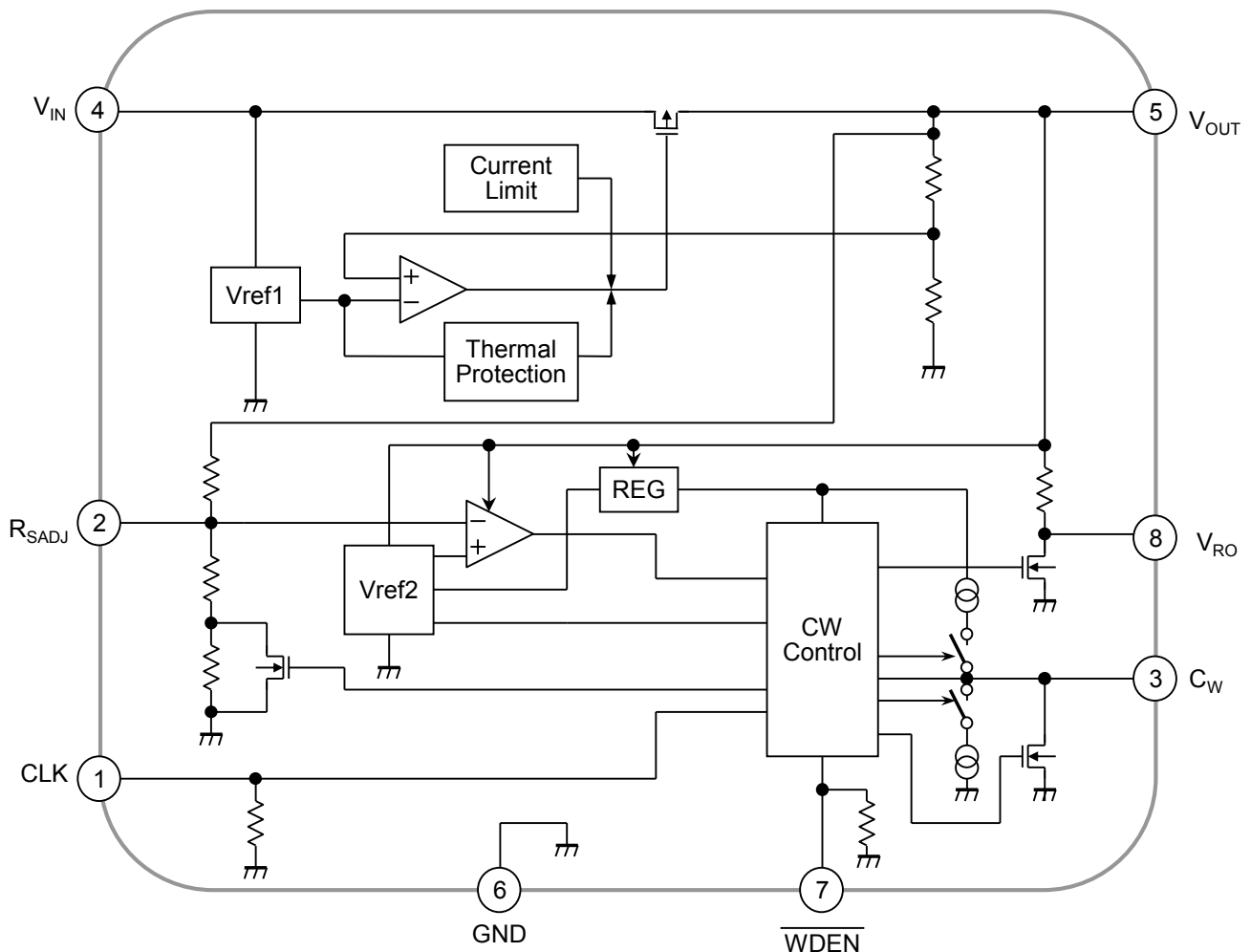
Status	Device Name	Version	Output Voltage	Detection Voltage
M.P.	NJW4113GM1-A46-T1	A	5.0V	4.6V
	NJW4113GM1-A41-T1			4.1V
PLAN	NJW4113GM1-B03-T1	B	3.3V	3.0V

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■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
CLK	1	Clock Input pin. Monitor the clock from CPU.
R _{SADJ}	2	For Adjusting Detection Voltage pin. It can optionally adjust Detection Voltage by connecting resistor divider. If it is not required, this pin should be "open".
C _W	3	Connects Capacitor pin for setting WDT Monitor Time, WDT Reset Time and Output Delay Hold time. It can optionally set time by external capacitor.
V _{IN}	4	Power Supply pin.
V _{OUT}	5	Output Voltage pin.
GND	6	GND pin.
$\overline{\text{WDEN}}$	7	Enable pin for WDT. When the High level is WDT active while Low level or OPEN is WDT inactive.
V _{RO}	8	Reset Output pin. When output voltage is below the detection voltage, Output Low level signal. V _{RO} pin pulls up to V _{OUT} internally with 100kΩ typ.
Exposed PAD	-	Connected to GND.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.3 to +45	V
Output Voltage	V_O	-0.3 to $V_{IN} \leq +6$	V
RESET Output Voltage	V_{RO}	-0.3 to +6	V
Clock Input Voltage	V_{CLK}	-0.3 to +5.5	V
WDEN Input Voltage	V_{WDEN}	-0.3 to + 5.5	V
RSADJ Pin Input Voltage	V_{RSADJ}	-0.3 to + 5.5	V
Power Dissipation	P_D	790(*1)	mW
		2500(*2)	
Junction Temperature	T_J	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 4Layers)

(4Layers inner foil: 74.2 x 74.2mm applying a thermal via hole to a board based on JEDEC standard JESD51-5)

■ INPUT VOLTAGE RANGE

$V_{IN} = 4.0V$ to 40V

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■ ELECTRICAL CHARACTERISTICS

(General Characteristics)

(Unless otherwise noted, $V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{SS}	WDT Active	-	37	70	μA
		WDT Active, $T_a = -40^\circ C$ to $+125^\circ C$	-	-	80	

(Regulator Block)

(Unless otherwise noted, $V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	$I_O=30mA$	-1.0%	-	+1.0%	V
		$I_O=30mA$, $T_a = -40^\circ C$ to $+125^\circ C$	-1.5%	-	+1.5%	
Output Current	I_O	$V_O \times 0.9$	500	-	-	mA
		$V_O \times 0.9$, $T_a = -40^\circ C$ to $+125^\circ C$	500	-	-	
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN}=V_O+1V$ to $40V$, $I_O=30mA$	-	-	0.05	%V
		$V_{IN}=V_O+1V$ to $40V$, $I_O=30mA$, $T_a = -40^\circ C / +125^\circ C(*3)$	-	-	0.05	
Load Regulation	$\Delta V_O / \Delta I_O$	$I_O=0mA$ to $500mA$	-	0.002	0.004	%mA
		$I_O=0mA$ to $500mA$, $T_a = -40^\circ C / +125^\circ C(*3)$	-	-	0.008	
		$I_O=30mA$ to $500mA$, $T_a = -40^\circ C / +125^\circ C(*3)$	-	-	0.0053	
Ripple Rejection	RR	$V_{IN}=V_O+2V$, $e_{in}=50mV_{rms}$, $f=1kHz$, $I_O=10mA$	-	45	-	dB
Dropout Voltage	ΔV_{IO}	$I_O=300mA$	-	0.3	0.5	V
		$I_O=300mA$, $T_a = -40^\circ C$ to $+125^\circ C$	-	-	0.78	
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T_a$	$I_O=30mA$, $T_a=0^\circ C$ to $125^\circ C$	-	± 50	-	ppm/ $^\circ C$

(*3): These parameter are guaranteed with only $-40^\circ C$ and $+125^\circ C$.

(Voltage Detector Block)

(Unless otherwise noted, $V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Detection Voltage	V_{DET}		-1.0%	-	+1.0%	V
		$T_a = -40^\circ C$ to $+125^\circ C$	-2.0%	-	+2.0%	
Hysteresis Voltage	V_{HYS}		80	100	120	mV
		$T_a = -40^\circ C$ to $+125^\circ C$	50	-	150	
Average temperature coefficient of Detection Voltage	$\Delta V_{DET} / \Delta T_a$	$T_a=0$ to $125^\circ C$	-	± 50	-	ppm/ $^\circ C$
C_W Pin Charge Current at Delay Hold	I_{CWD}	$V_{CW}=0.5V$	3	6	9	μA
		$V_{CW}=0.5V$, $T_a = -40^\circ C$ to $+125^\circ C$	3	-	9	
C_W Pin Threshold Voltage at Reset Release	V_{TCWD}		0.97	1.00	1.03	V
		$T_a = -40^\circ C$ to $+125^\circ C$	0.95	-	1.05	
R_{SADJ} Pin Voltage	V_{RSADJ}	$V_O=V_{DET}$ (Vo detected)	0.97	1.00	1.03	V
		$V_O=V_{DET}$ (Vo detected) $T_a = -40^\circ C$ to $+125^\circ C$	0.95	-	1.05	
Average temperature Coefficient of R_{SADJ} Pin Voltage	$\Delta V_{RSADJ} / \Delta T_a$	$T_a=0^\circ C$ to $+125^\circ C$	-	± 50	-	ppm/ $^\circ C$
Output Delay Hold time	t_{PR}	$C_W=0.01\mu F$, $V_{RO}=L \rightarrow H$	0.7	1.7	3.5	ms
		$C_W=0.01\mu F$, $V_{RO}=L \rightarrow H$, $T_a = -40^\circ C$ to $+125^\circ C$	0.3	-	3.8	
Low level RESET Output Voltage	V_{ROL}	$V_O=V_{DET}-0.5V$	-	0.02	0.2	V
		$V_O=V_{DET}-0.5V$, $T_a = -40^\circ C$ to $+125^\circ C$	-	-	0.2	
RESET Output Block Operating Voltage	V_{OPL}		0.8	-	-	V
		$T_a = -40^\circ C$ to $+125^\circ C$	0.8	-	-	
RESET Output Voltage at Start up	V_{ROU}	V_{IN} start up	-	0.05	-	V
Pull up resistor	R_{PU}		-	100	-	k Ω

■ ELECTRICAL CHARACTERISTICS

(Watchdog Timer Block)

(Unless otherwise noted, $V_{IN}=V_O+1V$, $C_{IN}=1.0\mu F$, $C_O=4.7\mu F$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock input High-level	V_{TCKH}	A version	4.0	-	-	V
		A version, $T_a = -40^\circ C$ to $+125^\circ C$	4.0	-	-	
		B version	2.6	-	-	
		B version, $T_a = -40^\circ C$ to $+125^\circ C$	2.6	-	-	
Clock input Low-level	V_{TCKL}	A version	-	-	1.0	V
		A version, $T_a = -40^\circ C$ to $+125^\circ C$	-	-	1.0	
		B version	-	-	0.7	
		B version, $T_a = -40^\circ C$ to $+125^\circ C$	-	-	0.7	
Clock Input Pulse Width	t_{CKW}		0.05	-	-	ms
		$T_a = -40^\circ C$ to $+125^\circ C$	0.05	-	-	
Clock Input Cycle	t_{CK}		0.1	-	-	ms
		$T_a = -40^\circ C$ to $+125^\circ C$	0.1	-	-	
C_W Pin Discharge Current	I_{CW}	$V_{CW} = 0.5V$	1.5	2	2.5	μA
		$V_{CW} = 0.5V$, $T_a = -40^\circ C$ to $+125^\circ C$	1.1	-	2.9	
C_W Pin Charge Current	I_{CWL}	$V_{CW} = 0.5V$	3	6	9	μA
		$V_{CW} = 0.5V$, $T_a = -40^\circ C$ to $+125^\circ C$	3	-	9	
High-side Threshold Voltage	V_{TCWH}		0.97	1.00	1.03	V
		$T_a = -40^\circ C$ to $+125^\circ C$	0.95	-	1.05	
Low-side Threshold Voltage	V_{TCWL}		0.18	0.2	0.22	V
		$T_a = -40^\circ C$ to $+125^\circ C$	0.16	-	0.24	
WDT Monitor Time	t_{WD}	$C_W=0.01\mu F$	2.9	4.0	5.8	ms
		$C_W=0.01\mu F$, $T_a = -40^\circ C$ to $+125^\circ C$	2.5	-	7.9	
WDT Reset Time	t_{WR}	$C_W=0.01\mu F$	0.6	1.3	2.9	ms
		$C_W=0.01\mu F$, $T_a = -40^\circ C$ to $+125^\circ C$	0.3	-	3.2	
WDEN Pin Threshold Voltage at WDT Disable	V_{TWDIS}		1.6	-	-	V
		$T_a = -40^\circ C$ to $+125^\circ C$	1.6	-	-	
WDEN Pin Threshold Voltage at WDT Enable	V_{TWEN}		-	-	0.3	V
		$T_a = -40^\circ C$ to $+125^\circ C$	-	-	0.3	

The above specification is a common specification for all output voltages.

Therefore, it may be different from the individual specification for a specific output voltage.

* These parameters are tested by Pulse Measurement.

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■ THERMAL CHARACTERISTICS

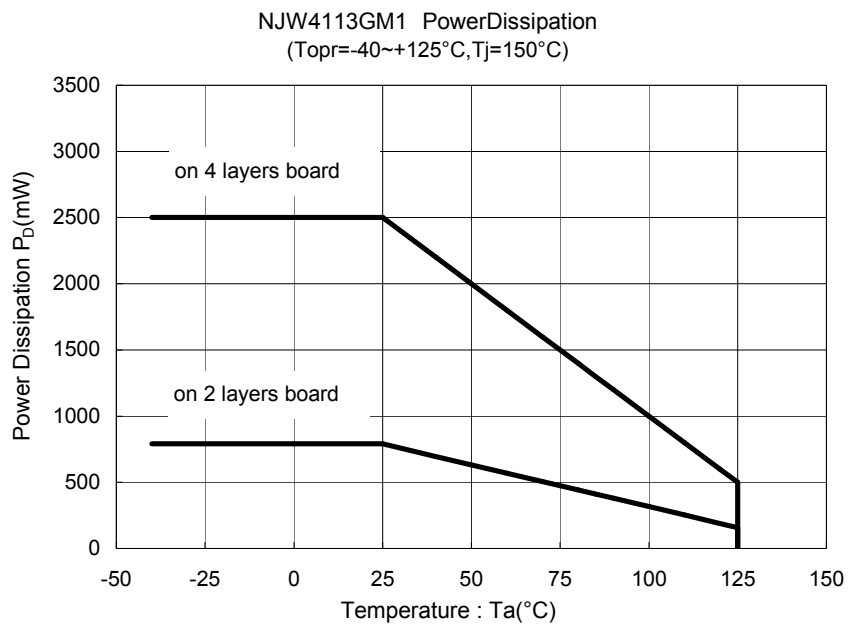
PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance	θ_{ja}	158(*3) 50(*4)	$^{\circ}C/W$
Junction-to-Top of package characterization parameter	ψ_{jt}	28(*3) 12(*4)	$^{\circ}C/W$

(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 2Layers)

(*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 4Layers)

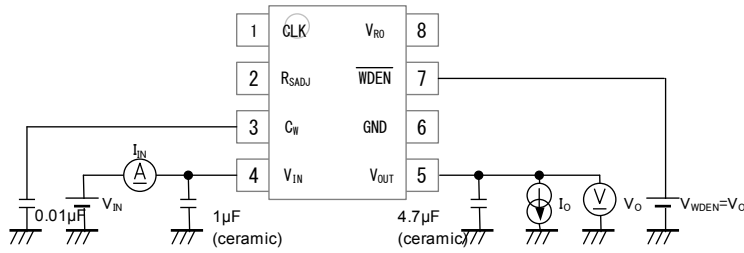
(4Layers inner foil: 74.2 x 74.2mm applying a thermal via hole to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

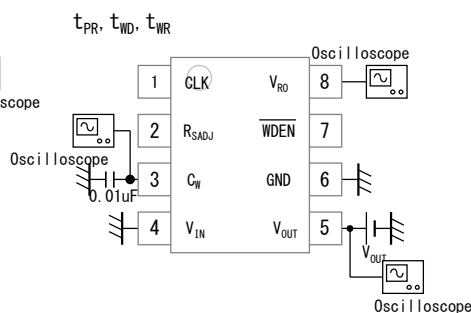
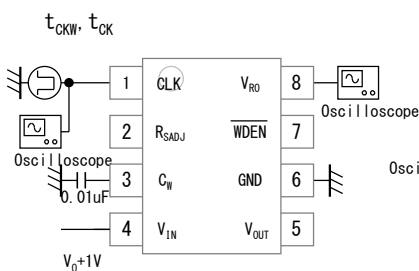
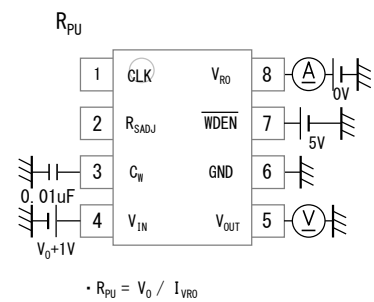
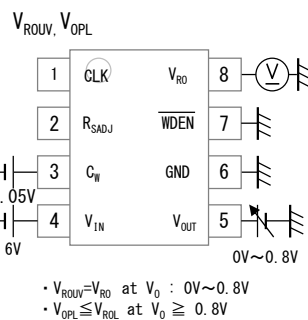
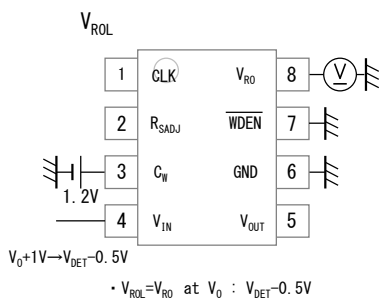
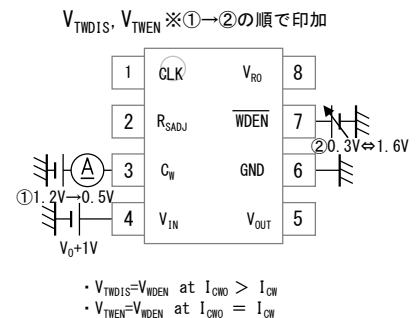
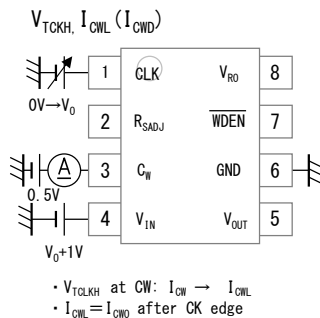
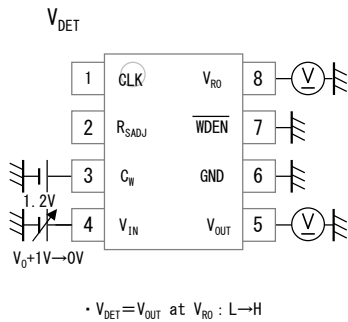
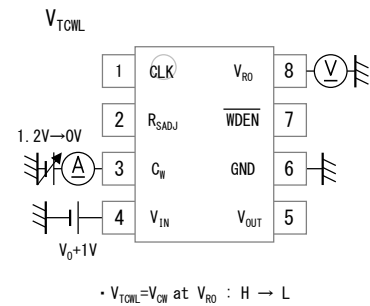
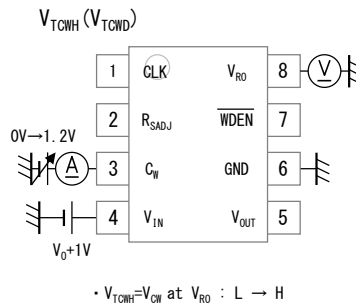
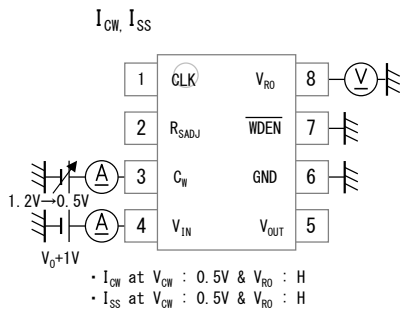


■ TEST CIRCUIT

・LDO BLOCK



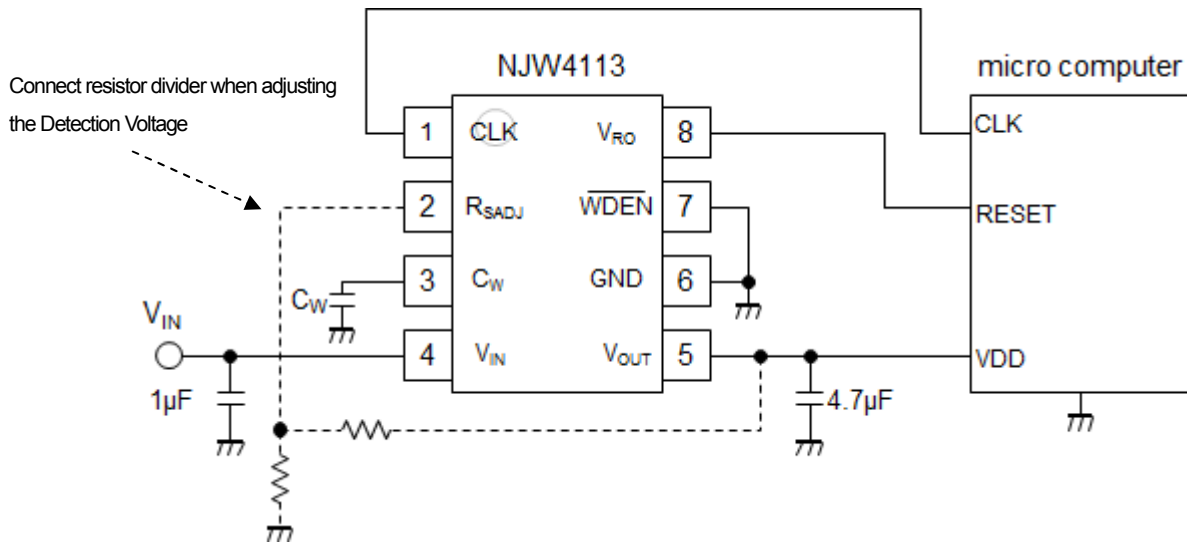
・EXCEPT LDO BLOCK * I_{CWO} : C_W Pin Current, I_{VRO} : V_{RO} Pin Current



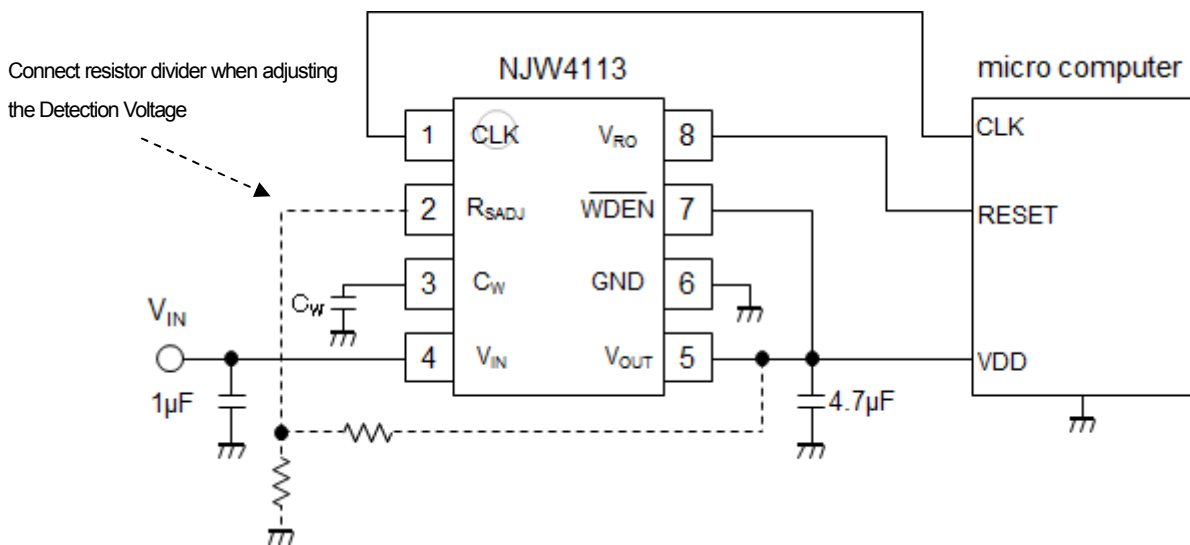
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■ TYPICAL APPLICATION

(1) Monitoring the output voltage of the regulator and the clock of microcomputer



(2) Only use the voltage detector (Watchdog Timer Disable)



*Input Capacitor C_{IN}

The input capacitor C_{IN} is required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{IN} as shortest path as possible to avoid the problem.

*Output Capacitor C_O

The output capacitor C_O will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess an output noise or an oscillation of the regulator due to lack of the phase compensation.

On the other hand, use of a larger C_O reduces an output noise and a ripple output, and also improves an output transient response when a load rapidly changes.

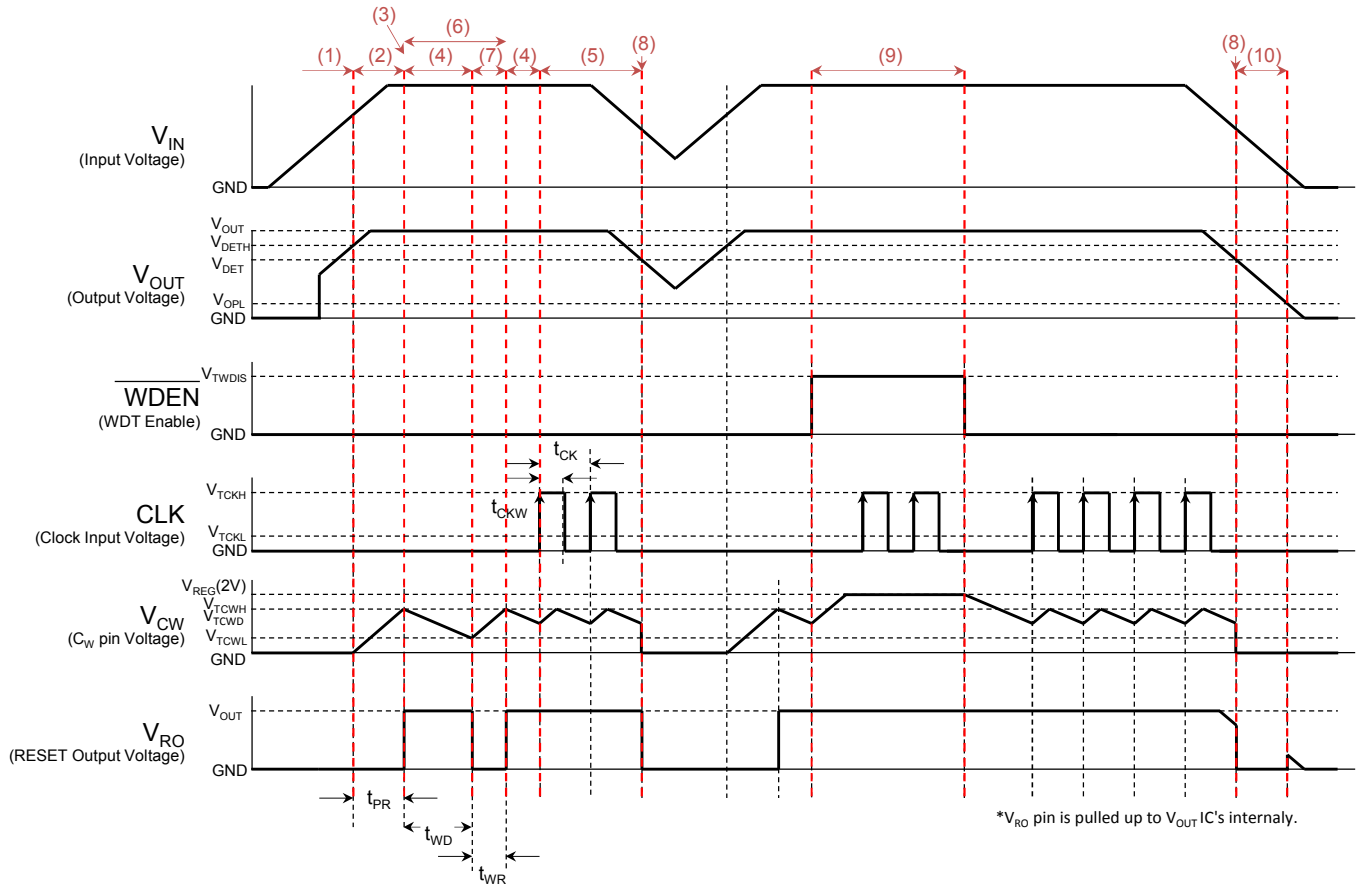
Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation

The recommended capacitance depends on the output voltage rank. Especially, a low voltage regulator requires larger C_O value.

In addition, you should consider varied characteristics of a capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O , recommend that have withstand voltage margin against an output voltage and superior temperature characteristics though this product is designed stability works with wide range ESR of capacitor including low ESR products.

■ TIMING CHART



■ OPERATION EXPLANATION

● Output delay time

The NJW4113 has the output delay time t_{PR} till the RESET outputs "H" in order to prevent malfunction due to chattering after the Output voltage V_{OUT} exceeds the RESET release voltage $V_{DETH} (=V_{DET}+V_{HYS})$

(1) Initialized state

When the Output voltage V_{OUT} is less than the RESET release voltage $V_{DETH} (=V_{DET}+V_{HYS})$, the C_W Pin voltage V_{CW} is 0V and the RESET Output Voltage V_{RO} is "L".

(2) Start of Output delay time

If V_{OUT} exceeds V_{DETH} , C_W pin capacitor is charged by the C_W Pin Charge Current at Delay Hold I_{CWD} (typ.6 μ A) and the output delay time is started. V_{RO} keeps "L" level while the output delay time.

In addition, return to a state of the "(1) Initialized state" ($V_{CW}=0V$, $V_{RO}="L"$) when V_{OUT} is less than V_{DETH} during charging C_W .

(3) Detectable state of the output voltage drop

When V_{CW} reaches the C_W Pin threshold Voltage at Reset Release V_{TCWD} (typ.1.0V), the RESET Output Voltage V_{RO} switched from "L" to "H" and the output voltage drop will be detectable.

The period from a point wherein V_{OUT} exceeds V_{DETH} to a point wherein V_{RO} turns to "H" is taken as t_{PR} . C_W is discharged by the C_W Pin Discharge Current I_{CW} (typ.2 μ A) after V_{CW} has reached V_{TCWD} and V_{CW} start to fall.

- Watchdog timer (WDT) Monitor Time, Watchdog timer (WDT) Reset Time

The NJW4113 can be set the WDT Monitor time t_{WD} for the monitoring the clock(CLK) of a microcomputer.

If it does not detect a CLK rising edge within t_{WD} , then V_{RO} pin outputs "L" level.

V_{RO} keeps "L", for the period which is set by the WDT Reset Time t_{WR} .

(4) Standby state of CLK rising edge detection.

CLK rising edge will be detectable after C_W is discharged by I_{CW} and V_{CW} is equal or less than the High-side Threshold Voltage V_{TCWH} (typ. 1.0V).

(5) When detect a CLK rising edge

When detects a CLK rising edge, C_W is switched from discharge cycle by I_{CW} to charge cycle by I_{CWL} (typ. 6 μ A) and V_{CW} rises. Then, V_{CW} reaches to V_{TCWH} , C_W is switched to discharge cycle and returns to state of the "(4) Standby state of CLK rising edge detection".

(6) When don't detect CLK rising edge

When V_{CW} reaches to the Low-side threshold Voltage V_{TCWL} (typ. 0.2V) without detecting CLK rising edge while C_W discharge cycle, V_{RO} is switched from "H" to "L" and C_W is switched to charge cycle.

The WDT Monitor Time t_{WD} is the period wherein V_{CW} falls from V_{TCWH} to V_{TCWL} without detecting CLK rising edge.

(7) Start of WDT Reset Time

V_{RO} is kept "L" while C_W is charged by I_{CWL} till V_{CW} reaches V_{TCWH} . When V_{CW} beyond V_{TCWH} , V_{RO} is switched from "L" to "H". Then returns to the watchdog timer monitor period as start to discharge capacitor C_W by I_{CW} .

The period which keeps V_{RO} ="L" is taken as WDT Reset Time t_{WR} .

- Detection of Output Voltage drop

(8) When it becomes $V_{OUT} < V_{DET}$.

When V_{OUT} becomes less than V_{DET} while t_{WD} or t_{WR} , V_{RO} is switched to "L" and V_{CW} is 0V due to C_W is rapidly discharged. Then operation returns to the "(1) Initialized state".

- Disable to WDT monitor function

(9) When Watchdog Timer Disenable pin \overline{WDEN} ="H".

The NJW4113 disables the WDT function by setting \overline{WDEN} ="H".

At this time, V_{CW} is fixed at 2V after C_W is charged to the IC's internal power supply (V_{REG} =2V). And if state of $V_{OUT} > V_{DET}$, V_{RO} keeps "H".

When setting \overline{WDEN} ="L" or "Open", C_W is discharged. After V_{CW} becomes less than V_{TCWH} , then WDT function is restarted.

If set \overline{WDEN} ="H" during the period of t_{WR} , WDT function stops after the t_{WR} period passes.

- At the time of an Input Voltage V_{IN} drops

(10) When the output voltage V_{OUT} drops to 0V.

V_{RO} keeps "L" till the output voltage V_{OUT} becomes around 0.8V.

■ SETTING METHOD OF PARTS

- C_W for the Watchdog timer reset time t_{WR} , the Watchdog timer monitor time t_{WD} and the RESET Output Delay Hold time t_{PR}

It is able to set t_{WR} , t_{PR} and t_{WD} by a capacitance of C_W .

Show a method to set the C_W from each condition as follows.

It applies any one of formula <1>, <4> or <7> for calculation of a C_W .

On the other hands, apply any one of formula <3>, <6> or <9> to calculate time from a C_W .

▪ When set C_W from the “Output Delay Hold time t_{PR} ”

The Output Delay Hold time t_{PR} is the period during V_{CW} changes from 0V to V_{TCWD} by the charge current I_{CWD} .

Therefore, a formula to calculate a value of capacitor C_W from t_{PR} is as follows:

$$C_W = \frac{I_{CWD}}{V_{TCWD}} \cdot t_{PR} \quad \dots \dots \dots <1>$$

It is able to calculate C_W simply, because parameter of I_{CWD} is $6\mu\text{A}(\text{typ.})$ and V_{TCWD} is $1.0\text{V}(\text{typ.})$.

$$C_W = \frac{6 \times 10^{-6}}{1.0} \cdot t_{PR} \quad *t_{PR}[\text{s}]$$

$$= (6 \times 10^{-6}) \cdot t_{PR} \quad [\text{F}] \quad \dots \dots \dots <2>$$

Also, the formula to calculate t_{PR} from C_W is as follows.

$$t_{PR} = \frac{C_W}{I_{CWD}} \cdot V_{TCWD} \quad * C_W[\text{F}]$$

$$= \frac{C_W}{6 \times 10^{-6}} \quad [\text{s}] \quad \dots \dots \dots <3>$$

▪ In case of set C_W from the “Watchdog timer monitor time t_{WD} ”

The WDT Monitor Time t_{WD} is the time until V_{CW} equal to V_{TCWL} by discharged I_{CW} after V_{CW} has reached V_{TCWD} or V_{TCWH} . Therefore, a formula to calculate a value of C_W from t_{WD} is as follows.

$$C_W = \frac{I_{CW}}{V_{TCWH} - V_{TCWL}} \cdot t_{WD} \quad \bullet \bullet \bullet \bullet \bullet \quad <4>$$

* use parameter of V_{TCWH} here because of $V_{TCWD}=V_{TCWH}$

It is able to calculate C_W simply, because parameter of “ I_{CWD} ” is $6\mu A$ (typ.), “ V_{TCWH} ” and “ V_{TCWL} ” is 1.0V (typ.).

$$C_W = \frac{2 \times 10^{-6}}{1.0 - 0.2} \cdot t_{WD}$$

$$= (2.5 \times 10^{-6}) \cdot t_{WD} \quad [F] \quad \bullet \bullet \bullet \bullet \bullet \quad <5> \quad *t_{WD}(s)$$

Also, the formula to calculate t_{WD} from C_W is as follows.

$$t_{WD} = \frac{C_W}{I_{CW}} \cdot (V_{TCWH} - V_{TCWL})$$

$$= (0.4 \times 10^6) \cdot C_W \quad [s] \quad \bullet \bullet \bullet \bullet \bullet \quad <6> \quad *C_W(F)$$

▪ in case of set C_W from the “Watchdog timer reset time t_{WR} ”

The WDT Reset Time t_{WR} is the time until V_{CW} reaches V_{TCWH} charged by I_{CWL} after V_{CW} has reached V_{TCWL} . Therefore, a formula to calculate a value of C_W from t_{WR} is as follows.

$$C_W = \frac{I_{CWL}}{V_{TCWH} - V_{TCWL}} \cdot t_{WR} \quad \bullet \bullet \bullet \bullet \bullet \bullet \quad <7>$$

It is able to calculate C_W simply, because parameter of I_{CWL} is $6\mu A$ (TYP), “ V_{TCWH} ” and “ V_{TCWL} ” is 1.0V (TYP).

$$C_W = \frac{6 \times 10^{-6}}{1.0 - 0.2} \cdot t_{WR}$$

$$= (7.5 \times 10^{-6}) \cdot t_{WR} \quad [F] \quad \bullet \bullet \bullet \bullet \bullet \bullet \quad <8> \quad *t_{WR}(s)$$

Also, the formula to calculate t_{WR} from C_W is as follows.

$$t_{WR} = \frac{C_W}{I_{CWL}} \cdot (V_{TCWH} - V_{TCWL})$$

$$= (0.133 \times 10^6) \cdot C_W \quad [s] \quad \bullet \bullet \bullet \bullet \bullet \bullet \quad <9> \quad *C_W(F)$$

Then, the relation between C_W and t_{PR} , t_{WD} and t_{WR} are showed as Fig.2.

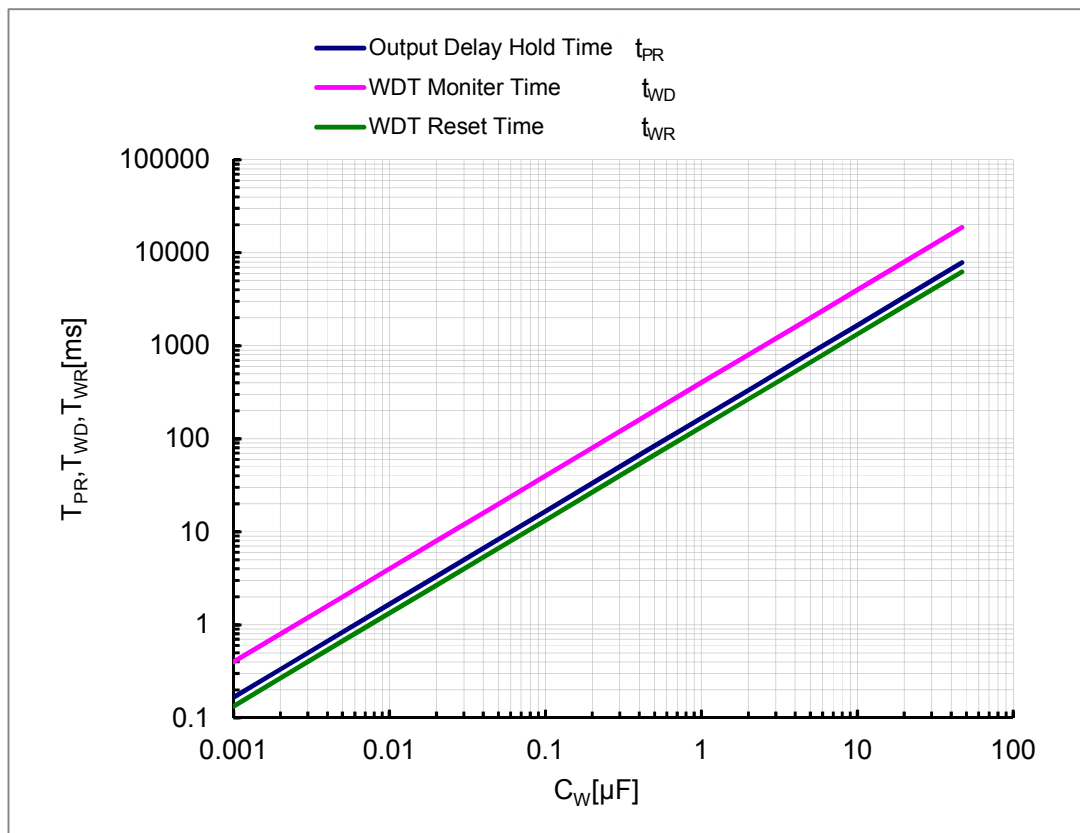


Fig.2 The relation of C_W and t_{PR} , t_{WD} , t_{WR}

- External resistor R_1, R_2 for detection voltage adjusting

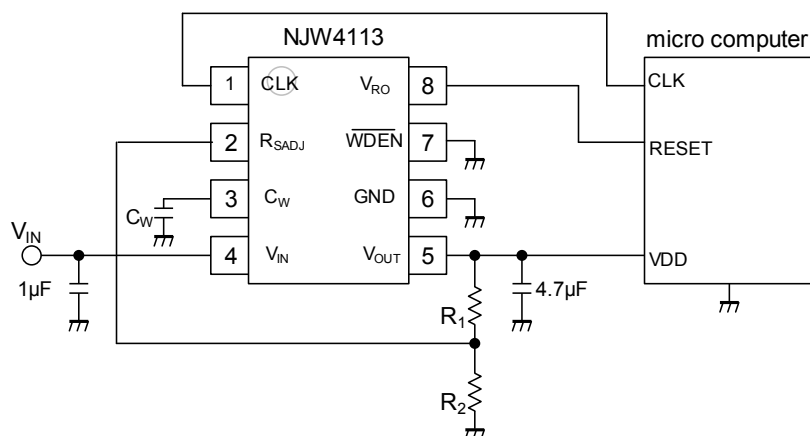


Fig.3. Typical application for detection voltage setting by external resistor

When optionally adjusts V_{DET} by external resistor as Fig.3, it is necessary to consider a value of resistor internal IC for detection voltage. Show a part including voltage detector circuit in the IC in Fig.4.

When connected resistor R_1 and R_2 , V_{DET} and V_{DETH} are calculated as follows.

[Detection Voltage V_{DET} (transistor M_1 : OFF)]

$$V_{DET} = \left\{ \frac{R_1}{R_2} \cdot \frac{1 + R_2 / (R_{D2} + R_{D3})}{1 + R_1 / R_{D1}} + 1 \right\} \cdot V_{REF} \quad \dots <10>$$

At the time of $R_1 \ll R_{D1}$, $R_2 \ll (R_{D2} + R_{D3})$, it can express approximate formula as follows.

$$V_{DET} = \left(\frac{R_1}{R_2} + 1 \right) \cdot V_{REF} \quad \dots <11>$$

[RESET release voltage V_{DETH} (transistor M_1 : ON)]

$$V_{DETH} = \left(\frac{R_1}{R_2} \cdot \frac{1 + R_2 / R_{D2}}{1 + R_1 / R_{D1}} + 1 \right) \cdot V_{REF} \quad \dots <12>$$

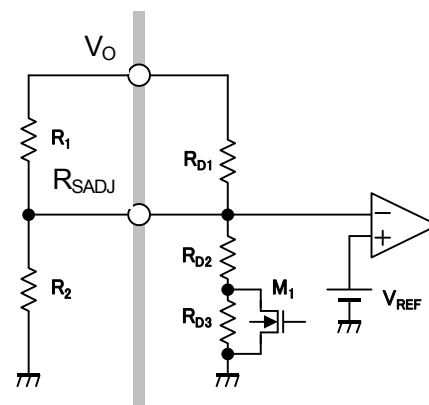


Fig.4. Part of voltage detector circuit

From calculation of V_{DET} and V_{DETH} , the Hysteresis Voltage V_{HYS} is as follows.

[Hysteresis Voltage V_{HYS}]

$$V_{HYS} = \frac{R_{D1} \cdot R_{D3}}{R_{D2} \cdot (R_{D2} + R_{D3}) \cdot (1 + R_{D1} / R_1)} \cdot V_{REF} \quad \dots <13>$$

The Resistors R_{D1} , R_{D2} and R_{D3} depend on a detection voltage rank. The values of resistors show the next page. The V_{REF} assumes 1.0V because it is equal to V_{RSADJ} prescribed by electrical characteristics.

According to formula <10>, it can express formula as follows when calculate value of R_2 from expected the detection voltage and R_1 .

$$R_2 = \frac{R_{D2} + R_{D3}}{\frac{R_{D2} + R_{D3}}{R_{D1}} \cdot (V_{DET} - 1) \cdot (1 + R_{D1} / R_1) - 1} \quad \dots <14>$$

NJW4113GM1-A46

The initial detection voltage of NJW4113GM1-A46 is set to 4.6V.

The value of resistors R_{D1} , R_{D2} and R_{D3} in the internal voltage detection circuit of IC are as Table.1.

It is expressed as follows when applying these parameters to formula <10>, <13> and <14>.

Assuming $V_{REF} = 1.0[V]$. The unit of resistors are “ Ω ”

[Detection Voltage V_{DET}]

$$V_{DET} = \frac{R_1}{R_2} \cdot \frac{1 + R_2 / (340 \times 10^3)}{1 + R_1 / (1224 \times 10^3)} + 1 \quad [V] \quad \dots <15>$$

[Hysteresis Voltage V_{HYS}]

$$V_{HYS} = \frac{0.109}{1 + (1224 \times 10^3) / R_1} \quad [V] \quad \dots <16>$$

[Calculation of resistor R_2]

$$R_2 = \frac{340 \times 10^3}{0.278 \cdot (V_{DET} - 1) \cdot \left(1 + \frac{1224 \times 10^3}{R_1}\right) - 1} \quad [\Omega] \quad \dots <17>$$

Table.1. The internal resistor values of the IC
[NJW4113GM1-A46]

R_{D1}	1224 k Ω
R_{D2}	330 k Ω
R_{D3}	10 k Ω

NJW4113GM1-A41

The initial detection voltage of NJW4113GM1-A41 is set to 4.1V.

The value of resistors R_{D1} , R_{D2} and R_{D3} in internal voltage detector circuit of IC are as Table.2.

It is expressed as follows when applying these parameters to formula <10>, <13> and <14>.

Assuming $V_{REF} = 1.0[V]$. The unit of resistors are “ Ω ”

[Detection Voltage V_{DET}]

$$V_{DET} = \frac{R_1}{R_2} \cdot \frac{1 + R_2 / (340 \times 10^3)}{1 + R_1 / (1054 \times 10^3)} + 1 \quad [V] \quad \dots <18>$$

[Hysteresis Voltage V_{HYS}]

$$V_{HYS} = \frac{0.094}{1 + (1054 \times 10^3) / R_1} \quad [V] \quad \dots <19>$$

[Calculation of resistor R_2]

$$R_2 = \frac{340 \times 10^3}{0.323 \cdot (V_{DET} - 1) \cdot \left(1 + \frac{1054 \times 10^3}{R_1}\right) - 1} \quad [\Omega] \quad \dots <20>$$

Table.2. The internal resistor values of the IC
[NJW4113GM1-A41]

R_{D1}	1054 k Ω
R_{D2}	330 k Ω
R_{D3}	10 k Ω

■ Attention in the use

▪ The handling for the noise

There is some possibility of output a reset signal ($V_{RO}="L"$) due to an external noise from the R_{SADJ} pin and V_{RSADJ} becomes less than V_{REF} momentarily.

When a reset signal outputs by an external noise, please insert the capacitor C_S for filters between the R_{SADJ} pin and the ground. (refer. Fig.5.)

When insert capacitor C_S , t_{PR} becomes longer than a calculated result by C_W (refer. Fig.6.)

The output delay time t_{PR} when inserting the capacitor C_S is as follows.

It assumes the delay time t_{DPR} by the C_S ,

$$t_{DPR} = \tau \cdot \ln \left\{ 1 / \left(1 - \frac{V_{RSADJ}}{V_{OUT}} \cdot \frac{R_{D1} + R_{D2}}{R_{D2}} \right) \right\} \dots <21>$$

$$\tau = \frac{R_{D1} \cdot R_{D2}}{R_{D1} + R_{D2}} \cdot C_S \dots <22>$$

Therefore, it can calculate in the following formula when assuming the output delay time t_{PR0} without C_S .

$$t_{PR} = t_{DPR} + t_{PR0} \dots <23>$$

$$t_{PR0} = \frac{C_W}{I_{CWD}} \cdot V_{TCWD}$$

Please refer to Table.1 and Table.2 for the value of resistors R_{D1} and R_{D2} , because it depends on a detection voltage rank.

The V_{RSADJ} assumes 1.0V because it is equal to V_{REF} .

Formula of t_{DPR} is shown on the next page.

When use external resistors R_1 and R_2 for adjusting detection voltage, R_{D1} and R_{D2} should replace as follows.

$$R_{D1} \rightarrow \frac{R_{D1} \cdot R_1}{R_{D1} + R_1}, \quad R_{D2} \rightarrow \frac{R_{D2} \cdot R_2}{R_{D2} + R_2}$$

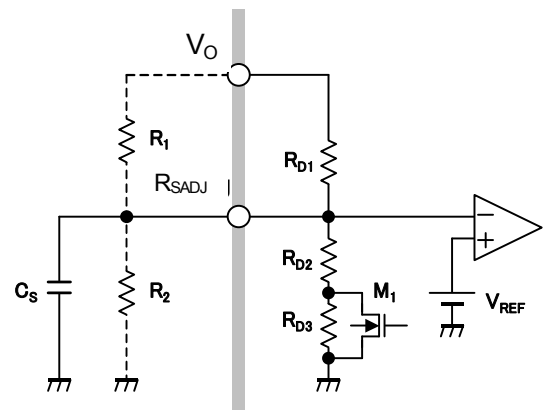


Fig.5. Handling for the noise

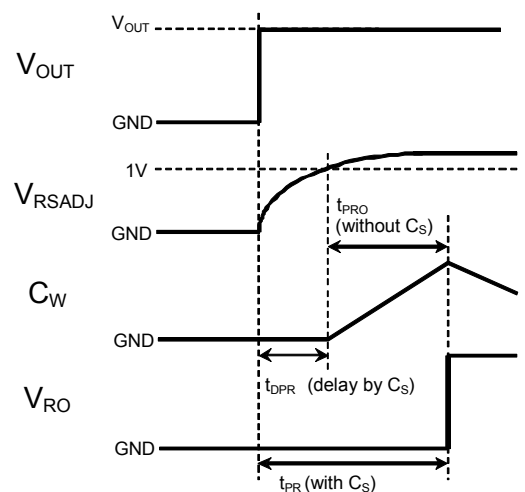


Fig.6. Each pin wave form when insert capacitor Cs

Formula of t_{DPR} in case of NJW4113GM1-A46

The t_{DPR} by the capacitor C_S can be calculated with formula <24> according to formulas <21> and <22>.

$$t_{DPR} = \frac{1224 \times 330}{1224 + 330} \cdot C_S \cdot \ln \left\{ \frac{1}{1 - \frac{1.0}{5.0} \cdot \frac{1224 + 330}{330}} \right\} \quad * V_{RSADJ} = 1.0[V], V_{OUT} = 5.0[V]$$

$$= 739.27 \times C_S \quad [s] \quad \bullet \bullet \bullet \bullet \quad <24> \quad * \text{Capacitor's } C_S \text{ unit is "F"}$$

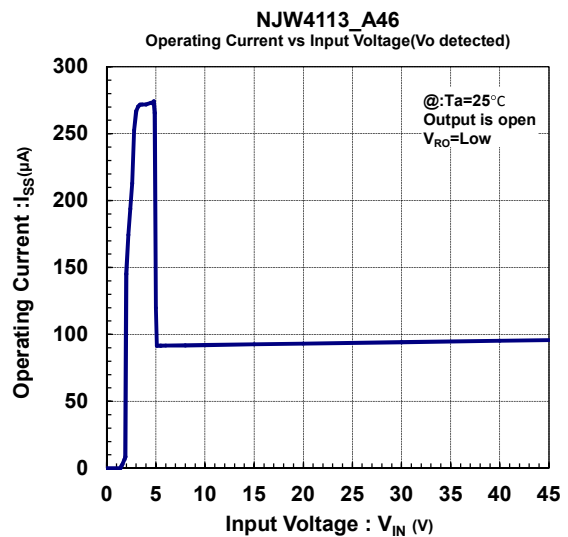
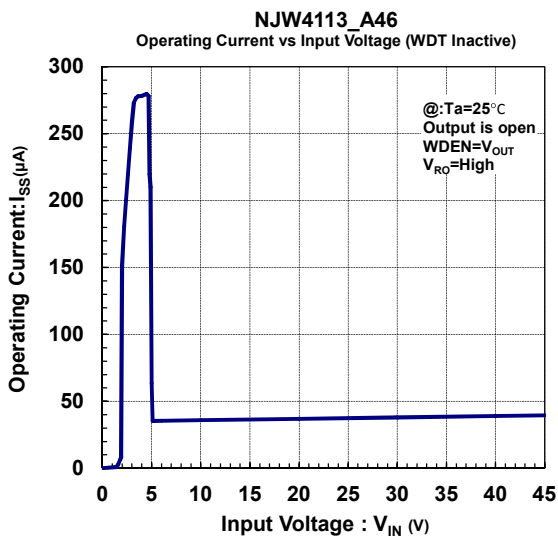
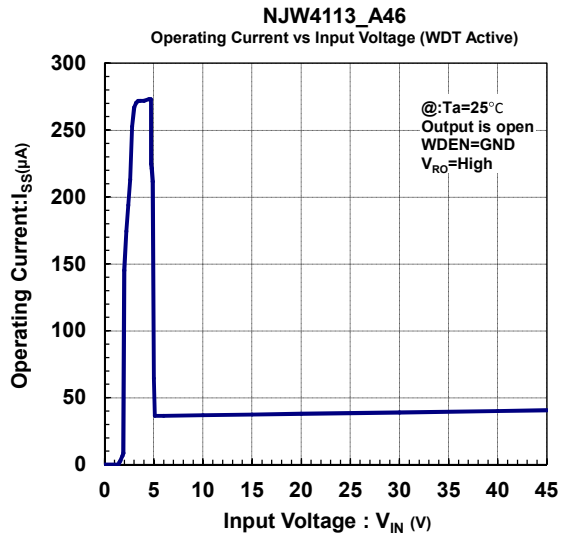
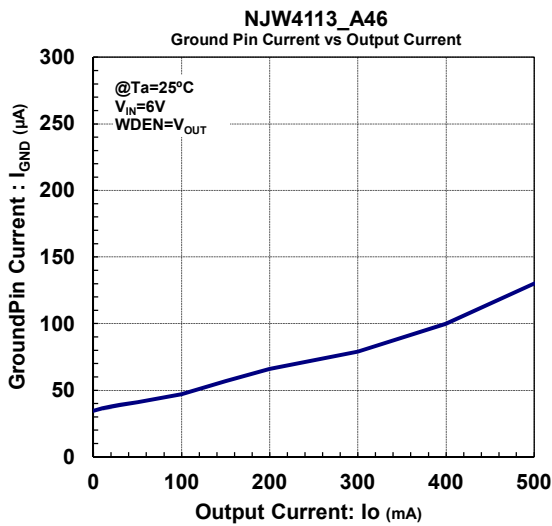
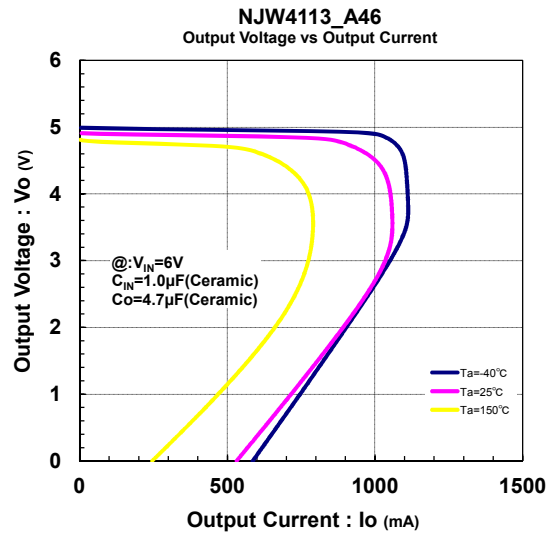
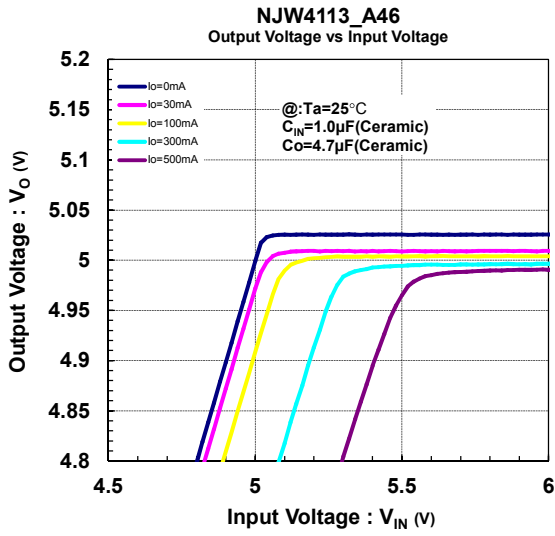
Formula of t_{DPR} in case of NJW4113GM1-A41

The t_{DPR} by the capacitor C_S can be calculated with formula <25> according to formulas <21> and <22>.

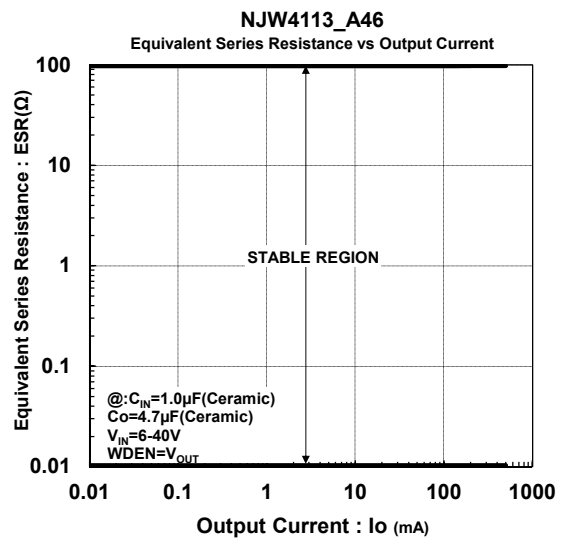
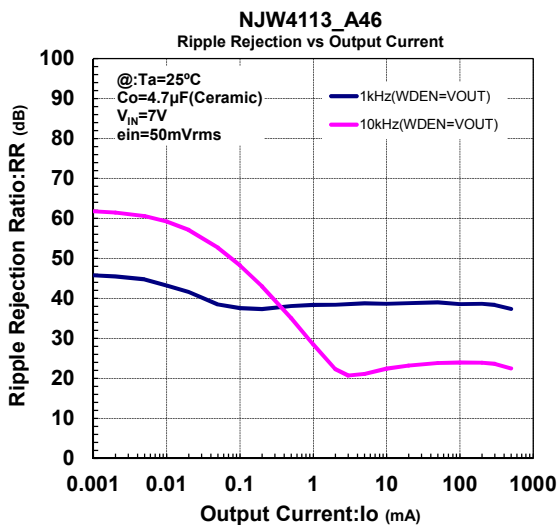
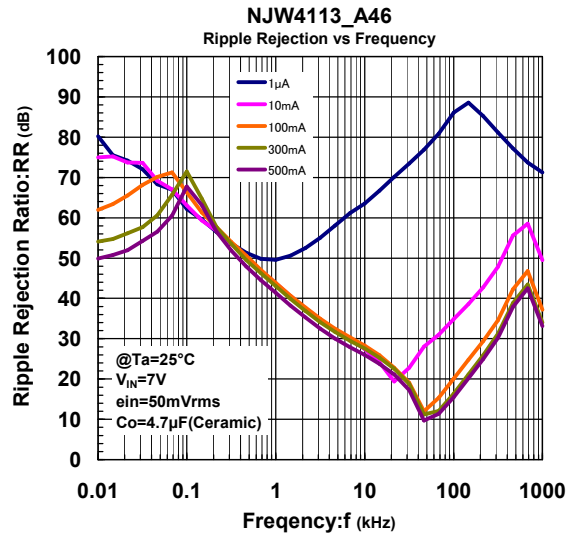
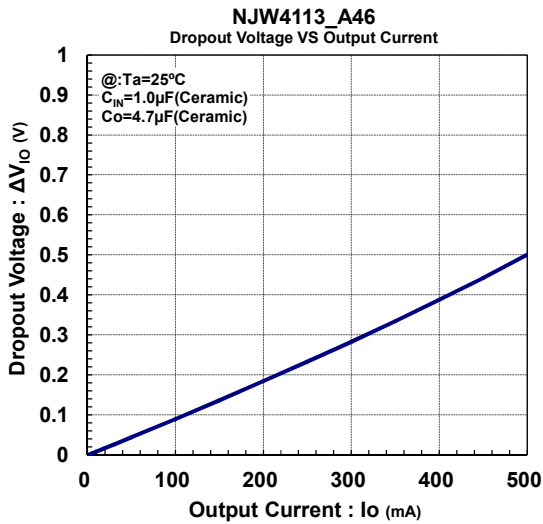
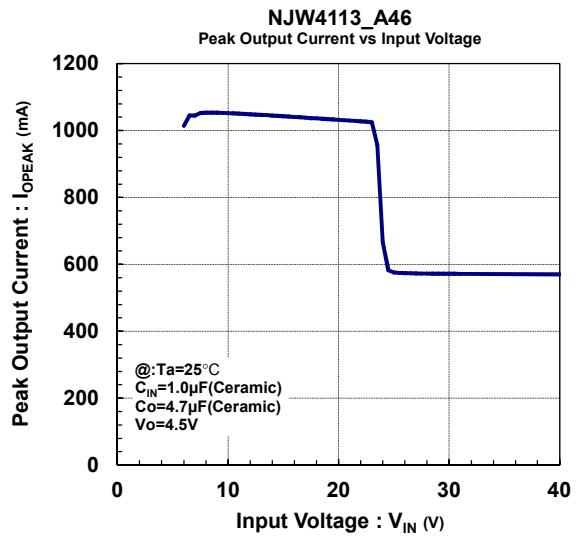
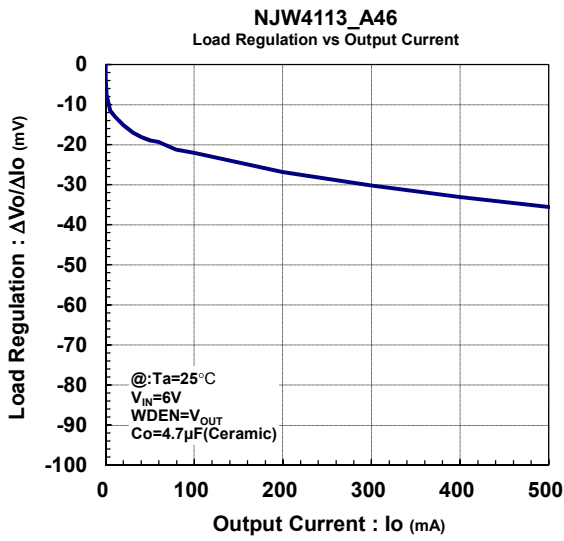
$$t_{DPR} = \frac{1054 \times 330}{1054 + 330} \cdot C_S \cdot \ln \left\{ \frac{1}{1 - \frac{1.0}{5.0} \cdot \frac{1054 + 330}{330}} \right\} \quad * V_{RSADJ} = 1.0[V], V_{OUT} = 5.0[V]$$

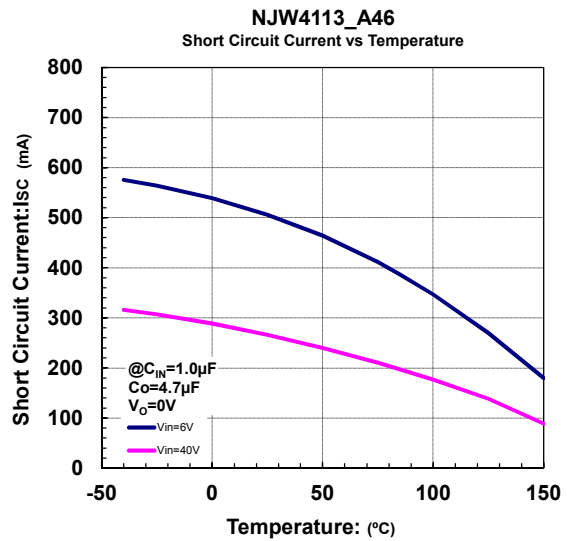
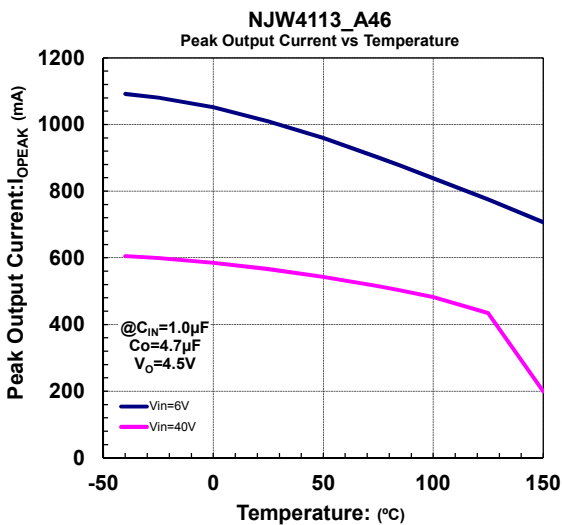
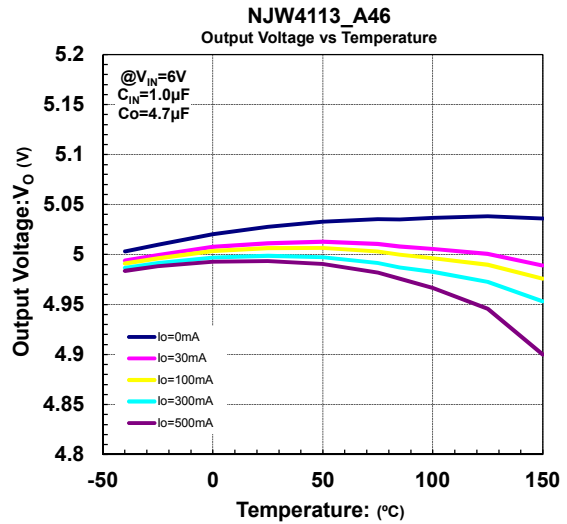
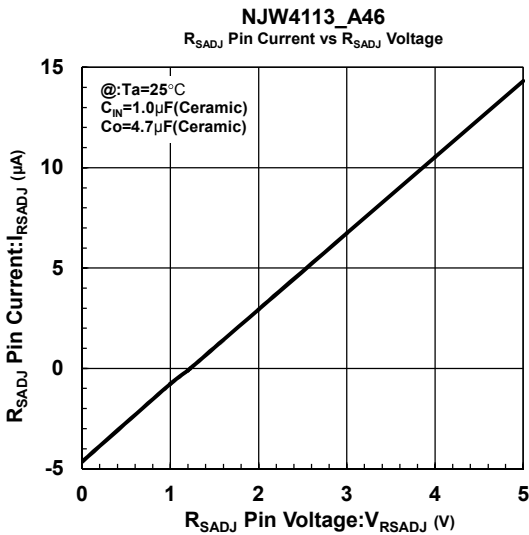
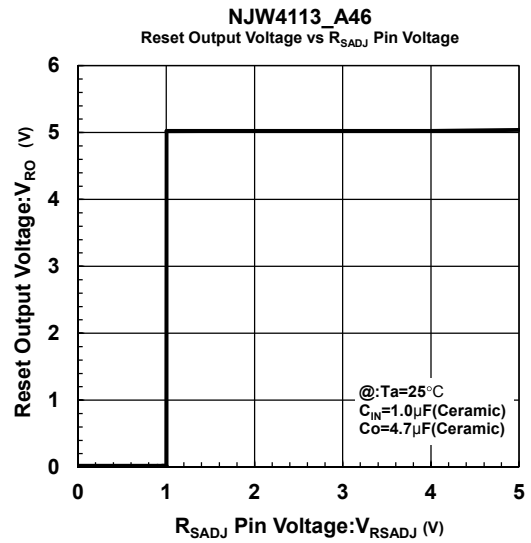
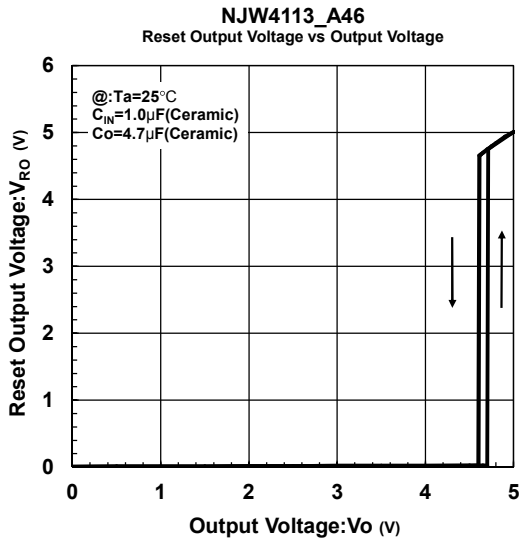
$$= 458.66 \times C_S \quad [s] \quad \bullet \bullet \bullet \bullet \quad <25> \quad * \text{Capacitor's } C_S \text{ unit is "F"}$$

TYPICAL CHARACTERISTICS

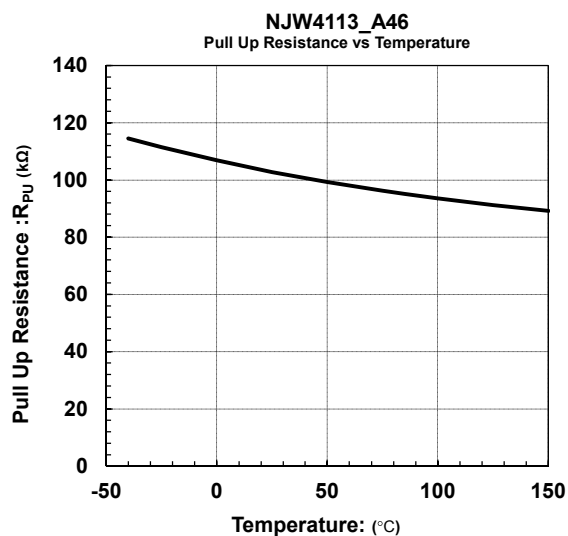
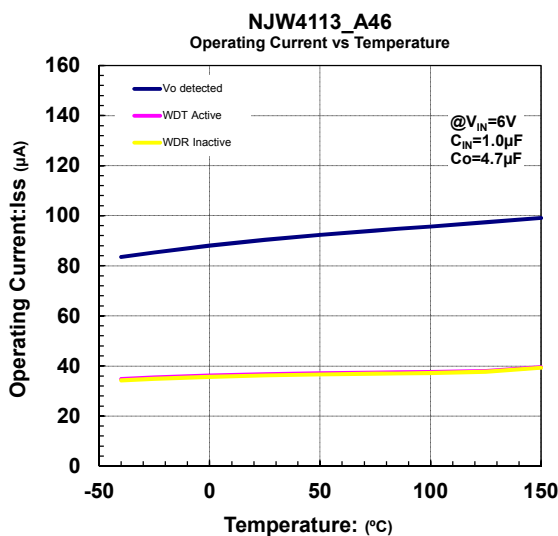
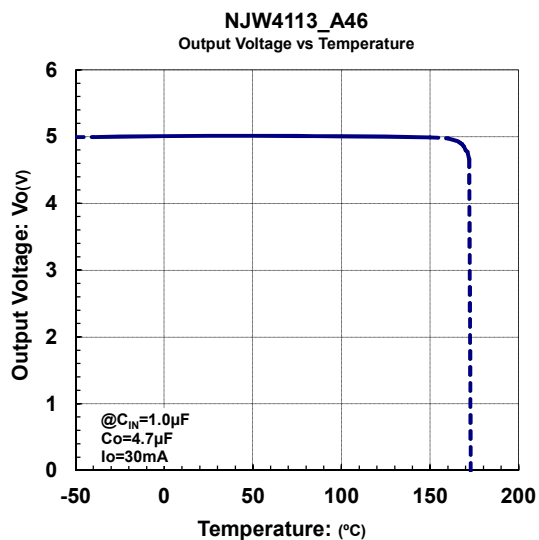
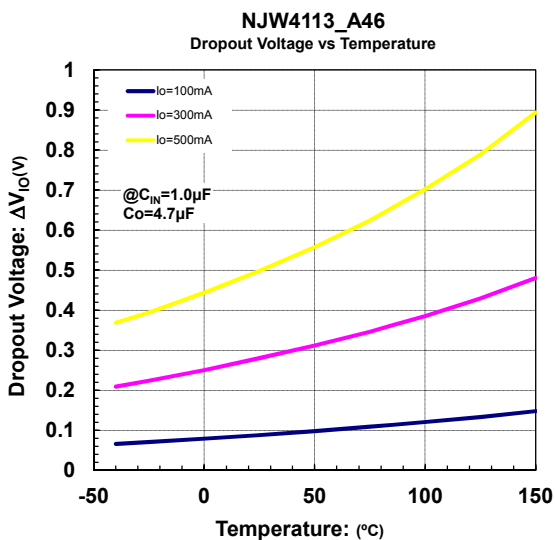
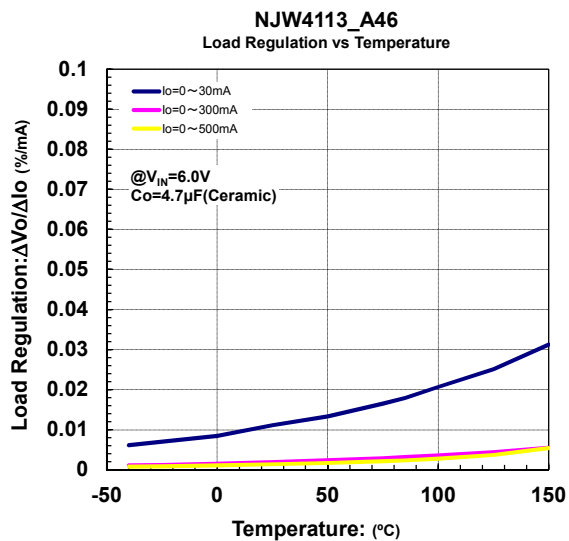
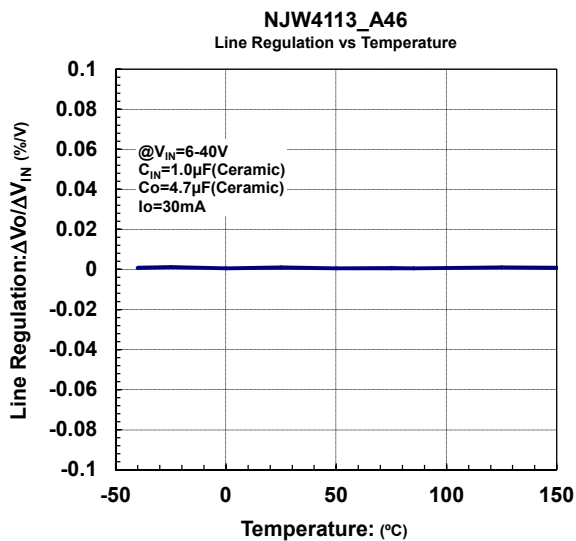


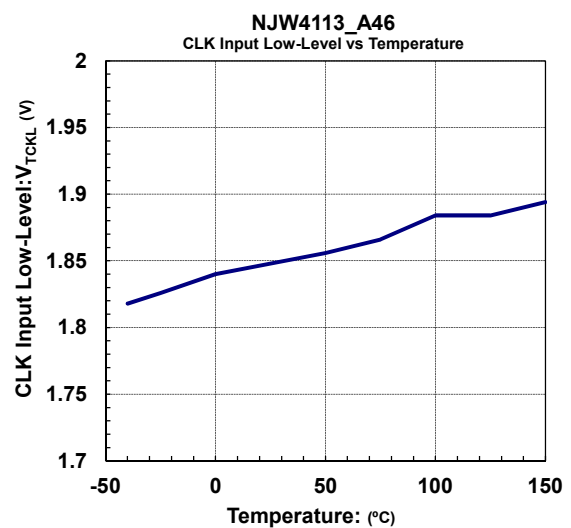
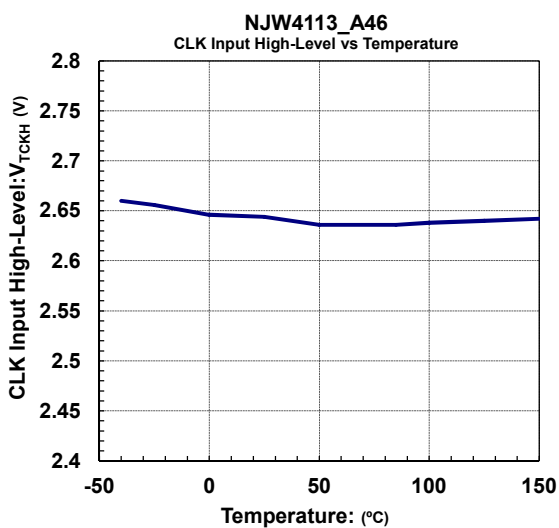
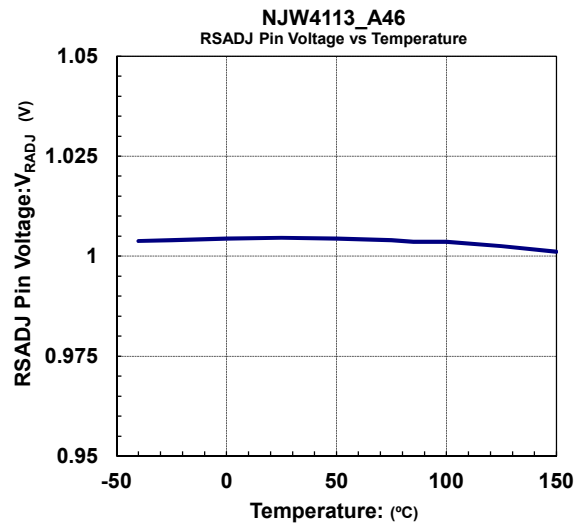
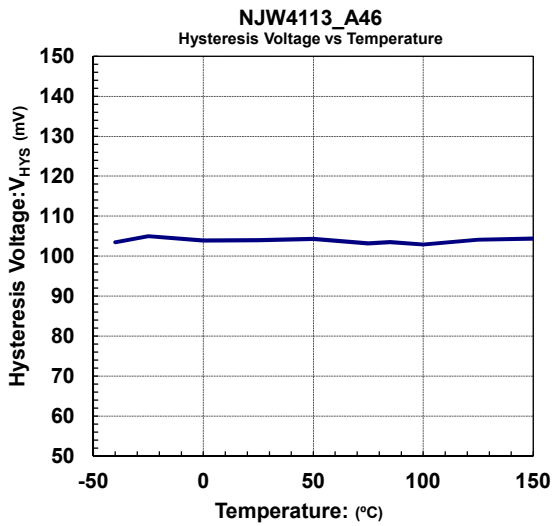
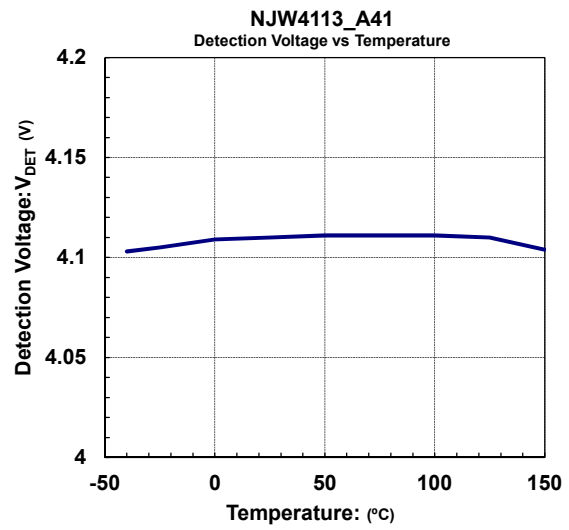
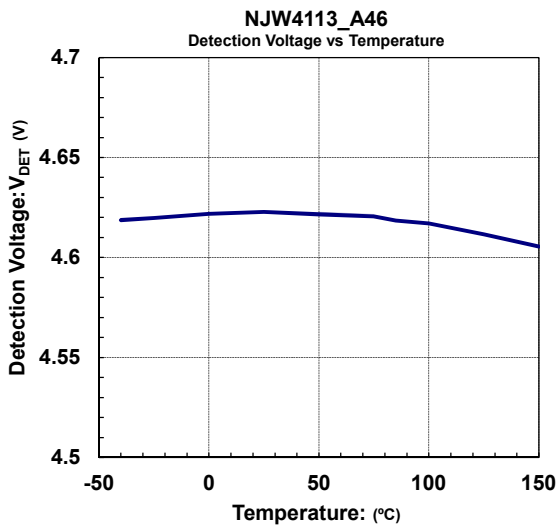
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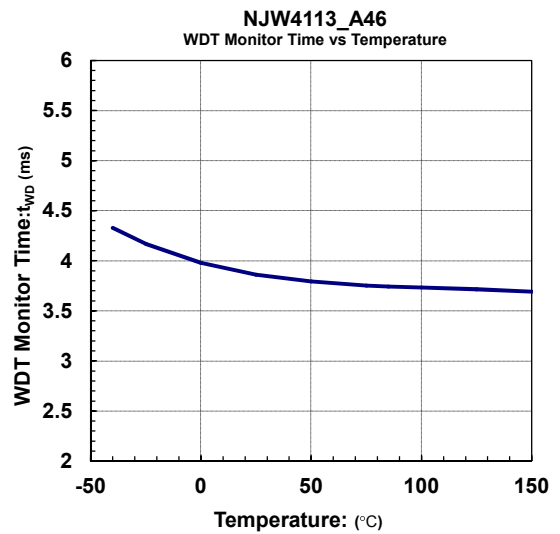
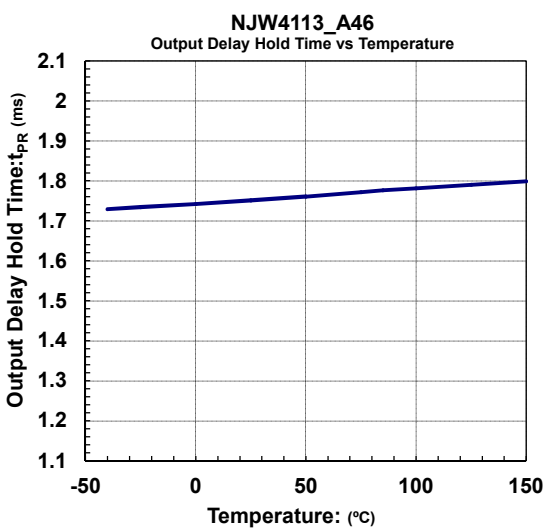
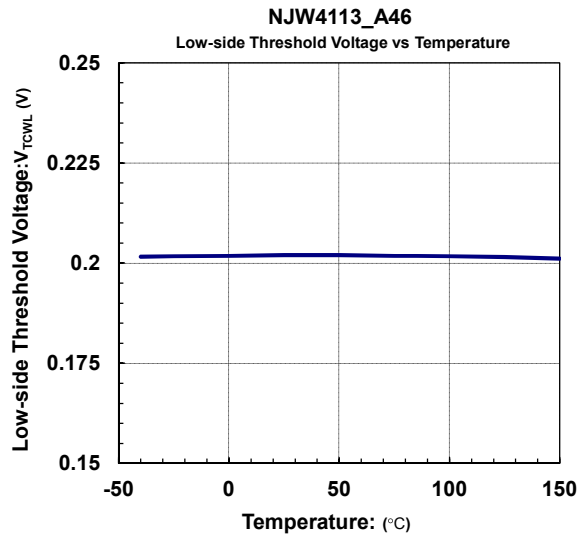
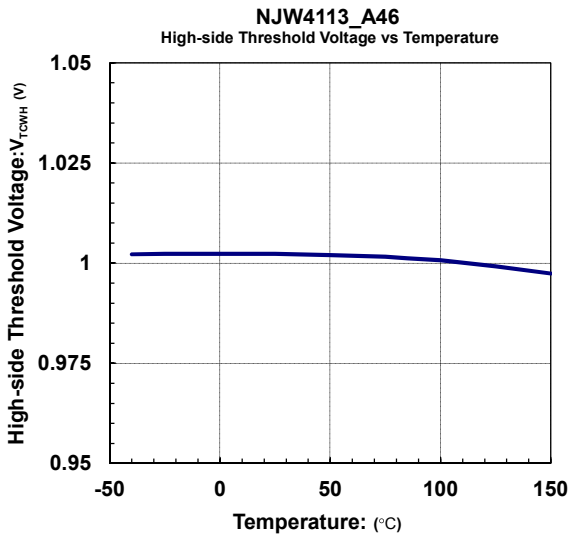
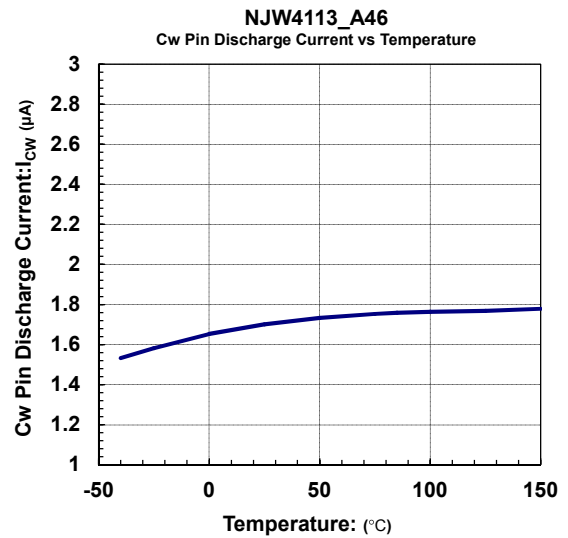
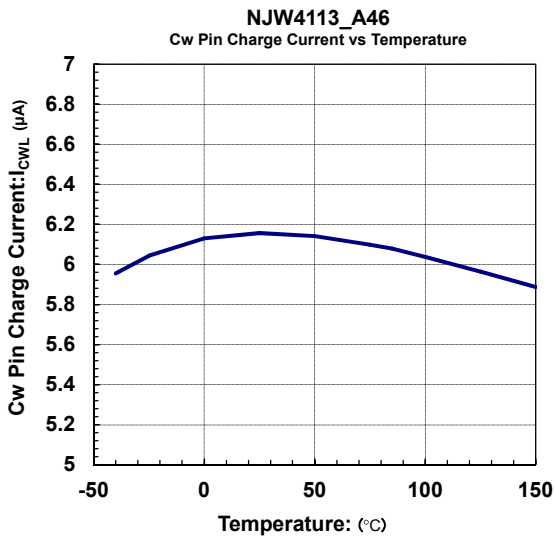


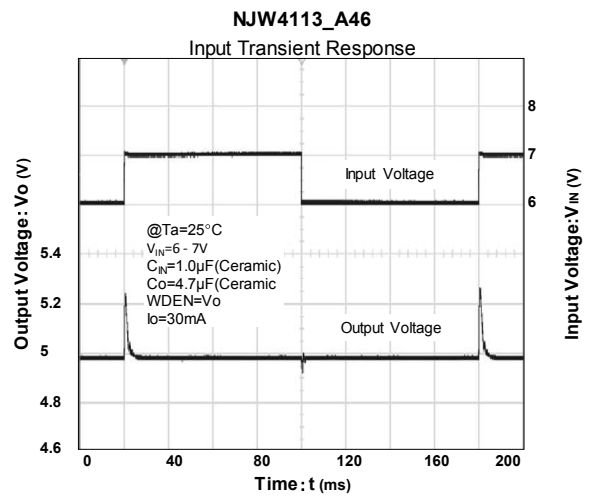
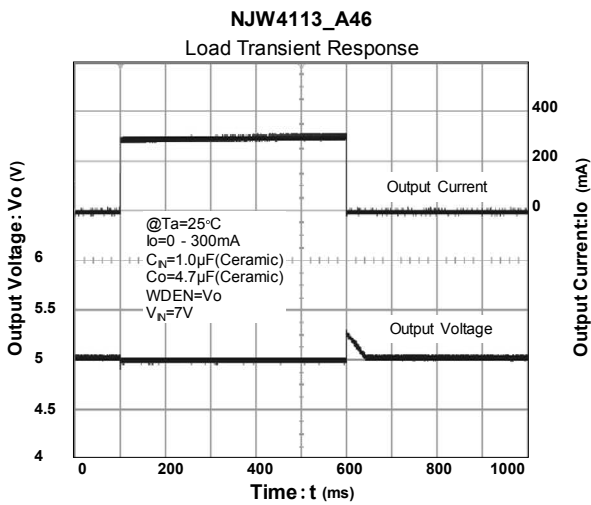
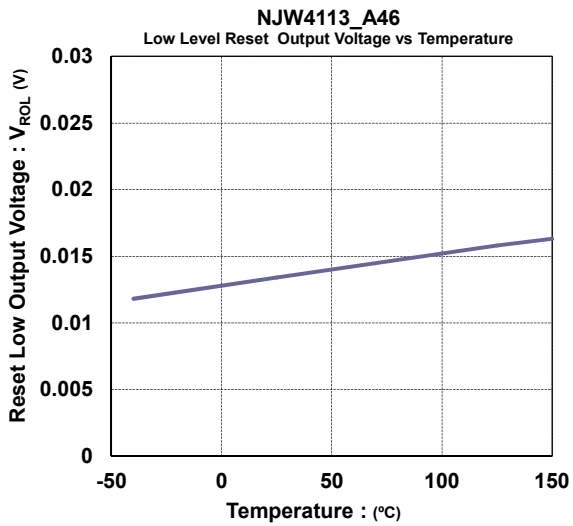
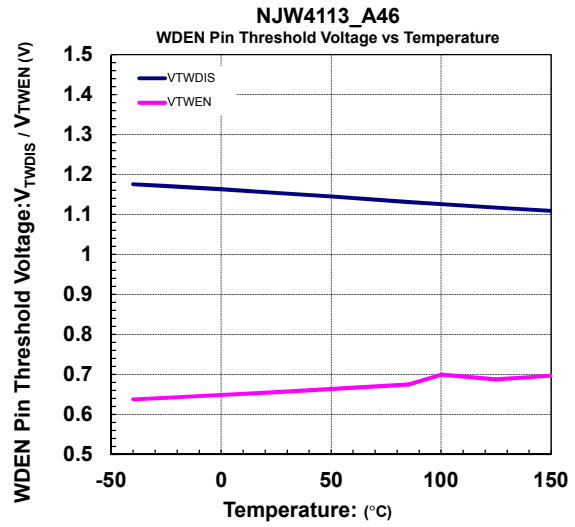
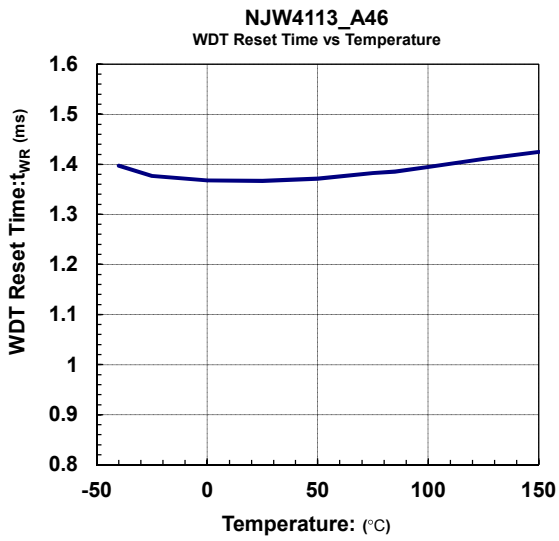
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NJW4113-T1





[CAUTION]

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