

High Voltage $I_o=1000\text{mA}$ Adjustable Low Dropout Regulator

■ GENERAL DESCRIPTION

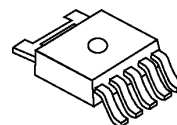
The NJW4188 is a high voltage and low current consumption low dropout regulator.

NJW4188 is an adjustable output voltage type, so it can provide the optimum selection for various applications.

NJW4188 is mounted to TO-252-5 package and corresponded to Low ESR capacitor (MLCC).

The wide input range and wide operate temperature make NJW4188 suitable for a, Car accessory, Industrial supplies demanded high reliability.

■ PACKAGE OUTLINE

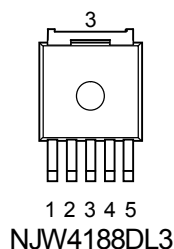


NJW4188DL3

■ FEATURES

- | | |
|--|----------------------------|
| ● Operating Voltage Range | 4.0V to 40V |
| ● Low Current Consumption | 55 μA typ. |
| ● Correspond to Low ESR capacitor (MLCC) | |
| ● Output Current | I_o (min.)=1000mA |
| ● Available Output Voltage Range | 2.0V to 15.0V |
| ● High Precision Reference Voltage | $V_{\text{ref}} \pm 1.0\%$ |
| ● ON/OFF Control | |
| ● Internal Thermal Overload Protection | |
| ● Internal Over Current Protection | |
| ● Package Outline | TO-252-5 |

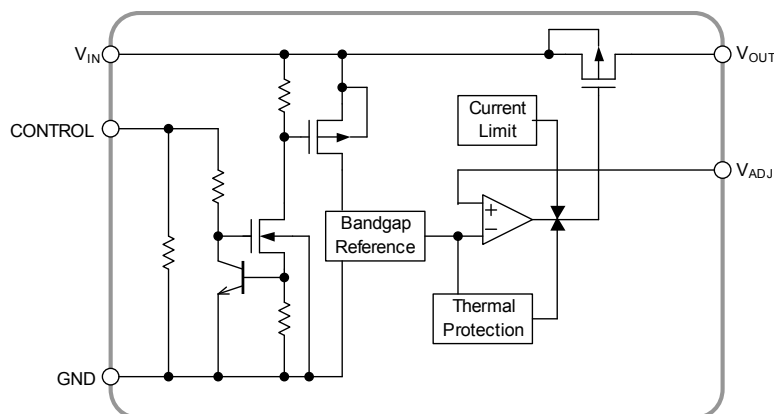
■ PIN CONFIGURATION



Pin Function

1. V_{IN}
2. CONTROL
3. GND
4. V_{ADJ}
5. V_{OUT}

■ BLOCK DIAGRAM



■ PRODUCTS CLASSIFICATION

Device Name	Spec	Spec Guarantee	Operating Temperature
NJW4188DL3	General Spec	25°C	-40°C ~+125°C
NJW4188DL3-T1	T1 Spec	-40°C ~+125°C	-40°C ~+125°C

This datasheet is applied to "NJW4188DL3".

Please refer to each datasheet for other version.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.3 to +45	V
Control Voltage	V_{CONT}	-0.3 to +45	V
Output Adjustable Voltage	V_{ADJ}	-0.3 to +6	V
Output Voltage	V_{OUT}	-0.3 ~ $V_{IN} \leq 17$	V
Power Dissipation	P_D	1190 (*1) 3125 (*2)	mW
Junction Temperature	T_J	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

(*2): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ OPERATING VOLTAGE RANGE

V_{IN} =4.0V to 40V

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_O \geq 3V$: $V_{IN} = V_O + 1V$, $C_{IN} = 1.0\mu F$, $C_O = 4.7\mu F$ ($3V \leq V_O < 3.4V$: $10\mu F$), $R_1 = 500k\Omega$, $T_a = 25^\circ C$)

$V_O < 3V$: $V_{IN} = 4.0V$, $C_{IN} = 1.0\mu F$, $C_O = 10\mu F$, $R_1 = 500k\Omega$, $T_a = 25^\circ C$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reference Voltage	V_{ref}		-1.0%	1.29	+1.0%	V
Quiescent Current	I_Q	$I_O = 0mA$, except I_{CONT}	-	55	90	μA
Quiescent Current at Control OFF	$I_{Q(OFF)}$	$V_{CONT} = 0V$	-	-	1	μA
Output Current	I_O	$V_O \times 0.9$	1000	-	-	mA
Line Regulation	$\Delta V_O / \Delta V_{IN}$	$V_{IN} = V_O + 1V$ to 40V, $I_O = 200mA$ ($V_O \geq 3V$) $V_{IN} = 4V$ to 40V, $I_O = 200mA$ ($V_O < 3V$)	-	-	0.03	% / V
Load Regulation	$\Delta V_O / \Delta I_O$	$I_O = 0$ to 1000mA	-	-	0.004	% / mA
Ripple Rejection	RR	$e_{in} = 200mV_{rms}$, $f = 1kHz$, $I_O = 10mA$, $V_O = 3.3V$	-	58	-	dB
Dropout Voltage	ΔV_{IO}	$I_O = 600mA$	-	0.27	0.42	V
Average Temperature Coefficient of Output Voltage	$\Delta V_O / \Delta T_a$	$T_a = 0^\circ C$ to $85^\circ C$, $I_O = 200mA$	-	± 50	-	ppm/°C
Control Current	I_{CONT}	$V_{CONT} = 1.6V$	-	1	3	μA
Control Voltage for ON-state	$V_{CONT(ON)}$		1.6	-	-	V
Control Voltage for OFF-state	$V_{CONT(OFF)}$		-	-	0.6	V
Available Output Voltage Range	V_O		2.0	-	15	V

* These parameters are tested by Pulse Measurement.

■ THERMAL CHARACTERISTICS

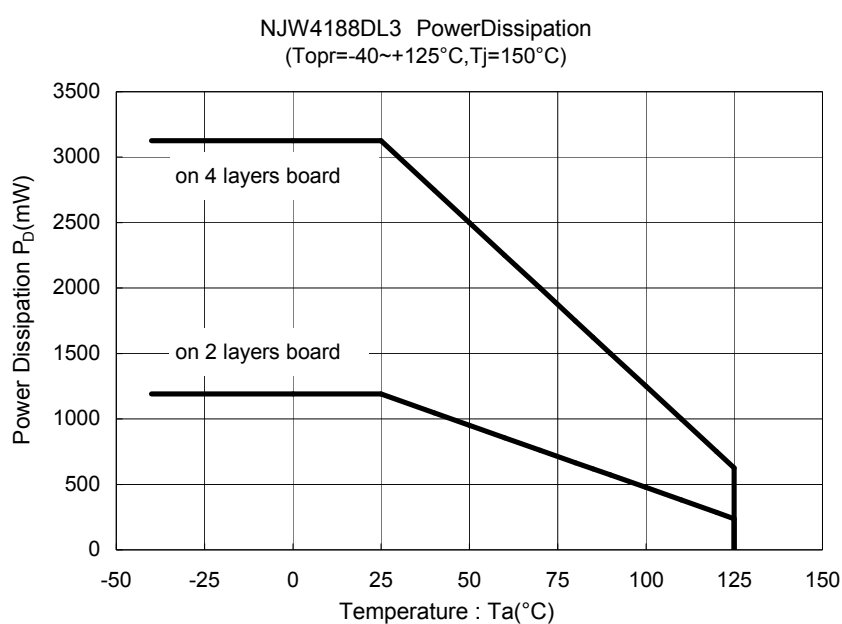
PARAMETER	SYMBOL	THERMAL RESISTANCE	UNIT
Junction-to-Ambient Temperature	θ_{ja}	105 (*3) 40 (*4)	$^{\circ}\text{C/W}$
Junction-to-Case surface	ψ_{jt}	17 (*3) 12 (*4)	$^{\circ}\text{C/W}$

(*3): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

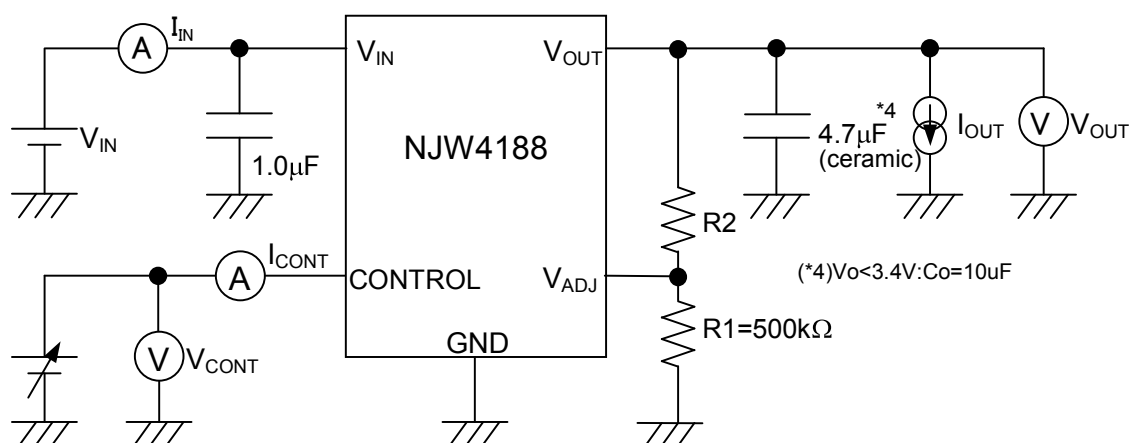
(*4): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

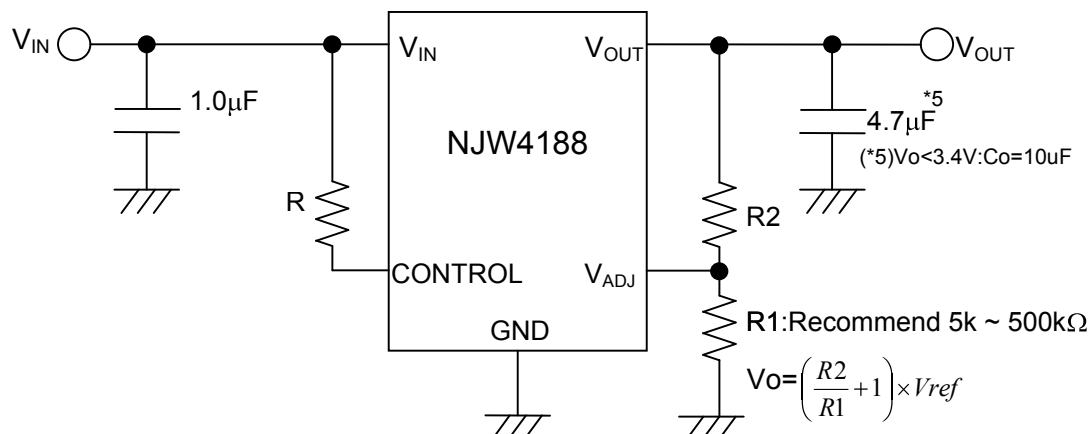


■ TEST CIRCUIT



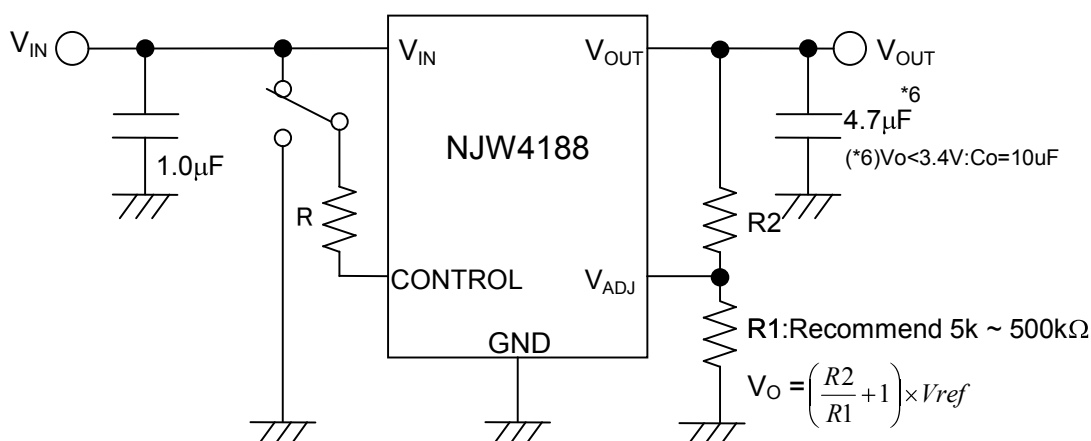
■ TYPICAL APPLICATION

① In the case where ON/OFF Control is not required



Connect control pin to V_{IN} pin

② In use of ON/OFF CONTROL



State of control pin:

- "H" → output is enabled.
- "L" or "open" → output is disabled.

*In the case of using a resistance "R" between V_{IN} and control.

If this resistor is inserted, it can reduce the control current when the control voltage is high.

The applied voltage to control pin should set to consider voltage drop through the resistor "R" and the minimum control voltage for ON-state.

The $V_{CONT(ON)}$ and I_{CONT} have temperature dependence as shown in the "Control Current vs. Temperature" and "Control Voltage vs. Temperature" characteristics. Therefore, the resistance "R" should be selected to consider the temperature characteristics.

*Feed back Resistance R1

The output voltage may rise against the set point by the leak current from the V_{OUT} pin at high temperature when this resistance is set too big.

Conversely, the current flowing to R1 grows big when R1 is set too small, and make the consumption current increase.

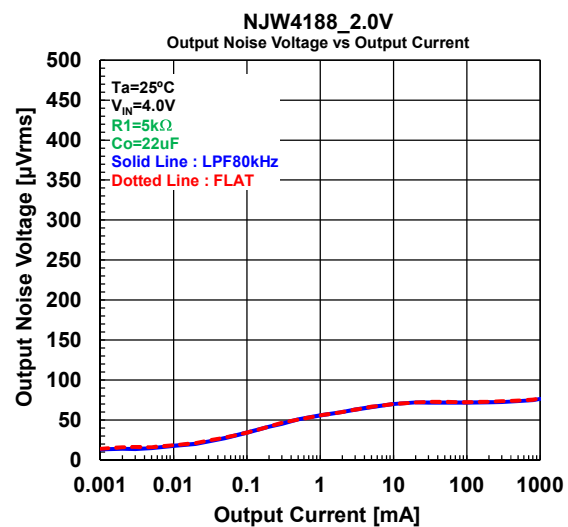
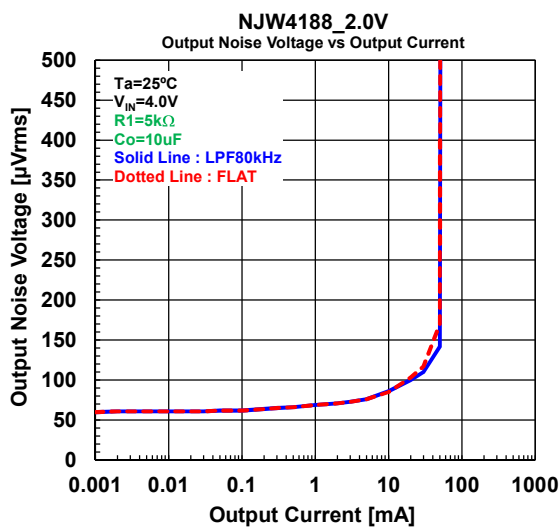
From the above, recommend $5k\Omega$ to $500k\Omega$ as a set range of R1.

But, the output noise voltage tends to increase with the resistance value of R1 become small.

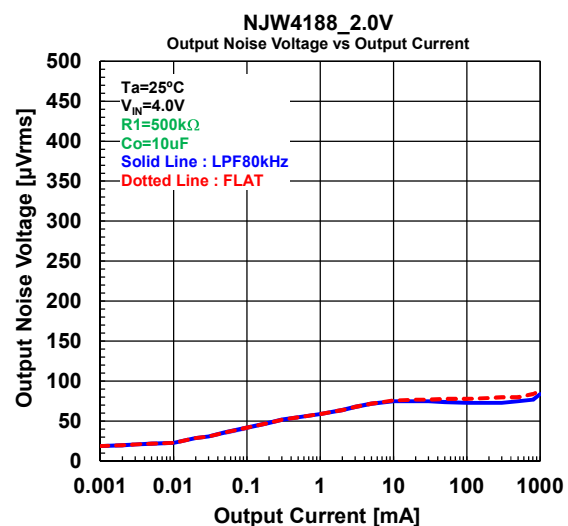
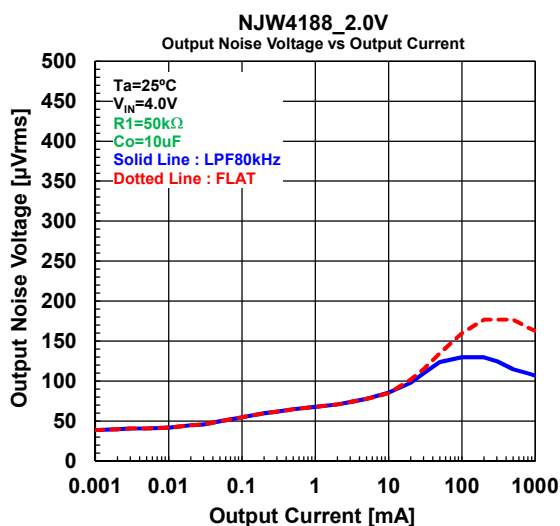
Especially, In the case of low output voltage setting such as $V_{OUT}=2.0V$, there is the possibility that the output voltage becomes unstable in the condition of recommended output capacitor ($C_o=10\mu F$) and too small feedback resistor (R1).

In that case, It can improve by making C_o or R1 bigger.

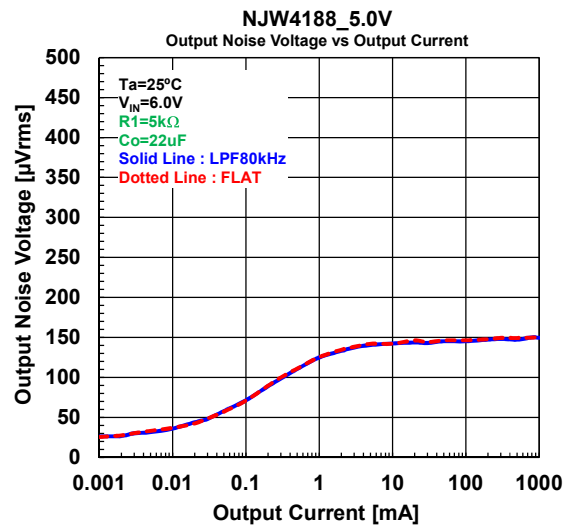
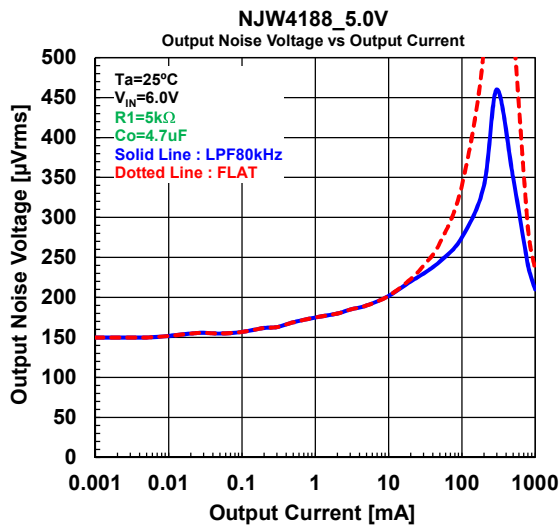
Show a characteristic example when changed a condition at the time of the $V_o=2.0V$ / $5.0V$ setting for reference.



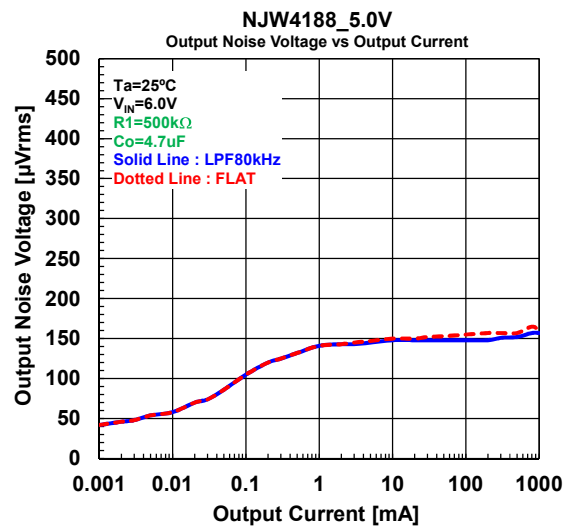
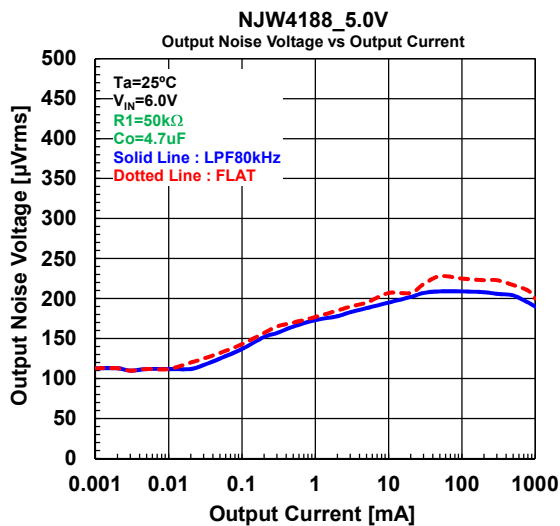
$V_{OUT}=2.0V$ Setting (R1=5kΩ, $C_o=10\mu F$ / $C_o=22\mu F$)



$V_{OUT}=2.0V$ Setting (R1=50kΩ / 500kΩ, $C_o=10\mu F$)



$V_{OUT}=5.0\text{V}$ Setting ($R1=5\text{k}\Omega$, $Co=4.7\mu\text{F}$ / $Co=22\mu\text{F}$)



$V_{OUT}=5.0\text{V}$ Setting ($R1=50\text{k}\Omega$ / $500\text{k}\Omega$, $Co=4.7\mu\text{F}$)

*Input Capacitor C_{IN}

The input capacitor C_{IN} is required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{IN} as shortest path as possible to avoid the problem

*Output Capacitor C_O

The output capacitor C_O will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess an output noise or an oscillation of the regulator due to lack of the phase compensation.

On the other hand, use of a larger C_O reduces an output noise and a ripple output, and also improves an output transient response when a load rapidly changes.

Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation

The recommended capacitance depends on the output voltage rank. Especially, a low voltage regulator requires larger C_O value.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O , recommend that have withstand voltage margin against an output voltage and superior temperature characteristics though this product is designed stability works with wide range ESR of capacitor including low ESR products.

*The notes of the evaluation when V_{OUT} pin is shorted to GND

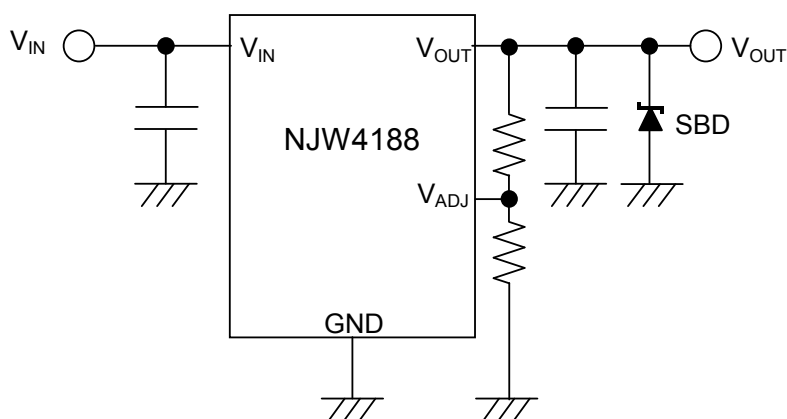
When evaluated short circuit test, the IC may break down because of regenerated energy by the parasitic inductance included in wiring pattern.

It phenomenon appears conspicuously when output voltage is high($V_{OUT}=8.0V$ or more)or connected to inductive load.

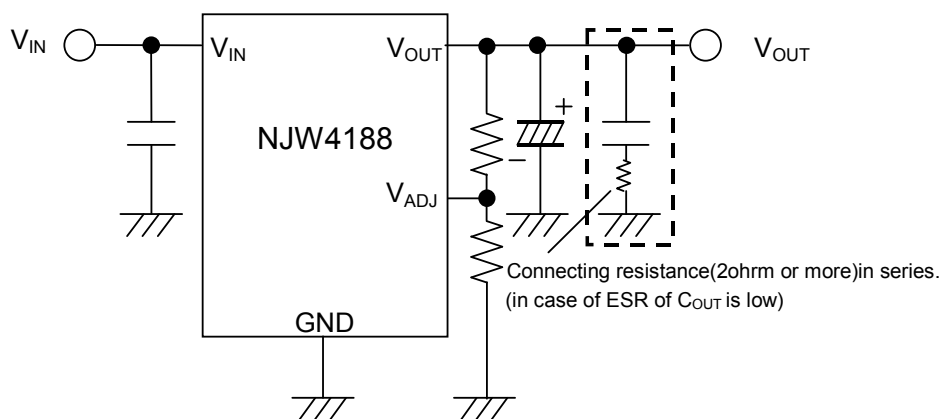
In case of short circuit in actual application, not likely to destruction of IC because of some of Resistance exist between load.

If happened above phenomenon by the short circuit test with the actual application, recommend connecting schottky barrier diode(SBD) between V_{OUT} pin and the GND or using output capacitor that have ESR more than 2ohm like a tantalum or aluminum electrolytic capacitor.(see below figure)

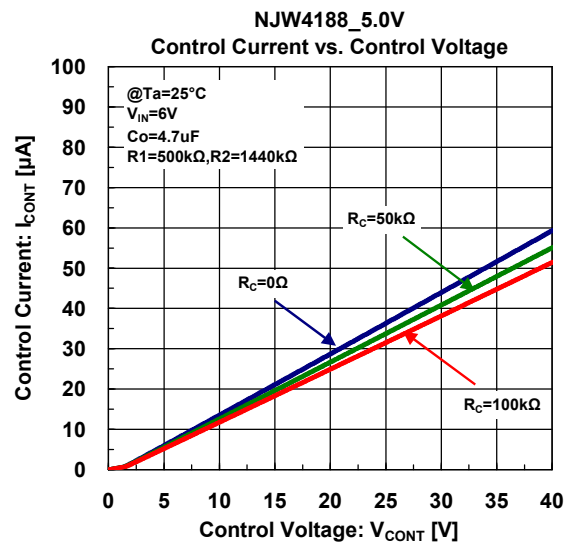
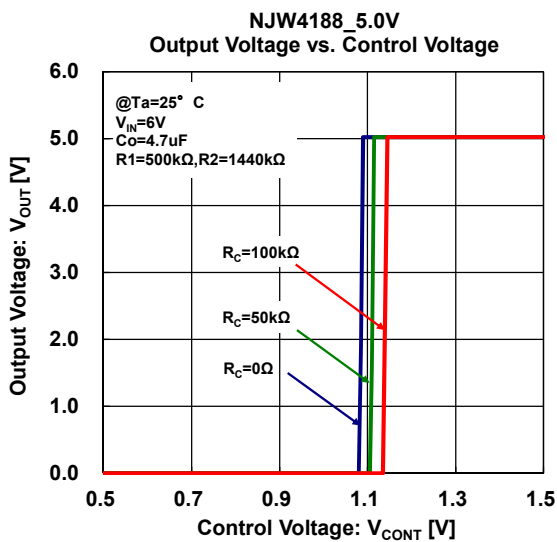
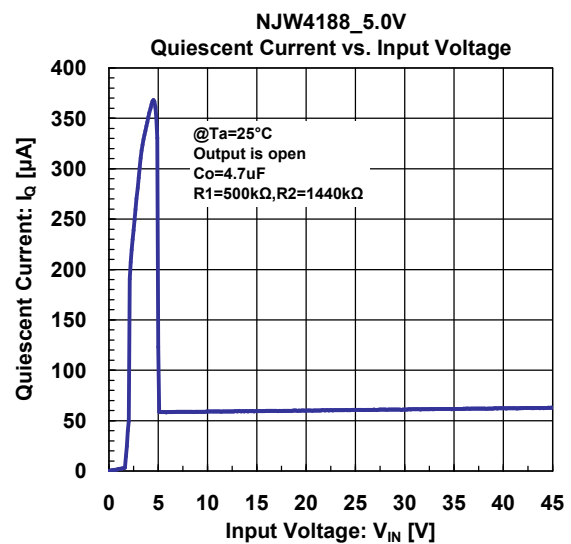
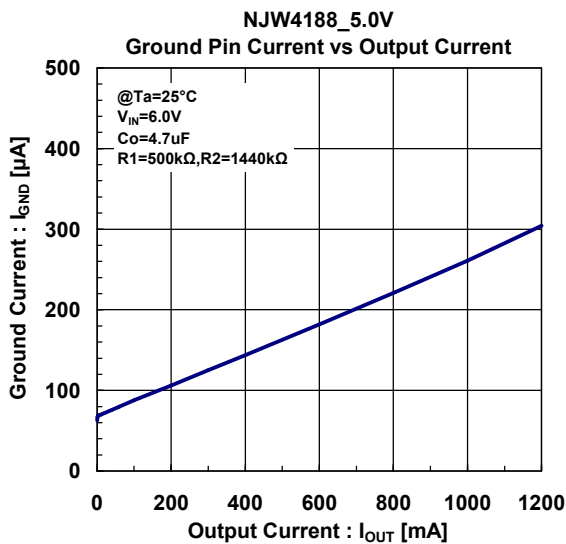
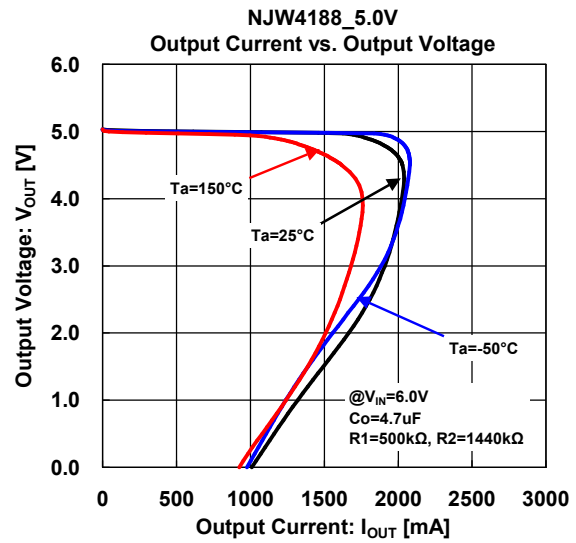
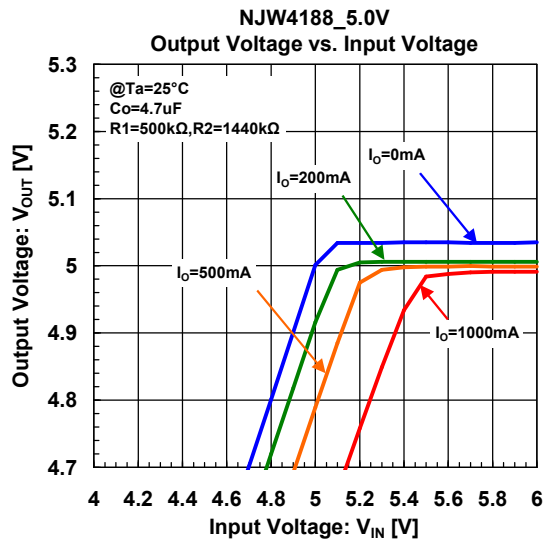
(a) In case of insert Schottky barrier diode between V_{OUT} pin- GND



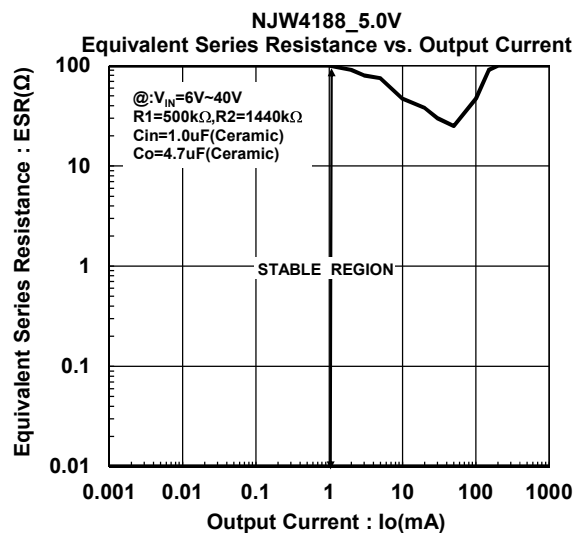
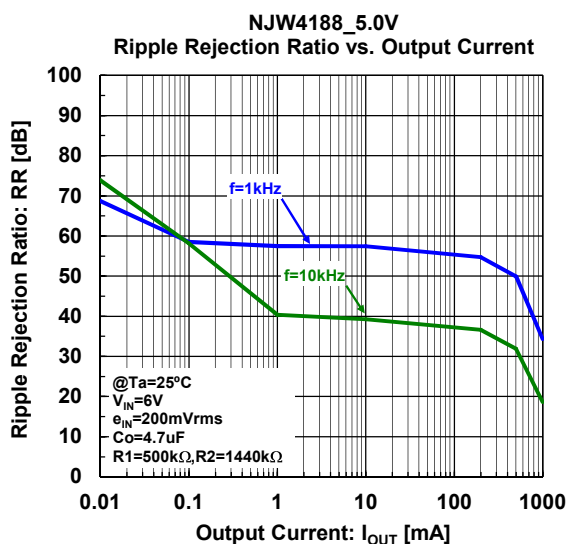
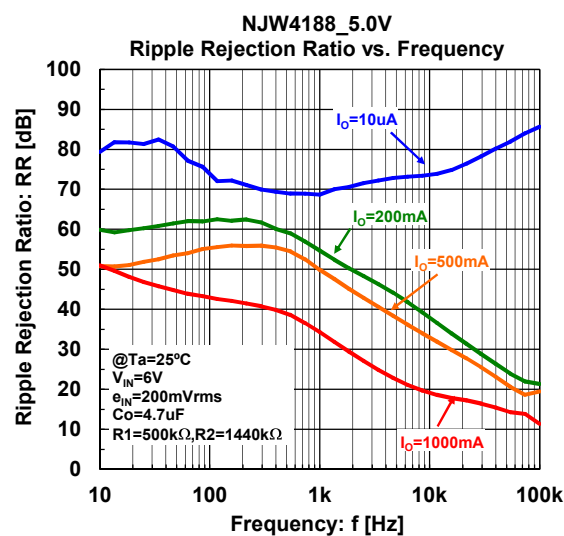
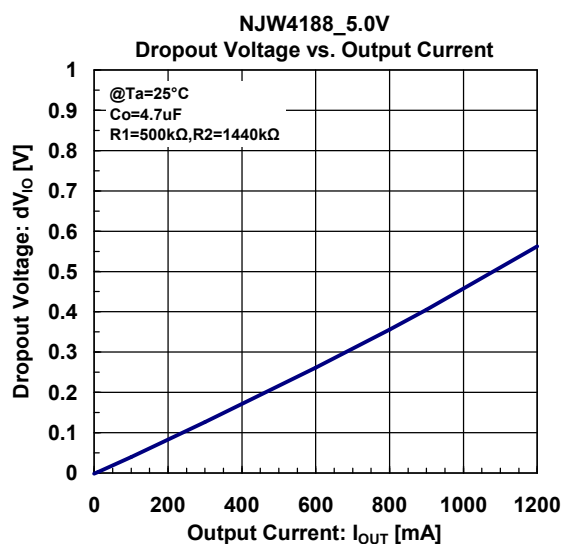
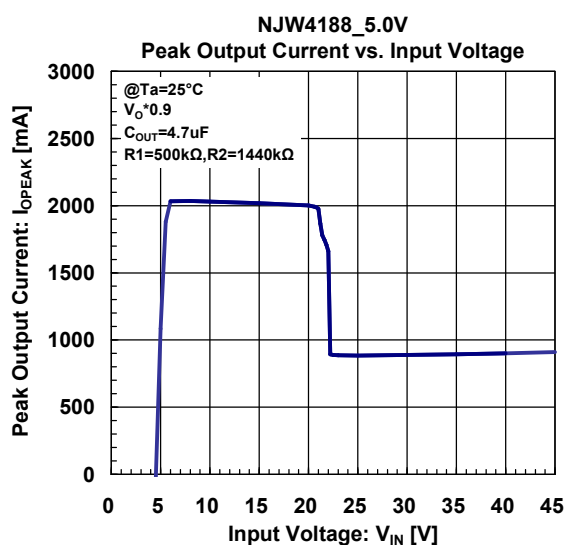
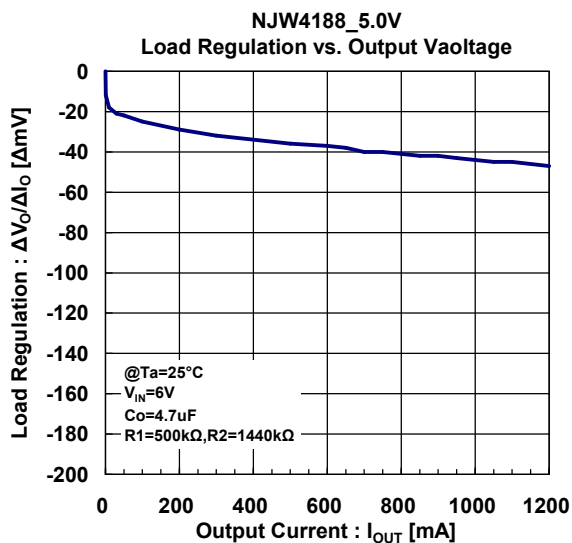
(b) In case of using the electrolysis capacitor or insert series resistance



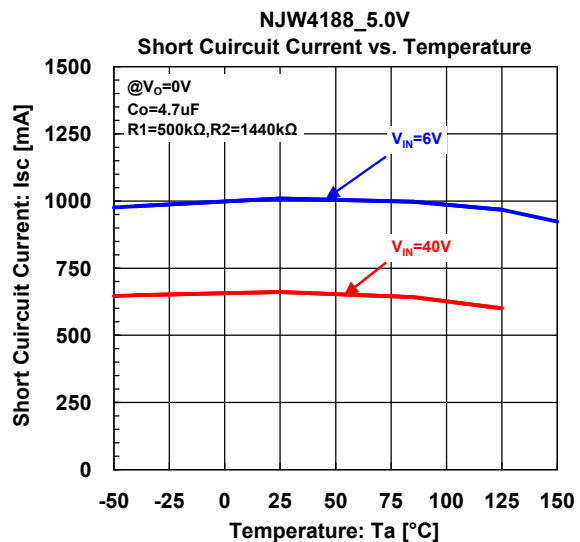
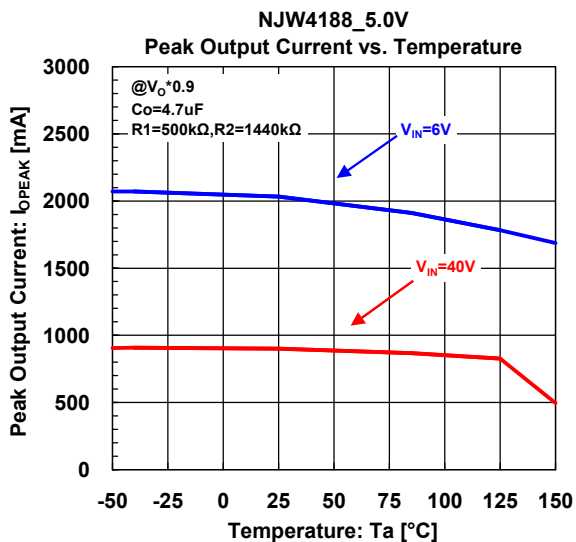
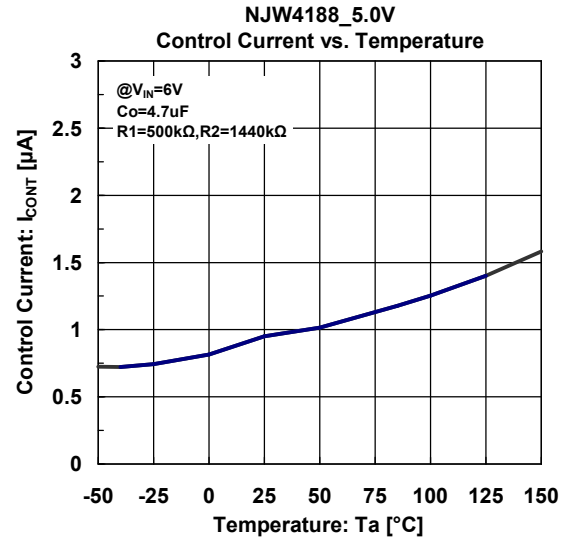
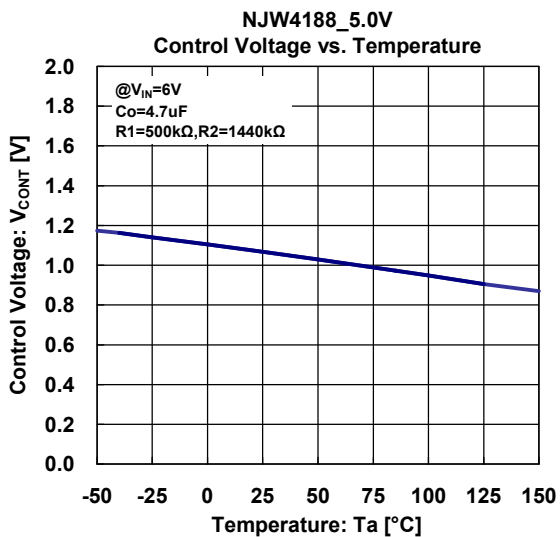
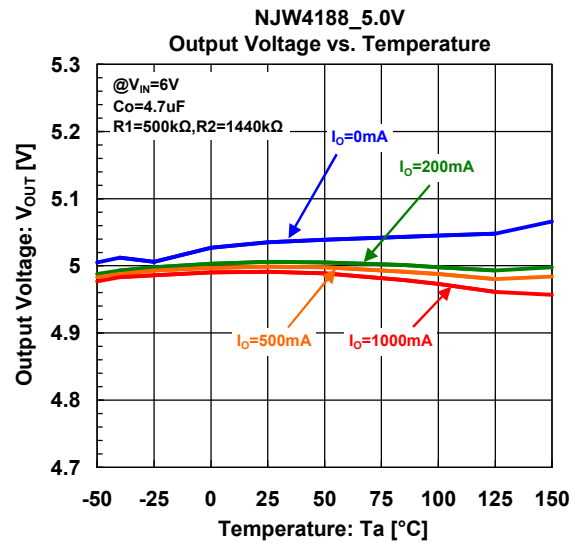
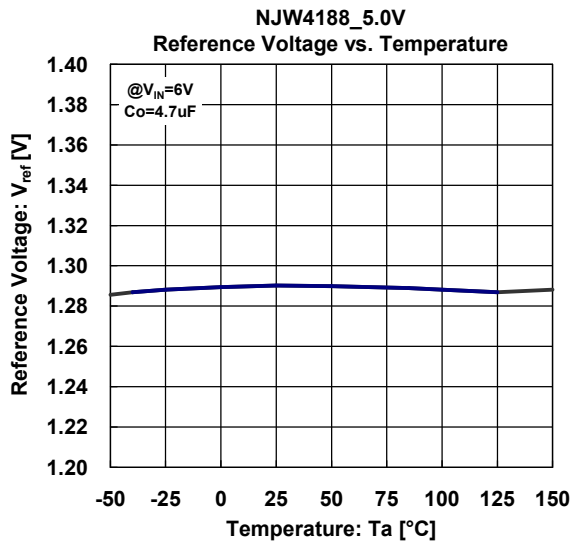
■ TYPICAL CHARACTERISTICS



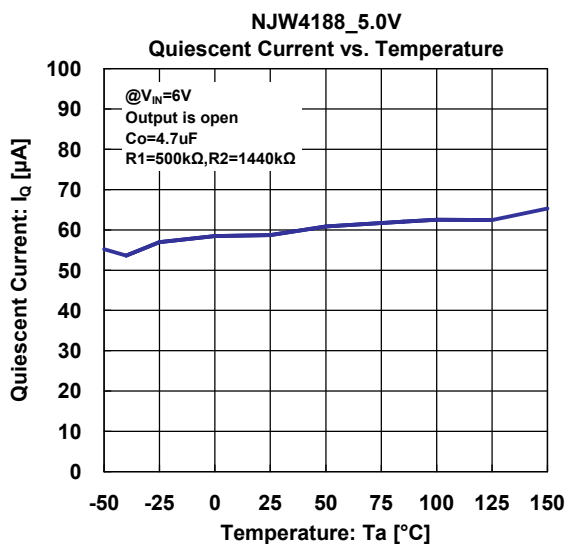
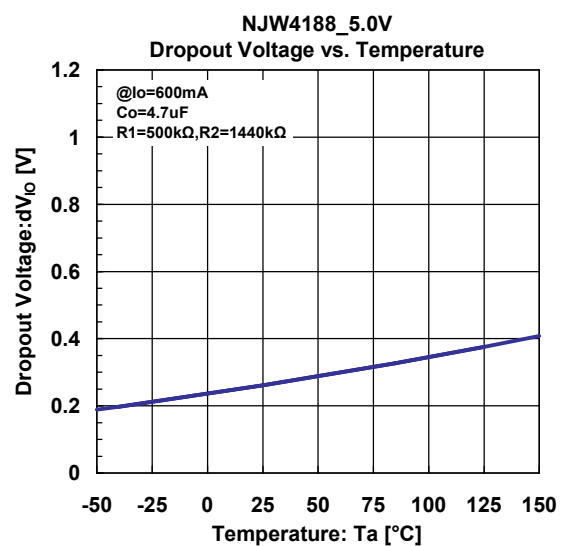
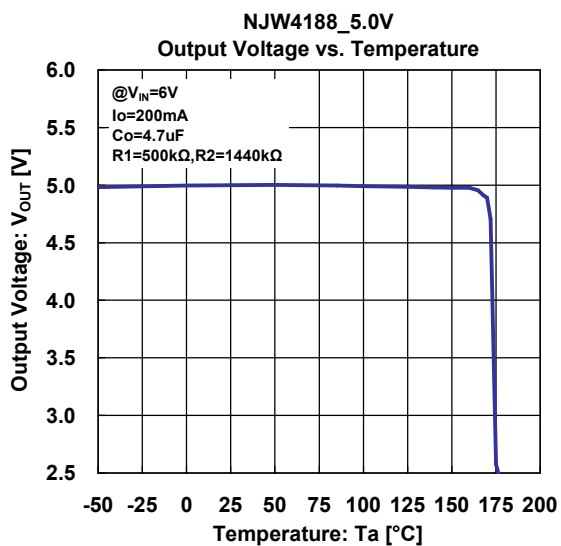
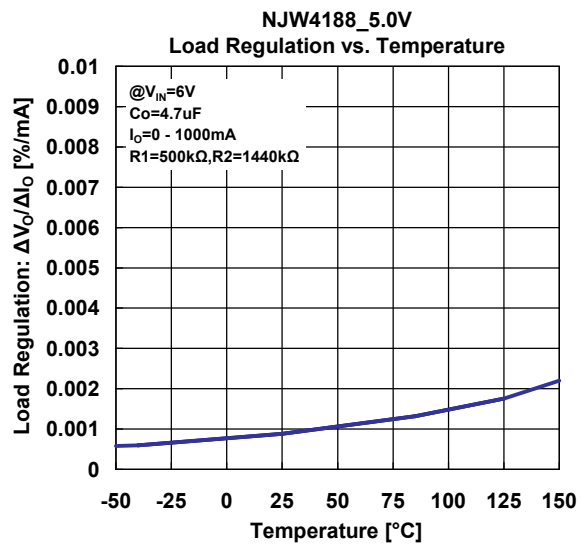
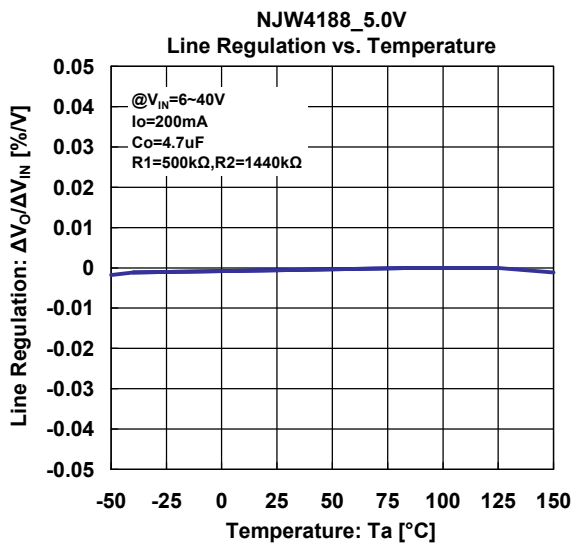
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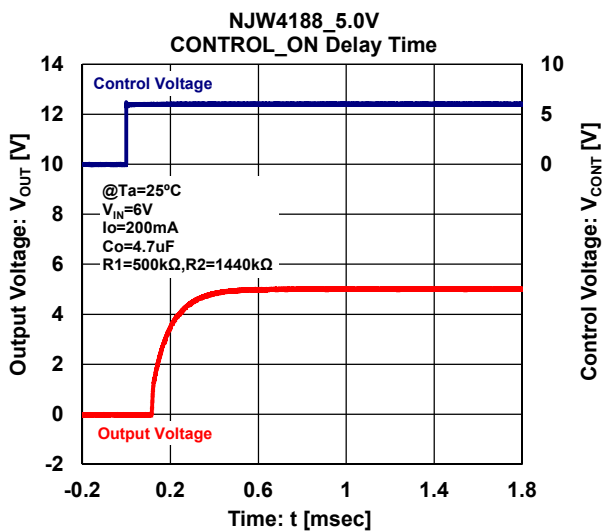
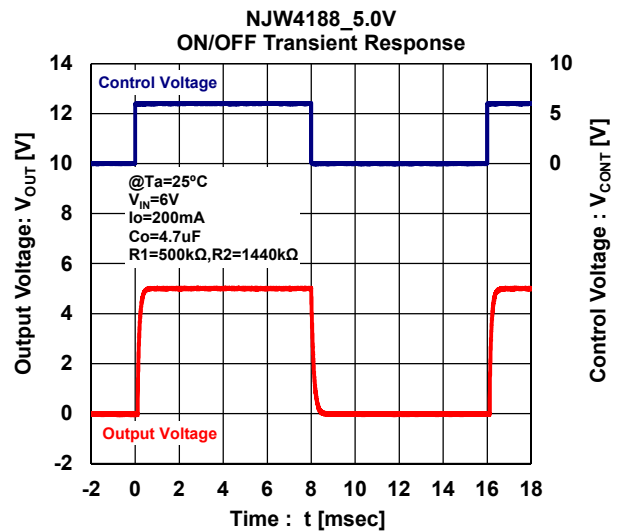
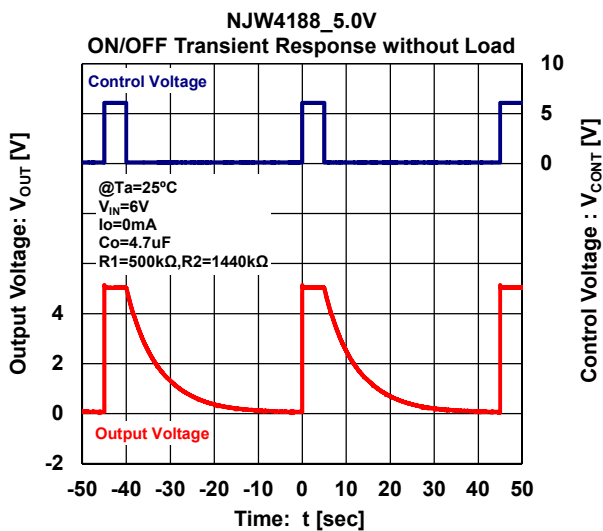
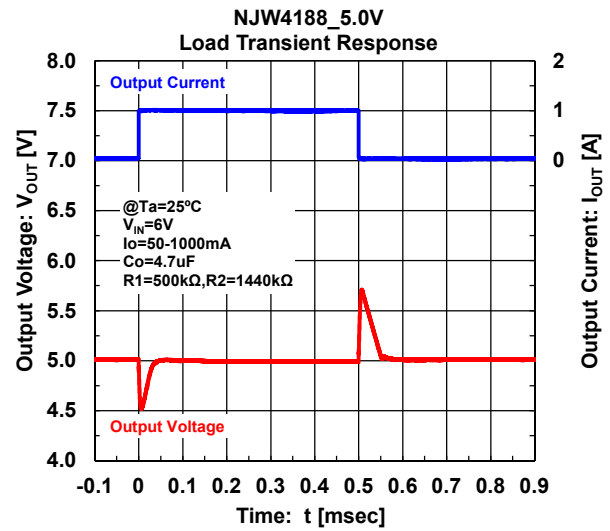
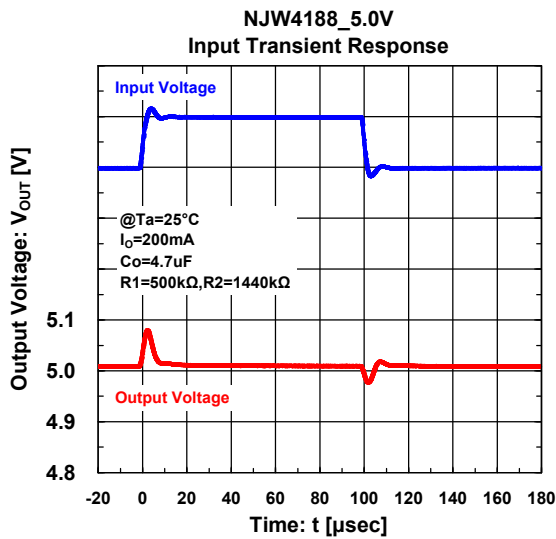
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[CAUTION]

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