Inverting Charge Pump IC

■ GENERAL DESCRIPTION

The NJW4191 is the inverting charge pump IC that operates wide 4.7V to 17V input range. With only the external part of an input/output capacitor and a charge pump capacitor, can compose the inverting voltage circuit. It has a high current capability and a corresponding to small-sized capacitor compared with conventional product such as popular 7660/7662.

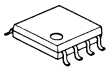
For usability, it has ON/OFF function, Output Voltage Adjustable function and external synchronous function.

The NJW4191 is suitable for the bias voltage of a liquid crystal panels, CCD, sensors and operational amplifiers.

There is the NJW4190 for doubler voltage output application.

■ PACKAGE OUTLINE

NJW4191R



NJW4191M

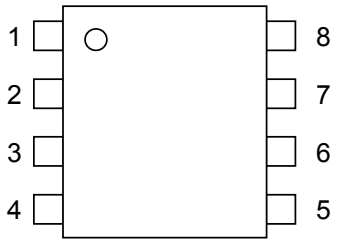
■ FEATURES

- Inverted Output -17V max.
- Wide Operating Voltage Range 4.7V to 17V
- Maximum Output Current 55mA max.
- Correspond to Ceramic Capacitor (MLCC)
- V_{OUT} Programmable
- ON/OFF Function
- Built-in Oscillation Circuit 300kHz typ.
- External Synchronization Function divide-by-4 counter (A ver.)
- Thermal Shutdown
- Function Compatible to NJU7660/NJU7662 Inverting Circuit*
- Package Outline NJW4191R : MSOP8 (VSP8)**
  NJW4191M : DMP8

* The NJW4191 is not pin compatible to NJU7660/62.

** MEET JEDEC MO-187-DA

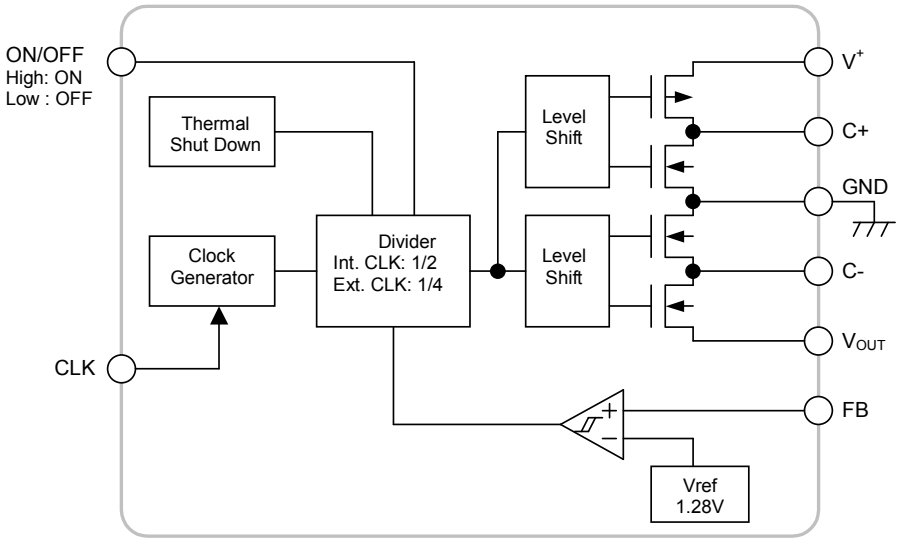
■ PIN CONFIGURATION



NJW4191R
NJW4191M

PIN FUNCTION
1. FB
2. C+
3. GND
4. C-
5. V_{OUT}
6. ON/OFF
7. CLK
8. V^+

■ BLOCK DIAGRAM



■ PRODUCT CLASSIFICATION

PART NUMBER	Divider
NJW4191R-A NJW4191M-A	External CLK: 1/4

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	MAXIMUM RATINGS	UNIT
Input Voltage	V^+	+20	V
FB pin Voltage	V_{FB}	+6 - $\lvert V_{OUT} \rvert$	V
ON/OFF pin Voltage	$V_{ON/OFF}$	-0.3 to +6	V
CLK pin Voltage	V_{CLK}	-0.3 to +6	V
Maximum Output Current	I_{OUT}	55	mA
Power Dissipation	P_D	MSOP8 (VSP8) : 595 (*1) DMP8 : 530 (*1)	mW
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-40 to +150	°C

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 2Layers)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+	4.7	–	17	V
External CLK Input Range A version (*2)	f_{CLK}	300	–	2,000	kHz
External CLK Duty Input Range	DUTY	45	–	80	%

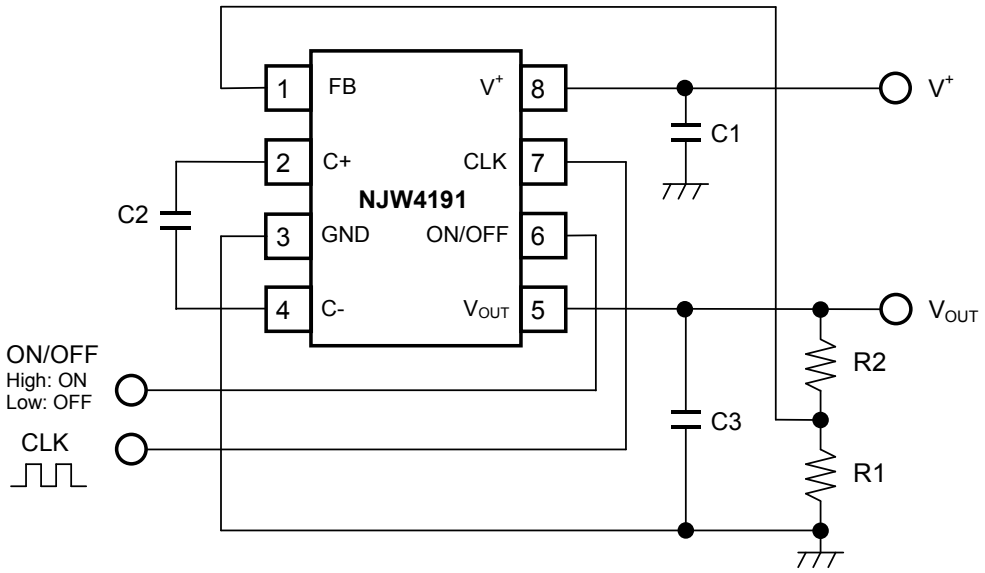
(*2): The oscillation frequency is output from the V_{OUT} pin that external clock input frequency divided by four (4).

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V^+= 10V, $V_{ON/OFF}$= 5V, V_{FB}= V_{OUT}, V_{CLK}=GND, C1=C2=C3=1μF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General Characteristics						
Supply Current	I_{DD1}	$V_{ON/OFF}$=5V, R_L=no Load	–	940	1,220	μA
	I_{DD2}	$V_{ON/OFF}$=GND	–	330	450	μA
Output Resistance	R_O	I_{OUT}=20mA	–	25	34	Ω
Oscillation Frequency	f_{OSC}		–	300	–	kHz
Power Efficiency	P_{EF}	R_L=500Ω	87	91	–	%
Voltage Conversion Efficiency	V_{EF}	R_L=no Load	97	99.9	–	%
ON/OFF Block						
ON Control Voltage	V_{ON}	$V_{ON/OFF}$= L → H	1.7	–	5.5	V
OFF Control Voltage	V_{OFF}	$V_{ON/OFF}$= H → L	0	–	0.3	V
ON/OFF pin Current	$I_{ON/OFF}$	$V_{ON/OFF}$=1.7V	–	3.5	7	μA
FB Block						
Detection Voltage	V_T	V_{FB}= L → H	-10%	1.28	+10%	V
FB pin Sink Current	I_{FB}	V_{FB}=5.5 - $\|V_{OUT}\|$	–	0.01	1	μA
CLK Block						
CLK Threshold (High)	V_{CLK_H}		2.4	–	5.5	V
CLK Threshold (Low)	V_{CLK_L}		0	–	0.7	V
CLK pin Sink Current	I_{CLK}	V_{CLK}=5.5V	–	6	10	μA

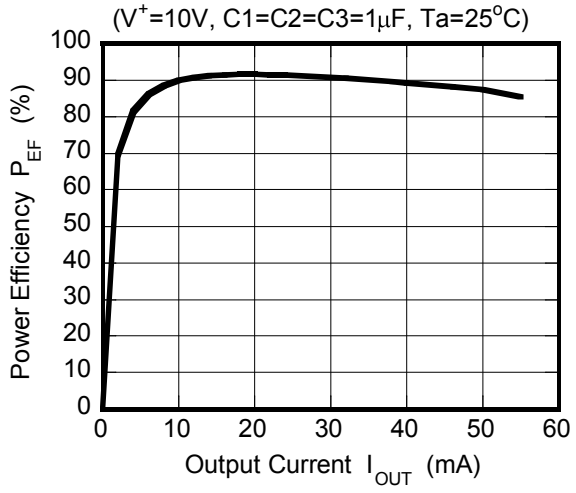
■ TYPICAL APPLICATION



■ CHARACTERISTICS

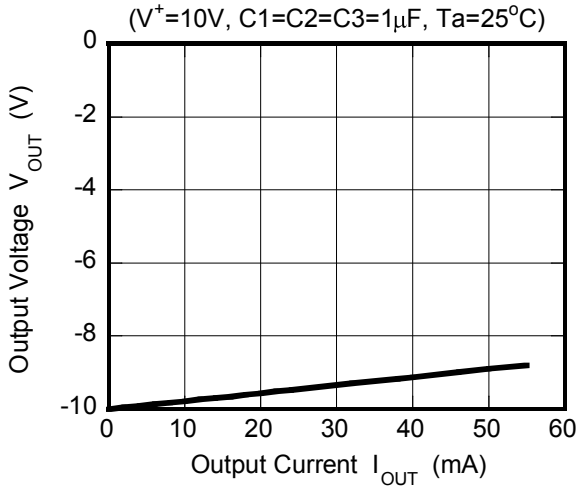
Power Efficiency vs. Output Current

(V^+=10V, C1=C2=C3=1μF, Ta=25°C)



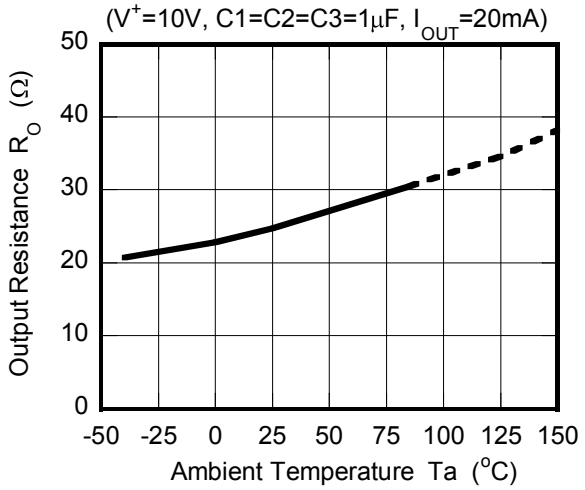
Output voltage vs. Output Current

(V^+=10V, C1=C2=C3=1μF, Ta=25°C)



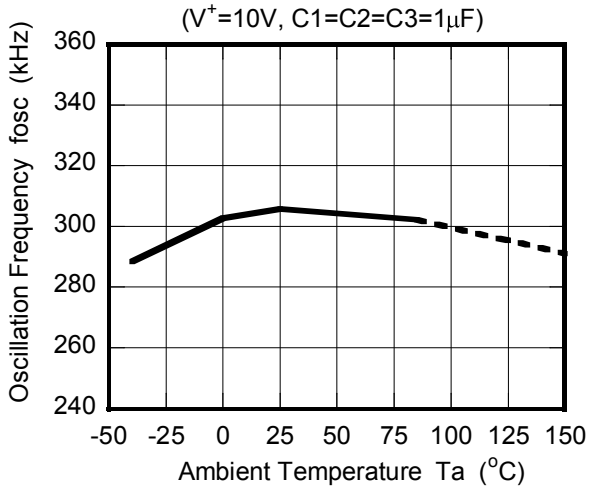
Output Resistance vs. Temperature

(V^+=10V, C1=C2=C3=1μF, I_{OUT}=20mA)



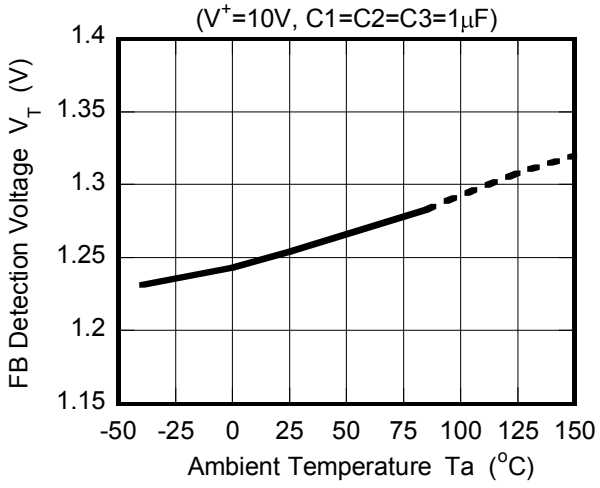
Oscillation Frequency vs. Temperature

(V^+=10V, C1=C2=C3=1μF)



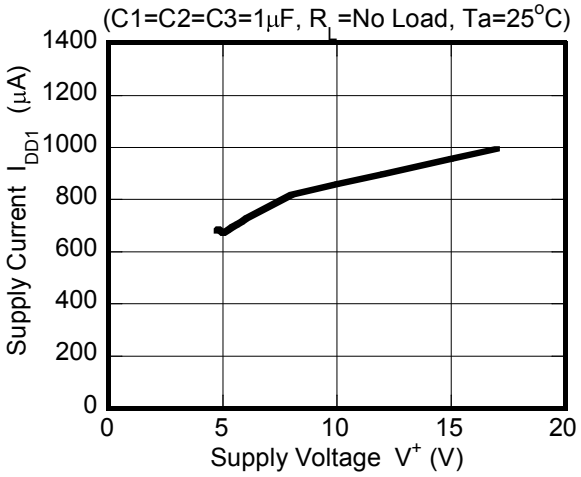
FB Detection Voltage vs. Temperature

(V^+=10V, C1=C2=C3=1μF)

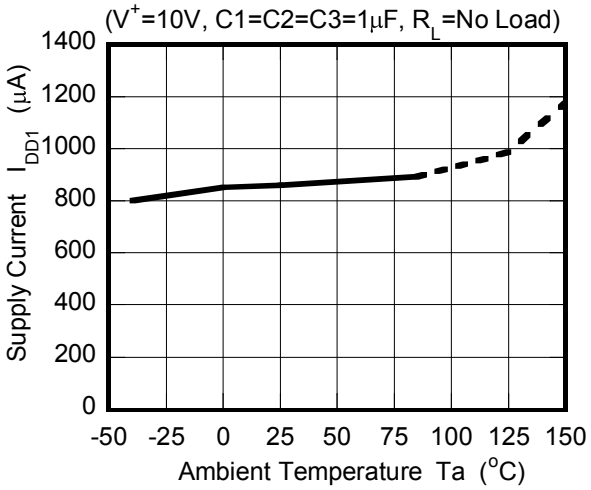


■ CHARACTERISTICS

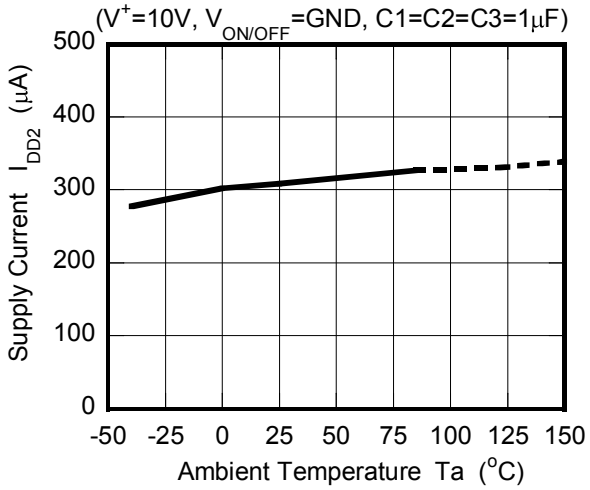
Supply Current vs. Supply Voltage
(C1=C2=C3=1μF, R_L =No Load, Ta=25°C)



Supply Current vs. Temperature
(V^+=10V, C1=C2=C3=1μF, R_L =No Load)



OFF state Supply Current vs. Temperature
(V^+=10V, $V_{ON/OFF}$=GND, C1=C2=C3=1μF)



■ Description of Block Features

● Feedback Circuit Section (FB Block)

FB circuit compares the reference voltage (1.28V±10%) and the divided voltage by the feedback resistor (R1 and R2). The output voltage is kept constant by intermittent operation. During the operation, the internal comparator is repeating an oscillation and stop. Moreover, the FB pin can be used for over voltage protection.

● Divider Section

When an external clock is not supplied, the internal clock that is generated internal oscillator is divided into 2 by internal divider, and the divided signal is supplied to level shifter. Therefore, the switching operation frequency becomes 150kHz, a half of the internal oscillator frequency in 300kHz.

If an external clock supplies, the external clock is divided into 4 by internal divider (A ver.), and the divided signal is supplied to level shifter. Therefore, the switching operation frequency becomes a quarter of an external clock frequency (A ver.).

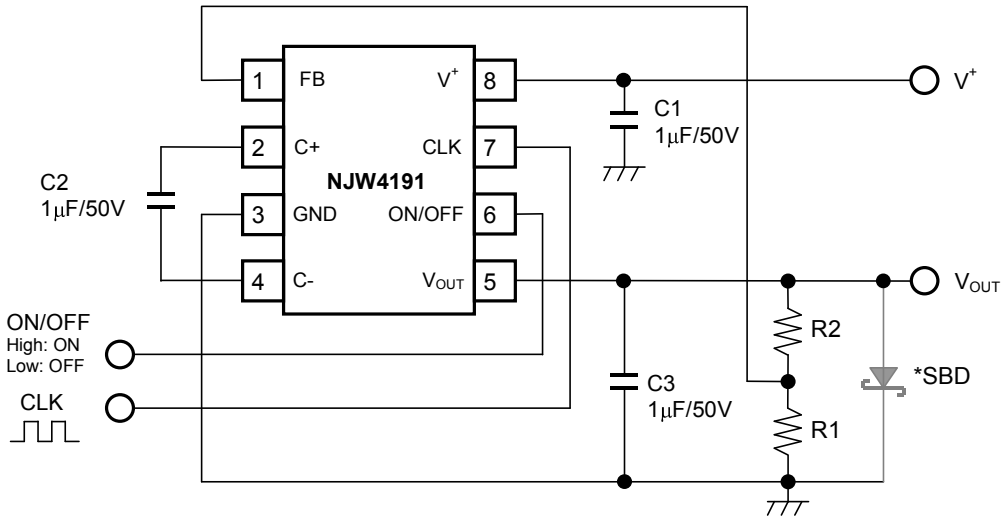
● ON/OFF Function

The NJW4191 has a built-in ON/OFF function. The ON/OFF pin is pulled-down by internal resister and it is set OFF state at normal mode. The Charge pump function turns on when supplied 1.7V or more into the ON/OFF pin.

● Thermal Shutdown Function

The NJW4191 has a built-in thermal shutdown function. When the junction temperature exceeds 160°C, an internal thermal shutdown circuit operates and it is stopped oscillator and divider. The result, charge pump operation is stopped. When the junction temperature deceases until around 150°C, the charge pump function restarts.

■ Application Information



* In case of connecting a load between V^+ and V_{OUT} or between other positive voltage and V_{OUT}.

C1: Murata GRM21BB31H105K
C2: Murata GRM21BB31H105K
C3: Murata GRM21BB31H105K

■ Capacitor Selection

Types and values of capacitors are very important parameter for stable operation and characteristics: ripple voltage, noise and so on. To reduce a ripple voltage and/or noise, uses low ESR capacitor for input capacitor (C1) and output capacitor (C3). Recommended capacitor value is 1μF or more.

A ripple voltage is decided by output capacitor value, oscillation frequency and output current. The ripple voltage (peak-to-peak voltage) can calculated as follows:

If increasing the output capacitor value, the inrush current increases but the ripple voltage is reduced.

Peak-to-peak ripple voltage is calculated by the following formula;

$$V_{RIP\_p-p} \cong \frac{I_{OUT}}{2 \times f_{OSC} \times C_3}$$

If a large electrolytic capacitor is used for the output capacitor(C3), it can be suppressed the transient change of charging or discharging and the output ripple voltage. The spike noise at the high frequency band can be reduced by using a superior high-frequency characteristics ceramic capacitor for the output capacitor (C3). One of effective method to reduce noise is a ceramic capacitor and an electrolytic capacitor connect in parallel. Moreover, it is effective to use a low pass filter such as RC filter.

In addition, the ripple voltage can be reduced by increasing the external clock frequency.

■ Application Information (Continued)

The flying capacitor (C2) decides charge pump strength. You should use a nonpolar type to flying capacitor (C2) to avoid inverting at startup. Recommended capacitor is a low ESR type (MLCC) and 1μF or more for the flying capacitor (C2) in order to supply the rated output current.

The theoretical formula of the minimum output resistance is given by the following;

$$R_{OL} = \frac{|-V_{IN}| - |V_{OUT}|}{I_{OUT}} \cong \frac{1}{f_{OSC} C_2}$$

Actual output resistance is shown as follows;

$$R_O = R_{ON(SW)} + R_{OL}$$

The internal output resistance of NJW4191 is 25Ω (typ.).

● Rush Current

The inrush current flows at the time of startup includes releasing from shutdown mode. Moreover, when the voltage difference between V^+ and V_{OUT} is larger, the spike current increases from the power supply. While the NJW4191 is operating, only the effective output impedance limits the output current. Therefore, take care it has possibility to cause influence to power source stability at the time of startup includes releasing from shutdown mode.

■ Application Information (Continued)

● Output Voltage Setting

The NJW4191 has the built-in output voltage program function, it is possible to set output voltage by feedback resisters; R1 and R2 (Fig.1.).

The operation of NJW4191 is the following:

1. The charge pump operation works until the output voltage setting value reaches.
2. The charge pump operation stops when the output voltage exceeds a setting value.
3. The charge pump operation restarts when the output voltage became below setting value.

It becomes intermittent operation that repeats from 1 to 3.

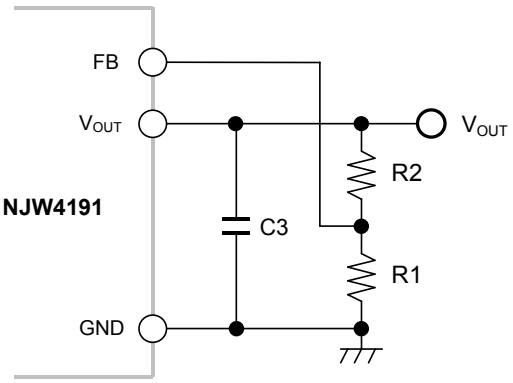


Fig. 1. Feed Back Resistor Setting

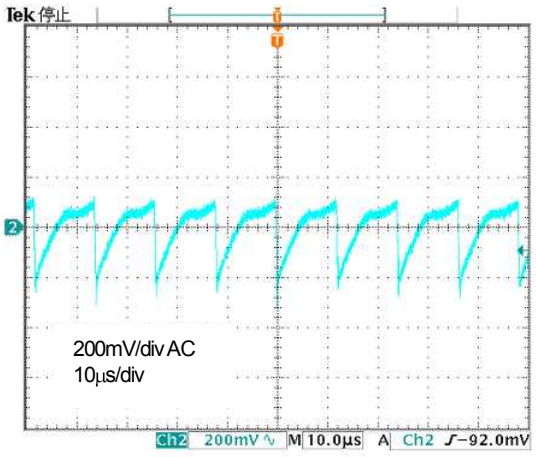
You should consider the sum of R1 and R2 becomes over 2MΩ to avoid malfunction by exogenous noise. At first, you should decide R2 value, and calculate R1 to become the required output voltage by the following formula;

$$|-V_{OUT}| = (1+ R1/R2) \times 1.28 \text{ [V]}$$

When the output voltage program function is unnecessary, connects FB pin to V_{OUT} pin.

At the time of charge pump operation, the discharge speed of output capacitor varies by a load condition. And the ripple voltage also varies that is generated by this intermittent operation. When the input voltage is higher, the ripple voltage becomes higher because an electric charge of the output capacitor increases. Moreover, the ripple voltage increases when a large flying capacitor (C2) is used.

The way to reduce the voltage ripple due to intermittent operation is to use a large capacitor to the output capacitor (C3). As a result, the transient change when the output voltage is charged / discharged can be reduced, and the low frequency ripple can be decreased. In case of light load and/or high input voltage applications, the low frequency ripple can be reduced by using small flying capacitor (C2) because the electric charge of output capacitor (C3) per switching frequency becomes smaller. However, using a small flying capacitor (C2) will decrease the efficiency and maximum output current.



(V^+=10V, $V_{OUT}\cong$ -5V, I_{OUT}=20mA
R1=30kΩ, R2=10kΩ, C1=C2=C3=1µF)

Fig. 2. Output Ripple Voltage Characteristic

● External Clock Synchronization Function

The NJW4191 has the built-in external clock synchronization function. When uses the external clock synchronization function, set the external clock duty from 45% to 80% and the external clock frequency from 300kHz to 2MHz (A ver.). If the external clock synchronization function is unnecessary, connects the CLK pin to GND.

■ Application Information (Continued)

● Application Tips

When the NJW4191 stops operating, the V_{OUT} pin becomes high impedance. If applying a positive voltage to the V_{OUT} pin from the outside during startup or non-operation, inserts SBD between the V_{OUT} pin and GND for NJW4191 protection.

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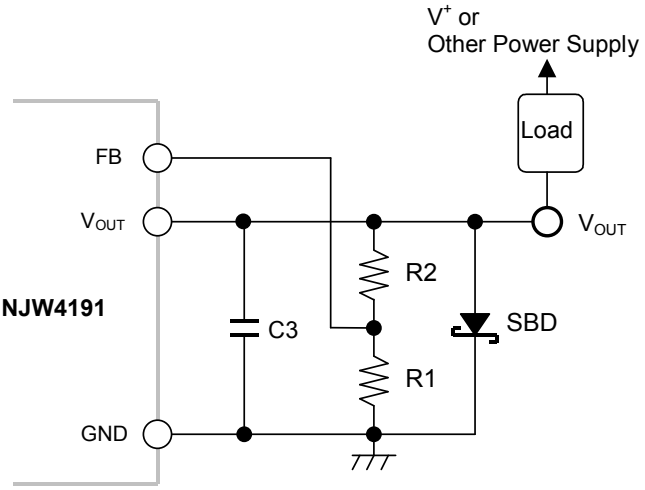

● Layout Tips

To reduce a switching noise and/or a ripple voltage, the design of PCB layout is very important. All capacitors should be arranged as close as possible to the NJW4191. In addition, the feedback resistor should be arranged as close as possible to the FB pin, because it is sensitive to exogenous noise.

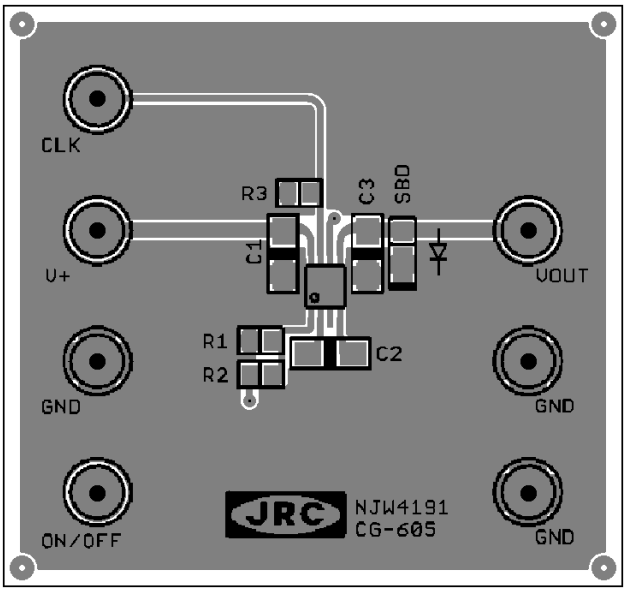

Fig. 4. PC Board Layout (Top)

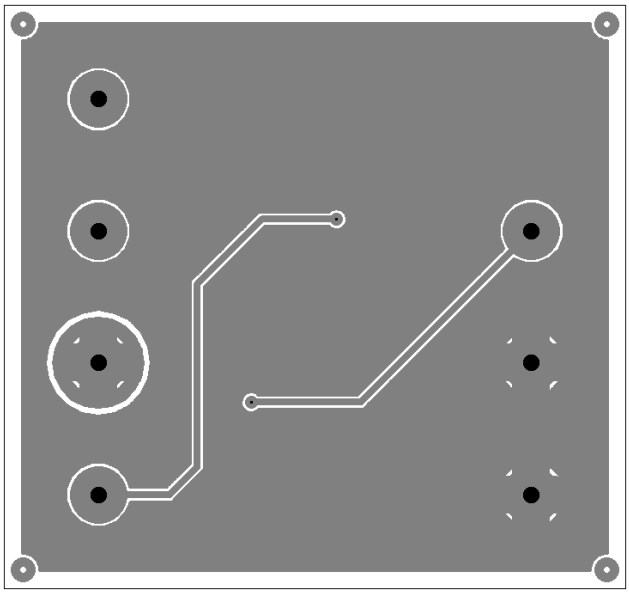

Fig. 5. PC Board Layout (Bottom)

■ Regarding replacement to an inverting application using NJU7660/62

The NJW4191 is upper product against NJU7660/62 and competitor's xxx7660/62 series. In case of replacing from NJU7660/62 to NJW4191, considers the following conditions.

	NJU7660/62		NJW4191
1pin:	NC pin	→	FB pin connect to V_{OUT} line.
6pin:	VR pin	→	ON/OFF pin connect to 5V power line.
7pin:	OSC pin	→	CLK pin connect to GND line.

You should insert SBD between V_{OUT} and GND for NJW4191 protection in case of connecting a load between V^+ and V_{OUT} or between other positive voltage and V_{OUT}.

MEMO