3 PHASE BRUSHLESS DC MOTOR CONTROLL IC

■ GENERAL DESCRIPTION

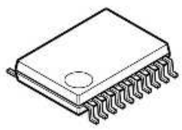
The NJW4305A is a 3 phase brush less DC motor controller IC.

It uses hall element signal inputs and generates motor driving waveform.

Output pre-driver is optimized to work with external Power MOS transistor for better power handling.

Using the NJW4305A, 3-phase DC motor application with speed control feature can be easily achieved

■ PACKAGE OUTLINE

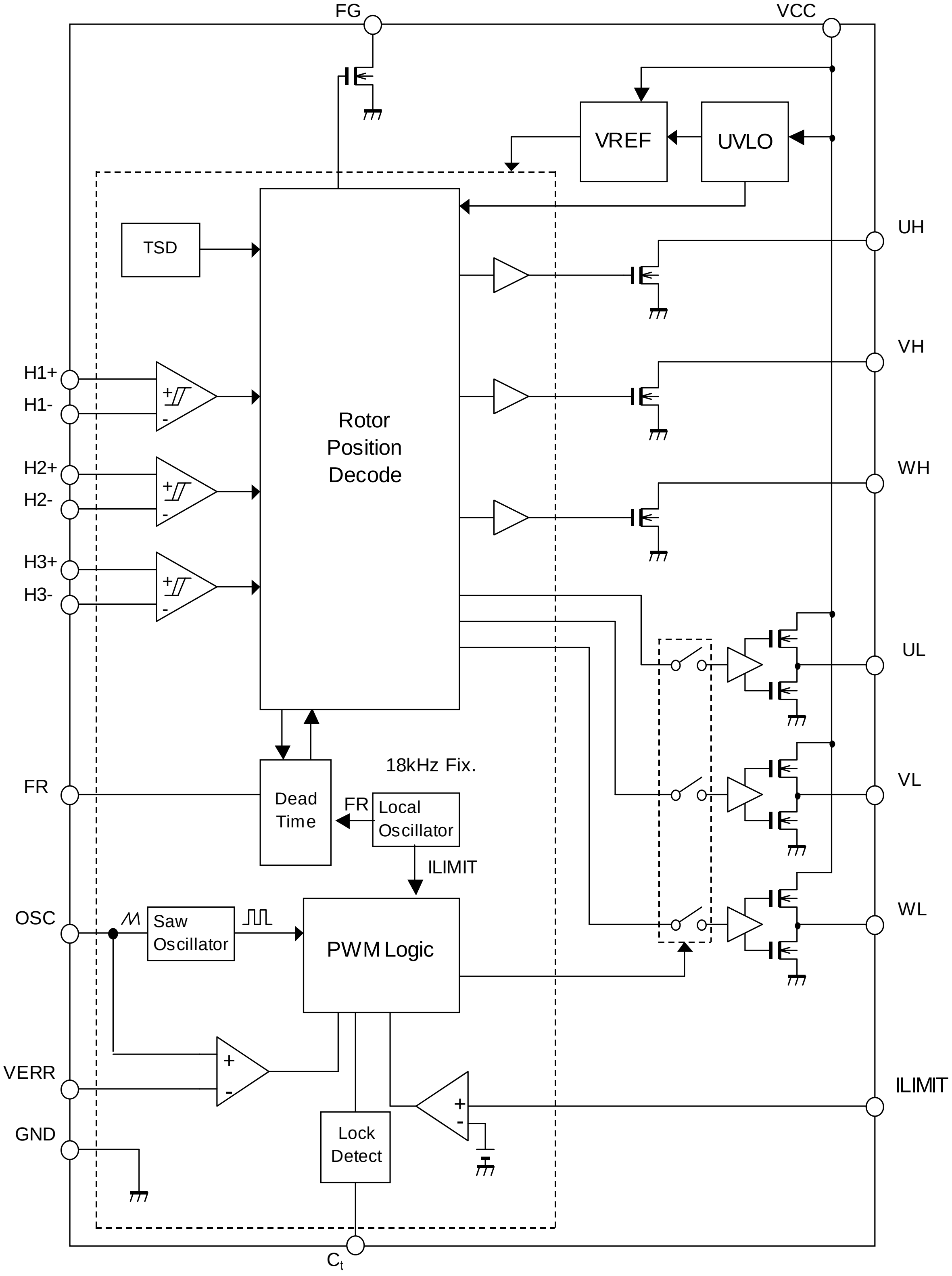


NJW4305AVC3
(SSOP20-C3)

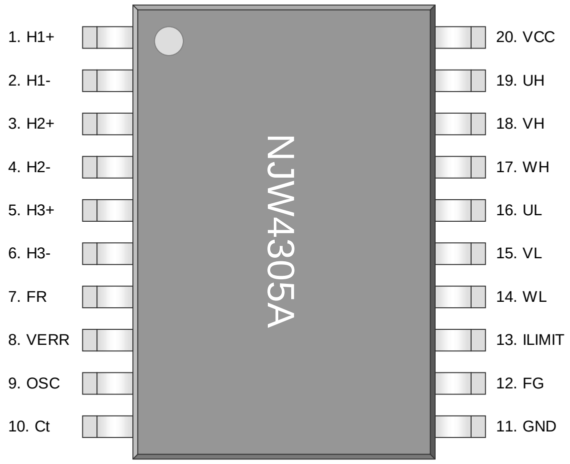
■ FEATURES

- ● Maximum Supply Voltage : 40V
- ● Operating Voltage Range : 7.3V to 36V
- ● Operating Ambient Temperature : - 40ºC to + 105ºC
- ● Quiescent Current : 3.2mA (typ.) at V_{CC}=24V
- ● FG Output
- ● Lock Protection Function (Auto Release)
- ● Forward / Reverse Function
- ● Over Current Detection Function
- ● Thermal Shutdown Function
- ● UVLO Protection Circuit
- ● Direct PWM Control : up to 150kHz
- ● Bi-CDMOS Technology
- ● Package Outline : SSOP20-C3

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION	NOTE
1	H1 +	Hall Element Input Pin H1 +	U Phase Hall Signal Input +
2	H1 -	Hall Element Input Pin H1 -	U Phase Hall Signal Input -
3	H2 +	Hall Element Input Pin H2 +	V Phase Hall Signal Input +
4	H2 -	Hall Element Input Pin H2 -	V Phase Hall Signal Input -
5	H3 +	Hall Element Input Pin H3 +	W Phase Hall Signal Input +
6	H3 -	Hall Element Input Pin H3 -	W Phase Hall Signal Input -
7	FR	Forward Reverse Select Signal Input	Low or Open = Forward Direction, H = Reverse Direction
8	VERR	Error Amp Voltage Input	Set of PWM Duty. Not use = Pull up
9	OSC	Connect Capacitor of PWM Control	Set of PWM Frequency
10	Ct	Connect Capacitor of Lock Protect	Set of ON Time for Lock Protection
11	GND	Ground	Connecting with Ground
12	FG	FG Output	Rotation speed output Pin Use = Pull up
13	ILIMIT	Over Current Detect	L = Operating, H = Stop Nonuse = Pull down
14	WL	WL Output Pin	W Phase Output for Low Arm
15	VL	VL Output Pin	V Phase Output for Low Arm
16	UL	UL Output Pin	U Phase Output for Low Arm
17	WH	WH Output Pin	W Phase Output for Upper Arm
18	VH	VH Output Pin	V Phase Output for Upper Arm
19	UH	UH Output Pin	U Phase Output for Upper Arm
20	VCC	Power Supply	Input DC Power

* All Ground Pins must be connected at the outside.
* Electrical potential of all unused output pins must be fixed at the outside.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Supply Voltage	V_{CC}	40	V	V_{CC} Pin
Hi Side Output Pin Voltage	V_{OH}	40	V	UH, VH, WH Pin
FG Pin Voltage	V_{FG}	7	V	FG Pin
Hall Input Pin Voltage	V_{IH}	7	V	H1+, H1-, H2+, H2-, H3+, H3- Pin
Logic Input Pin Voltage	V_{IN}	7	V	FR Pin
ILIMIT Pin Voltage	V_{LIM}	3.5	V	ILIMIT Pin
VERR Pin Voltage	V_{VERR}	7	V	VERR Pin
Hi Side Output Current	I_{OH}	150	mA	UH, VH, WH Pin
Low Side Output Current	I_{OL}	+100 / -150	mA	UL, VL, WL Pin
FG Output Current	I_{FG}	15	mA	FG Pin
Power Dissipation	P_D	1000	mW	Mounted on designated board based on EIA/JEDEC. 76.2*114.3*1.6mm 2Layer, FR-4
Operating Ambient Temperature	T_{opr}	- 40 to + 105	°C	
Storage Temperature	T_{stg}	- 50 to + 150	°C	

■ RECOMMENDED OPERATIONAL CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		7.3	24.0	36.0	V

■ PIN OPERATING CONDITION

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
► Hall Input Pin (H1+, H1-, H2+, H2-, H3+, H3-)						
Hall Input Sensitivity	ΔV_{MIH}	Peak to peak	0.08	-	-	V
Hall Input Voltage Range	V_{ICMIH}		0	-	3.5	V
► Logic Input Pin (FR)						
H Level Input Voltage	V_{HIN}		2	-	5.5	V
L Level Input Voltage	V_{LIN}		0	-	0.8	V
► VERR Pin						
Input Voltage Range	$V_{ICMVERR}$		0	-	5.5	V
PWM Input Frequency	$f_{IPWMVERR}$		-	-	150	kHz

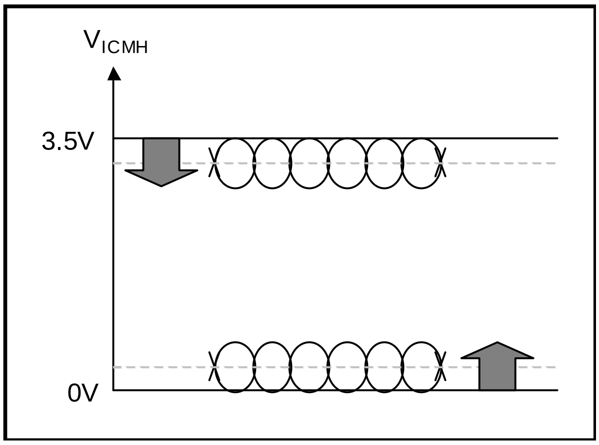
■ ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=0V, VERR=5V, OSC=1V, Ct=ILIMIT= 0V)

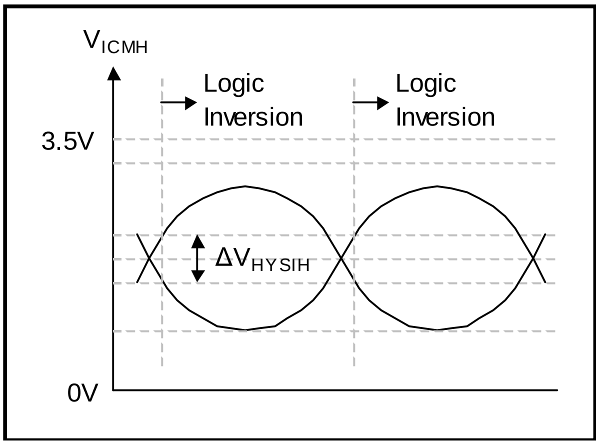
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
► GENERAL						
Quiescent Current 1	I_{CC1}	V_{CC} = 12V	2.4	2.9	3.8	mA
Quiescent Current 2	I_{CC2}	V_{CC} = 24V	2.7	3.2	4.1	mA
► THERMAL SHUTDOWN BLOCK (TSD)						
TSD Operating Temperature	T_{TSD1}		-	180	-	°C
TSD Recovery Temperature	T_{TSD2}		-	130	-	°C
TSD Hysteresis Temperature	ΔT_{TSD}		-	50	-	°C
► UNDER VOLTAGE LOCK OUT BLOCK						
UVLO Detect Voltage	V_{DUVLO}	V_{CC} Decreasing	6.0	6.45	7.19	V
UVLO Recovery Voltage	V_{RUVLO}	V_{CC} Increasing	6.01	6.6	7.2	V
UVLO Hysteresis Voltage Range	ΔV_{UVLO}		-	0.15	-	V
► LOCK DETECT BLOCK (C_t Pin)						
Lock Protection ON time	t_{ON}	Ct = 0.47µF	0.18	0.25	0.34	s
High Level Voltage	V_{HCt}		3.2	3.4	3.6	V
Low Level Voltage	V_{LCt}		0.8	1.0	1.2	V
Lock Charge Current	I_{CHGCt}	Ct = 0V → 2.5V	5.0	6.5	8.5	µA
Lock Discharge Current	$I_{DCHGCt1}$		0.3	0.65	0.9	µA
Lock Charge Discharge Current Ratio	I_{CHGCt} / I_{DCHGCt}		-	10	-	-
► HALL AMP BLOCK (H1+, H1-, H2+, H2-, H3+, H3- Pin)						
Hysteresis Voltage Range	ΔV_{HYSH}		10	30	50	mV
Input Bias Current	I_{BIH}	at 1 input	-	-	2	µA
► HIGH SIDE BLOCK (UH, VH, WH Pin)						
High Side Output Voltage	V_{OLH}	I_{SINK} = 50mA	-	0.5	1.2	V
High Side Leak Current	I_{OLEAKH}	V_{OH} = 36V	-	-	1	µA
► LOW SIDE BLOCK (UL, VL, WL Pin)						
Low Side Output Voltage1	V_{OHL1}	V_{CC} = 12V, I_{SOURCE} = 50mA	8.0	10.0	-	V
Low Side Output Voltage2	V_{OHL2}	V_{CC} = 24V, I_{SOURCE} = 50mA	8.0	10.0	-	V
Low Side Output L Voltage	V_{OLL}	I_{SINK} = 50mA	-	0.5	1.2	V
Low Side Clamp Voltage	V_{OCLL}	V_{CC} = 36V, I_{SOURCE} = 0.1mA	-	-	16.0	V
► FG OUTPUT BLOCK (FG Pin)						
Output Voltage	V_{OFG}	I_{FG} = 10mA	-	0.2	0.6	V
Leak Current	I_{LEAKFG}	V_{FG} = 5V	-	-	1	µA
► OVER CURRENT DETECT BLOCK (ILIMIT Pin)						
Detect Voltage	V_{DETLIM}		0.25	0.28	0.31	V
Input Bias Current	I_{BLIM}		-	1.0	2.0	µA
► ERROR AMP BLOCK (VERR Pin)						
PWM0% Detect Voltage	$V_{PWM1VERR}$	Output ON Duty = 0%	-	-	0.6	V
PWM100% Detect Voltage	$V_{PWM2VERR}$	Output ON Duty = 100%	3.5	-	-	V
Input Bias Current	I_{BVERR}		-	1.0	2.0	µA
► OSCILLATOR BLOCK (OSC Pin)						
Saw Wave Peak Voltage	V_{POSC}		2.7	3.0	3.3	V
Saw Wave Bottom Voltage	V_{BOSC}		0.8	1.0	1.2	V
OSC Charge Current	I_{CHGOSC}	OSC = 0V → 2.5V	50	80	120	µA
OSC Discharge Current	$I_{DCHGOSC}$	OSC = 5V → 2.5V	0.6	1.3	2.0	mA
Oscillation Frequency	f_{OSC}	C_{OSC} = 1000pF	-	35	50	kHz
► CONTROL INPUT BLOCK						
H Level Input Current	I_{HIN}	V_{IN} = 5V	30	50	100	µA
L Level Input Current	I_{LIN}	V_{IN} = 0V	-	-	1	µA
Pull Down Resistance	R_{IN}		-	100	-	kΩ

■ OPERATIONAL DEFINITION (TERMINAL and CIRCUIT)

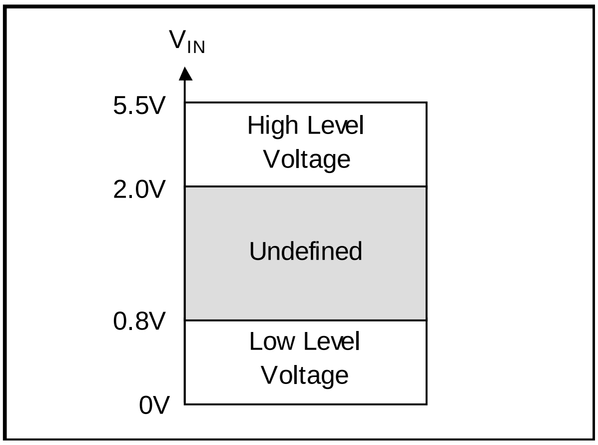
► Hole input Pin Common mode input voltage range



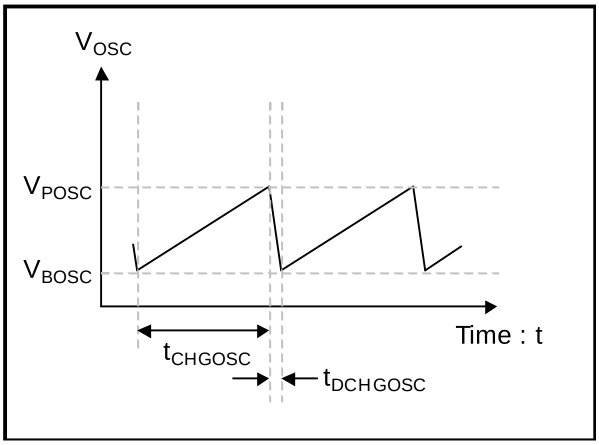
► Hall input hysteresis voltage width



► Input Pin

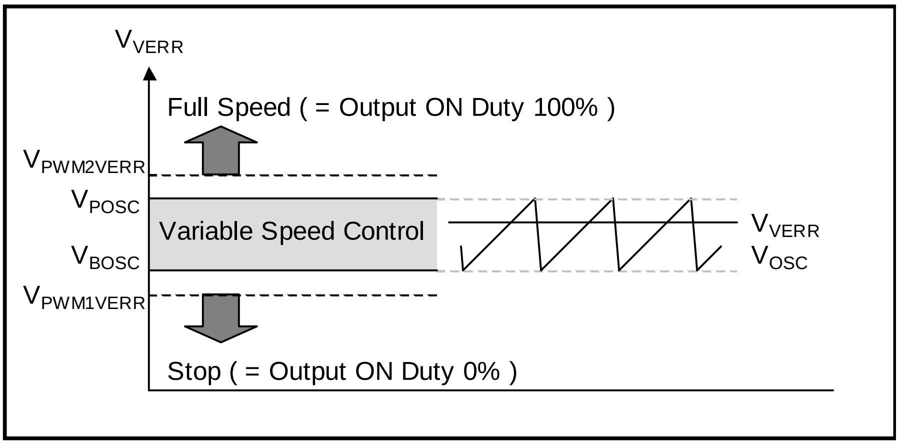


► Oscillation frequency

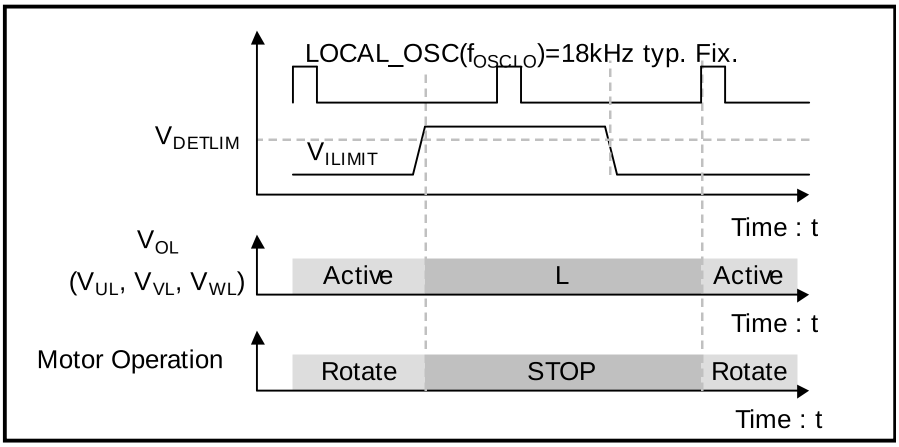


$f_{osc} = 1 / (t_{CHGOSC} + t_{DCHGOSC})$

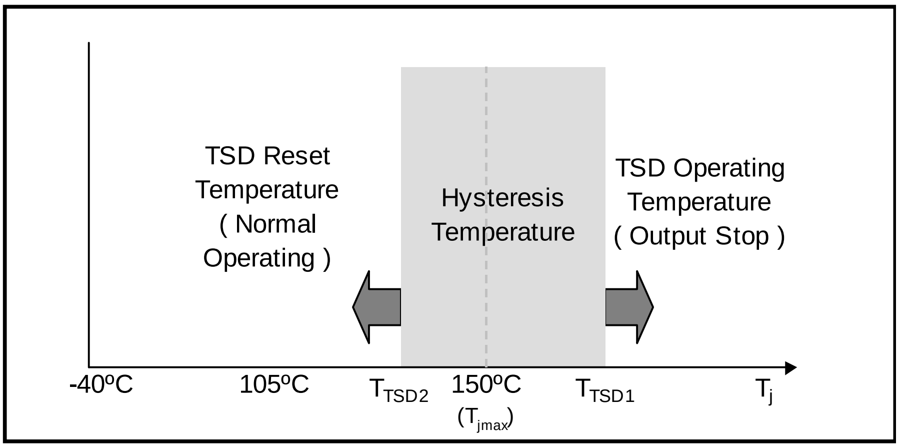
► PWM 0% / PWM 100% detect voltage



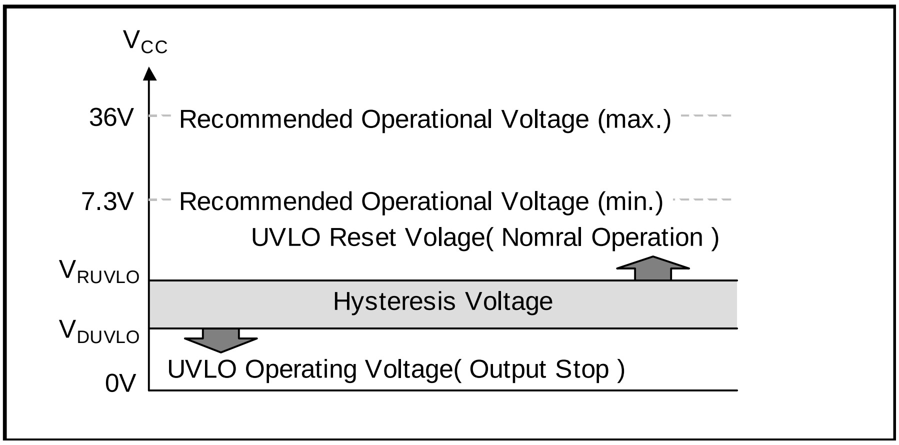
► Over current detect voltage



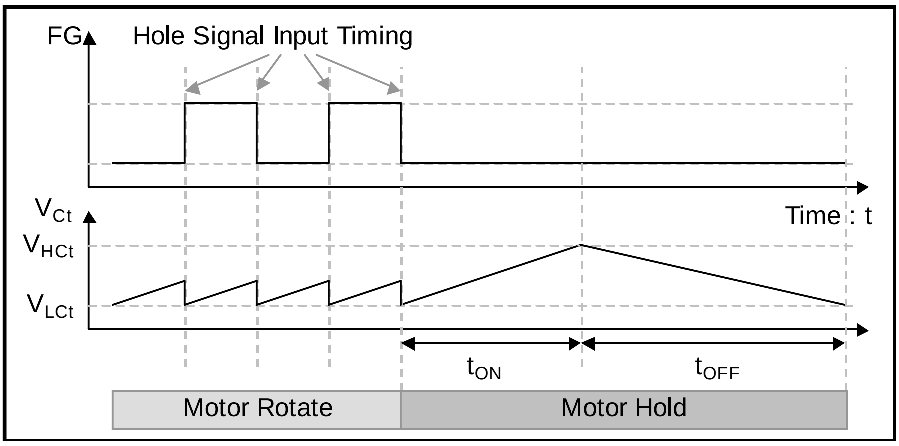
► Thermal shutdown (TSD) operational temperature



► Under voltage protection operating voltage



► Lock detect



■ TRUTH TABLE

Input vs. Output Truth table 1 (H1+ > H1 -, H2+ > H2 -, H3+ > H3 - = " H ", Don't Care = " X ")

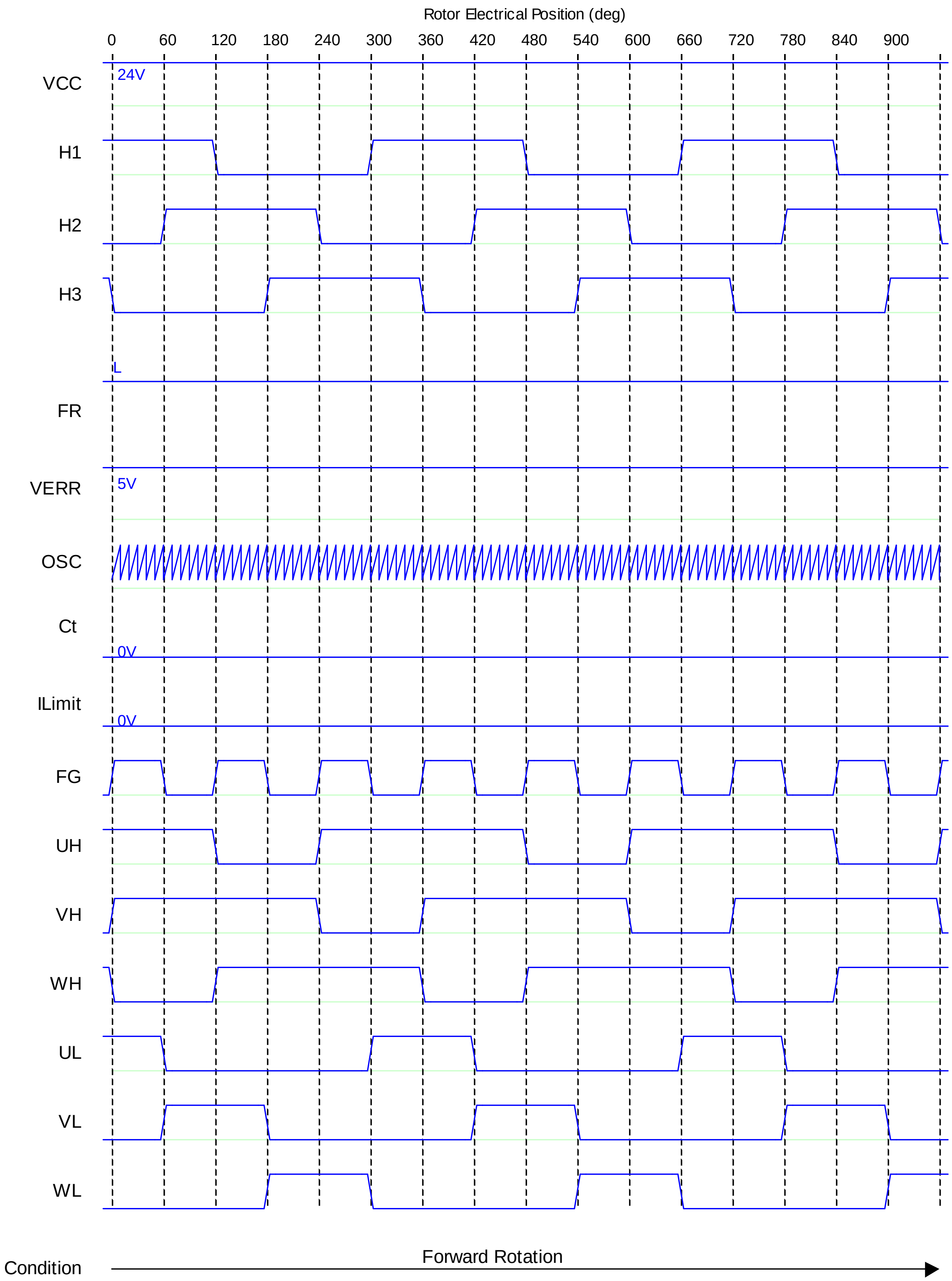
H1	H2	H3	TSD	UVLO	ILIMIT	VERR	OSC	Ct	FR	UH	VH	WH	UL	VL	WL	FG	COMMENT
H	L	L	OFF	OFF	OFF	H	L	L	L	Hi-Z	Hi-Z	L	H	L	L	Hi-Z	Forward
H	H	L								Hi-Z	Hi-Z	L	L	H	L	L	
L	H	L								L	Hi-Z	Hi-Z	L	H	L	Hi-Z	
L	H	H								L	Hi-Z	Hi-Z	L	L	H	L	
L	L	H								Hi-Z	L	Hi-Z	L	L	H	Hi-Z	
H	L	H								Hi-Z	L	Hi-Z	H	L	L	L	
H	L	L	OFF	OFF	OFF	H	L	L	H	L	Hi-Z	Hi-Z	L	L	H	Hi-Z	Reverse
H	H	L								Hi-Z	L	Hi-Z	L	L	H	L	
L	H	L								Hi-Z	L	Hi-Z	H	L	L	Hi-Z	
L	H	H								Hi-Z	Hi-Z	L	H	L	L	L	
L	L	H								Hi-Z	Hi-Z	L	L	H	L	Hi-Z	
H	L	H								L	Hi-Z	Hi-Z	L	H	L	L	
H	L	L	OFF	OFF	X	X	X	H	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	Lock Detect (Forward)
H	H	L								Hi-Z	Hi-Z	L				L	
L	H	L								L	Hi-Z	Hi-Z				Hi-Z	
L	H	H								L	Hi-Z	Hi-Z				L	
L	L	H								Hi-Z	L	Hi-Z				Hi-Z	
H	L	H								Hi-Z	L	Hi-Z				L	
H	L	L	OFF	OFF	X	L	H	L	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	PWM (Forward)
H	H	L								Hi-Z	Hi-Z	L				L	
L	H	L								L	Hi-Z	Hi-Z				Hi-Z	
L	H	H								L	Hi-Z	Hi-Z				L	
L	L	H								Hi-Z	L	Hi-Z				Hi-Z	
H	L	H								Hi-Z	L	Hi-Z				L	
H	L	L	OFF	OFF	X	X	X	H	H	L	Hi-Z	Hi-Z	L	L	L	Hi-Z	Lock Detect (Reverse)
H	H	L								Hi-Z	L	Hi-Z				L	
L	H	L								Hi-Z	L	Hi-Z				Hi-Z	
L	H	H								Hi-Z	Hi-Z	L				L	
L	L	H								Hi-Z	Hi-Z	L				Hi-Z	
H	L	H								L	Hi-Z	Hi-Z				L	
H	L	L	OFF	OFF	X	L	H	L	H	L	Hi-Z	Hi-Z	L	L	L	Hi-Z	PWM (Reverse)
H	H	L								Hi-Z	L	Hi-Z				L	
L	H	L								Hi-Z	L	Hi-Z				Hi-Z	
L	H	H								Hi-Z	Hi-Z	L				L	
L	L	H								Hi-Z	Hi-Z	L				Hi-Z	
H	L	H								L	Hi-Z	Hi-Z				L	
H	L	L	OFF	OFF	ON	H	X	L	L	Hi-Z	Hi-Z	L	L	L	L	Hi-Z	Over current protection
H	H	L								Hi-Z	Hi-Z	L				L	
L	H	L								L	Hi-Z	Hi-Z				Hi-Z	
L	H	H								L	Hi-Z	Hi-Z				L	
L	L	H								Hi-Z	L	Hi-Z				Hi-Z	
H	L	H								Hi-Z	L	Hi-Z				L	
H	L	L	OFF	OFF	ON	H	X	L	H	L	Hi-Z	Hi-Z	L	L	L	Hi-Z	Over current protection
H	H	L								Hi-Z	L	Hi-Z				L	
L	H	L								Hi-Z	L	Hi-Z				Hi-Z	
L	H	H								Hi-Z	Hi-Z	L				L	
L	L	H								Hi-Z	Hi-Z	L				Hi-Z	
H	L	H								L	Hi-Z	Hi-Z				L	
H	L	L	X	ON	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	Under voltage lock detect
H	H	L														L	
L	H	L														Hi-Z	
L	H	H														L	
L	L	H														Hi-Z	
H	L	H														L	
H	L	L	ON	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	Thermal shutdown
H	H	L														L	
L	H	L														Hi-Z	
L	H	H														L	
L	L	H														Hi-Z	
H	L	H														L	

Input vs. Output Truth table 2 (H1+ > H1 -, H2+ > H2 -, H3+ > H3 - = " H ", Don't Care = " X ")

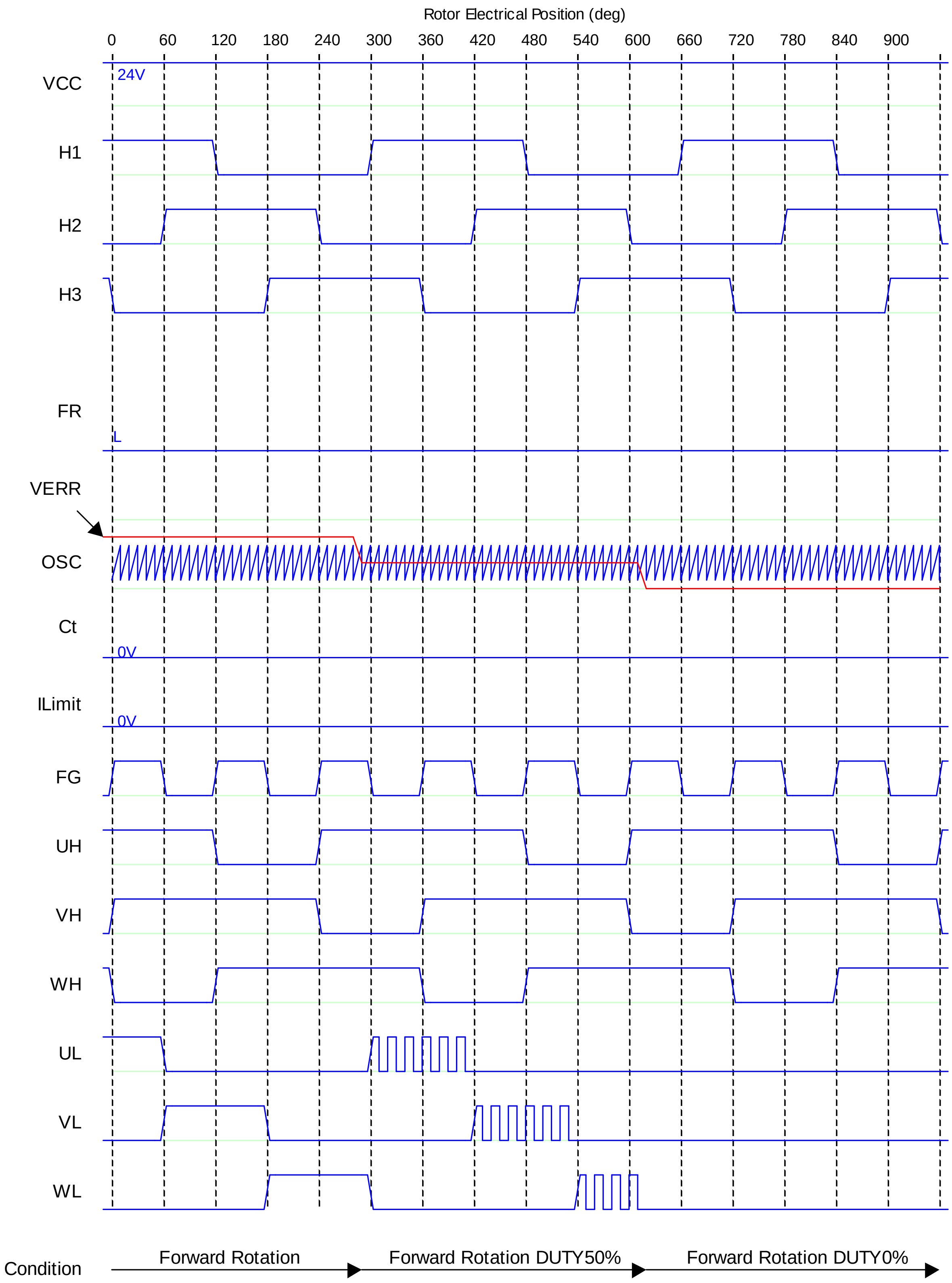
H1	H2	H3	TSD	UVLO	ILIMIT	VERR	OSC	Ct	FR	UH	VH	WH	UL	VL	WL	FG	COMMENT
H	H	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	L	L	L	Hi-Z	Error pattern Hole signal input
L	L	L															

■ **TIMING CHART**

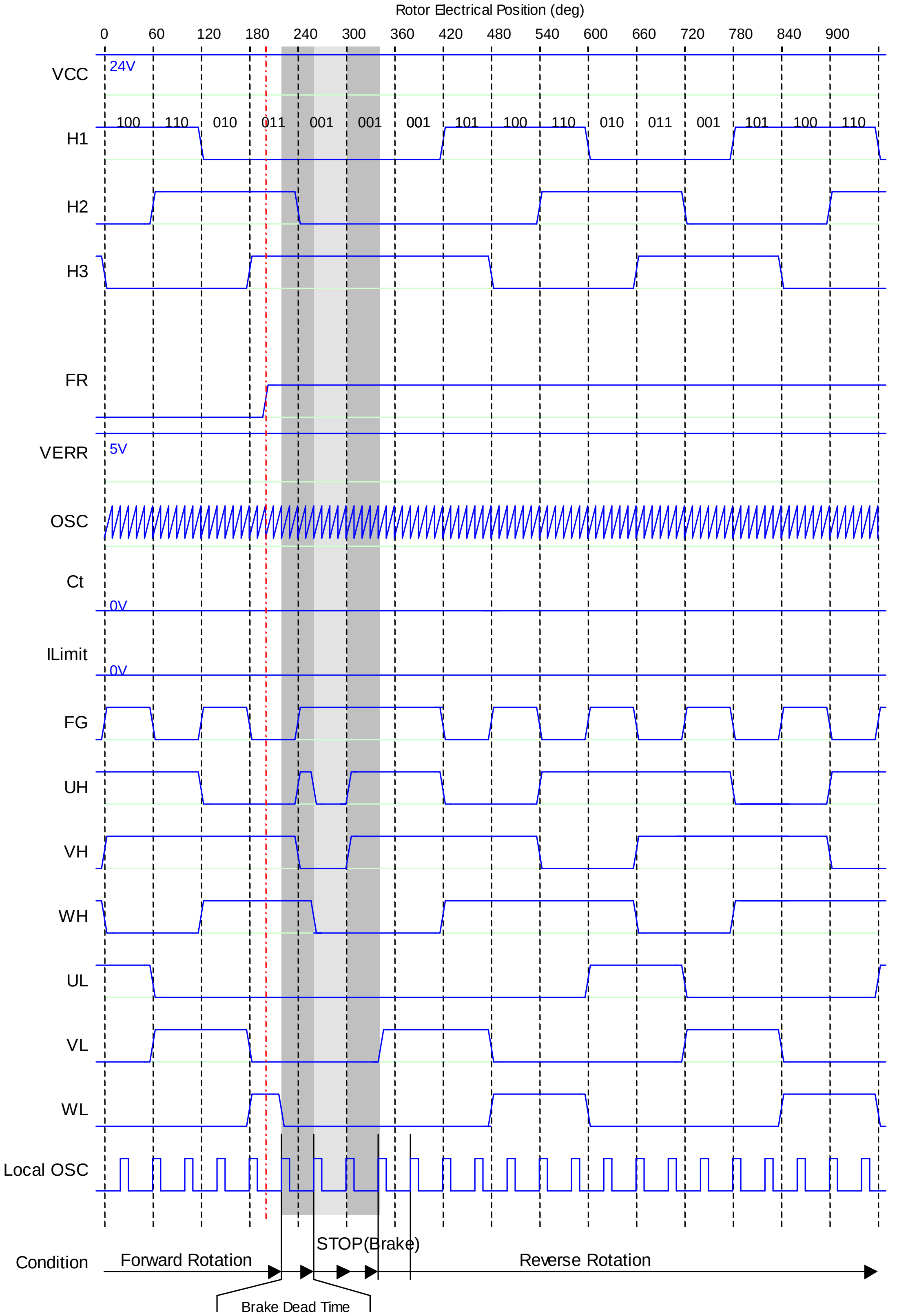
1. Forward Rotation



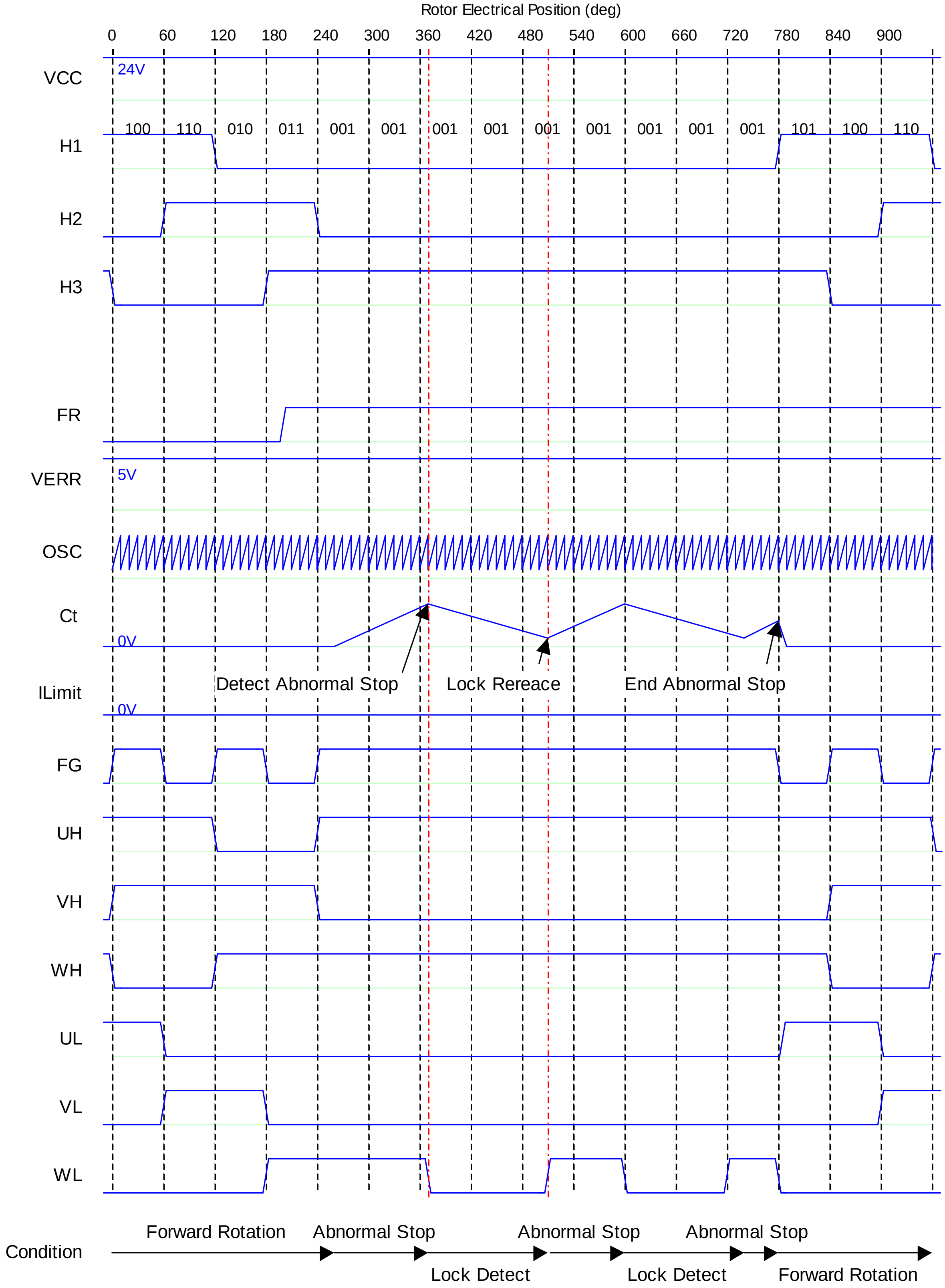
2. Forward Rotation at PWM



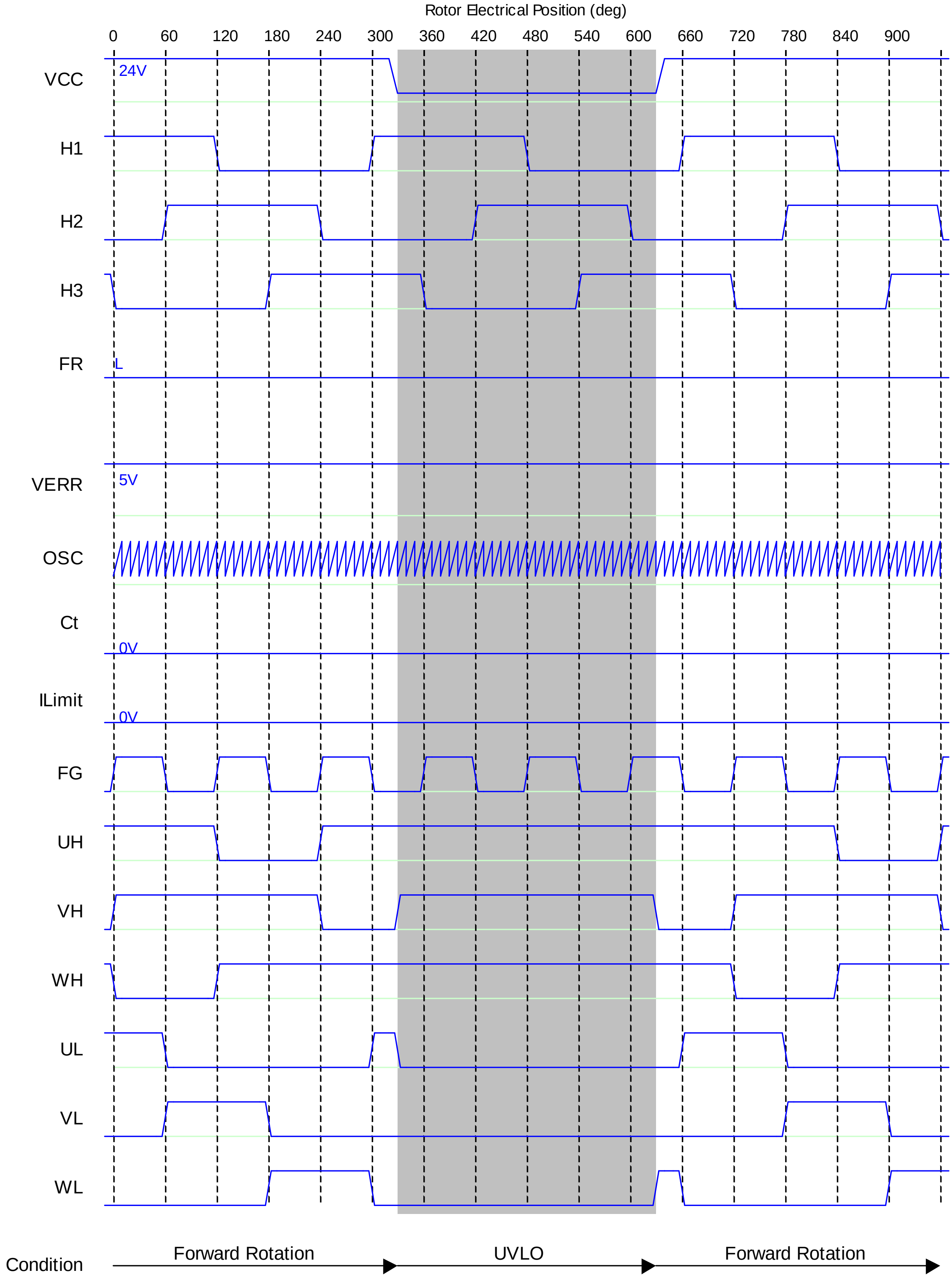
3. Change for Forward Rotate to Reverse Rotate



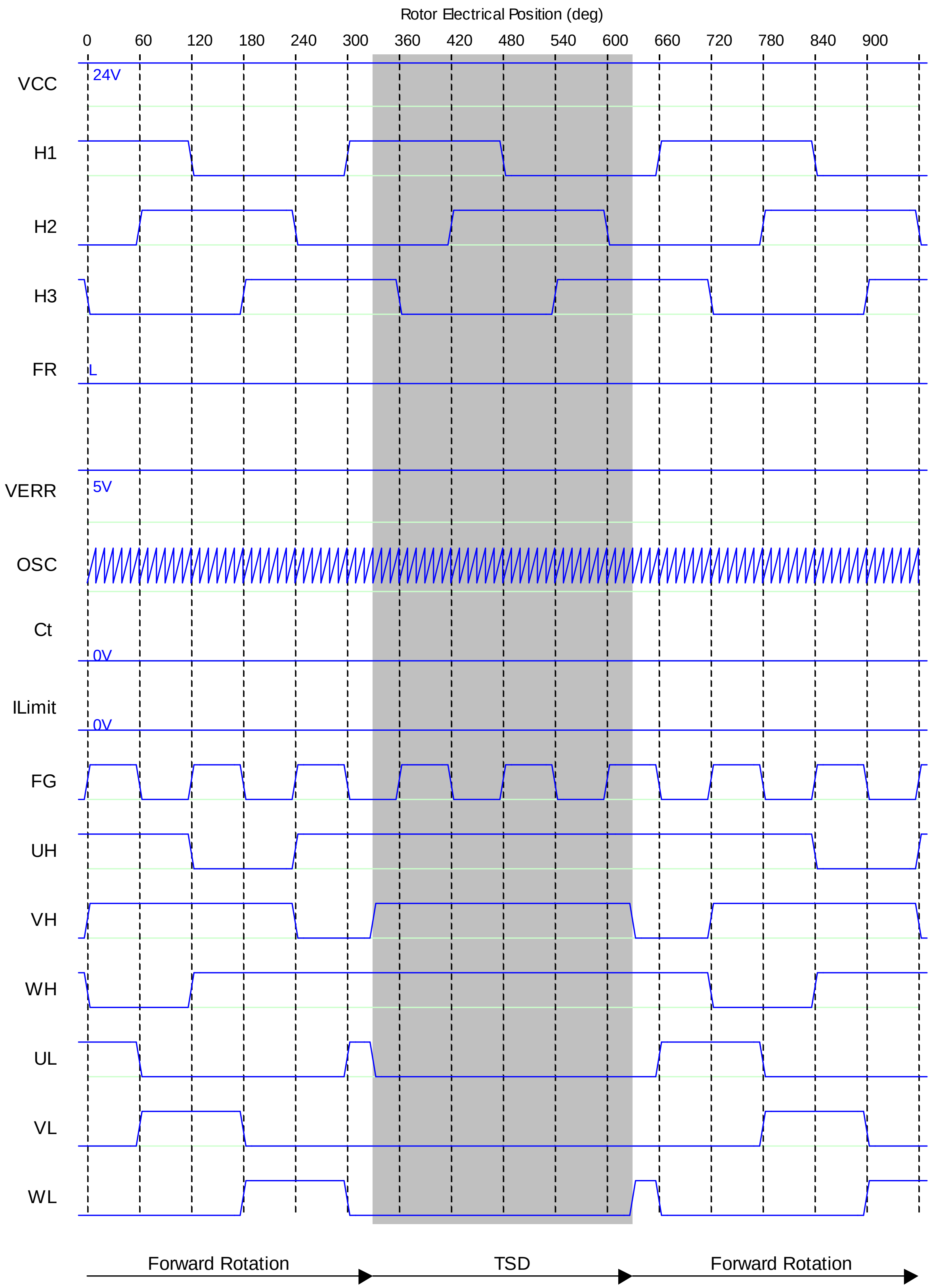
4. Forward Rotation → Lock Detect



5. Forward Rotation → UVLO



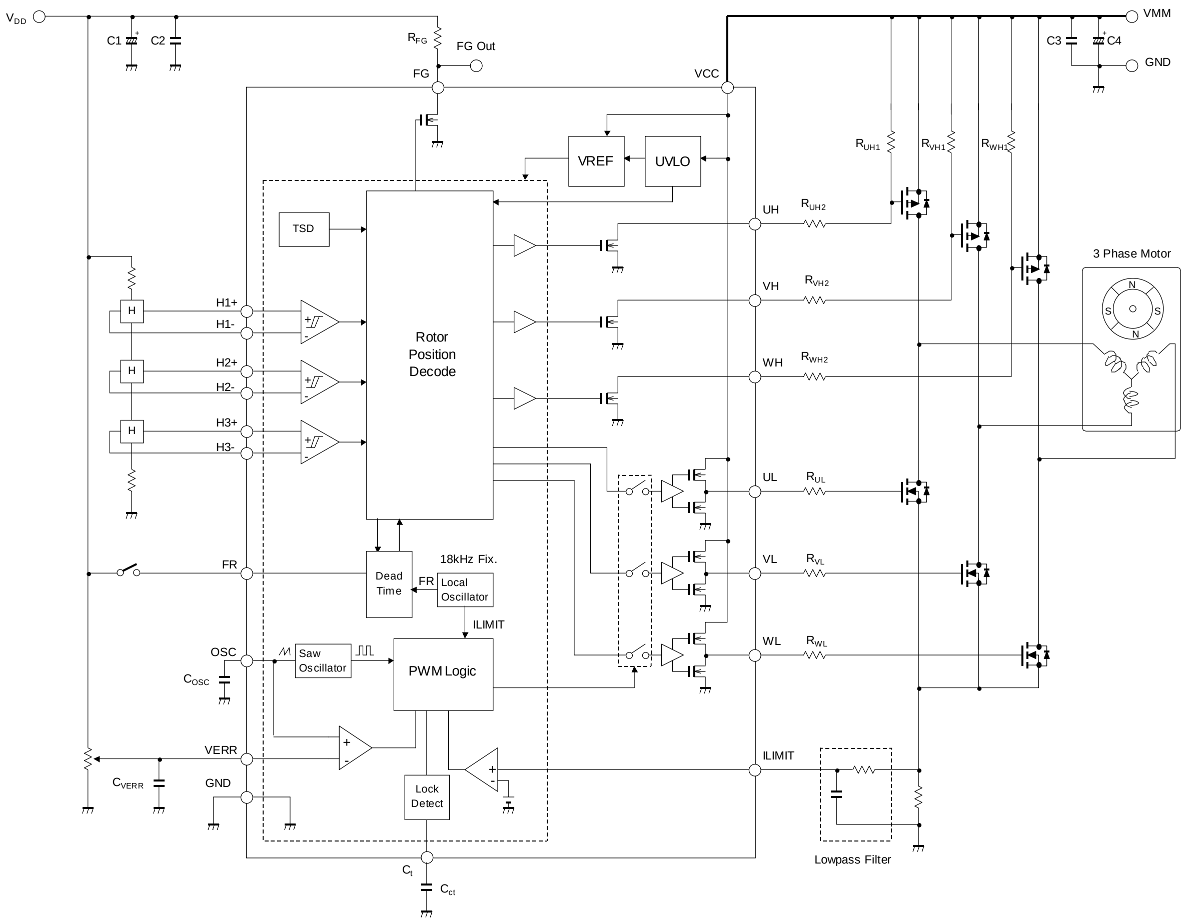
6. Forward → THD



Technical Information

■ TYPICAL APPLICATION

< MOS FET Drive Circuit, PWM Control, Operating Voltage V_{CC}=24V, Motor Voltage V_{MM}=24V >



Technical Information

■ FUNCTION DESCRIPTIONS

1. Hall Signal Input (H1+, H1-, H2+, H2-, H3+, H3- Pin)

1-1: Using Hall Device

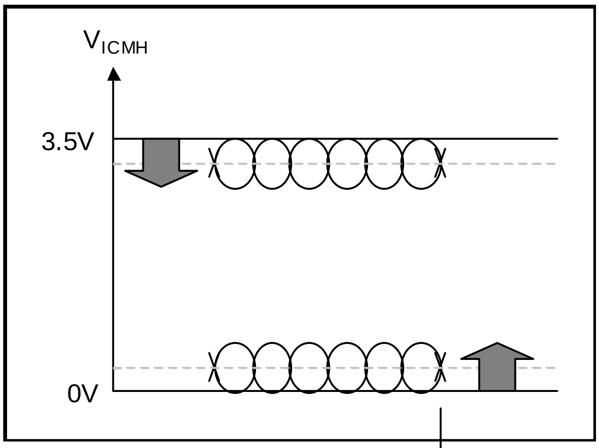
These pins are hall device input pin.

These are connected to input differential amplifier (hall amplifier) with hall device input pin.

When the Hall input level becomes "H" or "L" at the same time of three-phase, the outputs (WL, VL, UL, WH, VH, UH) become OFF.

The Rotor Position decode circuit judges like following that the voltage level is “H” at H + > H – and “L” at H + < H -.

The hall amplifier has the input hysteresis voltage of 50mV (max). You should input the amplitude greater than 100mVp-p with considering the margin.



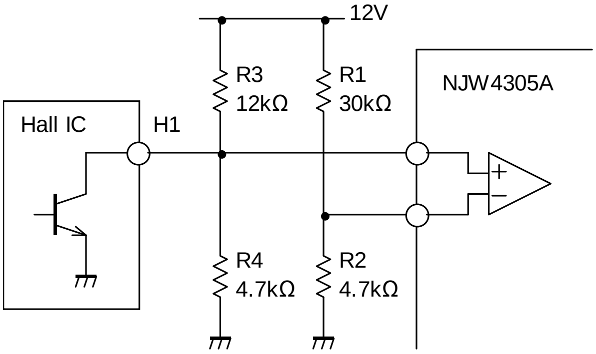
The hall signal peak value must not exceed V_{ICMIH}.

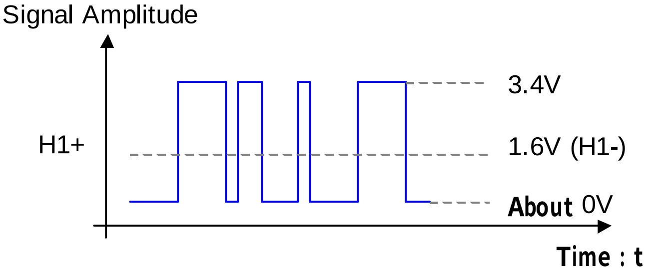
At this time, the hall signal peak value must not exceed the input common-mode input voltage range V_{ICMIH}. It should be used the hall bias resistance of same value at VCC and GND side. Some noise might overlap to the hall signal based on the GND level fluctuations by phase current change or the unbalance of an output signal course, etc. When the malfunction of the output chattering etc. occurs, it should connect between the positive pin and the negative pin with filter capacitor in range of from 1nF to 100nF.

1-2: Using Hall IC

This products is a usage hall device, but can use a hall ICs. But please add the voltage conversion circuit such as the figure because it is necessary to adapt the output amplitude of hall IC to the input voltage range of the IC. H1 is High, please set R3, R4 at the time of high so that the voltage ov VH1+ is as follows 3.5V.

< Hall IC – Hall Device Exchange Circuit >





Technical Information

2. Output Block (WL, VL, UL / WH, VH, UH Pin)

2-1: Output for Lower Arm (120º Excitation Output + ON/OFF Output)

It is an output pin that can drive directly Nch FET gate for three-phase motor lower arm. The phase switching signal is output that generated by the hall signal.

The output interrupter switch is built in. The PWM function by VERR/OSC, Protection function by Ct pin and OCP by ILIMIT are operating to the lower arm. Moreover, the voltage clamp circuit that prevents the excess voltage input to an external Nch FET gate is built in.

The output series resistance is suppressing the transient current and/or vibration at the time of switching. In case of using 3A to 5A class MOS FET, you should consider the resistance value in the range of 100Ω to 1,000Ω.

2-2: Output Upper Arm (120º Excitation Output)

It is an output pin that can drive directly Pch FET gate for three-phase motor upper arm. The phase switching signal is output that generated by the hall signal. Because these are open-drain configuration, pull-up resistor is required.

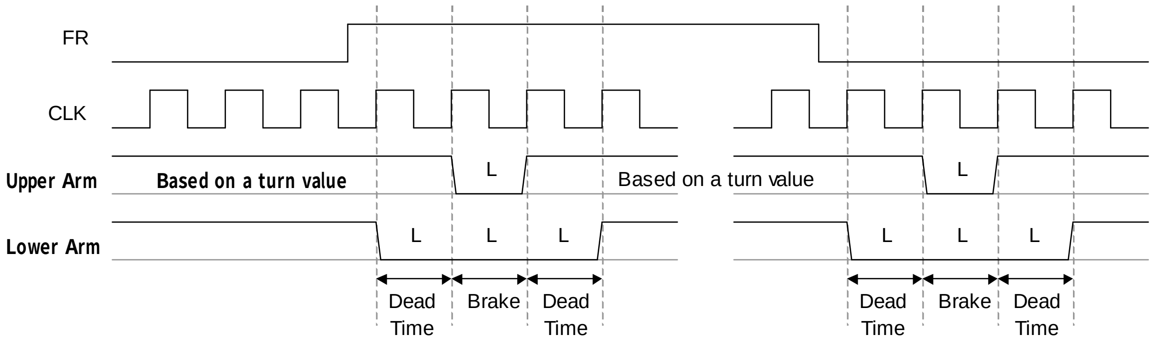
The upper arm output is different from the lower arm output, and the output interrupter switch is not built in.

You should consider gate output series resistor value in the range from 100Ω to 1,000Ω as with the lower arm.

And you should set pull-up resistor that ensures sufficient VGS.

3. Forward / Reverse Function Switching (FR Pin)

It is the pin that a motor forward / reverse function switching. It can switch the phase excitation sequence by the FR input logic. As a result, the direction where the motor is rotated can be switched. The sequence at the time of a motor rotation switching is shown below and the internal oscillator controls it. In addition, an internal oscillator is fixed with 18kHz, and becomes operation of normal rotation reversal at the 4th clock.



4. FG Output (FG Pin)

It is the pin that outputs the pulse at the cycle proportional to the rotation of a motor. This pin is open-drain output of 7V absolute maximum rating. This pin should be pull-up with resistor to power supply that is 5V or more.

This pin should be pull-up with resistor to power supply that is 5V or more. Do not connect this pin to power supply (VCC) or power supply for motor (VMM).

Technical Information

5. Oscillation Block (VERR, OSC Pin)

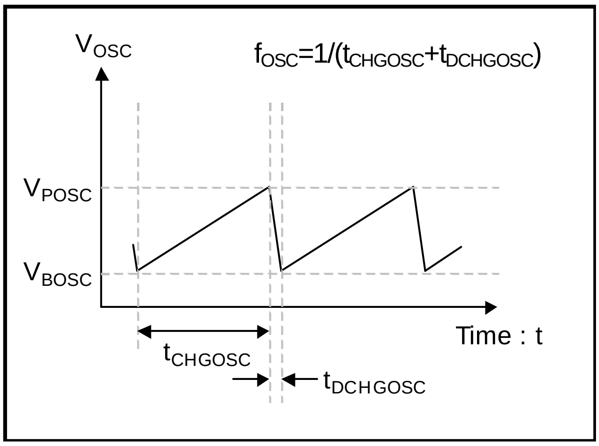
The PWM function is successively compared the DC voltage (V_{VERR}) that is input to the VERR and the triangular wave (sawtooth wave) voltage (V_{OSC}) generated from C_{OSC} connected with OSC.

As a result, the lower arm output is turned on at V_{VERR}>V_{OSC}.

The PWM frequency (f_{OSC}) is determined by the following elements that are charging/discharging to C_{OSC}. :

The triangular wave peak voltage (V_{POSC}), the bottom voltage (V_{BOSC}), the charge current (I_{CHGOSC}), and the discharge current (I_{DCHGOS}). It is possible to approximate from the relation of $I_{CHGOSC} \ll I_{DCHGOSC}$ by the following formula.

The C_{OSC} recommended value is from 330pF to 2200pF.

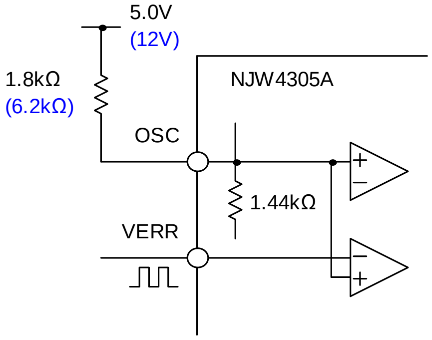


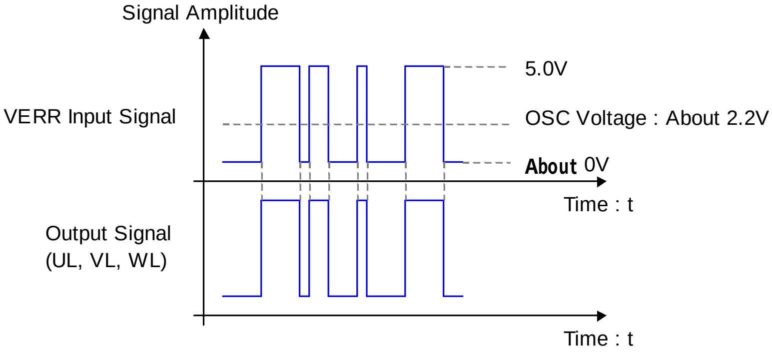
ITEM	SYMBOL	FORMULA
Oscillation Frequency	f_{OSC}	$f_{OSC} \cong 35 \times 10^6 / C_{OSC}$

It is possible to use the direct PWM input that inputs duty controlled logic signal to VERR, and chopping driving the lower arm output. In this case, it should be biased to the OSC pin voltage with approx 2V (between 1V and 3V).
In case of the ON duty is light at the time of the PWM signal is input to the VERR pin, the switching (power) device saturation and/or the ON resistance reduction might become insufficient. As the result, the switching device might cause unexpected heat.
You should confirm that external power device ASO having sufficient margin to your application.

Ex.: In cases of VERR=2.2V Fixed setting

When the pull-up voltage is 5V, it should be pulled-up to approx 1.8kΩ.
When the pull-up voltage is 12V, it should be pulled-up to approx 6.2kΩ.
The output ON is when VERR is 2.2V or more.



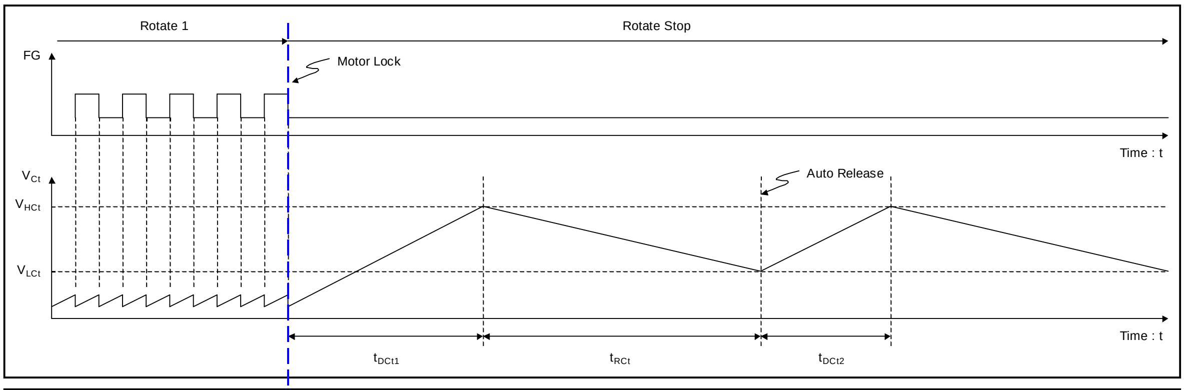


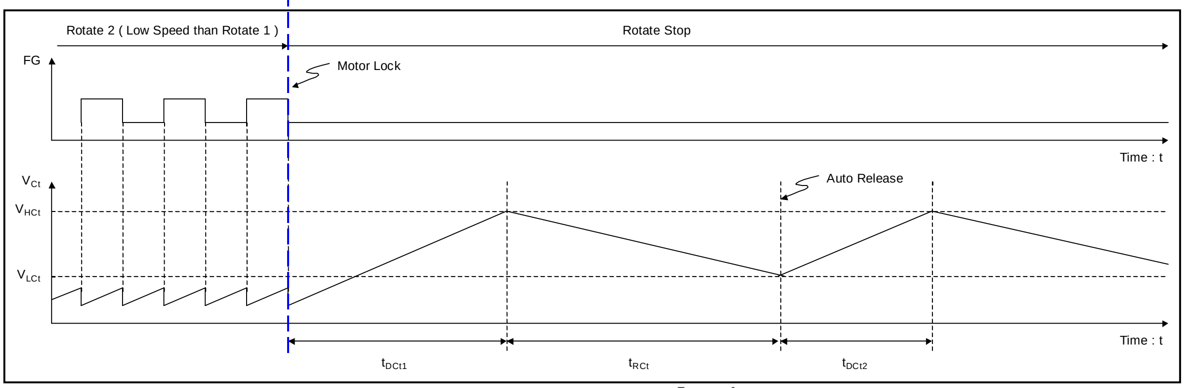
Technical Information

6. Lock Protection Circuit / Lock Protection Locked Time, Lock Protection Release Time (C_t Pin)

This pin is the setting pin for Lock Protection Time. It connects to capacitor (C_{Ct}).
Under normal conditions the Ct pin feeds charge current (I_{CHGCt}) through C_{Ct}. However, while the motor rotation the Ct is fast discharging C_{Ct} according to the edge timing of the FG signal. Therefore, the minute shape saw-tooth waveform appears as shown in the following figure at Ct pin. This Ct pin voltage V_{Ct} is approx 0V.
When the hall signal is stopped after the motor locked, the fast discharge is lost and V_{Ct} rises gradually. When the V_{Ct} reaches lock protection H level voltage (V_{HCt}), the low-side output (WL, VL, UL) becomes turned off (lock protection).
The lock protection locked time (t_{DCt1}) is defined the following: the time from the I_{CHGCt} charge start time to the output OFF.
When the V_{Ct} reaches the V_{HCt} once, the Ct pin is discharged by discharge current (I_{DCHGCt}), and the V_{Ct} pin voltage gradually comes down. The lock protection is released when V_{Ct} falls below lock protection L level voltage (V_{LCt}), and returns to normal output (auto release).
The lock protection release time (t_{RCt}) is defined the following: the time from the C_{Ct} discharge start time to the output OFF is released. Even if output OFF is released, CCt begins the charging again when the hall signal is not input with the motor locked. As a result, when V_{Ct} exceeds V_{HCt}, it becomes output OFF.
The lock protection re-locked time (t_{DCt2}) is defined the following: the time of until lock protection is re-operating.
It is attention that the definition is different from the lock protection locked time (tDCt1).
After that, the lock protection and an auto release are repeated for every t_{RCt} and t_{DCt2} until FG signal is generated.
The $t_{DCt1}/t_{DCt2}/t_{RCt}$ can be calculated by the following formulas. You should consider the C_{Ct} in the range of 0.1µF to 10µF.

ITEM	SYMBOL	FORMULA
Lock Protection Locked Time	t_{DCt1}	$t_{DCt} \cong V_{HCt} \times C_{Ct} / I_{CHGCt} = 0.523 \times 10^6 \times C_{Ct}$
Lock Protection Re-locked Time	t_{DCt2}	$t_{DCt1} \cong (V_{HCt}-V_{LCt}) \times C_{Ct} / I_{CHGCt} = 0.369 \times 10^6 \times C_{Ct}$
Lock Protection Release Time	t_{RCt}	$t_{RCt} \cong (V_{HCt}-V_{LCt}) \times C_{Ct} / I_{DCHGCt} = 3.69 \times 10^6 \times C_{Ct}$



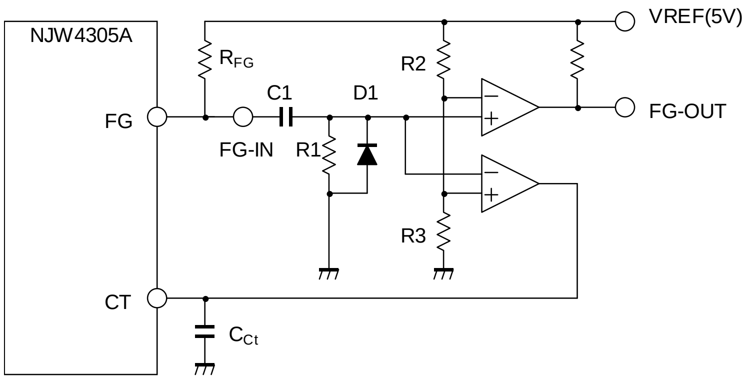


Technical Information

At the during rotation 1 in the left figure, V_{Ct} waveform becomes a sawtooth waveform of approx 0V as described above.
The during rotation 2 figure shows a case of slower status than at the during rotation 1 condition.
And it shows the saw tooth waveform peak rises.
When it is made extremely low-speed on the velocity changeable application etc., the FG signal edge timing might become long.
As a result, V_{Ct} might rise and the lock protection circuit malfunctions. To avoid the lock protection malfunction, you should consider Ct discharge circuit adding or value adjustment of Ct.
Moreover, when the Ct pin is connected to GND, this lock protection function is canceled.

< Low-speed Lock Protection Operation Avoidance Circuit >

It is Ct discharge circuit with the FG signal output. For example in the speed control application, the hall signals input timing becomes long at low speed time. Therefore, Ct voltage peak level rises and the lock protection circuit operates early.
The Vct rise is suppressed by extending the rapid discharge time of Cct with the differentiation circuit by C1 and R1 and the comparator.

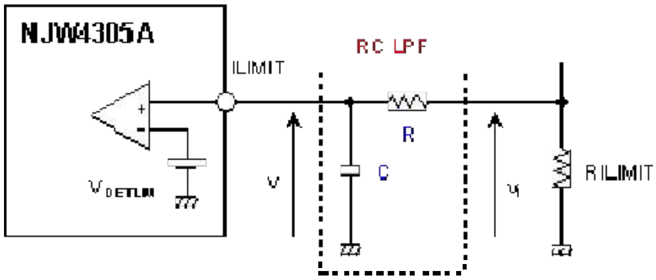


7. Over Current Detect Circuit (ILIMIT Pin)
When the voltage that exceeds the detection voltage V_{DETLIM}=0.28V typ. input to ILIMIT, all the lower arm output (UL, VL, WL) level is in “L” all. By flowing the resistor to match the source current of the lower arm of the external FET input to ILIMIT terminal voltages developed , and such a configuration can detect an overcurrent occurs in either r phase . ILIMIT will return as a trigger by local oscillator (typical frequency 18kHz) . This behavior is independent of the Hall signal, internal signal as rock protection and PWM signal from the VERR/OSC pins. If the speed of the motor is controlled by the duty signal input by external circuit to VERR, note that it can not output returns with the trigger by local oscillator , to stop the motor, therefore ILIMIT can be operated once.

Since not only the winding current of the motor ,spike current of the number 100ns about caused by the charging and discharging of the parasitic capacitance of the external FET flows , short surge pulses are frequently entered the ILIMIT to RILIMIT. When the behavior of the ILIMIT comparator reacts to short pulses of them, there is the PWM pulse missing, causing a reduction of torque and/or rotation speed of the motor.

By adding an RC low-pass filter to ILIMIT, it is possible to avoid the effects of such surge pulses.
The product of C and R, I set the output voltage V of the RC circuit does not exceed VDETLIM.
RC condition give the following:

$$R \cdot C > \frac{-t}{\ln\left(1 - \frac{V_{DETLIM}}{v_i}\right)}$$



Vi is the pulse voltage generated in the RILIMIT, t is the duration. ln means the natural logarithm.
In order to obtain the RC value, it is assigned to vi the amplitude of the surge pulse, t the duration and VDETLIM the target value with standard minimum and some margin in this equation. Adjust R and C as appropriate while cheking the actual equipment.

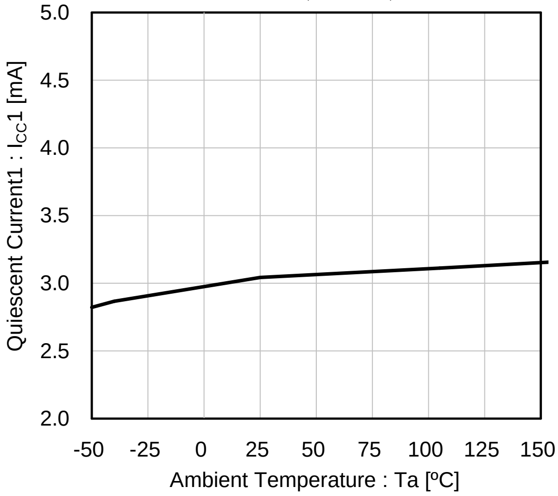
Example: VDETLIM = 0.22 [V] minimum standard and 0.03[V] margin, vi = 1 [V], for t = 1 [μs]
Ans.: RC>4.02E-6 It is available in a combination such as R=4.3kohm, C=1nF.

* Constant setting of other

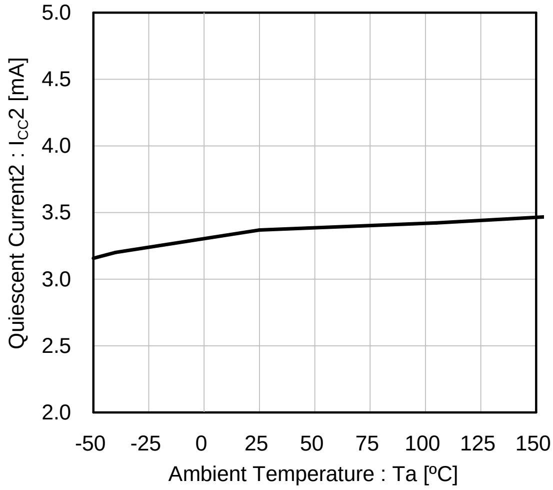
<Filter capacitor of the power supply>
In order to reduce the influence to the Hall bias current, be installed capacitors C1 and C2 suppress variations i In VDD near the Hall bias resistors.
C3 and C4 capacitors to suppress the fluctuation of the VMM by the motor winding current are also in consideration of the current loop, the wiring length to GND and the VMM do not be long carelessly.

■ ELECTRICAL CHARACTERISTICS EXAMPLES

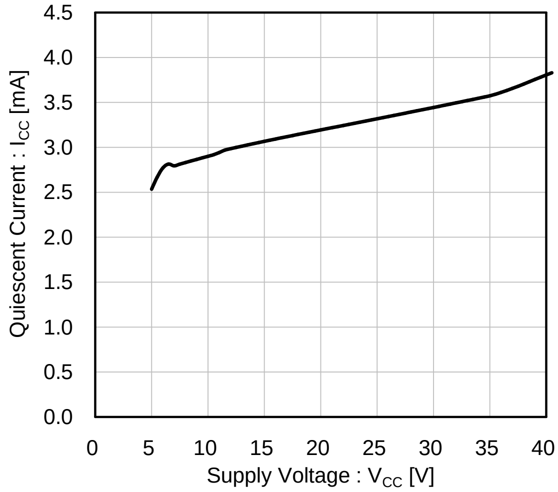
< GENERAL >
Quiescent Current1 vs. Ambient Temperature
V_{CC}=12V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



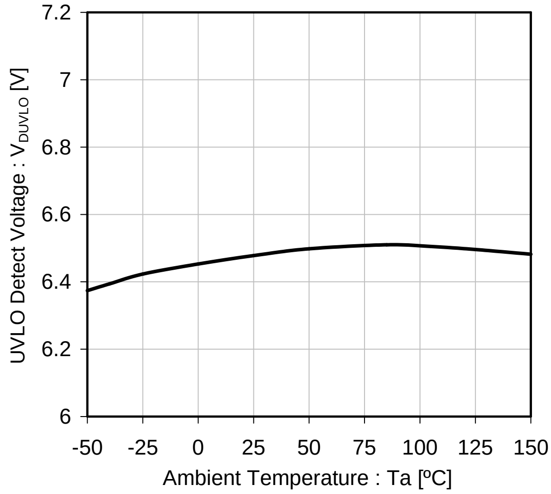
< GENERAL >
Quiescent Current1 vs. Ambient Temperature
V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



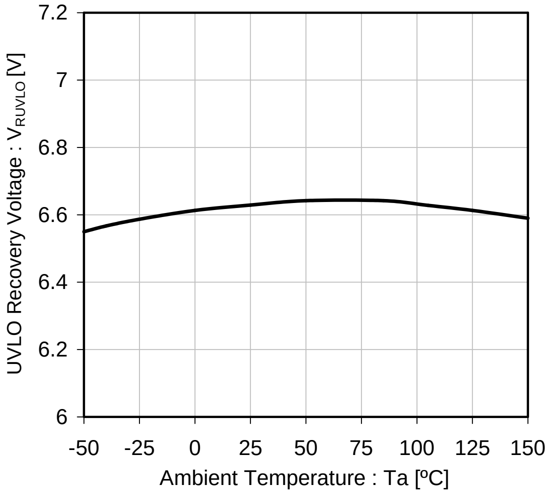
< GENERAL >
Quiescent Current vs. Supply Voltage
Ta=25ºC, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



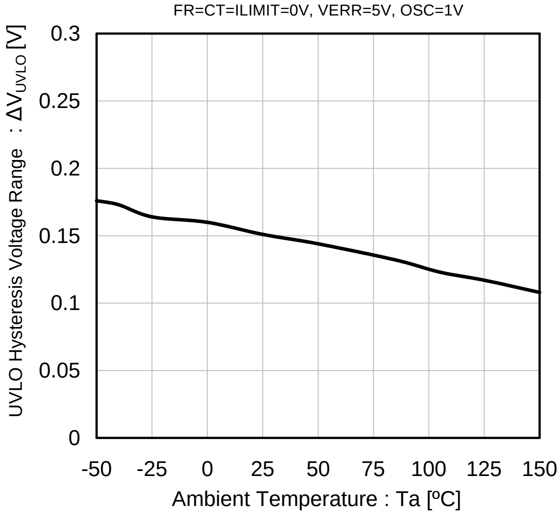
< UNDER VOLTAGE LOCK OUT BLOCK >
UVLO Detect Voltage vs. Ambient Temperature
V_{CC} Decreasing, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



< UNDER VOLTAGE LOCK OUT BLOCK >
UVLO Recovery Voltage vs. Ambient Temperature
V_{CC} Increasing, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V

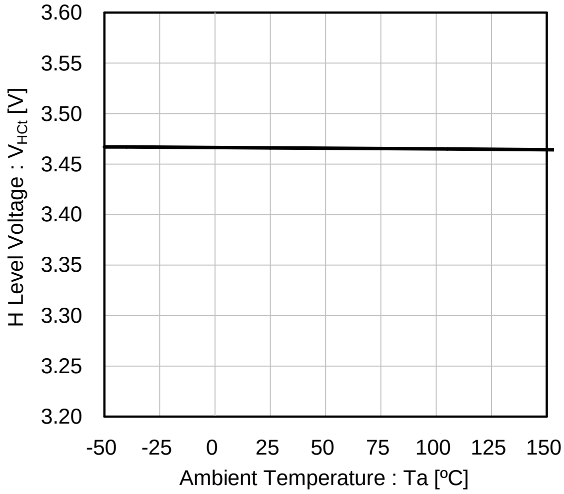


< UNDER VOLTAGE LOCK OUT BLOCK >
UVLO Hysteresis Voltage Range vs. Ambient Temperature
V_{CC} =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V

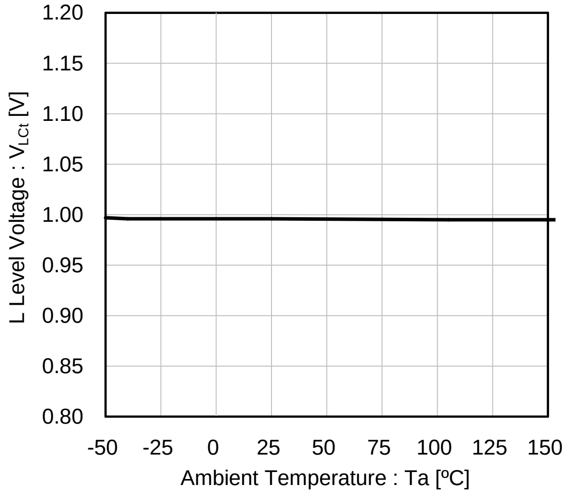


■ ELECTRICAL CHARACTERISTICS EXAMPLES

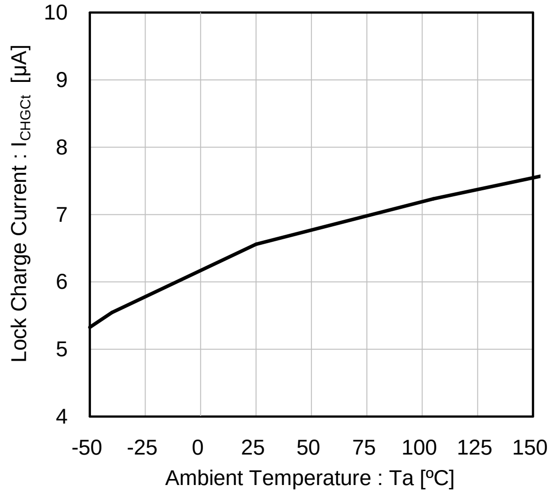
< LOCK DETECT BLOCK >
H Level Voltage vs. Ambient Temperature
V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=ILIMIT=0V, VERR=5V, OSC=1V



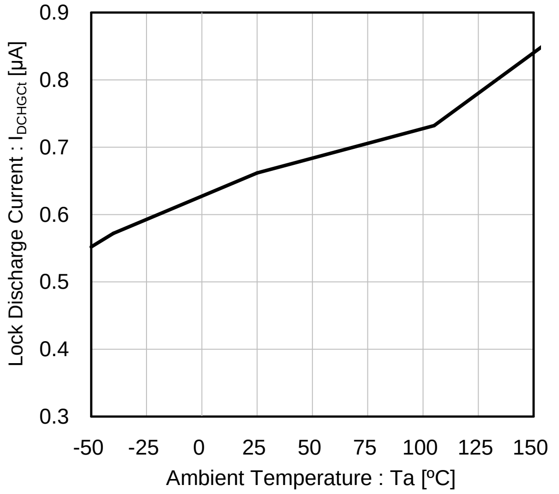
< LOCK DETECT BLOCK >
L Level Voltage vs. Ambient Temperature
V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=ILIMIT=0V, VERR=5V, OSC=1V



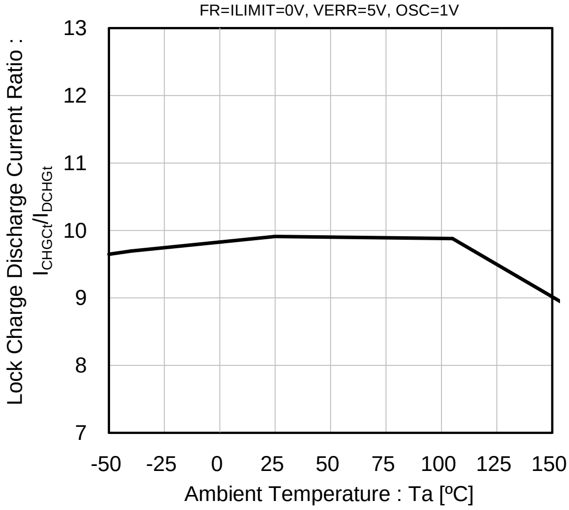
< LOCK DETECT BLOCK >
Lock Charge Current vs. Ambient Temperature
VCt=0V→2.5V, V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=ILIMIT=0V, VERR=5V, OSC=1V



< LOCK DETECT BLOCK >
Lock Discharge Current vs. Ambient Temperature
VCt=3.8V→2.5V,V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=ILIMIT=0V, VERR=5V, OSC=1V

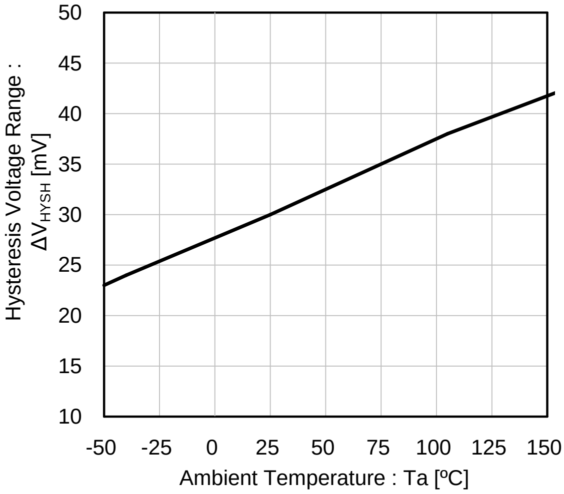


< LOCK DETECT BLOCK >
Lock Charge Discharge Current Ratio vs. Ambient Temperature
V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V,
FR=ILIMIT=0V, VERR=5V, OSC=1V

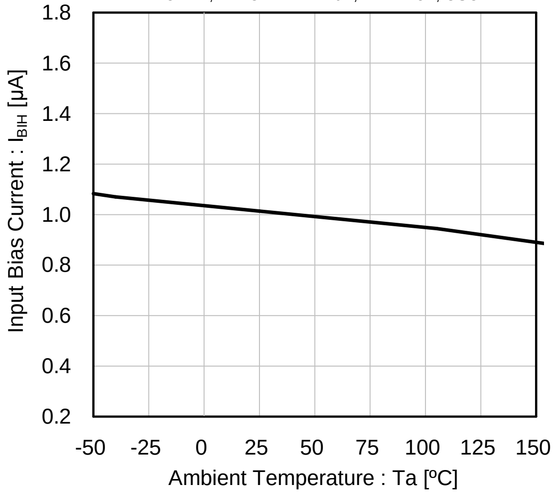


■ ELECTRICAL CHARACTERISTICS EXAMPLES

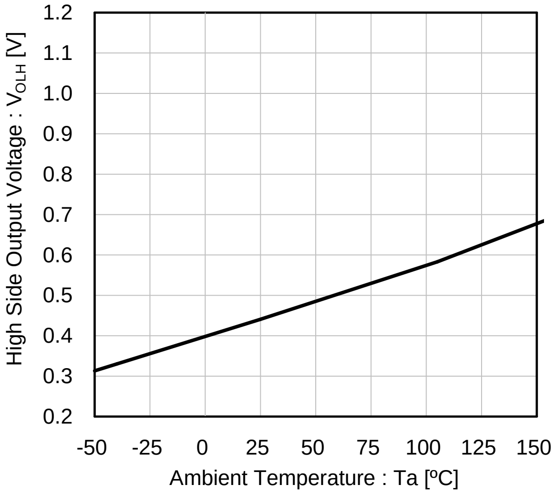
< HALL AMP BLOCK >
Hysteresis Voltage Range vs. Ambient Temperature
MEAS:VH1+, VCC=24V, H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



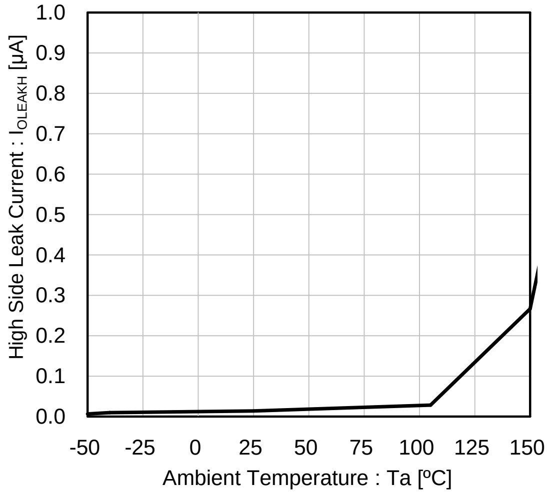
< HALL AMP BLOCK >
Input Bias Current vs. Ambient Temperature
H1+=1V, H1-=3V, MEAS:IH1+, VCC=24V, H3+=3V, H2+=1V, H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



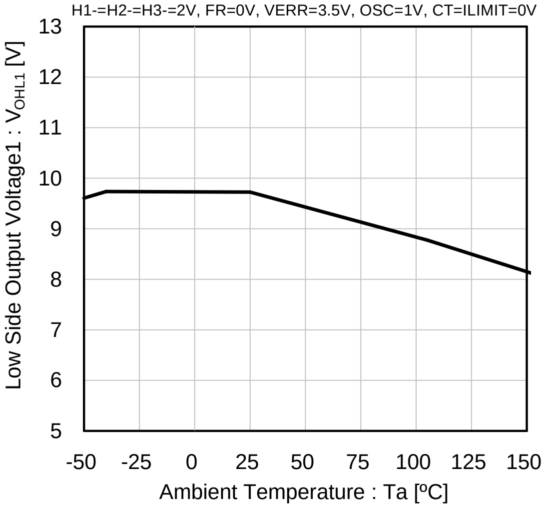
< HIGH SIDE OUTPUT BLOCK >
High Side Output Voltage vs. Ambient Temperature
H1+=H3+=1V, H2+=3V, UH=50mA, MEAS:VUH, V_{CC}=24V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



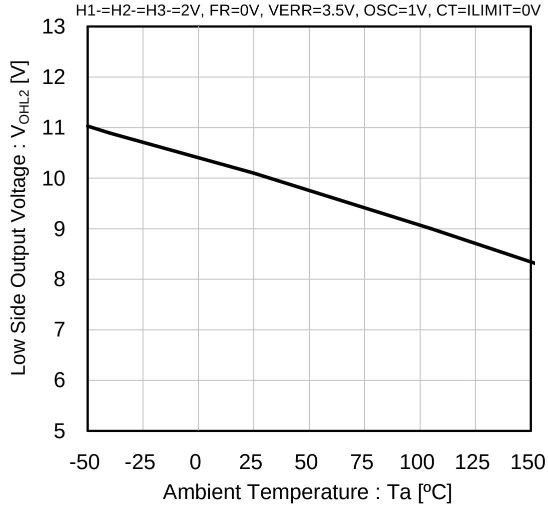
< HIGH SIDE OUTPUT BLOCK >
High Side Leak Current vs. Ambient Temperature
UH=36V, MEAS:IUH, V_{CC}=24V, H1+=H2+=H3+=3V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



< LOW SIDE OUTPUT BLOCK >
Low Side Output Voltage1 vs. Ambient Temperature
V_{CC}=12V, UL=-50mA, MEAS: VUL, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=0V, VERR=3.5V, OSC=1V, CT=ILIMIT=0V

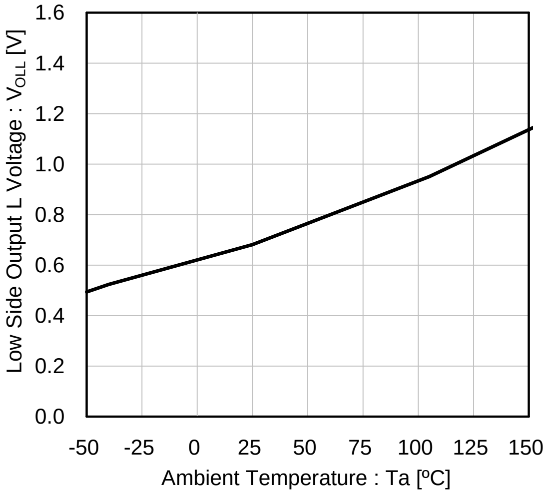


< LOW SIDE OUTPUT BLOCK >
Low Side Output Voltage vs. Ambient Temperature
V_{CC}=24V, UL=-50mA, MEAS: VUL, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=0V, VERR=3.5V, OSC=1V, CT=ILIMIT=0V

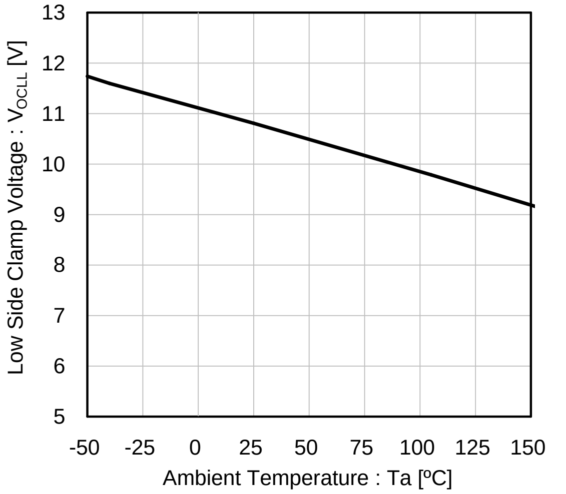


■ ELECTRICAL CHARACTERISTICS EXAMPLES

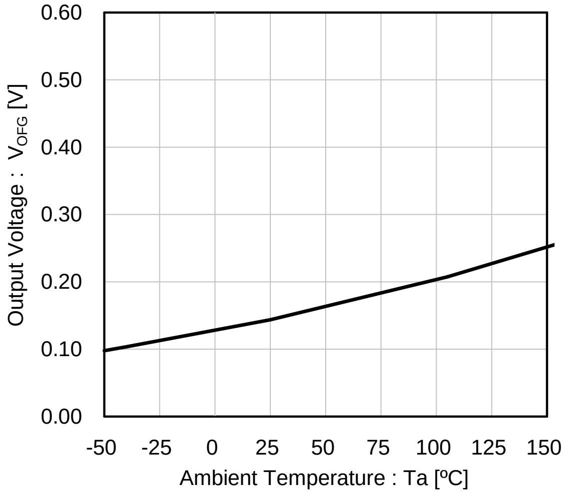
< LOW SIDE OUTPUT BLOCK >
Low Side Output L Voltage vs. Ambient Temperature
V_{CC}=24V, H1+=1V, H2+=H3+=3V, UL=150mA, MEAS:VUL,
H1-=H2-=H3-=2V, FR=0V, VERR=5V, OSC=1V, CT=ILIMIT=0V



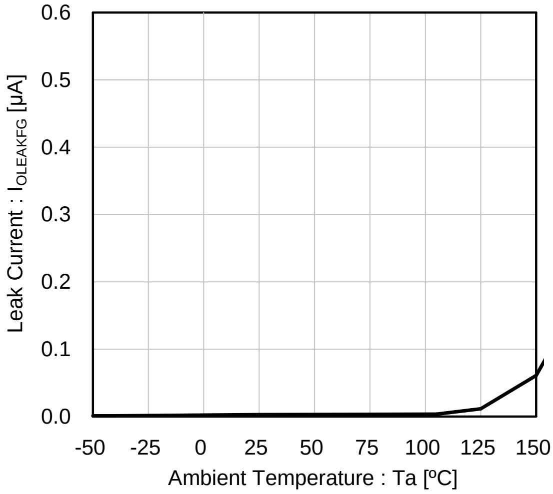
< LOW SIDE OUTPUT BLOCK >
Low Side Clamp Voltage vs. Ambient Temperature
V_{CC}=36V, UL=-0.1mA, MEAS:VUL, IH1+=H3+=3V, H2+=1V,
H1-=H2-=H3-=2V, FR=0V, VERR=3.5V, OSC=1V, CT=ILIMIT=0V



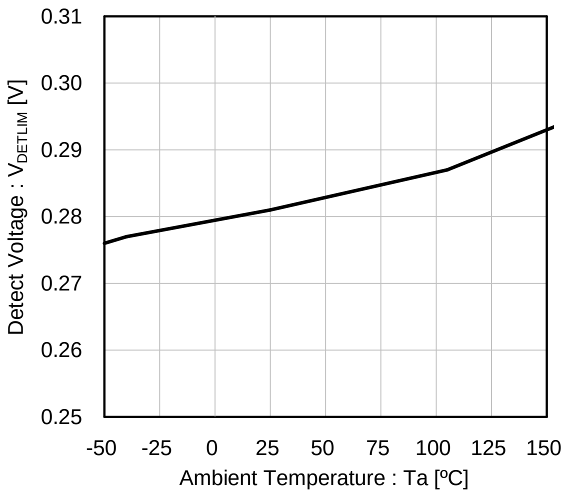
< FG OUTPUT BLOCK >
Output Voltage vs. Ambient Temperature
FG=10mA, V_{CC}=24V, H1+=H2+=H3+=3V, H1-=H2-=H3-=2V,
FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



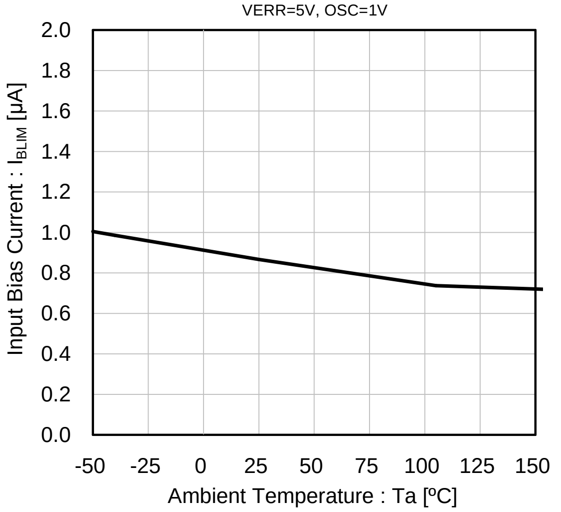
< FG OUTPUT BLOCK >
Leak Current vs. Ambient Temperature
H1+=1V, FG=5V, V_{CC}=24V, H2+=H3+=3V, UL=150mA,
H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=1V



< OVER CURRENT DETECT BLOCK >
Detect Voltage vs. Ambient Temperature
V_{CC}=24V, H1+=H2+=H3+=3V, H1-=H2-=H3-=2V,
FR=CT=0V, VERR=5V, OSC=1V

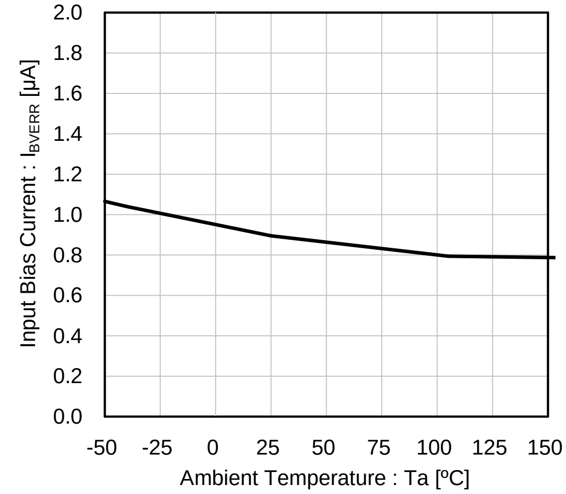


< OVER CURRENT DETECT BLOCK >
Input Bias Current vs. Ambient Temperature
V_{CC}=24V, H1+=H2+=H3+=3V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V,
VERR=5V, OSC=1V

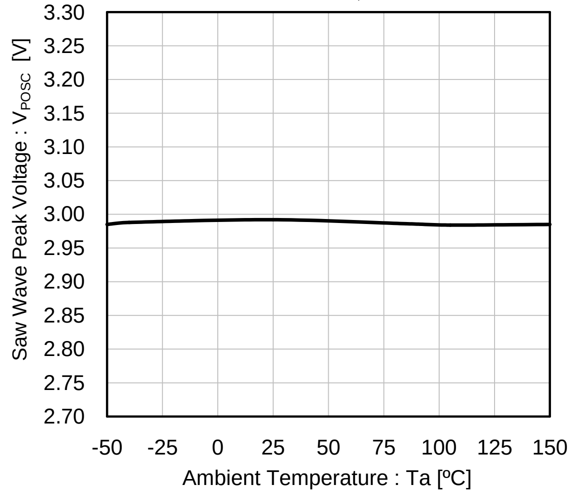


■ ELECTRICAL CHARACTERISTICS EXAMPLES

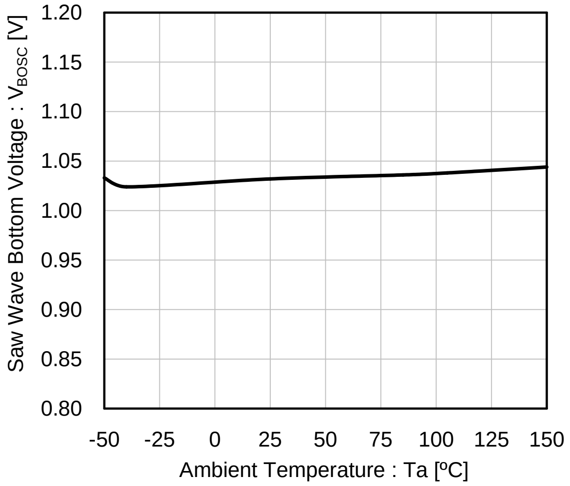
< ERROR AMP BLOCK >
Input Bias Current vs. Ambient Temperature
VERR=0V, V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, OSC=1V



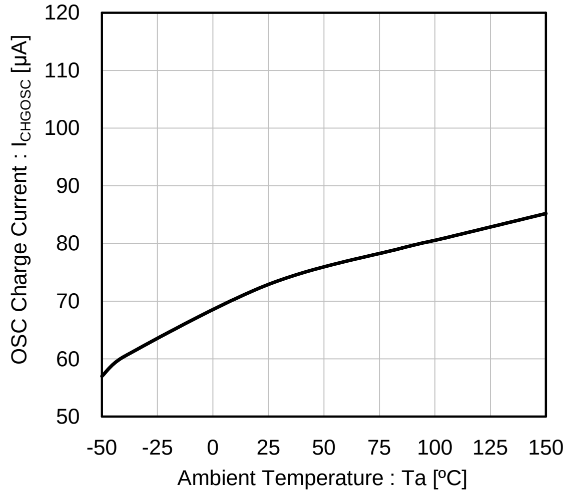
< OSCILLATOR BLOCK >
Saw Wave Peak Voltage vs. Ambient Temperature
V_{CC} =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V



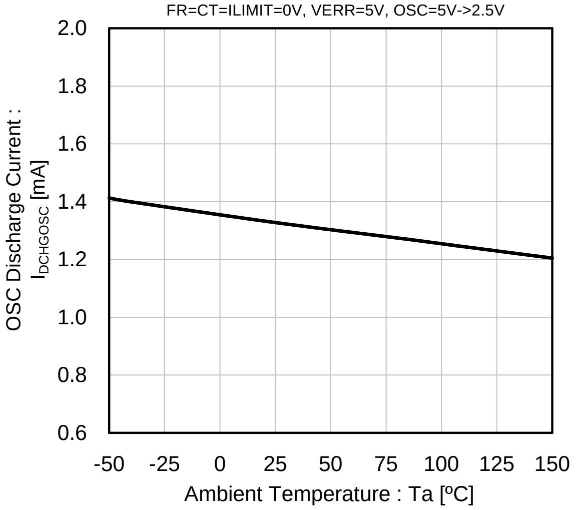
< OSCILLATOR BLOCK >
Saw Wave Bottom Voltage vs. Ambient Temperature
V_{CC} =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V



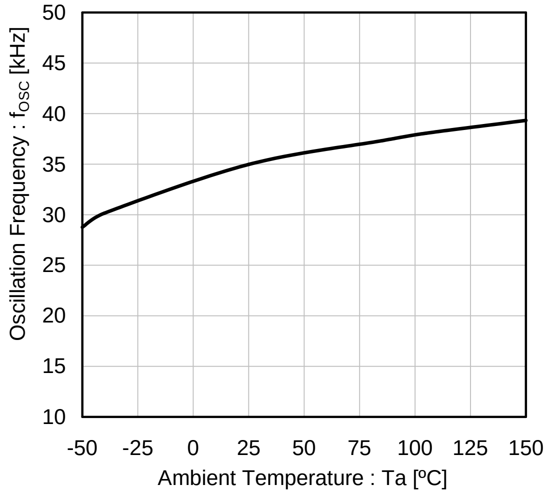
< OSCILLATOR BLOCK >
OSC Charge Current vs. Ambient Temperature
V_{CC} =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=0V->2.5V



< OSCILLATOR BLOCK >
OSC Discharge Current vs. Ambient Temperature
VCC =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V, OSC=5V->2.5V

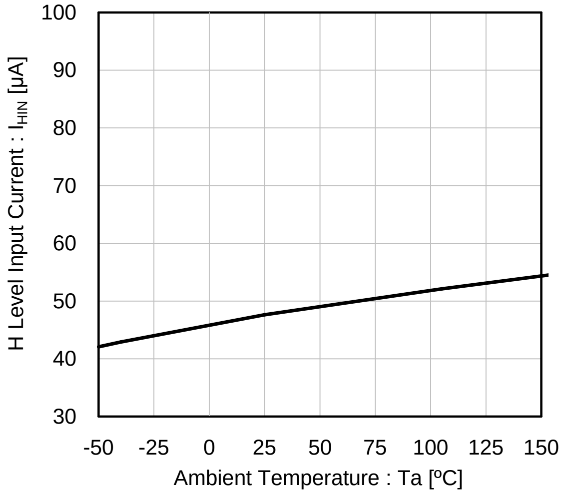


< OSCILLATOR BLOCK >
Oscillation Frequency vs. Ambient Temperature
Cosc=1000pF, V_{CC} =24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, FR=CT=ILIMIT=0V, VERR=5V

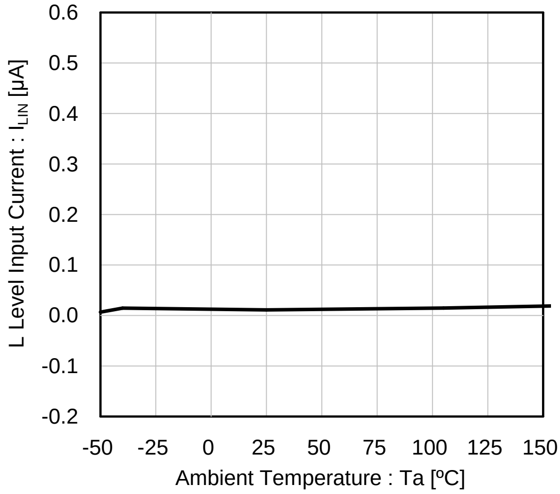


■ ELECTRICAL CHARACTERISTICS EXAMPLES

< CONTROL INPUT BLOCK >
H Level Input Current vs. Ambient Temperature
FR=5V, V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, CT=ILIMIT=0V, VERR=5V, OSC=1V



< CONTROL INPUT BLOCK >
L Level Input Current vs. Ambient Temperature
FR=0V, V_{CC}=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, CT=ILIMIT=0V, VERR=5V, OSC=1V



< CONTROL INPUT BLOCK >
Pull Down Resistance vs. Ambient Temperature
FR=5V, VCC=24V, H1+=H3+=3V, H2+=1V, H1-=H2-=H3-=2V, CT=ILIMIT=0V, VERR=5V, OSC=1V