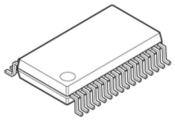
PULSE INPUT STEPPER MOTOR DRIVER

■ GENERAL DESCRIPTION

The NJW4372 is a high efficiency bipolar drive stepper motor driver IC, which controls steps and direction by simple input pulse train. DMOS H bridge outputs realize high efficiency, low heat motor application. The control circuit is optimized for logic power supplies and interfaces. Therefore it corresponds to plural kind of logic voltages such as 5.0V and 3.3V.

The NJW4372 has PWM constant current circuits, a Torque Select function, an Enable function and a Brake function. These easy and convenient functions make NJW4372 suitable for various applications.

■ PACKAGE OUTLINE

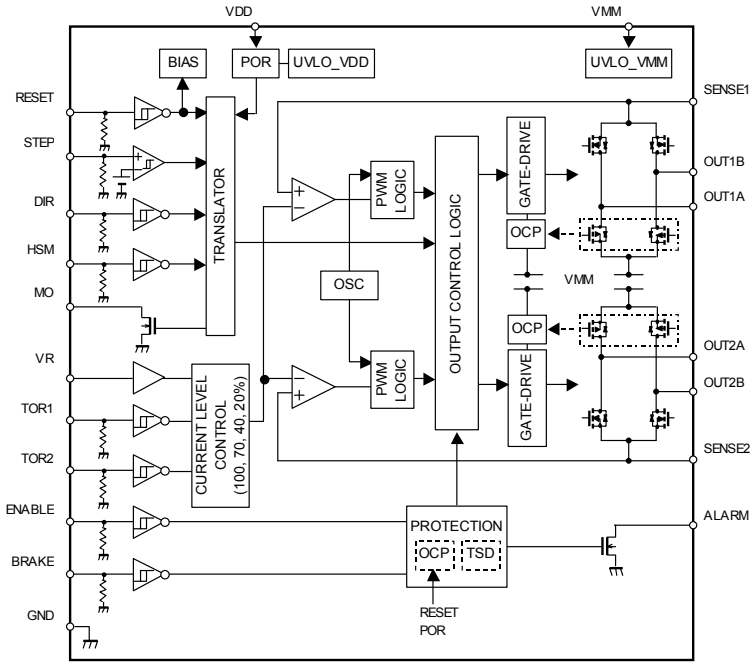


NJW4372V

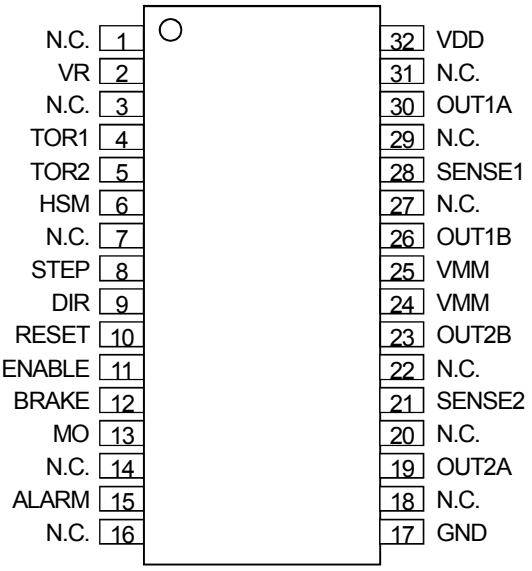
■ FEATURES

- Logic Supply Voltage V_{DD}=2.7V to 5.5V
- Motor Supply Voltage V_{MM}=9V to 36V
- Output Current Io=500mA typ.
- Low ON Resistance Output $R_{O(H+L)}$ = 0.8Ω typ.
- Low Quiescent Current I_{DD}=0.75mA typ. / I_{MM}=1.65mA typ.
- STEP&DIR (pulse train) Input Control
- TTL Compatible Input
- Constant Current Control
- Maximum Current Select (Torque Select) Function
- Step Mode (Full / Half step) Select, ENABLE, RESET Function
- BRAKE (High side outputs turn on) Function
- MO, ALARM Output Function
- Protection Circuit OCP, UVLO, TSD
- BCD Technology
- Package SSOP32

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



SSOP32

■ PIN DESCRIPTION

PIN No. SSOP32	PIN NAME	I/O	FUNCTION	NOTES
1,3,7,14,16,18 20,22,27,29,31	N.C.	-	No Connection	Not Internally Connected
2	VR	I	Reference Voltage Input Pin	It connects to an arbitrary reference voltage for setting maximum output current.
4	TOR1	I	Maximum Output Current Setting Pin 1/ 2	Output current setting by combination with TOR1/ 2. TOR1/2: H/H=20%, L/H=40%, H/L=70%, L/L=100%
5	TOR2			
6	HSM	I	Full/ Half Step Mode Setting Pin	L=Full step mode, H=Half step mode
8	STEP	I	Stepping Pulse Input Pin	Input pin of rotation control Translator is triggered by positive edge of STEP Pulse.
9	DIR	I	Direction Setting Pin	L=Forward (CW), H=Reverse (CCW)
10	RESET	I	Reset Input Pin	L=Translator is initialized and outputs turn off. If OCP is operating, OCP is released. H=Normal Operation
11	ENABLE	I	Enable Input Pin	L=Outputs turn off, H=Normal Operation
12	BRAKE	I	Brake Input Pin	L=Normal Operation H=High side Outputs ON and Low side outputs OFF.
13	MO	O	MO Output Pin	When Translator is in initial sequence, the output is L.
15	ALARM	O	Alarm Output Pin	When the internal OCP or TSD operation is detected, the output is L.
17	GND	-	Logic Ground Pin	Logic Ground
19	OUT2A	O	2ch Output Pin A	-
21	SENSE2	I/O	Current Sensing Resistance Connection Pin 2	It connects to resistor for the current sensing of the 2ch side. At the unused time, it connects with GND.
23	OUT2B	O	2ch Output Pin B	-
24,25	VMM	-	Motor Voltage Supply Pin	Motor Voltage Supply (Both pins must be connected together externally on SSOP32.)
26	OUT1B	O	1ch Output Pin B	-
28	SENSE1	I/O	Current Sensing Resistance Connection Pin 1	It connects to resistor for the current sensing of the 1ch side. At the unused time, it connects with GND.
30	OUT1A	O	1ch Output Pin A	-
32	VDD	-	Logic Voltage Supply Pin	Logic Voltage Supply

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Logic Supply Pin Voltage	V_{DD}	6	V	VDD Pin
Motor Supply Pin Voltage	V_{MM}	40	V	VMM Pin
Output Pin Voltage	Vo	40	V	OUT1A ,OUT1B, OUT2A, OUT2B Pin
SENSE Pin Voltage	V_{SENSE}	6	V	SENSE1, SENSE2 Pin
Logic Input Pin Voltage	V_{IN}	6	V	STEP, DIR, HSM, RESET, ENABLE, BRAKE, TOR1, TOR2 Pin
		V_{DD}	V	VR Pin
ALARM Output Pin Voltage	V_{ALARM}	6	V	ALARM Pin
MO Output Pin Voltage	V_{MO}	6	V	MO Pin
Output Pin Current	I_O	800	mA	OUT1A ,OUT1B, OUT2A, OUT2B Pin
ALARM Output Pin Current	I_{ALARM}	20	mA	ALARM Pin
MO Output Pin Current	I_{MO}	20	mA	MO Pin
Operating Ambient Temperature	Topr	-40 to +85	°C	-
Junction Temperature	Tj	-40 to +150	°C	-
Storage Temperature	Tstg	-50 to +150	°C	-
Power Dissipation (SSOP32)	P_D	1135	mW	Mounted on 2Layers PCB (*1)
		1785	mW	Mounted on 4Layers PCB (*2)

(*1): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 2Layers)

(*2): Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 4Layers, Inner Cu area : 74.2×74.2mm)

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic Supply Pin Voltage	V_{DD}		2.7	-	5.5	V
Motor Supply Pin Voltage	V_{MM}		9	-	36	V

■ PIN OPERATING CONDITIONS

(V_{DD}=3.3V/5.0V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
■ Input Pin 1 (STEP Pin)						
H Level Input Voltage	V_{IH}		2.0	-	V_{DD}	V
L Level Input Voltage	V_{IL}		0	-	0.8	V
Input Pulse Width	tp		2	-	-	μs
■ Input Pin 2 (DIR, HSM, RESET, ENABLE, BRAKE, TOR1, TOR2 Pin)						
H Level Input Voltage 1	V_{IH1}	V_{DD}=5.0V	2.4	-	V_{DD}	V
H Level Input Voltage 2	V_{IH2}	V_{DD}=3.3V	2.0	-	V_{DD}	V
L Level Input Voltage	V_{IL}		0	-	0.8	V
Data Setup Time	t_{DS}	Except TOR1, TOR2	1	-	-	μs
Data Hold Time	t_{DH}	Except TOR1, TOR2	1	-	-	μs
■ Input Pin 3 (VR Pin)						
VR Pin Voltage	V_{VR}		1	-	V_{DD}	V
■ Output Pin (OUT1A, OUT1B, OUT2A, OUT2B, MO, ALARM Pin)						
Output Pin Voltage	V_O		-	-	36	V
ALARM Output Pin Voltage	V_{ALARM}		0	-	5.5	V
MO Output Pin Voltage	V_{MO}		0	-	5.5	V
■ SENSE Pin (SENSE1, SENSE2 Pin)						
SENSE Pin Voltage	V_{SENSE}		-	-	1	V

■ **ELECTRICAL CHARACTERISTICS** (V_{MM}=24V, V_{DD}/V_{IN}=5.0V, TOR1/TOR2=0V, R_{MO}=5kΩ, R_{ALARM}=5kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
■ GENERAL						
Logic Block Quiescent Current	I_{DD}	Except I_{IH}	-	0.75	1.5	mA
Motor Block Quiescent Current	I_{MM}		-	1.65	3.0	mA
■ INPUT BLOCK 1 (STEP Pin)						
Input Hysteresis Voltage 1	V_{IHYS1}		-	0.5	-	V
Input Hysteresis Voltage 2	V_{IHYS2}	V_{DD}=3.3V	-	0.45	-	V
H Level Input Current	I_{IH}	V_{IN}=5.0V	25	50	100	μA
L Level Input Current	I_{IL}	V_{IN}=0V	-	1.6	5	μA
Input Pull Down Resistance	R_{IN}		-	100	-	kΩ
■ INPUT BLOCK 2 (DIR, HSM, RESET, ENABLE, BRAKE, TOR1, TOR2 Pin)						
Input Hysteresis Voltage 1	V_{IHYS1}		-	0.25	-	V
Input Hysteresis Voltage 2	V_{IHYS2}	V_{DD}=3.3V	-	0.2	-	V
H Level Input Current	I_{IH}	V_{IN}=5.0V, per 1 input	25	50	100	μA
L Level Input Current	I_{IL}	V_{IN}=0V, per 1 input	-200	0	+200	nA
Input Pull Down Resistance	R_{IN}		-	100	-	kΩ
■ INPUT BLOCK 3 (VR Pin)						
Input Current	I_{IN}		-200	0	+200	nA
■ MOTOR OUTPUT BLOCK (OUT1A, OUT1B, OUT2A, OUT2B Pin)						
High Side Output ON Resistance	R_{OH}	Io=500mA	-	0.4	0.6	Ω
Low Side Output ON Resistance	R_{OL}	Io=500mA	-	0.4	0.6	Ω
R_{OH} Temperature Coefficient	$\Delta R_{OH}/\Delta Tj$	Io=500mA, Tj=-40°C to 150°C	-	1.7	-	mΩ/°C
R_{OL} Temperature Coefficient	$\Delta R_{OL}/\Delta Tj$	Io=500mA, Tj=-40°C to 150°C	-	1.8	-	mΩ/°C
High Side Leak Current	I_{OLEAKH}	ENABLE=0V, V_{MM}=36V, Vo=0V	-	-	1	μA
Low Side Leak Current	I_{OLEAKL}	ENABLE=0V, V_{MM}=36V, Vo=36V	-	-	1	μA
High Side Reverse Voltage	V_{ORH}	Io=-500mA	-	0.85	-	V
Low Side Reverse Voltage	V_{ORL}	Io=-500mA	-	0.85	-	V
Dead Time	t_{DEAD}		-	500	-	ns
Delay Time	t_{DELAY}		-	600	-	ns
OCP Detection Current	I_{OCP}	(*3)	1.5	2	-	A
OCP Delay Time	t_{OCP}	Except tb, (*3)	-	200	-	ns
■ SENSE BLOCK (SENSE1, SENSE2 Pin)						
Sense Pin Leak Current	$I_{LEAKSENSE}$	ENABLE=0V	-120	-80	-	μA
■ MO OUTPUT (MO Pin)						
L Level Output Voltage	V_{MO}	I_{MO}=10mA	-	0.15	0.3	V
MO Pin Leak Current	I_{LEAKMO}	V_{MO}=5.5V	-	-	1	μA
■ ALARM BLOCK (ALARM Pin)						
L Level Output Voltage	V_{ALARM}	I_{ALARM}=10mA	-	0.15	0.3	V
ALARM Pin Leak Current	$I_{LEAKALARM}$	V_{ALARM}=5.5V	-	-	1	μA
■ CHOPPER OSCILLATOR BLOCK						
OSC Frequency 1	f_{S1}		40	50	60	kHz
OSC Frequency 2	f_{S2}	V_{DD}=3.3V	20	31	42	kHz
Blanking Time	tb		-	1.2	-	μs

(*3): OCP function is available when V_{DD} is in Recommended Operating Voltage.

(Please consider having a sufficient tolerance to transitional voltage change between V_{DD} pin and GND pin.)

■ ELECTRICAL CHARACTERISTICS

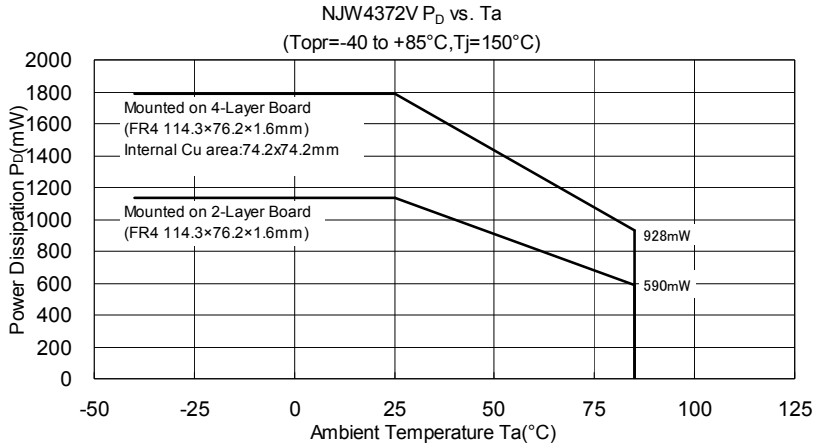
(V_{MM}=24V, V_{DD}/V_{IN}=5.0V, TOR1/TOR2=0V, R_{MO}=5kΩ, R_{ALARM}=5kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
■ CONSTANT CURRENT DETECTION BLOCK							
Detection Voltage 1 (100% Current Level)	V_{TOR1}	TOR1=L, TOR2=L		460	500	540	mV
			VR=3.3V	290	330	370	mV
Detection Voltage 2 (70% Current Level)	V_{TOR2}	TOR1=H, TOR2=L		310	350	390	mV
			VR=3.3V	191	231	271	mV
Detection Voltage 3 (40% Current Level)	V_{TOR3}	TOR1=L, TOR2=H		160	200	240	mV
			VR=3.3V	92	132	172	mV
Detection Voltage 4 (20% Current Level)	V_{TOR4}	TOR1=H, TOR2=H		60	100	140	mV
			VR=3.3V	26	66	106	mV
■ THERMAL SHUTDOWN BLOCK							
TSD Operating Temperature	T_{TSD1}			-	170	-	°C
TSD Recovery Temperature	T_{TSD2}			-	140	-	°C
TSD Hysteresis Temperature	ΔT_{TSD}			-	30	-	°C
■ UNDER VOLTAGE LOCK OUT BLOCK 1 (LOGIC BLOCK)							
UVLO Operating Voltage	V_{UVLO1}			1.7	2.0	2.3	V
UVLO Recovery Voltage	V_{UVLO2}			1.85	2.15	2.45	V
UVLO Hysteresis Voltage	ΔV_{UVLO}			0.05	0.15	0.3	V
■ UNDER VOLTAGE LOCK OUT BLOCK 2 (MOTOR BLOCK)							
UVLO Operating Voltage	V_{UVLO1}			6.5	7.0	7.5	V
UVLO Recovery Voltage	V_{UVLO2}			6.8	7.3	7.8	V
UVLO Hysteresis Voltage	ΔV_{UVLO}			0.2	0.3	0.4	V

■ THERMAL RESISTANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Junction - Ambient Thermal Resistance 1	θ_{ja_1}	Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 2Layers)	-	-	110	°C/W
Junction - Case Surface Thermal Resistance 1	Ψ_{jt_1}	Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 2Layers)	-	17	-	°C/W
Junction - Ambient Thermal Resistance 2	θ_{ja_2}	Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 4Layers, Inner Cu area : 74.2×74.2mm)	-	-	70	°C/W
Junction - Case Surface Thermal Resistance 2	Ψ_{jt_2}	Mounted on glass epoxy board based on EIA/JEDEC. (114.3×76.2×1.6mm, FR-4, 4Layers, Inner Cu area : 74.2×74.2mm)	-	8	-	°C/W

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ TRUTH TABLE

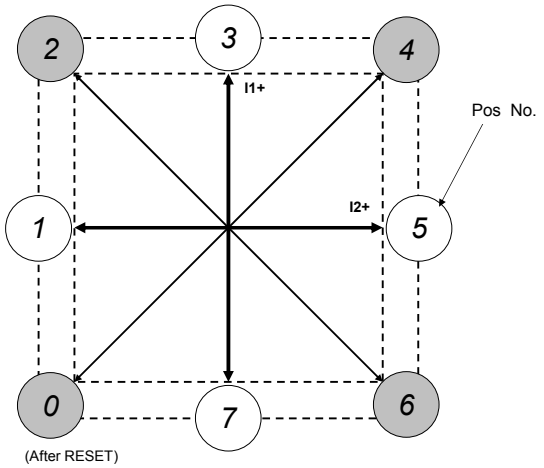
INPUT					OUTPUT	STATE	NOTES
RESET	ENABLE	BRAKE	HSM	DIR	ALARM		
H	H	L	H	H	H	Reverse(CCW), Half Step	Logical progress via STEP
			L			Reverse(CCW), Full Step	Logical progress via STEP
			H	L		Forward, Half Step	Logical progress via STEP
			L			Forward, Full Step	Logical progress via STEP
		H	H/L	H/L		Brake (High side Outputs ON + Low side Outputs OFF)	Logical progress via STEP
	L	H/L				Outputs OFF	Logical progress via STEP
L	H/L	H/L				Translator is initialized + Outputs OFF	OCP release in its operation
-	-	-	-	-	H	Outputs OFF in the event of UVLO_VDD or UVLO_VMM	If POR operated, Translator is initialized
-	-	-	-	-	L	Outputs OFF in the event of OCP or TSD	-

*OFF : HiZ state

*When the VDD voltage is less than 1.6V, POR may operate.
Using POR function by VDD voltage control for initialization is not recommended.

■ STEP SEQUENCE and ROTOR POSITION (Pos) SEQUENCE

STEP No.		Pos No.	I1	I2	NOTES
FULL	HALF				
0	0	0	-100%	-100%	After RESET
-	1	1	0%	-100%	
1	2	2	100%	-100%	
-	3	3	100%	0%	
2	4	4	100%	100%	
-	5	5	0%	100%	
3	6	6	-100%	100%	
-	7	7	-100%	0%	



FULL STEP, FORWARD SEQUENCE

STEP	After RESET	1	2	3	4
POS	0	2	4	6	0
OUT1A	L	H	H	L	L
OUT1B	H	L	L	H	H
OUT2A	L	L	H	H	L
OUT2B	H	H	L	L	H
MO	L	H	H	H	L

FULL STEP, REVERSE SEQUENCE

STEP	After RESET	1	2	3	4
POS	0	6	4	2	0
OUT1A	L	L	H	H	L
OUT1B	H	H	L	L	H
OUT2A	L	H	H	L	L
OUT2B	H	L	L	H	H
MO	L	H	H	H	L

HALF STEP, FORWARD SEQUENCE

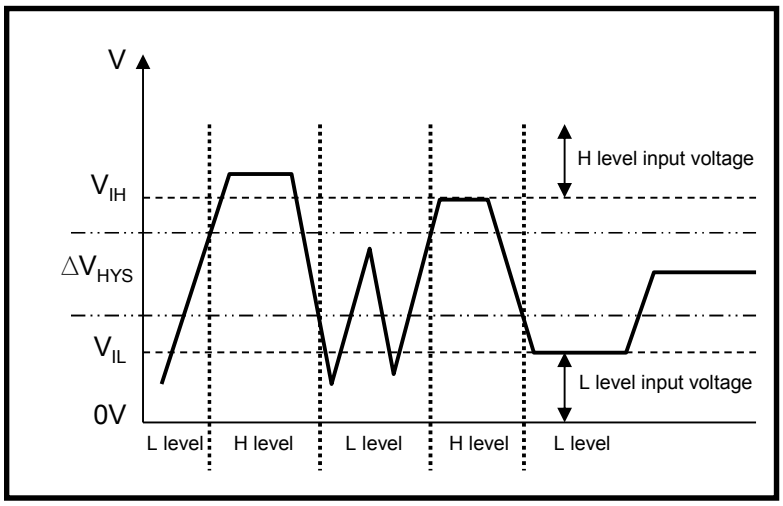
STEP	After RESET	1	2	3	4	5	6	7	8
POS	0	1	2	3	4	5	6	7	0
OUT1A	L	HiZ	H	H	H	HiZ	L	L	L
OUT1B	H	HiZ	L	L	L	HiZ	H	H	H
OUT2A	L	L	L	HiZ	H	H	H	HiZ	L
OUT2B	H	H	H	HiZ	L	L	L	HiZ	H
MO	L	H	H	H	H	H	H	H	L

HALF STEP, REVERSE SEQUENCE

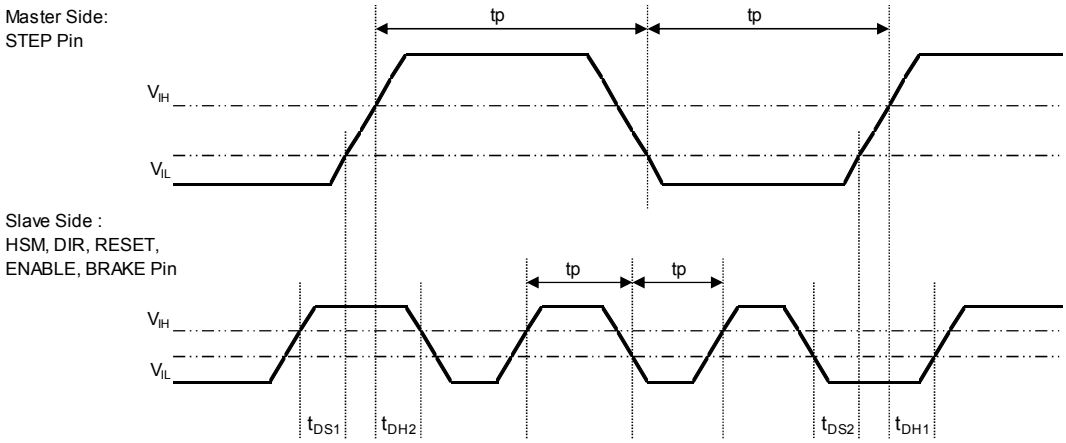
STEP	After RESET	1	2	3	4	5	6	7	8
POS	0	7	6	5	4	3	2	1	0
OUT1A	L	L	L	HiZ	H	H	H	HiZ	L
OUT1B	H	H	H	HiZ	L	L	L	HiZ	H
OUT2A	L	HiZ	H	H	H	HiZ	L	L	L
OUT2B	H	HiZ	L	L	L	HiZ	H	H	H
MO	L	H	H	H	H	H	H	H	L

■ OPERATIONAL DEFINITION (Pin and CIRCUIT)

▪ Logic Input Pin Voltage Definition



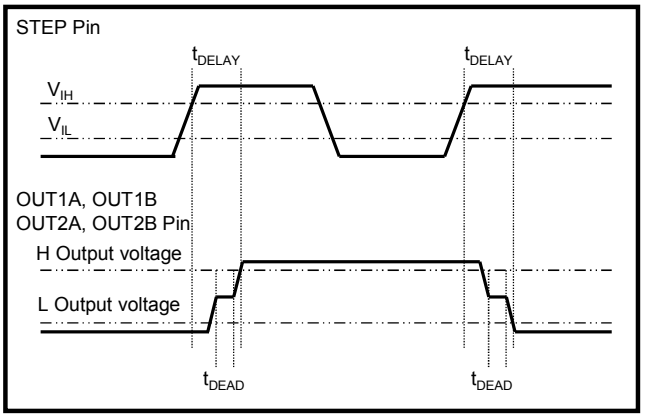
▪ Logic Input Pin Timing Definition



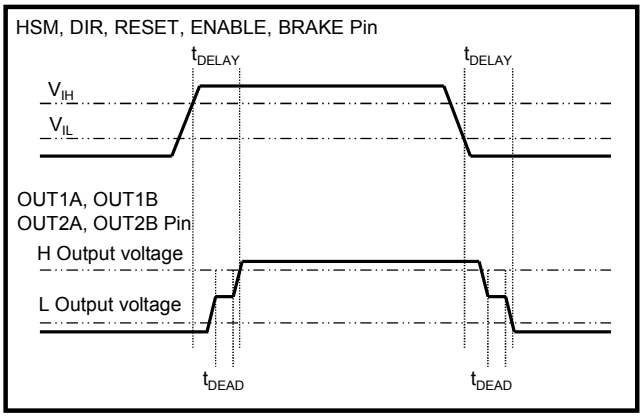
Data Setup Time (t_{DS1}, t_{DS2}) and Data Hold Time (t_{DH1}, t_{DH2}) defined on the positive edge of the STEP signal.
t_{DS1}, t_{DH1} applied to HSM, DIR, RESET and ENABLE Pins. t_{DS2}, t_{DH2} applied to HSM, DIR and BRAKE Pins.

▪ Input to Output Delay Timing Definition

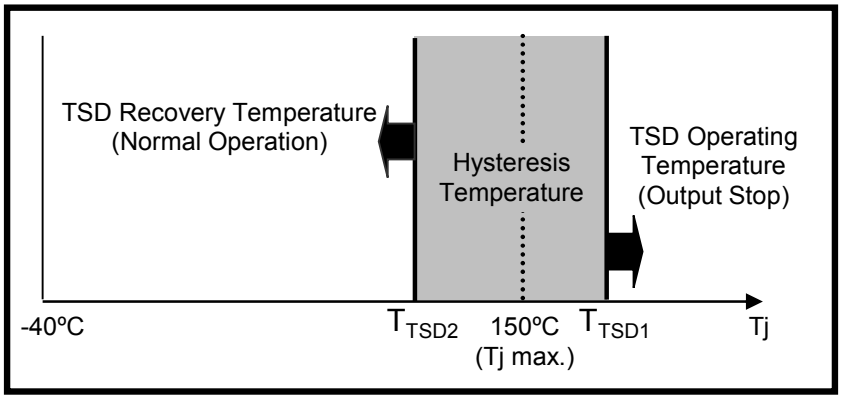
▪STEP Pin



▪DIR, HSM, RESET, ENABLE, BRAKE Pin

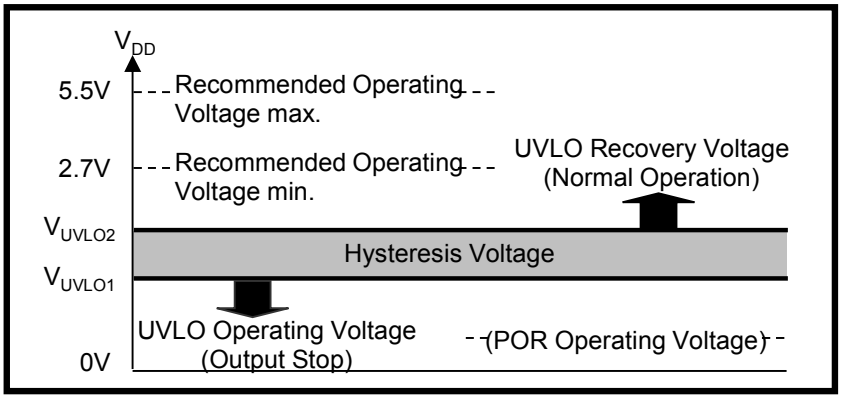


▪ TSD Operational Definition

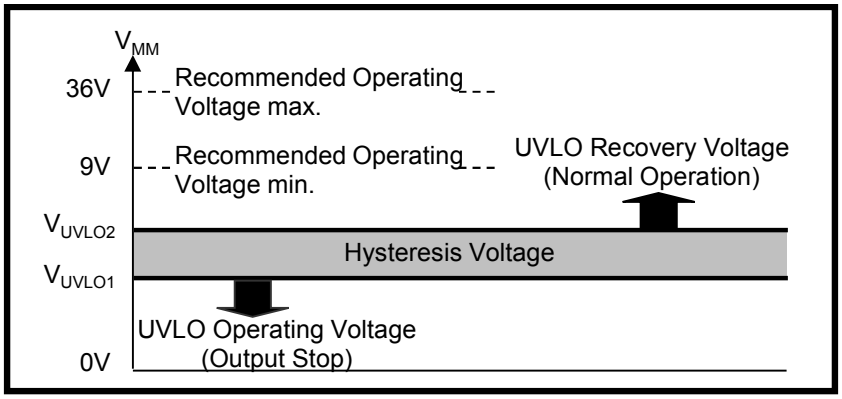


▪ UVLO Operational Definition

Logic Power Supply Block



Motor Power Supply Block



■ PIN STATE (Logic Block)

▪Input Pin

STEP : Input pin of rotaion control

STEP	Function
Positive Edge	Advance of the sequence one increment
Negative Edge	Keeping previous conditions
OPEN	Keeping previous conditions (Internally Pull Down)

HSM : Input pin of step mode control

HSM	Function
H	Half Step Mode
L	Full Step Mode
OPEN	Full Step Mode (Internally Pull Down)

DIR : Input pin of direction control

DIR	Function
H	Reverse(CCW)
L	Forward(CW)
OPEN	Forward(CW) (Internally Pull Down)

RESET : Input pin of initialized conditions

RESET	Function
H	Normal operation (ACTIVE)
L	Initialization+Outputs OFF +OCP release
OPEN	Initialization+Outputs OFF +OCP release (Internally Pull Down)

ENABLE : Input pin of outputs ON/ OFF control

ENABLE	Function
H	Normal operation (ACTIVE)
L	Outputs OFF
OPEN	Outputs OFF (Internally Pull Down)

BRAKE : Input pin of brake control

BRAKE	Function
H	Brake operation (Upper outputs ON+Low er outputs OFF)
L	Normal operation
OPEN	Normal operation (Internally Pull Down)

TOR1/2 : Input pin of output current level setting

TOR1	TOR2	Function
H	H	Output current level 20%
L/OPEN	H	Output current level 40%
H	L/OPEN	Output current level 70%
L/OPEN	L/OPEN	Output current level 100%

*OPEN: Internally Pull Down

▪Output Pin

MO : Output pin of motor origin position

MO	Function
H	Not initial sequence
L	Initial sequence

ALARM : Output pin of ALARM detection

ALARM	Function
H	Normal operation
L	ALARM operation (Outputs OFF)

■ SEQUENCE STATE

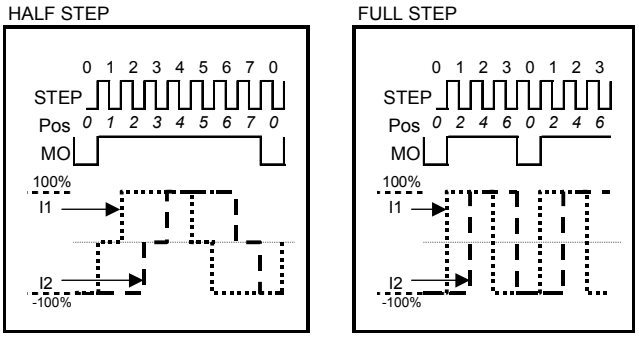
▪ Output Turn On State

Output current state after RESET

STEP MODE	I1(%)	I2(%)
FULL STEP	-100	-100
HALF STEP	-100	-100

I1 : OUT1B→OUT1A=-100%

I2 : OUT2B→OUT2A=-100%



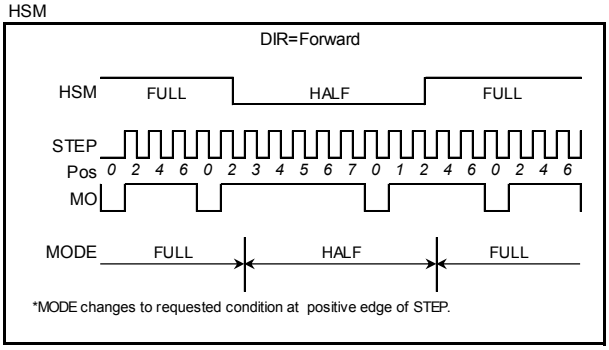
▪ Changing Timing by Input Condition

Timing of taking effect in input changed

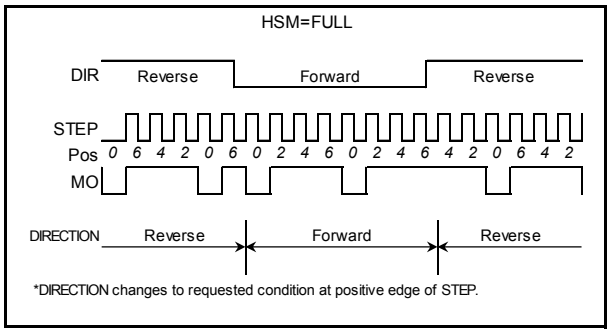
PIN NAME	Change Timing
HSM	Next STEP Positive Edge
DIR	Next STEP Positive Edge
RESET	Promptly
ENABLE	Promptly
BRAKE	Promptly
TOR1/2	Promptly

The priority of function: RESET > ENABLE > BRAKE.

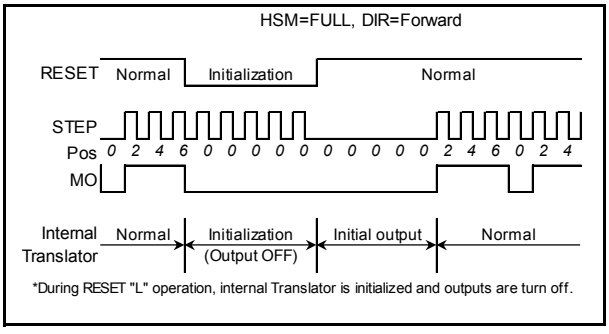
HSM



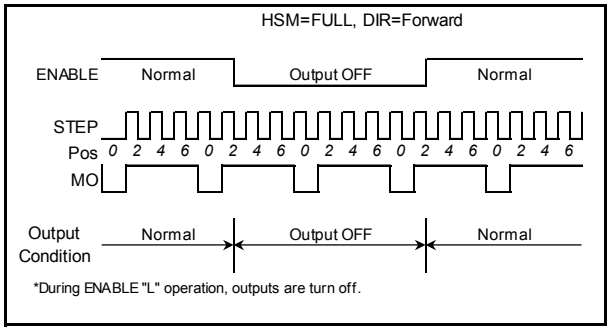
DIR



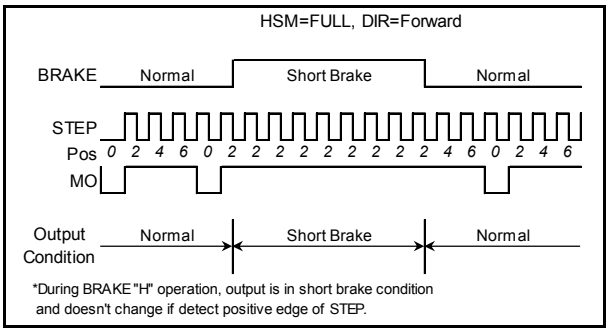
RESET



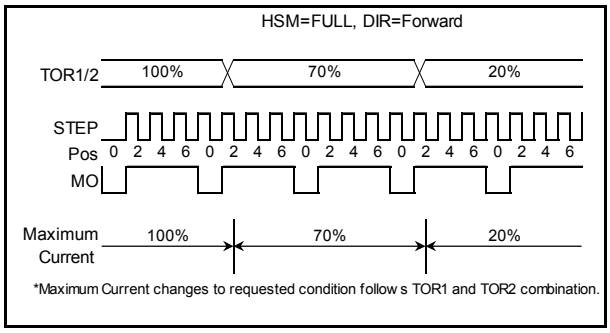
ENABLE



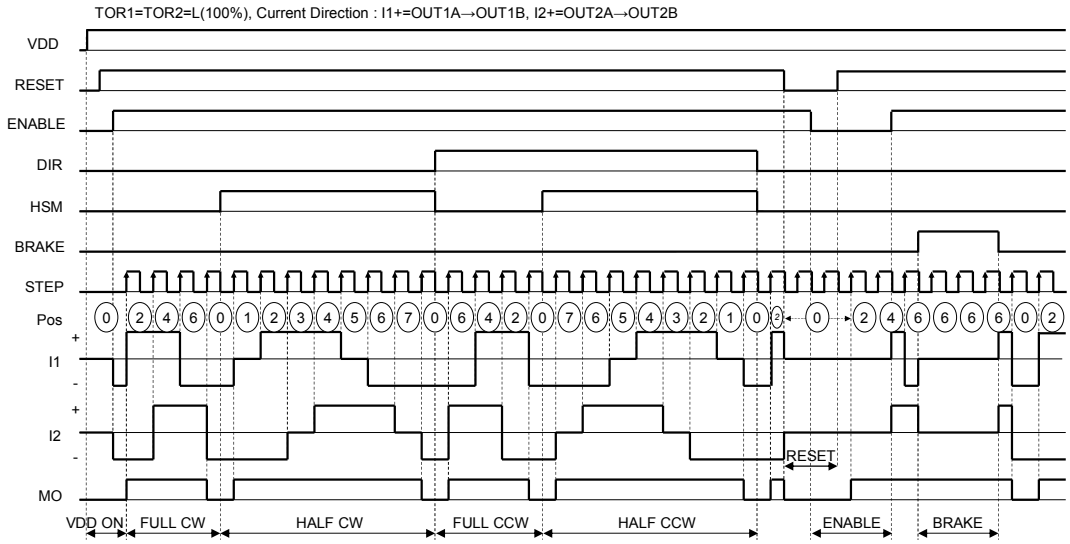
BRAKE



TOR1/ 2

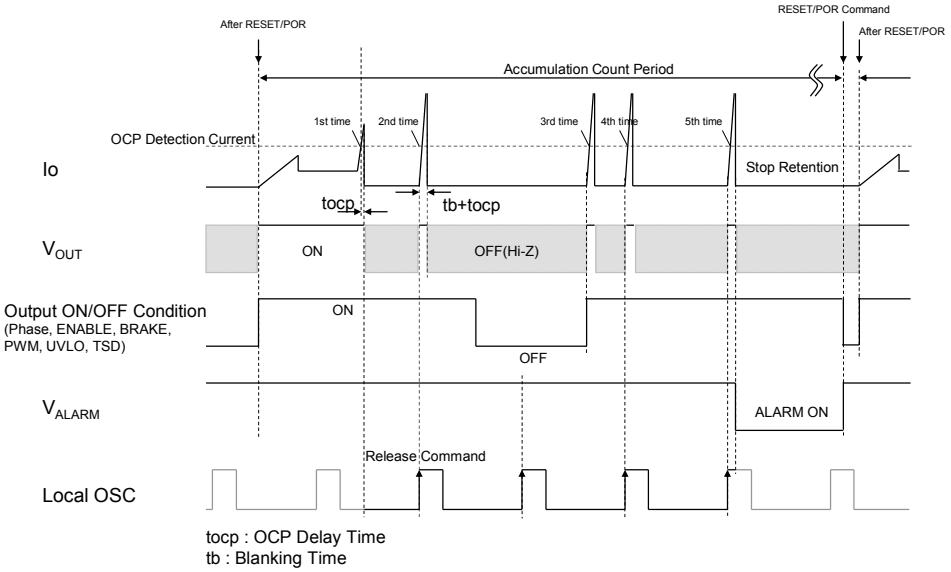


■ TIMING CHART



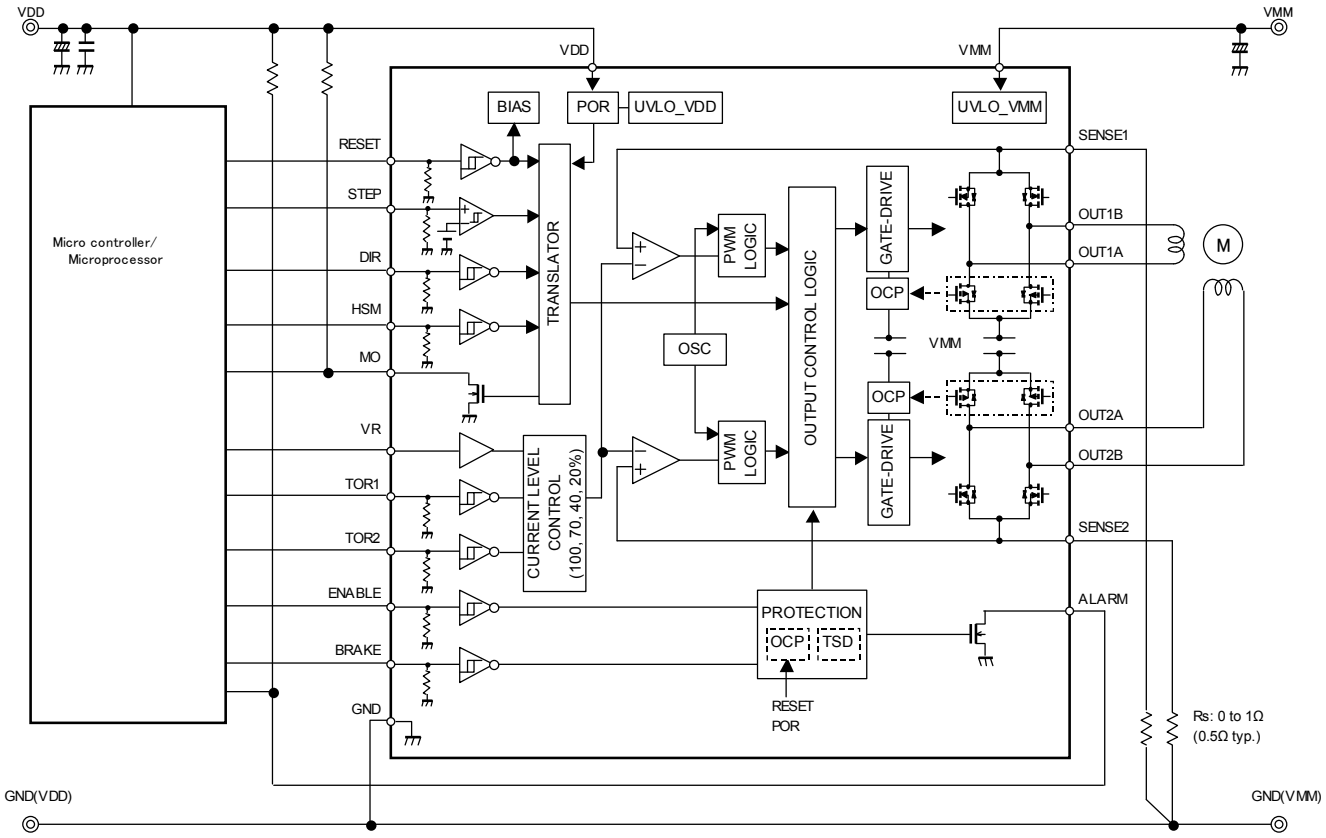
- During Power ON sequence, set RESET, ENABLE and STEP pins to "L" level for preventing malfunction.
- When RESET pin is "L" level, motor outputs are turned off and Translator is initialized.
  During this period, Translator can't accept STEP signal.
- When ENABLE pin is "L" level, motor outputs are turned off but Translator isn't initialized.
  During this period, Translator can accept STEP signal. When STEP signal is received, Translator operates sequence.
- When BRAKE pin is "H" level, all high side FETs are turned on and the breaking current flows through motor winding.
  During this period, Translator can't accept STEP signal.
- The priority of function is as follows: RESET > ENABLE > BRAKE.

■ OCP FUNCTION TIMING CHART



- The OCP circuit counts the OCP detection during the period of RESET or POR (Power-on).
  When OCP circuit detects five times, OUT pins turn off and retain, then ALARM pin outputs ALARM signal.
  After first OCP detection, the motor outputs are turned off temporarily.
  However, motor outputs restart by trigger of internal Local OSC until five times.
- Detection count, latch-off status and ALARM output can release by the following way.
  (1) Restart logic power supply (Power on Reset) (2) Input RESET signal
- The interval time between OCP detection and turning off is depend on output status.
  When ON state, the interval time is OCP Delay Time "tocp".
  Otherwise the interval time adds tocp and Blanking Time "tb".

■ TYPICAL APPLICATION



■ FUNCTION DESCRIPTION

The NJW4372 outputs constant current for the windings of a bipolar stepper motor.

The logic input block adopts STEP&DIR(pulse train) input control.

Phase logic sequence is generated by internal translator, it is triggered by STEP input.

• Constant Current Control (PWM Chopper)

The constant current control is achieved by PWM control of Low side FET switching of H-bridge.

The motor current is compared with reference voltage on the comparator block by using external current sensing resistor.

PWM logic block makes blanking time to filtering transient current in order to avoid malfunction of PWM control.

The value of constant current at 100% setting is decided by VR pin voltage and external sense resistor.

Besides, the combination of TOR1 and TOR2 pins (2bits) select one from four different values (100%, 70%, 40%, 20%) of constant current.

When ENABLE or RESET is activated, the motor outputs are disabled.

The value at 100% setting of constant current "Iopeak" is calculated by VR pin voltage and external sence resistor "Rs" as follows:

$$I_{Opeak} = 0.1 \bullet V_R / R_S \ [A]$$

For example, in the case of Rs=0.5Ω and VR=2.5V, Iopeak is obtained as 0.5A.

■ LOGIC INPUT BLOCKS

The internal composition of Logic inputs are the following three types.

• Input Block 1 (STEP pin)

This pin adopts the hysteresis comparator input circuit.

This block composes of large hysteresis voltage and pulldown resistance for noise immunity.

• Input Block 2 (DIR, HSM, RESET, ENABLE, BRAKE, TOR1, TOR2 pins)

These pins adopt the schmitt-inverter input circuit.

Therefore, the input threshold voltage and the hysteresis voltage depend on the VDD voltage.

When the input control voltage is different from the VDD, the input voltage needs to take input threshold voltage into consideration enough.

These pins have noise immunity by the hysteresis voltage and pulldown resistance.

However, if these pins aren't used, they connect to VDD or GND.

• Input Block 3 (VR pin)

This pin adopts the buffer input circuit.

If this pin is connected by external resistor network, the impedance has no influence between external resistance and inner resistance.

However, when this pin isn't used, it must connect to VDD.

■ STEP - Stepping Pulse

The Translator advances the phase-sequence at every positive edge of the STEP.

In FULL step mode, the pulse turns the stepper motor at the basic step angle.

In HALF step mode, two pulses are required to turn the motor at the basic step angle.

The DIR (direction) signal and HSM (HALF/FULL mode) are latched to the STEP positive edge, therefore these signals must be established before positive edge of the STEP.

■ DIR - Direction

The DIR signal determines the step direction.

The DIR can be changed anytime. However, direction is decided by step, so if it is simultaneous with positive edge of the STEP, it is probable to cause miss-steps. Therefore, make sure the margin larger than Data Setup Time.

■ HSM - HALF/FULL Step Mode

The HSM signal determines the step mode of motor control.

When HSM pin is on "L" level, the Translator is set to FULL step mode.

The HSM can be changed anytime. However, mode is decided by step, so if it is simultaneous with positive edge of the STEP, it is probable to cause miss-steps. Therefore, make sure the margin larger than Data Setup Time.

■ RESET - Initialization

The 2-Phase stepper motor repeats sequence to same winding at every multiple of four of the basic step angle.
Therefore, the Translator repeats phase-sequence at every four pulses in FULL step mode and every eight pulses in HALF step mode.
When RESET pin is on “L” level, the translator is initialized phase sequence and the motor outputs are turned off.
Moreover, the Translator can’t accept STEP signal during this period.

■ ENABLE - ON/OFF Control

The ENABLE signal activates all of the H-Bridge outputs.
When ENABLE pin is on “L” level, the motor outputs are turned off.
However, the Translator can accept STEP signal during this period.

■ BRAKE - Short Brake

Generally, when a stepper motor stops, rotor gradually stops with damped vibration (It is called settling time).
The settling time depends on the motor speed or load conditions and takes more than 100msec.
It also affects the speed enhancement of the system.
The brake functions short-circuit both ends of the coil in order to shorten the settling time.
Once the coil is short-circuited, BEMF generates short current and it effects as brake function. Therefore, rotor stops quickly.
When BRAKE pin is "H" level, high side FETs of the H-bridge are turned on, and brake function is activated.

■ VR - Reference Voltage

The VR voltage is reference voltage for internal comparator.
The VR voltage is divided to voltage of 1/10 by internal resistance and becomes the reference voltage at 100% setting of constant current.
Input circuit of VR pin is buffer circuit without influence from external resistors.

■ TOR1/2 - Current Level Setting

The combination of TOR1 and TOR2 pins (2bits) select one from four different torques (current values).

TOR1/2 : Input pin of output current level setting

TOR1	TOR2	Function
H	H	Output current level 20%
L/OPEN	H	Output current level 40%
H	L/OPEN	Output current level 70%
L/OPEN	L/OPEN	Output current level 100%

*OPEN: Internally Pull Down

This function can achieve torque control, low heat generation and power-saving to purpose of various motions.

<Example>

- Reducing holding torque (motor current)
- Optimizing motor current according to required torque when constant rotation speed
- Increase motor current when accelerate or slowdown

■ UVLO - Under Voltage Lockout Protection

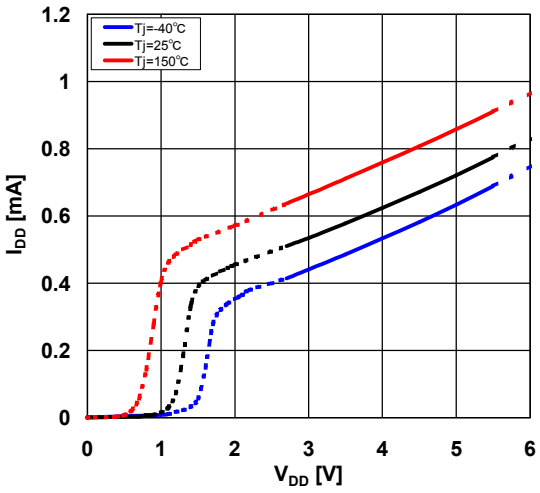
The NJW4372 has two internal UVLO functions for monitoring Logic (VDD) and Power (VMM) Supply Voltage independently.
When either VDD or VMM voltage is less than the UVLO operating voltage, the motor outputs are turned off.
In regard to VDD, when power-on operation or VDD is remarkably low voltage (less than 1.6V), there is possibility that the Translator is initialized by internal POR function.

■ MO - Motor Origin Monitor

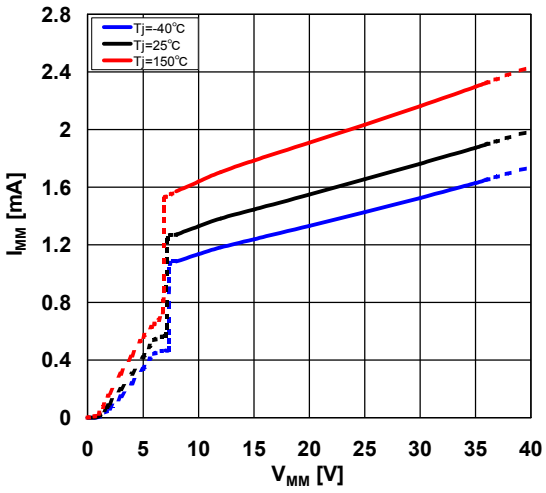
In initialized position of the translator, MO pin outputs “L” level for indicating to external devices that it is the initial pattern of output status.
In the case of high accuracy position control of stepping motor system, it can be performed by matching machine-zero position signal and electric MO output signal.

■ TYPICAL CHARACTERISTICS

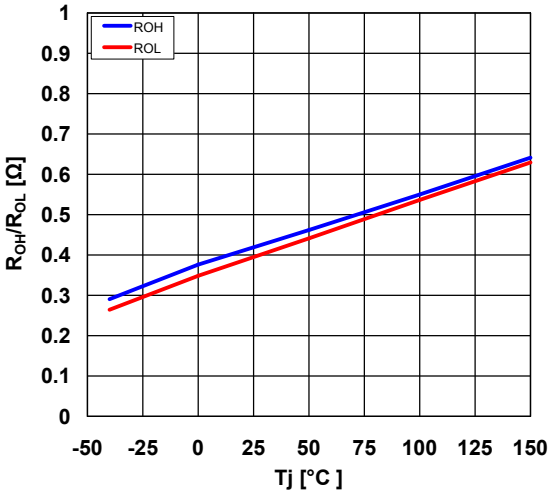
V_{DD} vs. I_{DD}
V_{MM}=24V



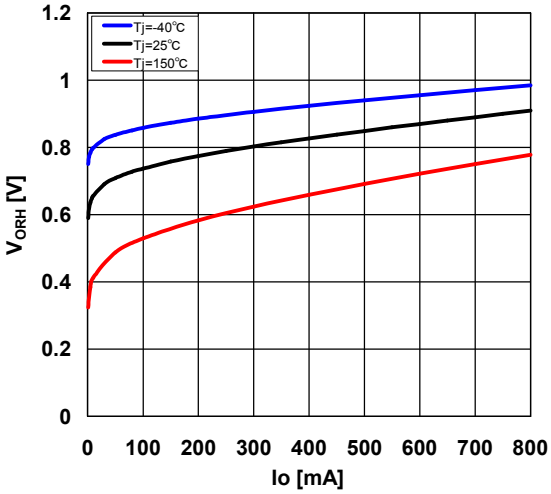
V_{MM} vs. I_{MM}
V_{DD}=5.0V



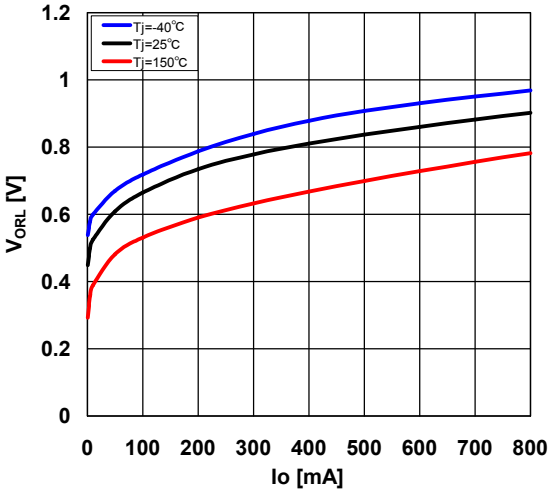
Tj vs. R_{OH}/R_{OL}
V_{DD}=5.0V, V_{MM}=24V, Io=500mA



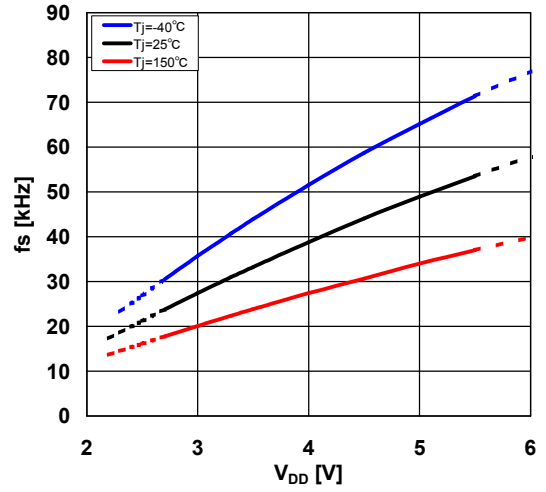
Io vs. V_{ORH}
V_{DD}=5.0V, V_{MM}=24V



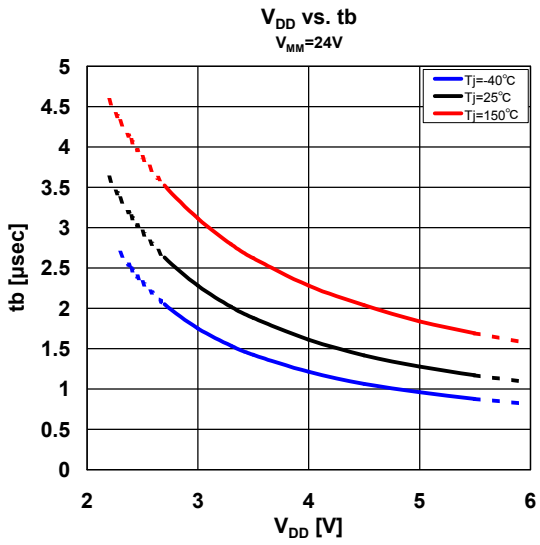
Io vs. V_{ORL}
V_{DD}=5.0V, V_{MM}=24V

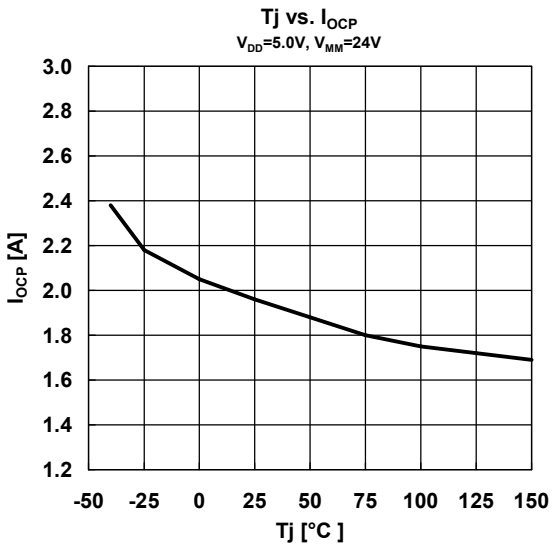


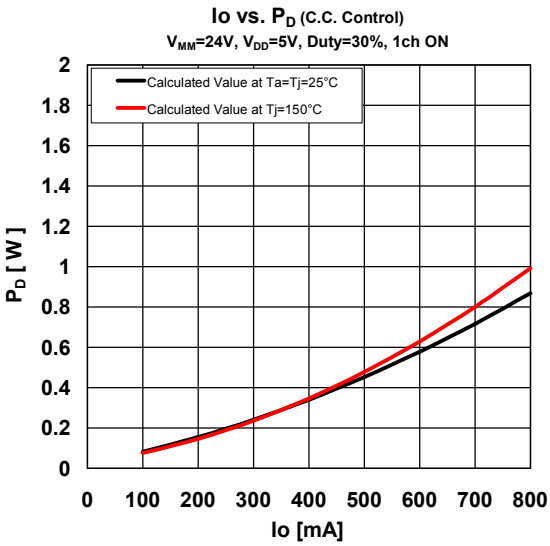
V_{DD} vs. fs
V_{MM}=24V

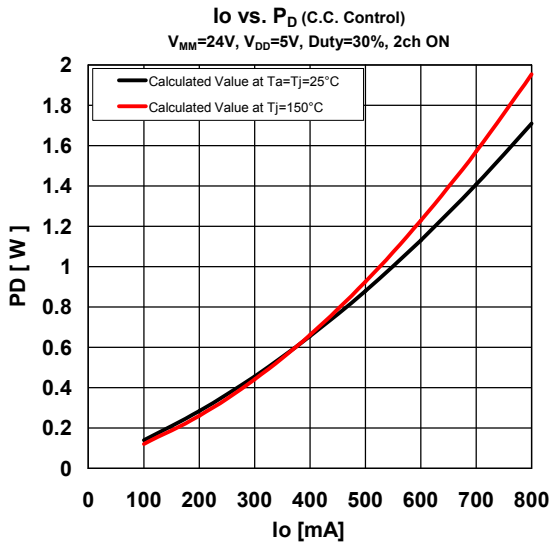


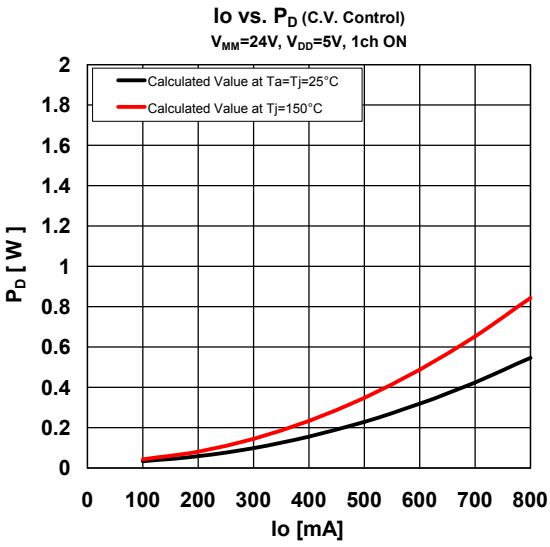
■ TYPICAL CHARACTERISTICS

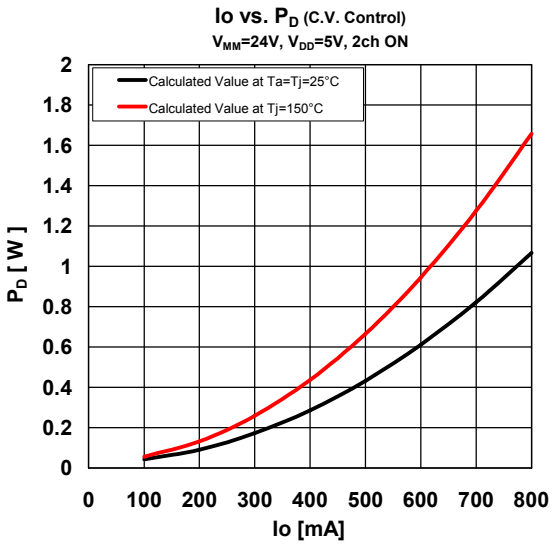












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