# I2C Controlled White LED Driver IC for Backlight

## ■ GENERAL DESCRIPTION

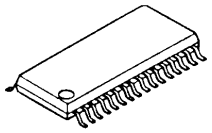
The NJW4605 is a high efficiency multiple strings white LED driver for backlight. This device is composed with 3-channel constant current drivers, step-up switching regulator that can drive up to 24pcs LED.

Each constant current driver is able to supply maximum current of 80mA per channel. And the accuracy of supply current between each driver is ±2.0% (max.) controlled by high precision current control circuit. The NJW4605 can control luminance by PWM signal input, and also features variable switching frequency between 300kHz and 1MHz.

When an abnormal LED lighting occurs, the FLT Pin sends out signals notifying the abnormality to the controller such as CPU. The NJW4605 operates over a wide supply voltage range from 6V to 30V, and operating temperature is up to 105ºC.

This very wide operating temperature range makes the IC ideal for medium sized LCD backlights, such as car navigations, note PC, and applications for amusement device.

## ■ PACKAGE OUTLINE

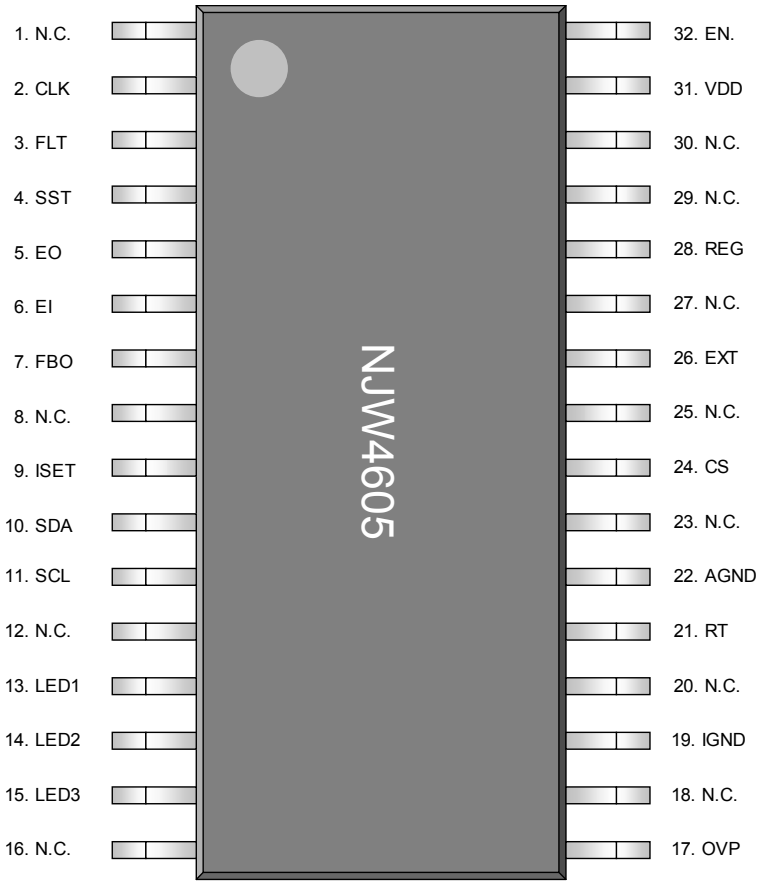


NJW4605V

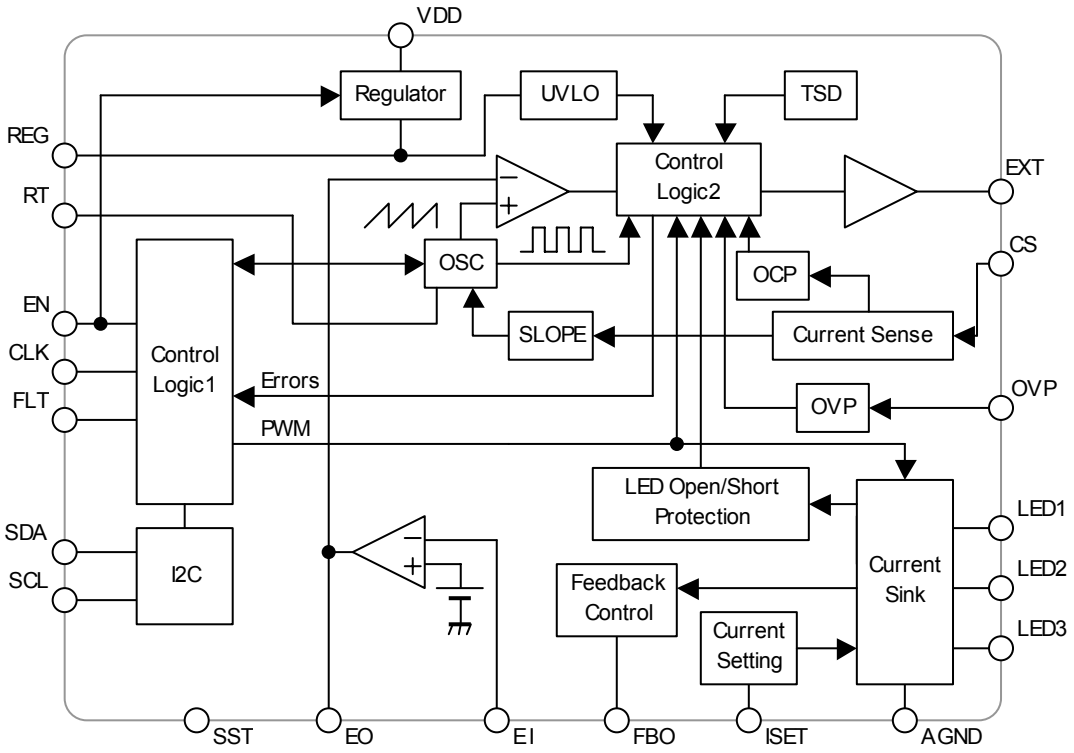
## ■ FEATURE

- Operating Voltage Range 6.0V to 30V
- Constant Current Driver 10mA to 80mA (each channel)
- LED Current ±2% max. (@$I_{LED}$=40mA)
- Switching Frequency 300kHz to 1MHz
- I2C BUS Control
- Luminance Control with PWM technique
- Soft-start Function
- FAULT Signal Output
- LED Open / Short Protection
- PWM Luminance Duty Ratio 0.1% Setting Available @ $f_{PWM}$=200Hz
- Over Current Protection
- Over Voltage Protection
- Under Voltage Lock Out Circuit
- Thermal Shutdown Circuit
- Package SSOP32

## ■ PIN CONFIGURATION




## ■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

| PARAMETER | SYMBOL | MAXIMUM RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V^+$ | +35 | V |
| LED Pin Voltage | $V_{LED1}$, $V_{LED3}$, $V_{LED3}$ | –0.3 to +40 | V |
| OVP Pin Voltage | $V_{OVP}$ | –0.3 to +42 | V |
| EN Pin Voltage | $V_{EN}$ | –0.3 to +35 | V |
| REG Pin Voltage | $V_{REG}$ | –0.3 to +6 | V |
| Each Pin Voltage: CS, EXT, SST, EO, EI, FBO, ISET, RT | $V_{SC}$, $V_{EXT}$, $V_{SST}$, $V_{EO}$, $V_{EI}$, $V_{FBO}$, $V_{ISET}$, $V_{RT}$ | –0.3 to $V_{REG}$ | V |
| FLT Pin Voltage | $V_{FLT}$ | –0.3 to +6 | V |
| Each Pin Voltage CLK, SCL, SDA | $V_{CLK}$, $V_{SCL}$, $V_{SDA}$ | –0.3 to +6 | V |
| EXT Pin Output Current | $I_{EXT}$ | ±100 | mA |
| Power Dissipation | $P_D$ | 1,200 (*1)<br>1,800 (*2) | mW |
| Operating Junction Temperature | $T_j$ | –40 to +150 | °C |
| Operating Temperature Range | $T_{opr}$ | –40 to +105 | °C |
| Storage Temperature Range | $T_{stg}$ | –50 to +150 | °C |

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cu area: 74.2×74.2mm

■ **RECOMMENDED OPERATING CONDITIONS** (Ta=25°C)

| PARAMETER | SYMBOL | OPERATING RANGE | UNIT |
|---|---|---|---|
| Supply Voltage | $V^+$ | 6 to 30 | V |
| LED Drive Current (*3) | $I_{LED1}$~ $I_{LED3}$ | 10 to 80 | mA |
| EN Pin Voltage | $V_{EN}$ | 0 to 35 | V |
| Each Pin Voltage: CLK, SCL, SDA | $V_{SLK}$, $V_{SCL}$, $V_{SDA}$ | 0 to 5.5 | V |
| Oscillation Frequency | $f_{OSC}$ | 0.3 to 1 | MHz |
| External Synchronous Oscillation Frequency (*4) | $f_{OSC\_SYNC}$ | 0.3 to 1 | MHz |

(*3): per 1channel

(*4): The $f_{OSC\_SYNC}$ range is the following: $1.1 \times f_{OSC} < f_{OSC\_SYNC} < 1.5 \times f_{OSC}$

■ THERMAL CHARACTERISTICS

| PARAMETER | SYMBOL | THERMAL RESISTANCE | UNIT |
|---|---|---|---|
| Junction to Ambient Temperature | $\theta_{ja}$ | 104 ( *1 )<br>69.4 ( *2 ) | °C/W |
| Junction to Case | $\psi_{jt}$ | 19.3 ( *1 )<br>13.1 ( *2 ) | °C/W |

(*1) : Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2) : Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers), internal Cupper area: 74.2×74.2mm

■ **ELECTRICAL CHARACTERISTICS** (Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=25°C)

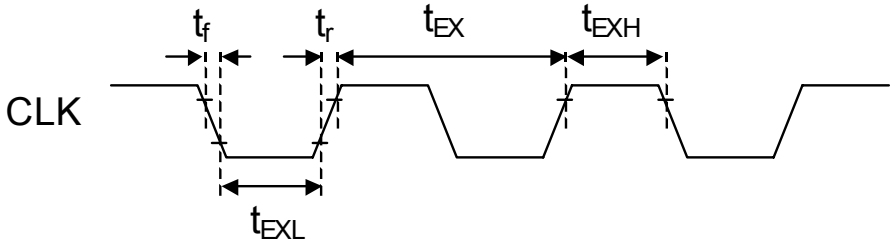
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < General Characteristics > | | | | | | |
| Quiescent Current 1 (Operating) | $I_{Q1}$ | Switching | - | 3.3 | 6.6 | mA |
| Quiescent Current 2 (Operating) | $I_{Q2}$ | PWM Duty = 0/1024, No switching | - | 2.4 | 4.8 | mA |
| Quiescent Current 3 (Standby) | $I_{Q3\_OFF}$ | $V_{EN}$ = 0V, $V_{REG}$ = 0V | - | - | 1 | μA |
| < Built-in Regulator > | | | | | | |
| REG Pin Voltage | $V_{REG}$ | $I_{REG}$ = 0mA, PWM Duty = 0/1024 | 4.75 | 5.0 | 5.25 | V |
| Line Regulation | $\Delta V_{REG-VDD}$ | $V_{IN}$ = 6 to 35V, $I_{REG}$ = 0mA, PWM Duty = 0/1024 | -10 | 20 | 40 | mV |
| Load Regulation | $\Delta V_{REG-IO}$ | $I_{REG}$ = 0 to 20mA, PWM Duty = 0/1024 | - | 40 | 100 | mV |
| REG Pin Output Current (*5) | $I_{OREG}$ | $V_{REG}$ × 0.95, PWM Duty = 0/1024 | 20 | - | - | mA |
| < Under Voltage Lock Out (UVLO) Block > | | | | | | |
| UVLO Release Voltage (REG output) | $V_{RUVLO}$ | | 3.4 | 3.9 | 4.4 | V |
| UVLO Operating Voltage (REG output) | $V_{DUVLO}$ | | 3.3 | 3.8 | 4.3 | V |
| UVLO Hysteresis Voltage Width (REG output) | $\Delta V_{UVLO}$ | $V_{RUVLO}$ - $V_{DUVLO}$ | - | 0.1 | - | V |
| < EN, CLK, SCL, SDA, RT, SST, FLT Pin > | | | | | | |
| EN Pin "H" Level Voltage (Operating) | $V_{IH\_EN}$ | | 2 | - | 5.5 | V |
| EN Pin "L" Level Voltage (Standby) | $V_{IL\_EN}$ | | 0 | - | 0.4 | V |
| EN Pin Input "H" Level Leak Current | $I_{IH\_EN\_LEAK}$ | $V_{EN}$ = 5.0V | -1 | - | 4.5 | μA |
| EN Pin Input "L" Level Leak Current | $I_{IL\_EN\_LEAK}$ | $V_{EN}$ = 0V | -1 | - | - | μA |
| CLK Pin Input "H" Level Voltage | $V_{IH\_CLK}$ | | 2.1 | - | 5.5 | V |
| CLK Pin Input "L" Level Voltage | $V_{IL\_CLK}$ | | 0 | - | 0.8 | V |
| CLK Pin Input "H" Level Leak Current | $I_{IH\_CLK\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| CLK Pin Input "L" Level Leak Current | $I_{IL\_CLK\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SCL Pin Input "H" Level Voltage | $V_{IH\_SCL}$ | | 2.1 | - | 5.5 | V |
| SCL Pin Input "L" Level Voltage | $V_{IL\_SCL}$ | | 0 | - | 0.8 | V |
| SCL Pin Input "H" Level Leak Current | $I_{IH\_SCL\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| SCL Pin Input "L" Level Leak Current | $I_{IL\_SCL\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SDA Pin Input "H" Level Voltage | $V_{IH\_SDA}$ | | 2.1 | - | 5.5 | V |
| SDA Pin Input "L" Level Voltage | $V_{IL\_SDA}$ | | 0 | - | 0.8 | V |
| SDA Pin Input "H" Level Leak Current | $I_{IH\_SDA\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| SDA Pin Input "L" Level Leak Current | $I_{IL\_SDA\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SDA Pin Output "L" Level Voltage | $V_{OL\_SDA}$ | $I_O$=3mA | - | - | 0.4 | V |

(*5): Built-in 5V Regulator can drive current

■ **ELECTRICAL CHARACTERISTICS** (Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=25°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < EN, CLK, SCL, SDA, RT, SST, FLT Pin > | | | | | | |
| SST Pin Source Current | $I_{SST\_SOURCE}$ | $V_{SST}$ = 1.5V | 3.5 | 5.5 | 7.5 | μA |
| SST Pin Sink Current | $I_{SST\_SINK}$ | $V_{SST}$ = 1.5V, $V_{OVP}$ = 41V | 0.60 | 1.25 | 2.10 | μA |
| SST Pin ON Resistance | $R_{SST\_ON}$ | $V_{REG}$ = 3.2V | 0.6 | 1.0 | 1.4 | kΩ |
| SST Pin Voltage at Operating | $V_{SST\_OPR}$ | | - | 3.3 | - | V |
| SST Reset Voltage | $V_{SST\_RES}$ | | - | 0.1 | - | V |
| FLT Pin Output "L" Level Voltage | $V_{FLT}$ | $I_{FLT}$ = 500μA | - | 0.25 | 0.5 | V |
| FLT Pin Leak Current | $I_{FLT\_LEAK}$ | $V_{FLT}$ = 5.0V | - | - | 1 | μA |
| < Output Driver (EXT Pin) > | | | | | | |
| Output "H" ON Resistance | $R_{OH\_EXT}$ | $I_{EXT}$ = −20mA | - | 8.4 | 16.8 | Ω |
| Output "L" ON Resistance | $R_{OL\_EXT}$ | $I_{EXT}$ = 20mA | - | 2.8 | 5.6 | Ω |
| EXT Pin Output "H" Level Voltage | $V_{OH\_EXT}$ | $I_{EXT}$ = −20mA | 4.3 | 4.8 | - | V |
| EXT Pin Pull Down Resistance | $R_{PD\_EXT}$ | $V_{EN}$ = 0V, $V_{REG}$ = 0V | 50 | 100 | 150 | kΩ |
| < Oscillator Circuit > | | | | | | |
| Oscillation Frequency | $f_{OSC}$ | | 0.585 | 0.650 | 0.715 | MHz |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{EI}$ = 0V | 84 | 89 | 93 | % |
| Minimum Duty Cycle | $D_{MIN}$ | | - | 10 | - | % |
| < Exterior Input Clock > | | | | | | |
| External System Clock Maximum Frequency | $f_{EX\_sys}$ | | - | - | 1.5 | MHz |
| External System Clock Pulse Width "L" Time | $t_{EXL}$ | | 100 | - | - | ns |
| External System Clock Pulse Width "H" Time | $t_{EXh}$ | | 100 | - | - | ns |
| Rise Time | $t_r$ | | - | - | 300 | ns |
| Fall Time | $t_f$ | | - | - | 300 | ns |

< External Clock >



■ **ELECTRICAL CHARACTERISTICS** (Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=25°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < Over Current Protection Circuit > | | | | | | |
| Current Limit Detect Voltage 1 | $V_{DCS1}$ | OCP (instruction) = 0 | 0.214 | 0.35 | 0.476 | V |
| Current Limit Detect Voltage 2 | $V_{DCS2}$ | OCP (instruction) = 1 | 0.135 | 0.25 | 0.355 | V |
| CS Pin Leak Current | $I_{CS\_LEAK}$ | $V_{CS}$ = 1.0V, $V_{EN}$ = 0V | -1 | - | 1 | μA |
| Current Limit Delay Time | $t_{CS\_LEAK}$ | $V_{CS}$ = 0.4V | - | 200 | - | ns |
| < Over Voltage Protection (OVP) Circuit > | | | | | | |
| OVP Operating Voltage | $V_{DOVP}$ | | 28.4 | 30.4 | 32.4 | V |
| OVP Release Voltage | $V_{ROVP}$ | | 24.4 | 26.4 | 28.4 | V |
| OVP Hysteresis Voltage Width | $\Delta V_{OVP}$ | $V_{DOVP}$ - $V_{ROVP}$ | - | 4 | - | V |
| OVP Pin Input Current 1 | $I_{OVP1}$ | $V_{OVP}$ = 27V | - | 24 | 48 | μA |
| OVP Pin Input Current 2 | $I_{OVP2}$ | $V_{OVP}$ = 42V | 550 | 900 | 1800 | μA |
| OVP Pin Leak Current | $I_{OVP\_LEAK}$ | $V_{EN}$ = 0V, $V_{OVP}$ = 42V | - | - | 1 | μA |
| < Error Amplifier Block > | | | | | | |
| Reference Voltage | $V_{REF\_EA}$ | | 0.57 | 0.6 | 0.63 | V |
| EI Pin Input Bias Current | $I_{EI}$ | | -0.1 | - | 0.1 | μA |
| EO Pin Source Current | $I_{EO\_SOURCE}$ | $V_{EI}$ = 0.5V, $V_{EO}$ = 0.6V | 15 | 22 | 31 | μA |
| EO Pin Sink Current | $I_{EO\_SINK}$ | $V_{EI}$ = 0.8V, $V_{EO}$ = 0.6V | 300 | 500 | 700 | μA |
| < Constant Current Circuit > | | | | | | |
| LED Drive Current (*3) | $I_{LED1}$ $I_{LED3}$ $I_{LED3}$ | $R_{ISET}$ = 10kΩ, $V_{LED1}$ to $V_{LED3}$ = 0.9V | 77.6 | 80 | 82.4 | mA |
| | | $R_{ISET}$ = 20kΩ, $V_{LED1}$ to $V_{LED3}$ = 0.77V | 38.4 | 40 | 41.6 | |
| LED Drive Current Matching (*6) | $I_{MLED}$ | $R_{ISET}$ = 10kΩ, $V_{LED1}$ to $V_{LED3}$ = 0.9V | -3 | 0 | +3 | % |
| | | $R_{ISET}$ = 20kΩ, $V_{LED1}$ to $V_{LED3}$ = 0.77V | -2 | 0 | +2 | |
| LED Short Protection Detect Voltage | $V_{LED\_SHORT}$ | | 8 | 9 | 10 | V |
| LED Short Protection Detect Delay Time | $t_{LED\_SHORT}$ | $V_{LED1}$ to $V_{LED3}$ = 11V | - | 50 | - | μs |
| LED Open Protection Detect Voltage | $V_{LED\_OPEN}$ | $V_{OVP}$ = 41V | 0.6 | 0.8 | 1.0 | V |
| LED Pin Leak Current (*3) | $I_{LED\_LEAK}$ | $V_{EN}$ = 0V, $V_{LED}$ = 36V | - | - | 1 | μA |
| LED Pin Control Voltage (*7) | $V_{CLED1}$~ $V_{CLED3}$ | $R_{ISET}$ = 10kΩ, $I_{LED}$ = 80mA | 0.8 | 1.05 | 1.3 | V |
| | | $R_{ISET}$ = 20kΩ, $I_{LED}$ = 40mA | 0.67 | 0.92 | 1.17 | |
| ISET Maximum Setting Current | $I_{SET\_MAX}$ | | 140 | - | 270 | μA |
| Maximum LED Current (*3, *8) | $I_{LED\_MAX}$ | | 120 | - | 230 | mA |

(*3): each 1channel

(*6): ($I_{LED}$ - ILED_AVG) / ILED_AVG ×100, ILED_AVG = ($I_{LED1}$ + ILED2 + ILED3 + ILED4) / 4
The $I_{LED}$ referred is given in the following parameters; $I_{LED1}$, $I_{LED2}$, $I_{LED3}$, and $I_{LED4}$.

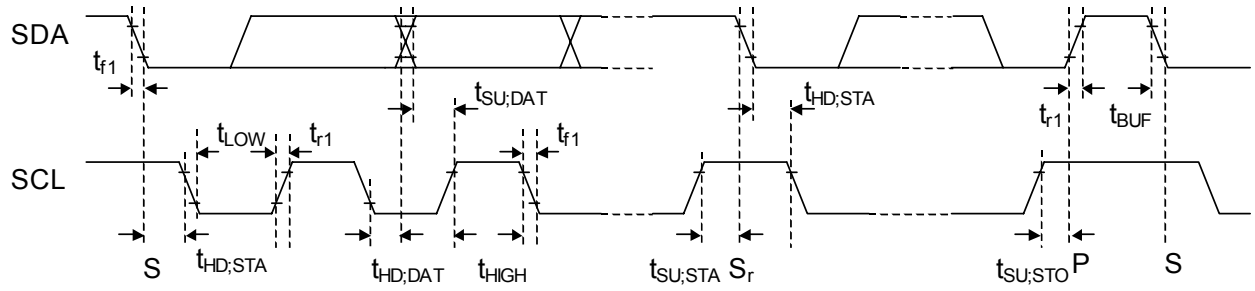
(*7): at 1channel operating

(*8): It is a peak current that flows to LED terminal by the time the ISET terminal short-circuit protection circuit operates. You should set the LED driving current from 10mA to 80mA range.

■ **ELECTRICAL CHARACTERISTICS** (Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=25°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < I2C Bus Timing (High Speed Mode) > | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | SCL | - | - | 400 | kHz |
| Hold Time (Repeat) [START] Condition | $t_{HD;STA}$ | SCL, SDA | 0.6 | - | - | μs |
| SCL Clock "L" Time | $t_{LOW}$ | SCL | 1.3 | - | - | μs |
| SCL Clock "H" Time | $t_{HIGH}$ | SCL | 0.6 | - | - | μs |
| Repeat [START] Condition Setup Time | $t_{SU;STA}$ | SCL, SDA | 0.6 | - | - | μs |
| Data Hold Time | $t_{HD;DAT}$ | SCL, SDA | 0 | - | 0.9 | μs |
| Data Setup Time | $t_{SU;DAT}$ | SCL, SDA | 100 | - | - | ns |
| Rise Time 1 | $t_{r1}$ | SCL, SDA | - | - | 300 | ns |
| Fall Time 1 | $t_{f1}$ | SCL, SDA | - | - | 300 | ns |
| [STOP] Condition Setup Time | $t_{SU;STO}$ | SCL, SDA | 0.6 | - | - | μs |
| Bus Free Time Between [STOP] - [START] | $t_{BUF}$ | SDA | 1.3 | - | - | μs |

< I2C Bus Timing >




S: Start Condition

$S_r$: Repeat Start Condition

P: Stop Condition

■ **ELECTRICAL CHARACTERISTICS2**

(Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=-40°C to 105°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < General Characteristics > | | | | | | |
| Quiescent Current 1 (Operating) | $I_{Q1}$ | Switching | - | - | 6.6 | mA |
| Quiescent Current 2 (Operating) | $I_{Q2}$ | PWM Duty = 0/1024, No switching | - | - | 4.8 | mA |
| Quiescent Current 3 (Standby) | $I_{Q3\_OFF}$ | $V_{EN}$ = 0V, $V_{REG}$ = 0V | - | - | 1 | μA |
| < Built-in Regulator > | | | | | | |
| Output Voltage | $V_{REG}$ | $I_{REG}$ = 0mA, PWM Duty = 0/1024 | 4.75 | - | 5.25 | V |
| Line Regulation | $\Delta V_{REG-VDD}$ | $V_{IN}$ = 6 to 35V, $I_{REG}$ = 0mA, PWM Duty = 0/1024 | -10 | - | 60 | mV |
| Load Regulation | $\Delta V_{REG-IO}$ | $I_{REG}$ = 0 to 20mA, PWM Duty = 0/1024 | - | - | 120 | mV |
| < Under Voltage Lock Out (UVLO) Block > | | | | | | |
| UVLO Release Voltage (REG output) | $V_{RUVLO}$ | | 3.4 | - | 4.4 | V |
| UVLO Operating Voltage (REG output) | $V_{DUVLO}$ | | 3.3 | - | 4.3 | V |
| < EN, CLK, SCL, SDA, RT, SST, FLT Pin > | | | | | | |
| EN Pin "H" Level Voltage (Operating) | $V_{IH\_EN}$ | | 2 | - | 5.5 | V |
| EN Pin "L" Level Voltage (Standby) | $V_{IL\_EN}$ | | 0 | - | 0.4 | V |
| EN Pin Input "H" Level Leak Current | $I_{IH\_EN\_LEAK}$ | $V_{EN}$ = 5.0V | -1 | - | 4.5 | μA |
| EN Pin Input "L" Level Leak Current | $I_{IL\_EN\_LEAK}$ | $V_{EN}$ = 0V | -1 | - | - | μA |
| CLK Pin Input "H" Level Voltage | $V_{IH\_CLK}$ | | 2.1 | - | 5.5 | V |
| CLK Pin Input "L" Level Voltage | $V_{IL\_CLK}$ | | 0 | - | 0.8 | V |
| CLK Pin Input "H" Level Leak Current | $I_{IH\_CLK\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| CLK Pin Input "L" Level Leak Current | $I_{IL\_CLK\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SCL Pin Input "H" Level Voltage | $V_{IH\_SCL}$ | | 2.1 | - | 5.5 | V |
| SCL Pin Input "L" Level Voltage | $V_{IL\_SCL}$ | | 0 | - | 0.8 | V |
| SCL Pin Input "H" Level Leak Current | $I_{IH\_SCL\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| SCL Pin Input "L" Level Leak Current | $I_{IL\_SCL\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SDA Pin Input "H" Level Voltage | $V_{IH\_SDA}$ | | 2.1 | - | 5.5 | V |
| SDA Pin Input "L" Level Voltage | $V_{IL\_SDA}$ | | 0 | - | 0.8 | V |
| SDA Pin Input "H" Level Leak Current | $I_{IH\_SDA\_LEAK}$ | $V_{CLK}$ = 5.0V | -1 | - | 1 | μA |
| SDA Pin Input "L" Level Leak Current | $I_{IL\_SDA\_LEAK}$ | $V_{CLK}$ = 0V | -1 | - | - | μA |
| SDA Pin Output "L" Level Voltage | $V_{OL\_SDA}$ | $I_O$=3mA | - | - | 0.4 | V |

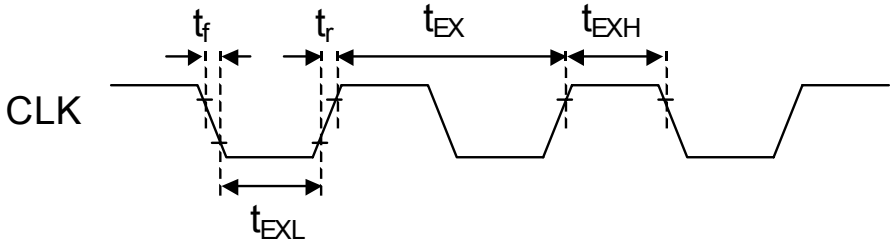
(*5): Built-in 5V Regulator can drive current

■ **ELECTRICAL CHARACTERISTICS2**

(Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=-40°C to 105°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < EN, CLK, SCL, SDA, RT, SST, FLT Pin > | | | | | | |
| SST Pin Source Current | $I_{SST\_SOURCE}$ | $V_{SST}$ = 1.5V | 3 | - | 7.5 | μA |
| SST Pin Sink Current | $I_{SST\_SINK}$ | $V_{SST}$ = 1.5V | 0.50 | - | 2.10 | μA |
| SST Pin ON Resistance | $R_{SST\_ON}$ | $V_{REG}$ = 3.2V | 0.6 | - | 1.6 | kΩ |
| FLT Pin Output "L" Level Voltage | $V_{FLT}$ | $I_{FLT}$ = 500μA | - | - | 0.5 | V |
| FLT Pin Leak Current | $I_{FLT\_LEAK}$ | $V_{FLT}$ = 5.0V | - | - | 1 | μA |
| < Output Driver (EXT Pin) > | | | | | | |
| EXT Pin Output "H" Level Voltage | $V_{OH\_EXT}$ | $I_{EXT}$ = -5mA | 4.40 | - | - | V |
| < Oscillator Circuit > | | | | | | |
| Oscillation Frequency | $f_{OSC}$ | | 0.585 | - | 0.715 | MHz |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{EI}$ = 0V | 84 | - | 93 | % |
| < External Input Clock > | | | | | | |
| External System Clock Maximum Frequency | $f_{EX}$ | | - | - | 1.5 | MHz |
| External System Clock Pulse Width "L" Time | $t_{EXL}$ | | 100 | - | - | ns |
| External System Clock Pulse Width "H" Time | $t_{EXh}$ | | 100 | - | - | ns |
| Rise Time | $t_r$ | | - | - | 300 | ns |
| Fall Time | $t_f$ | | - | - | 300 | ns |

< External Clock >



■ **ELECTRICAL CHARACTERISTICS2**

(Unless other noted, $V^+$=12V, $V_{EN}$=5V, $C_{REG}$=1μF, $R_{ISET}$=10kΩ, $R_T$=47kΩ, $T_a$=-40°C to 105°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| < Over Current Protection Circuit > | | | | | | |
| Current Limit Detect Voltage 1 | $V_{DCS1}$ | OCP (instruction) = 0 | 0.195 | - | 0.495 | V |
| Current Limit Detect Voltage 2 | $V_{DCS2}$ | OCP (instruction) = 1 | 0.135 | - | 0.355 | V |
| CS Pin Leak Current | $I_{CS\_LEAK}$ | $V_{CS}$ = 1.0V, $V_{EN}$ = 0V | -2 | - | 2 | μA |
| < Over Voltage Protection (OVP) Circuit > | | | | | | |
| OVP Operating Voltage | $V_{DOVP}$ | | 28.4 | - | 32.4 | V |
| OVP Release Voltage | $V_{ROVP}$ | | 24.4 | - | 28.4 | V |
| OVP Pin Input Current 1 | $I_{OVP1}$ | $V_{OVP}$ = 27V | - | - | 48 | μA |
| OVP Pin Input Current 2 | $I_{OVP2}$ | $V_{OVP}$ = 42V | 450 | - | 1900 | μA |
| OVP Pin Leak Current | $I_{OVP\_LEAK}$ | $V_{EN}$ = 0V, $V_{OVP}$ = 42V | - | - | 1 | μA |
| < Error Amplifier Block > | | | | | | |
| Reference Voltage | $V_{REF\_EA}$ | | 0.564 | - | 0.636 | V |
| EI Pin Input Bias Current | $I_{EI}$ | | -0.1 | - | 0.1 | μA |
| EO Pin Source Current | $I_{EO\_SOURCE}$ | $V_{EI}$ = 0.5V, $V_{EO}$ = 0.6V | 15 | - | 31 | μA |
| EO Pin Sink Current | $I_{EO\_SINK}$ | $V_{EI}$ = 0.8V, $V_{EO}$ = 0.6V | 300 | - | 700 | μA |
| < Constant Current Circuit > | | | | | | |
| LED Drive Current (*3) | $I_{LED1}$<br>$I_{LED3}$<br>$I_{LED3}$ | $R_{ISET}$ = 20kΩ,<br>$V_{LED1}$ to $V_{LED3}$ = 0.77V | 38 | - | 42 | mA |
| LED Drive Current Matching (*6) | $I_{MLED}$ | $R_{ISET}$ = 20kΩ,<br>$V_{LED1}$ to $V_{LED3}$ = 0.77V | -3 | - | +3 | % |
| LED Short Protection Detect Voltage | $V_{LED\_SHORT}$ | | 8 | - | 10 | V |
| LED Open Protection Detect Voltage | $V_{LED\_OPEN}$ | $V_{OVP}$ = 41V | 0.6 | - | 1.0 | V |
| LED Pin Leak Current | $I_{LED\_LEAK}$ | $V_{EN}$ = 0V, $V_{LED}$ = 36V | - | - | 1 | μA |
| LED Pin Control Voltage (*6) | $V_{CLED1}$~<br>$V_{CLED3}$ | $R_{ISET}$ = 20kΩ, $I_{LED}$ = 40mA | 0.67 | - | 1.17 | V |
| ISET Maximum Setting Current | $I_{SET\_MAX}$ | | 140 | - | 270 | μA |

(*3): each 1channel

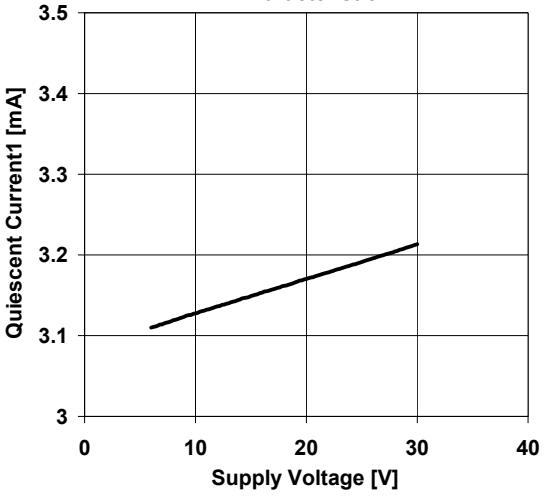
(*6): ($I_{LED}$ - ILED_AVG) / ILED_AVG ×100, ILED_AVG = ($I_{LED1}$ + ILED2 + ILED3 + ILED4) / 4

The $I_{LED}$ referred is given in the following parameters; $I_{LED1}$, $I_{LED2}$, $I_{LED3}$, and $I_{LED4}$.

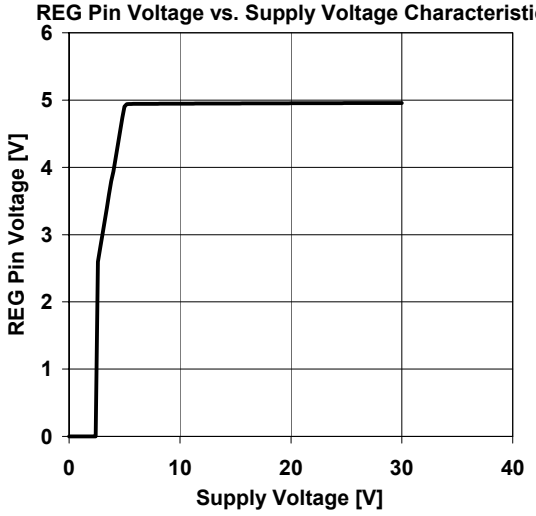
(*7): at 1channel operating

■ ELECTRICAL CHARACTERISTICS

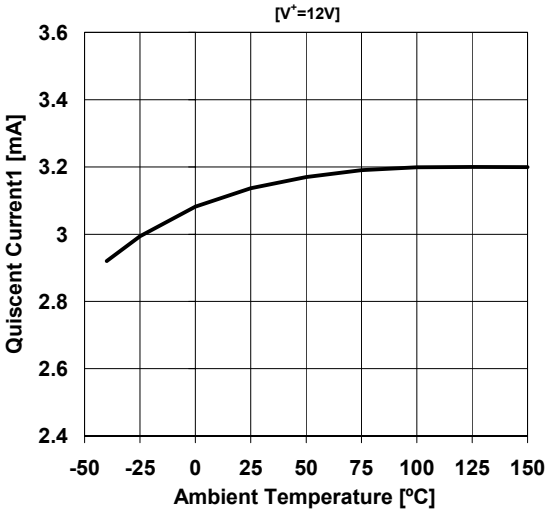
Quiescent Current1 vs. Supply Voltage Characteristic



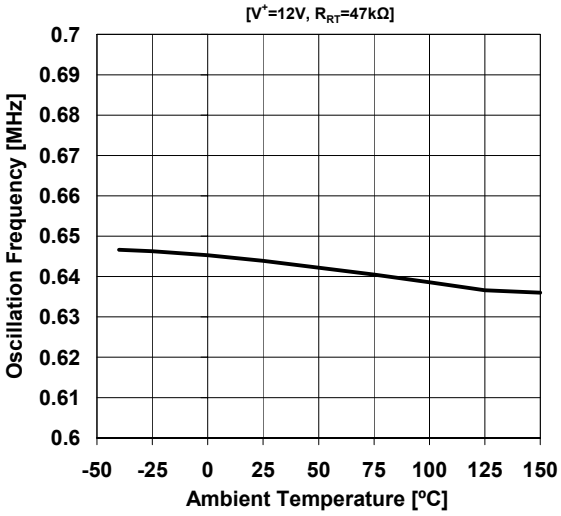

REG Pin Voltage vs. Supply Voltage Characteristic



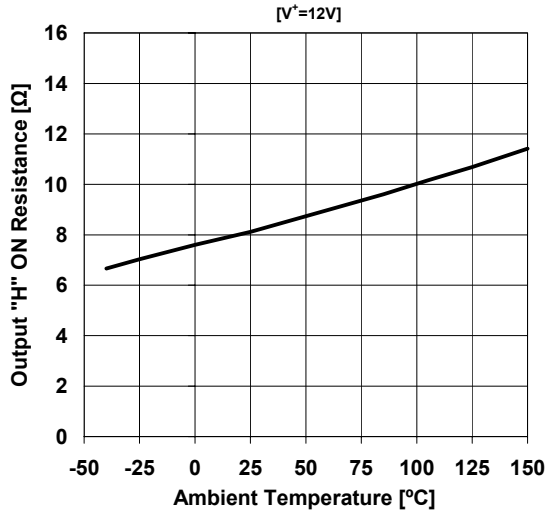

Quiscent Current1 vs. Ambient Temperature Characteristic
[$V^+$=12V]



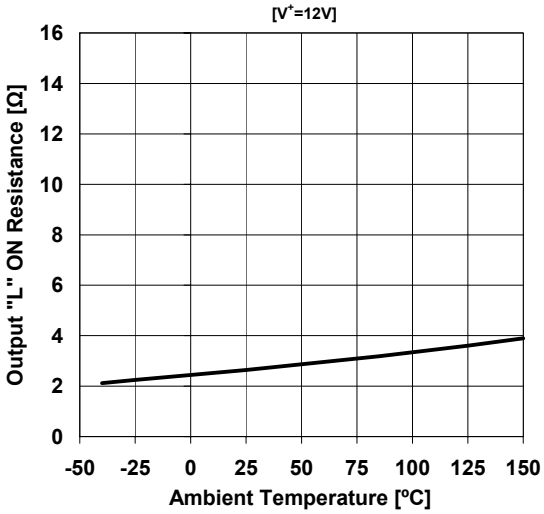

Oscillation Frequency vs. Ambient Temperature Characteristic
[$V^+$=12V, $R_{RT}$=47kΩ]




Output "H" ON Resistance vs. Ambient Temperature Characteristic
[$V^+$=12V]

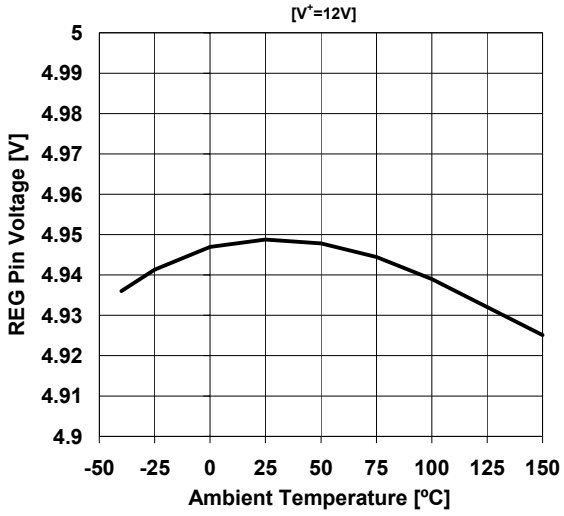



Output "L" ON Resistance vs. Ambient Temperature Characteristic
[$V^+$=12V]

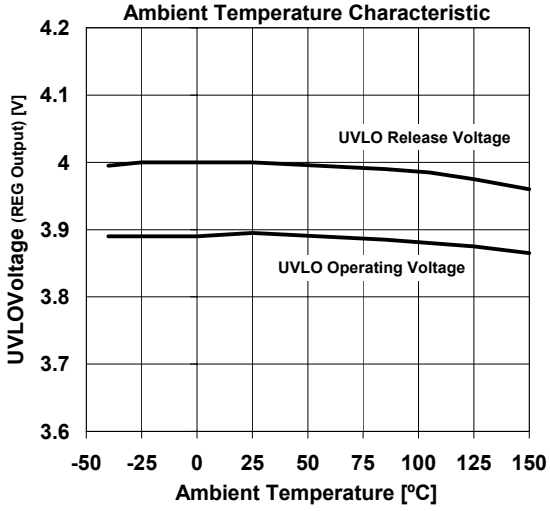


■ ELECTRICAL CHARACTERISTICS

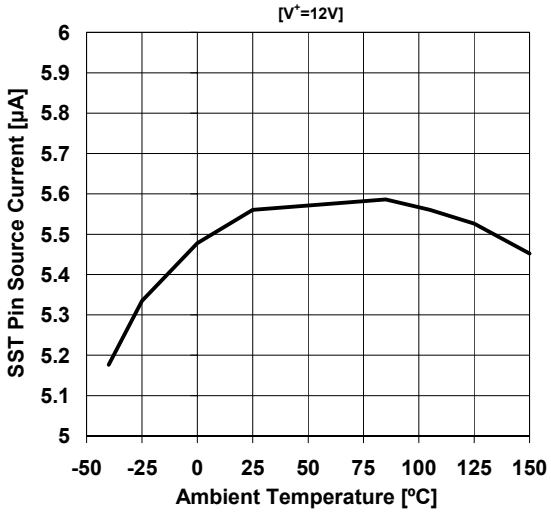
REG Pin Voltage vs.
Ambient Temperature Characteristic
[V+=12V]



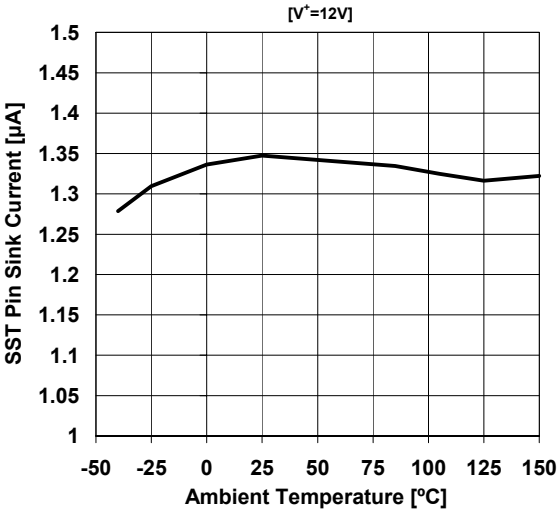

UVLOVoltage (REG Output) vs.
Ambient Temperature Characteristic



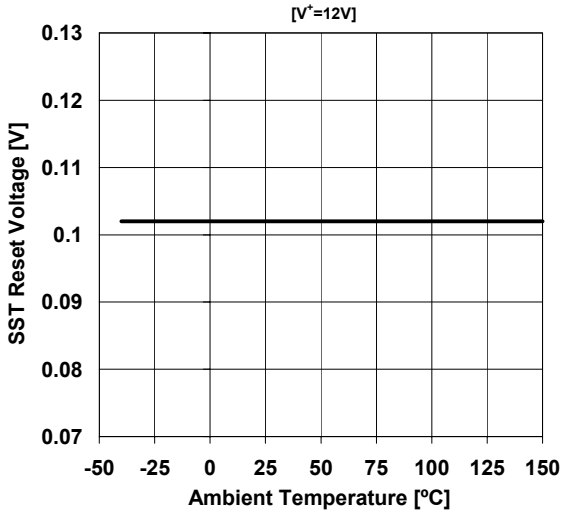

SST Pin Source Current vs.
Ambient Temperature Characteristic
[V+=12V]




SST Pin Sink Current vs.
Ambient Temperature Characteristic
[V+=12V]

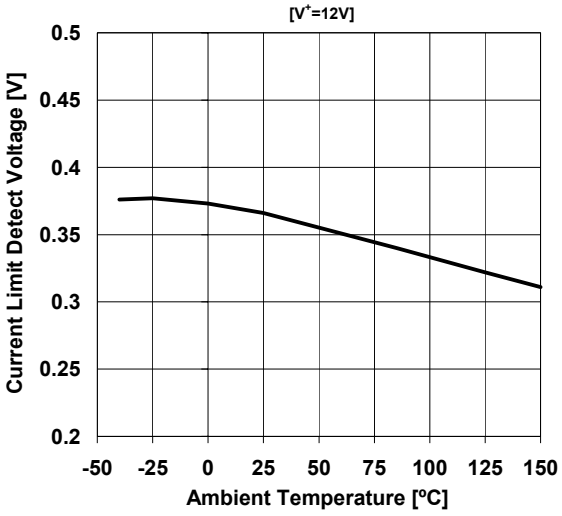



SST Reset Voltage vs.
Ambient Temperature Characteristic
[V+=12V]

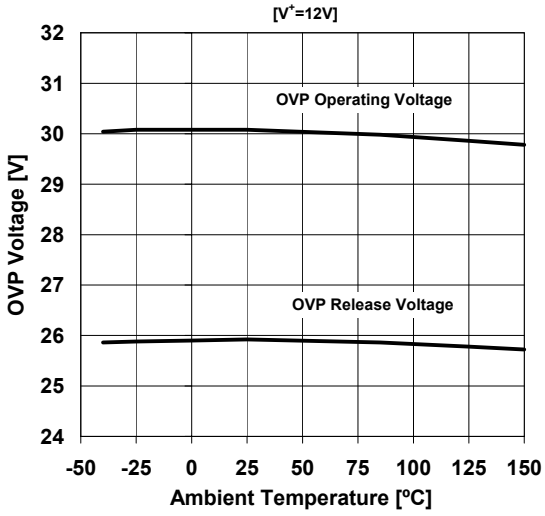


■ ELECTRICAL CHARACTERISTICS

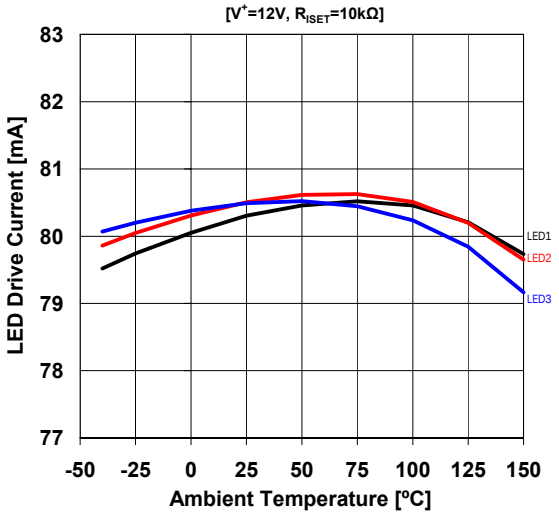
Current Limit Detect Voltage vs.
Ambient Temperature Characteristic
[$V^+$=12V]



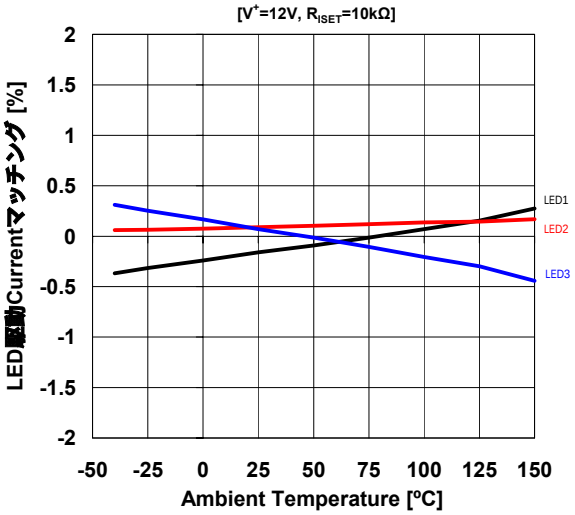

OVP Voltage vs.
Ambient Temperature Characteristic
[$V^+$=12V]




LED Drive Current vs.
Ambient Temperature Characteristic
[$V^+$=12V, $R_{ISET}$=10kΩ]



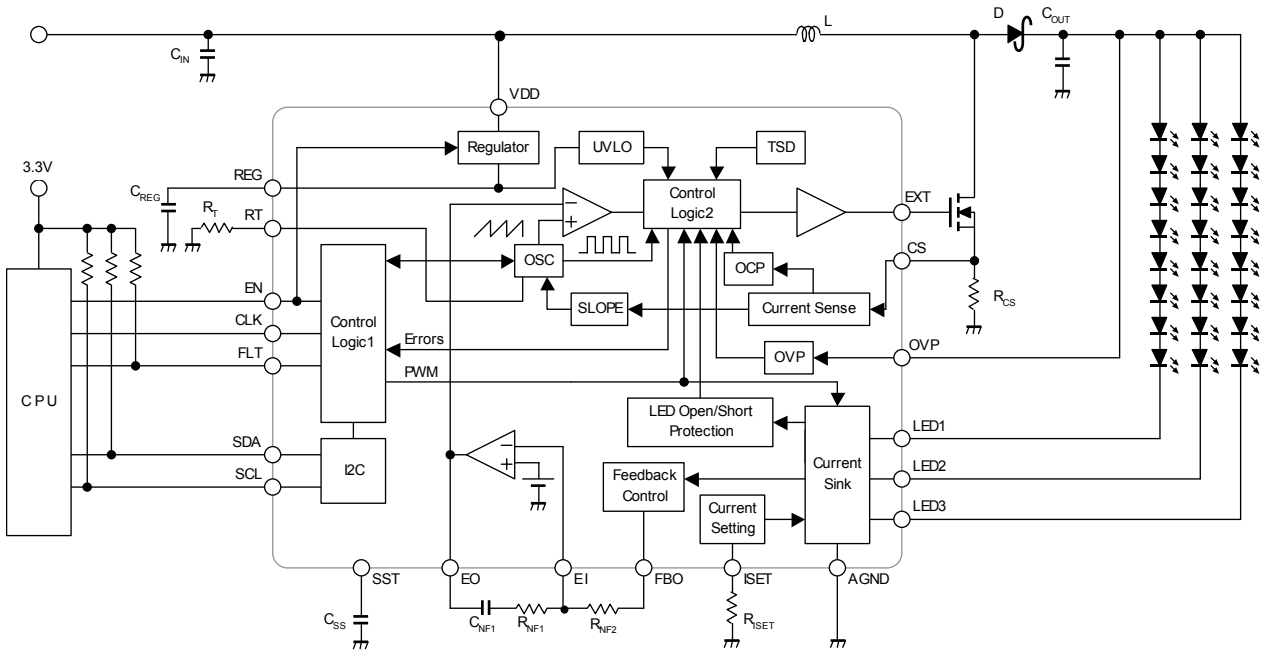

LED Drive Current Matching vs.
Ambient Temperature Characteristic
[$V^+$=12V, $R_{ISET}$=10kΩ]



## ■ PIN DISCRIPTION

| PIN NAME | FUNCTION |
|---|---|
| AGND | GND Pin for Analog Block |
| CLK | External Clock Input Pin |
| CS | Boost Circuit Current Detect Pin |
| EI | Error Amplifier Input Pin |
| EN | Enable Pin |
| EO | Error Amplifier Output Pin |
| EXT | Output Pin for External Power MOSFET Driving |
| FBO | Feedback Control Output Pin |
| FLT | Fault Status Output Pin (Open Drain Type)<br>"L" Level at Normal Operation<br>"High Impedance" at Fault Detection |
| ISET | ILED Setting Resister Connect Pin |
| IGND | GND Pin for Constant Current Circuit |
| LED1 | Constant Current Circuit Output Pin |
| LED2 | |
| LED3 | |
| N.C. | Non Connection |
| OVP | Over Voltage Protection Circuit Sense Pin |
| REG | Built-in Regulator (5V) Output Pin |
| SCL | I2C Serial Clock Input Pin |
| SDA | I2C Serial Data Input Pin |
| SST | Soft Start Capacitor (CSS) Connect Pin |
| RT | Oscillating Frequency Setting Pin |
| VDD | Power Supply Pin |

## ■ TYPICAL APPLICATION



## ■ Description of Functions

### 1. GENERAL

The NJW4605 is a high efficiency multiple strings white LED driver for backlight. This device is composed with 3-channel constant current drivers, step-up switching regulator that can drive up to 24pcs LED. Each constant current driver is able to supply maximum current of 80mA per channel. And the accuracy of supply current between each driver is ±2.0% (max.) controlled by high precision current control circuit. The NJW4605 can control luminance by PWM signal input, and also features variable switching frequency between 300kHz and 1MHz. The NJW4605 operates over a wide supply voltage range from 6V to 30V, and operating temperature is up to 105ºC. One of big feature of the NJW4605 is gradual dimming function. It can realize natural dimming by built-in pulse dimming signal-generating circuit.

The NJW4605 has various protection circuits: LED Open/Short Protection, Over Current Protection, Over Voltage Protection, Thermal Shutdown, Under voltage Lockout and ISET pin Short Protection. When these protection circuits detect fault status, it can be read the fault status by I2C interface.

### 2. LED Luminance Setting

There are 4 methods for LED Luminance Setting as follows.

2.1 LED Current Setting by ISET Pin
2.2 LED Current Magnification Setting
2.3 LED Luminance Setting by External Input Pulse Dimming Signal
2.4 LED Luminance Setting by Internal Pulse Dimming Circuit

2.1 LED Current Setting by ISET Pin

The LED current can be set connecting resistance ($R_{ISET}$) between the ISET Pin and the AGND Pin.
The Maximum LED current range can be set in the 5mA to 10mA range. The equation is the following.

ILED1 to ILED3 = 800 [times] × 1.0 [V] / $R_{ISET}$ = 800 / $R_{ISET}$

(Ex. ILED = 80mA setting, $R_{ISET}$=10kΩ)

2.2 LED Current Magnification Setting

The LED current can be set 18-pattern magnification against ILED (MAX) that set by $R_{ISET}$. It will set by the I2C instruction. (Refer to 9.4 LED Current Setting)

2.3 LED Luminance Setting by External Input Pulse Dimming Signal

It can set the LED luminance by DUTY cycle of CLK pin input signal.
CLK pin voltage is “H”: LEDs turn on.
CLK pin voltage is “L”: LEDs turn off and LED pin becomes high impedance.

2.4 LED Luminance Setting using Internal Pulse Dimming Circuit

The NJW4605 has Pulse Dimming Circuit (Gradual Dimming Circuit).
1/1024 at the frame period is controlled as minimum PWM width of at the pulse dimming circuit. You can set the frame frequency and the pulse dimming signal width.
One (1) period of Pulse Dimming Signal becomes one (1) frame.
It will set by the I2C instruction. (Refer to 9.7 Pulse Dimming Data Setting)

### 3. Gradual Dimming

The Gradual Dimming is a function that changes it while interpolating the middle data to the PWM data newly set from the PWM data that has already been set. It can realize natural dimming by pulse dimming signal using 1024 step. The gradual dimming effect/no effect, gradual dimming execution time and calculation table will set by the I2C instruction.
(Refer to 9.6 Gradual Dimming Setting and 9.8 Gradual Dimming Start)

**4. Standby Mode**

When the EN pin voltage is less than EN Pin "L" Level Voltage ($V_{IL\_EN}$), the NJW4605 becomes standby mode. At this time, each pin status is the following. If standby mode is not used, you should connect the EN pin to VDD pin.

| EN | Each Pin Status at Standby Mode | | | | | |
|---|---|---|---|---|---|---|
| | REG | FLT | EXT | LED1-3 | SST | OVP |
| $EN \leq V_{IL\_EN}$ | 0V | Hi-Z | 0V | Hi-Z | 0V | Hi-Z |

**5. Fault Output**

The FLT pin is NMOS FET open drain output. At normal operating, the NMOS FET is ON. When any protection circuits were working, the NMOS FET is OFF and becomes high impedance. It can detect a fault status via RFLT (47kΩ) by connecting to REG pin or external power supply. The fault-detected conditions are as follows.

| INPUT | CONDITION | DESCRIPTION |
|---|---|---|
| REG | $V_{REG} \leq V_{RUVLO}$ | UVLO Circuit Operating |
| OVP | $V_{OVP} \geq V_{DOVP}$ | Over Voltage Protection Operating |
| LED1 to 3 | $V_{LED} \geq V_{LED\_SHORT}$ | LED Short Detection at any one of LED line. |
| | $V_{LED} \leq V_{LED\_OPEN}$ , $V_{OVP} \geq V_{DOVP}$ | LED Open Detection at any one of LED line. |
| EN | $V_{EN} \leq V_{IL\_EN}$ | Standby Mode |
| ISET | $I_{LED1\sim3} \geq I_{LED\_MAX}$ | ISET Pin short Protection |
| Temperature | $Tj \geq Tjmax$ | Thermal Shutdown Circuit Operating over Tjmax |
| CS | $V_{CS} \geq V_{DCS}$ | Over Current Protection Timer Latch Mode.<br>(In the case of the state of $V_{CS} \geq V_{DCS}$ continues at the time of $T_{CST}$ or more.) |

[Explanation of Sign in Table]

$V_{RUVLO}$: UVLO Release Voltage $V_{DOVP}$: OVP Operating Voltage $V_{LED\_SHORT}$: LED Short Protection Detection Voltage
$I_{LED\_MAX}$: Maximum LED Current $V_{CS}$: CS Pin Voltage $V_{LED\_OPEN}$: LED Open Protection Detection Voltage
$V_{LED}$: LED Pin Voltage $V_{EN}$: EN Pin Voltage $V_{IL\_EN}$: EN Pin "L" Level Voltage
$V_{OVP}$: OVP Pin Voltage $V_{REG}$: REG Pin Voltage
Refer to electrical characteristics about detail spec

It can be confirmed a fault status by data reading from serial interface. You should remove a fault cause to release fault status.

Regarding each string LED Open /Short Protection circuit, only when each LED pin setting is enabled it is effective. Therefore, with setting to disable status the LED pin that is detected open/short by initial setting instruction, FLT output becomes normal operation (output). However because the error information remains to internal register, it returns the error flag information by reading out of I2C interface until the information is reset by the EN pin and so on.

It can be inverted the output logic and control of FLT Pin by initial instruction. (Refer to 9.2.2 FLT Pin Output Control)

**6. Soft Start**

The soft start function works when shifting to turn on state from turn off state of lighting after the power supply is turned on. The soft start execution time is decided by soft start capacity CSS and the load current. The SST pin charging current is 5μA (typ.) during soft start operating. During the CSS charging time, the PWM output DUTY that output from the EXT pin is limited on the condition that the SST pin voltage ($V_{SST}$) is less than the EO pin voltage ($V_{EO}$). And, when the following protection circuit operations were detected, the CSS is discharged and VSST becomes to 0V. When it returns to normal operating status from this status, the soft-start function restarts. Also when it returns to normal operation from standby mode by EN pin, a soft start function operates.

| INPUT | Re-SOFT START CONDITION | CONDITION DESCRIPTION |
|---|---|---|
| REG | $V_{REG} \leq V_{RUVLO}$ | UVLO Circuit Operating |
| OVP | $V_{OVP} \geq V_{DOVP}$ | Over Voltage Protection Operating.<br>Discharging by $I_{SST\_SINK}$(1.25μA Typ.) |
| Temperature | $Tj \geq Tjmax$ | Thermal Shutdown Circuit Operating over Tjmax |
| ISET | $I_{ISET} \geq I_{SET\_MAX}$ | ISET Pin short Protection |

**7. Internal Clock, External Clock and Synchronization with External Clock**

The internal clock is used for the system clock and the switching frequency of the power transistor of the boost circuit. The internal clock frequency can be adjusted in range of from 300kHz to 1MHz by the resistance of between AGND pin and RT pin. Moreover, it is able to input an external clock from the CLK pin. The internal clock and the external clock are switched by the instruction. When the power supply is turned on, the internal clock is used.

When the external clock is used, you select either the system clock or the pulse dimming signal by the instruction. (You should select the [Synchronization with External Clock] when you want to adjust the switching frequency of boost circuit power transistor.)

【Synchronization with External Clock】

When using the internal clock it synchronizes to the external clock by inputting the external clock that is faster than the built-in oscillation circuit frequency from the CLK pin. You should set the external clock frequency with the range of up to +50% against built-in oscillation frequency. Moreover, should set the DUTY ratio within the range of 40 to 60%

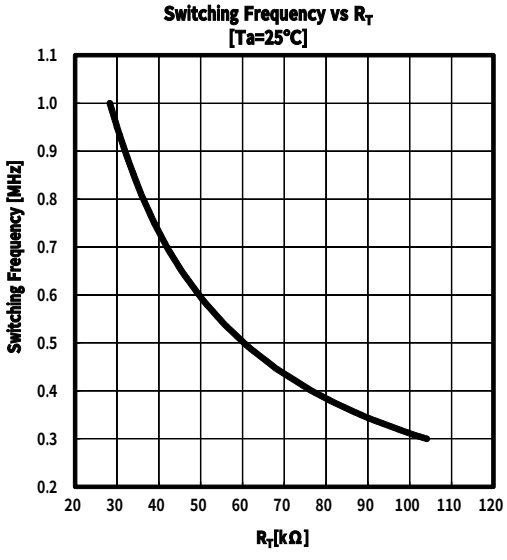
*) The system clock is used to clock for the gradual dimming circuit operation and for clock pulse dimming signal generation. Moreover, it is used for the timer of the protection circuit.

【Oscillation Frequency】

The internal Oscillation Frequency is calculated by the following equation.

$$R_T[k\Omega] = \frac{30550}{f_{osc}[kHz]} \times \alpha \quad (\alpha: \text{Correction Value})$$

| $f_{OSC}$[kHz] | correction valueα |
|---|---|
| 1000 | 0.957 |
| 950 | 0.965 |
| 900 | 0.973 |
| 850 | 0.978 |
| 800 | 0.983 |
| 750 | 0.988 |
| 700 | 0.993 |
| 650 | 1 |
| 600 | 1.008 |
| 550 | 1.015 |
| 500 | 1.022 |
| 450 | 1.028 |
| 400 | 1.036 |
| 350 | 1.046 |
| 300 | 1.057 |



**8. Protection Circuits**

| | Detect Pin | Each Pin Status at Any Protection Circuit Operating | | | | |
|---|---|---|---|---|---|---|
| | | FLT | EXT | LED1 to 3 | SST | |
| LED Short Protection | LED1 to 3 | Hi-Z | – | Hi-Z | – | LED Pin that is short circuit detected becomes Hi-Z |
| LED Open Protection | LED1 to 3 | Hi-Z | – | – | – | |
| Over Current Protection | CS | – | L | – | – | Release per Oscillation Cycle |
| Over Current Protection Timer Latch | CS | Hi-Z | L | – | – | |
| Over Voltage Protection | OVP | Hi-Z | L | Hi-Z | L | Released LED Short Protection |
| Thermal Shutdown | – | Hi-Z | L | Hi-Z | L | |
| UVLO | REG | Hi-Z | L | Hi-Z | L | |
| ISET Pin Short Protection | ISET | Hi-Z | L | Hi-Z | L | |

* It can be changed the state of FLT Pin by the instruction. (Refer to 9.2.2 FLT Pin Output Control)
About the above table, it is in the case of default setting (FT1=FT0=0).

8.1 LED Short Protection

When some LED pin voltage becomes more than LED Short Protection detection voltage, the constant current circuit operation of this LED pin stops. Other constant current circuit and boost circuit that normally operates continue to operate. This circuit has detection delay time (approx. 50μs) to prevent malfunction by LED pin voltage ringing. The operation release condition of the short protection circuit is the following.

To be standby state by dropping EN pin voltage.
To operate the UVLO circuit by dropping power supply voltage ($V^+$).
To operate Over Voltage Protection Circuit by doing OVP pin voltage more than $V_{DOVP}$.

8.2 LED Open Protection

The overvoltage protection operates when the OVP pin voltage becomes more than the OVP operation voltage ($V_{DOVP}$). At that time, when the one of the LED pin voltage is less than the LED open protection detection voltage ($V_{LED\_OPEN}$), the LED will be detected as open failure. As the result, the voltage signal of the LED pin is disconnected from the boost circuit. The overvoltage protection is released by this function then the boost circuit restarts. And the boost circuit output voltage is controlled by the voltage signal of remaining LED pin. Then the normal LED string will re-light.

The LED pin of the LED open protection status will return to normal operation when it becomes more than the LED open detection voltage protection ($V_{LED\_OPEN}$). Moreover, the FLT pin status returns to the output at the time of a normal operation.

8.3 Over Current Protection

When the difference voltage between the CS pin and the AGND pin becomes more than the current limitation detection voltage, the EXT pin voltage becomes to "L" level by the over current protection circuit. As a result, the overcurrent is prevented from flowing to external MOSFET for the boost circuit.

The overcurrent protection operation operates by the pulse-by-pulse method per each rise pulse. Moreover, it can latch after a definite period of time by combining with a timer latch function. For example, when the pulse-by-pulse type OCP operates 1024 times, the EXT pin is fixed to L level and the boost circuit will stop. To cancel the timer latch, after removing the over-current cause, it will be reset by the instruction or switch to standby mode.
(Refer to 9.5 Over Voltage Protection Threshold Voltage/Over Current Protection Setting)

8.4 Over Voltage Protection

When you want to use the OVP function, should connect the OVP pin to the boost circuit output terminal. (Refer to TYPICAL APPLICATION) When the boost circuit output voltage carries out an abnormal rise and exceeds OVP operating voltage ($V_{DOVP}$), the boost circuit operation stops and the LED1/2/3 driving current stops, too. The overvoltage protection circuit operation will drop the OVP pin voltage to sink by the OVP pin input current2 ($I_{OVP2}$). In addition, the SST pin voltage will drop taking a definite period of time by the SST pin sink current ($I_{SST\_SINK}$). By this function, when the overvoltage protection circuit operates, certain delay time is given for the re-soft start.

When the OVP pin voltage becomes less than the OVP release voltage ($V_{ROVP}$) and the SST pin voltage becomes less than the SST reset voltage ($V_{SST\_RES}$), the overvoltage protection will be released and the soft start will restart.

It can be selected the OVP operating voltage ($V_{DOVP}$) from 3 (three) values by the instruction.

(Refer to 9.5 Over Voltage Protection Threshold Voltage/Over Current Protection Setting)

8.5 Thermal Shutdown

When the chip junction temperature exceeds Tjmax, internal thermal shutdown circuit operates and internal boost circuit stops. When the chip junction temperature goes down than Tjmax, internal thermal shutdown circuit operating is released. And at this time, soft-start operation is restarted.

8.6 Under Voltage Lockout (UVLO)

When the REG pin voltage drops less than the UVLO operating voltage ($V_{DUVLO}$) by the power supply startup time or power supply voltage dropping, the UVLO circuit operates. At this time, the EXT pin output becomes “L” level and the LED1 to LED3 driving current is stopped. And the FLT pin becomes high impedance. When the REG pin voltage becomes more than the UVLO release voltage ($V_{RUVLO}$), the UVLO function is released.

When the UVLO circuit operates, all system is reset. Therefore, all instruction register value becomes zero (0).

8.7 ISET Pin Short Protection

When the ISET pin is shorted to AGND or IGND, a driven LED may break down by overcurrent. To prevent a LED breaking down, the ISET pin sink current ($I_{SET}$) exceeds the ISET pin short detecting current ($I_{SET\_MAX}$), the ISET pin short protection circuit operates. At this time, the internal boost circuit operation stops, too.

When the ISET pin sink current ($I_{SET}$) becomes less than the ISET pin short detecting current ($I_{SET\_MAX}$), the ISET pin short protection function is released.

8.8 Fault Status

When any one of the above protection circuits (8.1 to 8.7) operates, the error flag is generated internally as latch signal. The fault status can be read from the serial interface. (Refer to 9.9 Fault/BUSY)

8.9 External Clock Signal Synchronization Function of internal oscillation frequency

It can be synchronized internal oscillation frequency to Clock signal input from CLK pin. The synchronization range is +50% against the internal oscillation frequency set by RT.

**9. Serial Interface**

I2C Slave Address is 0110_001x.

- WRIGHT 62h
- READ 63h

Parity Bit

You should send the parity to MSB so that 1 of parity bit data becomes odd-number. When the parity bit is match, the data becomes effective. The setting example is the following.

| Setting Data | Parity | Parity Bit Data |
|---|---|---|
| 0001_1011b[1Bh] | 1 | 1001_1011b[9Bh] |
| 0110_1110b[6Eh] | 0 | 0110_1110b[6Eh] |

When the parity is not match, the ACK is not return and the later data is ignored. When the parity is not match, you should re-send the data from start condition. The parity bit is not into the I2C slave address.

9.1 Instruction Table

It is available the operating setting and fault reading by I2C interface.

It is possible to write in an instruction continuously by auto-increment function, until I2C stop conditions are satisfied.

(*: Don't care)

| INSTRUCTION | | ADDRESS | FUNCTION | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| (1) | INITIAL SETTING | 00h | PRTY | EXT1 | EXT0 | FT1 | FT0 | LED3EN | LED2EN | LED1EN | LED1 Pin ON/OFF (LED1EN)<br>LED2 Pin ON/OFF (LED2EN)<br>LED3 Pin ON/OFF (LED3EN)<br>FLT Pin Output Control (FT1 to FT0)<br>External Clock/Pulse Dimming Signal Input Switching (EXT1 to EXT0) |
| (2) | FRAME FREQUENCY SETTING | 01h | PRTY | * | * | FD4 | FD3 | FD2 | FD1 | FD0 | Frame Frequency Divide Rate Setting (FD4 to FD0) |
| (3) | LED CURRENT SETTING | 02h | PRTY | * | * | * | I3 | I2 | I1 | I0 | LED Current Magnification Setting (I3 to I0) |
| (4) | OVER VOLTAGE PROTECTION THRESHOLD /OVER CURRENT PROTECTION SETTING | 03h | PRTY | SLOPE | OCP | OCP1 | OCP0 | OCPTIM | OVP1 | OVP0 | Over Voltage Protection Threshold Setting (OVP1 to OVP0)<br>Over Current Protection Setting (OCP, OCP1 to OCP0, OCPTIM)<br>Current Feedback Rate Switching (SLOPE) |
| (5) | GRADUAL DIMMING SETTING | 04h | PRTY | * | * | COEF1 | COEF0 | FRM2 | FRM1 | FRM0 | Gradual Dimming Frame Setting: (FRM2 to FRM0)<br>Gradual Dimming Coefficient Setting: (COEF1 to COEF0) |
| (6) | PULSE DIMMING SIGNAL DATA SETTING | 05h | PRTY | PWM10 | PWM9 | PWM8 | PWM7 | PWM6 | PWM5 | PWM4 | Pulse Dimming Signal: PWM higher-order Data Setting |
| | | 06h | PRTY | * | * | * | PWM3 | PWM2 | PWM1 | PWM0 | Pulse Dimming Signal: PWM Lower-order Data Setting |
| (7) | GRADUAL DIMMING START | 07h | PRTY | * | * | * | * | * | SKIP | START | Gradual Dimming Start (START)<br>Not use Gradual Dimming (SKIP) |
| | DO NOT USE | 08h ~ FFh | * | * | * | * | * | * | * | * | DO NOT USE |

Note1; PRTY: Parity Bit

Note2: When the UVLO operates, system is reset. At this time, all instruction register value becomes zero (0).

**Instruction Code**

9.2 Initial Setting

It can be set ON/OFF of the LED Pin and Clock changing by initial instruction.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 00h | PRTY | EXT1 | EXT0 | FT1 | FT0 | LED3EN | LED2EN | LED1EN |

9.2.1 LED Pin Enable

LED1EN: LED1 Pin Enable/Disable Switching

LED2EN: LED2 Pin Enable/Disable Switching

LED3EN: LED3 Pin Enable/Disable Switching

0: Disable State (LED Turn-off)

1: Enable State

The error flag signal is not output from pin(s) of disabled status. The FLT pin output changes to normal operation output with to set to disable status the LED pin that is detected open/short. However because the error information remains to internal register, it can read the error flag information out. With to clear the error flag information or to reset by the EN pin and so on, the internal register is reset. When to set to enabled status any one of LED3EN, LED2EN and LED1EN from all pin disabled status, the soft start circuit will start.

9.2.2 FLT Pin Output Control

FT1: Error Flag Operating Status Switching (Non-inverted/Inverted Output) from FLT Pin

FT0: Forced Output Fixed of FLT Pin

At Power Supply On, FT1 and FT2 become 0(zero) during UVLO operation.

| FT1 | FT0 | FLT Pin | At Normal Operating | At Protection Circuit(s) Operating |
|---|---|---|---|---|
| 0 | 0 | Status Output | 0V | Hi-Z |
| 0 | 1 | Status Inverted Output | Hi-Z | 0V |
| 1 | 0 | Forced 0 voltage Output | 0V | 0V |
| 1 | 1 | Forced Hi-Z Output | Hi-Z | Hi-Z |

9.2.3 External Clock/Pulse Dimming Signal Input Switching

EXT1, EXT0:

The signal from CLK Pin is changed to “System Clock” or “Pulse Dimming Signal”.

| EXT1 | EXT0 | Boost Circuit Clock (*) | System Clock | Pulse Dimming Signal |
|---|---|---|---|---|
| 0 | 0 | Built-in Oscillation/CLK Pin Input (Synchronization with Clock Signal) | Built-in Oscillation/CLK Pin Input (Synchronization with Clock Signal) | Generated by Gradual Dimming Circuit (Synchronization with System Clock) |
| 0 | 1 | Built-in Oscillation | CLK Pin Input Clock Signal | Generated by Gradual Dimming Circuit (Synchronization with System Clock) |
| 1 | 0 | Built-in Oscillation | Built-in Oscillation | CLK Pin Input Signal (Synchronization with System Clock) |
| 1 | 1 | Built-in Oscillation | Built-in Oscillation | CLK Pin Input Signal |

* Boost Circuit Clock: it is the switching signal of power transistor of boost circuit.

At EXT1=EXT0=0 Setting

- A built-in oscillator is used by shorting the CLK pin and the REG pin or the AGND pin .
- Through the inputting of a faster clock signal than built-in oscillator frequency to the CLK pin, it can synchronize input clock signal and built-in oscillator frequency.

At EXT1=0, EXT0=1 Setting

- The input clock signal from the CLK pin is used as the system clock. Since the pulse dimming signal is generated from the system clock, it synchronizes with the clock signal inputted from the CLK pin. The built-in oscillator frequency is used as the boost circuit clock.

At EXT1=1, EXT0=0 Setting

- The input clock signal from the CLK pin is used as the pulse dimming signal. At this time, the gradual dimming circuit stops. The pulse dimming signal is retimed by built-in oscillation frequency. Therefore, the pulse dimming signal slower than the system clock period is lost. Moreover, the pulse dimming signal is output synchronized to built-in oscillator frequency. The built-in oscillator frequency is used as the boost circuit clock.

At EXT1=1, EXT0=1 Setting

- The input clock signal from the CLK pin is used as the pulse dimming signal. The gradual dimming circuit is stopped. The gradual dimming circuit stops. The signal that is input as the external input is output as the pulse dimming signal as it is. The built-in oscillator frequency is used as the boost circuit clock.

9.3 Frame Frequency Setting

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 01h | PRTY | * | * | FD4 | FD3 | FD2 | FD1 | FD0 |

9.3.1 Frame Frequency Setting

FD4 TO FD0:

It can set the frame frequency of gradual dimming. The frame frequency is decided by oscillation frequency (or external clock frequency) and set frame divided rate. You should select appropriate oscillation frequency and divided rate (table below) according to your application.

Frame Divide Rate Setting

| FD4 | FD3 | FD2 | FD1 | FD0 | Divide Rate | Frame Frequency (Hz) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | $f_{OSC}$ =800kHz | $f_{OSC}$ =1MHz | $f_{OSC}$ =1.5MHz |
| 0 | 0 | 0 | 0 | 0 | 1 | 781 | 977 | 1465 |
| 0 | 0 | 0 | 0 | 1 | 1/2 | 391 | 488 | 732 |
| 0 | 0 | 0 | 1 | 0 | 1/3 | 260 | 326 | 488 |
| 0 | 0 | 0 | 1 | 1 | 1/4 | 195 | 244 | 366 |
| 0 | 0 | 1 | 0 | 0 | 1/5 | 156 | 195 | 293 |
| 0 | 0 | 1 | 0 | 1 | 1/6 | 130 | 163 | 244 |
| 0 | 0 | 1 | 1 | 0 | 1/7 | 112 | 140 | 209 |
| 0 | 0 | 1 | 1 | 1 | 1/8 | 98 | 122 | 183 |
| 0 | 1 | 0 | 0 | 0 | 1/9 | 87 | 109 | 163 |
| 0 | 1 | 0 | 0 | 1 | 1/10 | 78 | 98 | 146 |
| 0 | 1 | 0 | 1 | 0 | 1/11 | 71 | 89 | 133 |
| 0 | 1 | 0 | 1 | 1 | 1/12 | 65 | 81 | 122 |
| 0 | 1 | 1 | 0 | 0 | 1/13 | 60 | 75 | 113 |
| 0 | 1 | 1 | 0 | 1 | 1/14 | 56 | 70 | 105 |
| 0 | 1 | 1 | 1 | 0 | 1/15 | 52 | 65 | 98 |
| 0 | 1 | 1 | 1 | 1 | 1/16 | 49 | 61 | 92 |
| 1 | 0 | 0 | 0 | 0 | 1/17 | 46 | 57 | 86 |
| 1 | 0 | 0 | 0 | 1 | 1/18 | 43 | 54 | 81 |
| 1 | 0 | 0 | 1 | 0 | 1/19 | 41 | 51 | 77 |
| 1 | 0 | 0 | 1 | 1 | 1/20 | 39 | 49 | 73 |
| 1 | 0 | 1 | 0 | 0 | 1/21 | 37 | 47 | 70 |
| 1 | 0 | 1 | 0 | 1 | 1/22 | 36 | 44 | 67 |
| 1 | 0 | 1 | 1 | 0 | 1/23 | 34 | 42 | 64 |
| 1 | 0 | 1 | 1 | 1 | 1/24 | 33 | 41 | 61 |
| 1 | 1 | 0 | 0 | 0 | 1/25 | 31 | 39 | 59 |
| 1 | 1 | 0 | 0 | 1 | 1/26 | 30 | 38 | 56 |
| 1 | 1 | 0 | 1 | 0 | 1/27 | 29 | 36 | 54 |
| 1 | 1 | 0 | 1 | 1 | 1/28 | 28 | 35 | 52 |
| 1 | 1 | 1 | 0 | 0 | 1/29 | 27 | 34 | 51 |
| 1 | 1 | 1 | 0 | 1 | 1/30 | 26 | 33 | 49 |
| 1 | 1 | 1 | 1 | 0 | 1/31 | 25 | 32 | 47 |
| 1 | 1 | 1 | 1 | 1 | 1/32 | 24 | 31 | 46 |

9.4 LED Current Setting

It can be set the LED current magnification by the LED Current Setting instruction.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 02h | PRTY | | | | I3 | I2 | I1 | I0 |

It can be adjusted the LED Current 16-patterns magnification by the instruction.

| I3 | I2 | I1 | I0 | Current Magnification | LED Current (typ.) ILED=80mA |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1/16 | 5.0 mA |
| 0 | 0 | 0 | 1 | 2/16 | 10.0 mA |
| 0 | 0 | 1 | 0 | 3/16 | 15.0 mA |
| 0 | 0 | 1 | 1 | 4/16 | 20.0 mA |
| 0 | 1 | 0 | 0 | 5/16 | 25.0 mA |
| 0 | 1 | 0 | 1 | 6/16 | 30.0 mA |
| 0 | 1 | 1 | 0 | 7/16 | 35.0 mA |
| 0 | 1 | 1 | 1 | 8/16 | 40.0 mA |
| 1 | 0 | 0 | 0 | 9/16 | 45.0 mA |
| 1 | 0 | 0 | 1 | 10/16 | 50.0 mA |
| 1 | 0 | 1 | 0 | 11/16 | 55.0 mA |
| 1 | 0 | 1 | 1 | 12/16 | 60.0 mA |
| 1 | 1 | 0 | 0 | 13/16 | 65.0 mA |
| 1 | 1 | 0 | 1 | 14/16 | 70.0 mA |
| 1 | 1 | 1 | 0 | 15/16 | 75.0 mA |
| 1 | 1 | 1 | 1 | 16/16 | 80.0 mA |

9.5 Over Voltage Protection Threshold Voltage/Over Current Protection Setting

It can be set the Over Voltage Protection Threshold and the Over Current Protection Circuit Operation.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 03h | PRTY | SLOPE | OCP | OCP1 | OCP0 | OCPTIM | OVP1 | OVP0 |

The Over Voltage Protection Threshold Table is as the following.

| OVP1 | OVP0 | Over Voltage Threshold (V) |
|---|---|---|
| 0 | 0 | 30.4 (typ.) |
| 0 | 1 | 34.2 (typ.) |
| 1 | 0 | 38.0 (typ.) |
| 1 | 1 | It Sinks to AGND from OVP Pin at OVP Pin Input Current2 ($I_{OVP2}$). |

Over Current Protection Circuit Operation Setteing1

| OCPTIM | Over Current Protection Circuit | | |
|---|---|---|---|
| | Protection Function | Fault Output | Gate Driver Output (EXT Pin) |
| 0 | Pulse by Pulse & Timer Latch | Output | Stop |
| 1 | Pulse by Pulse | Not Output | - |

The NJW4605 is built the over current protection circuit of 2 types.

• Pulse-by-Pulse type: It protects the circuit per switching (boost) pulse.

• Timer Latch type: When the overcurrent is detected for a certain period by the pulse-by-pulse method, the internal boost circuit is stopped and the gate driver output (EXT pin) is stopped. It can be set the overcurrent detection period by the instruction based on the time of 1024 times of the boost switching (oscillation frequency 650kHz setting (1.575ms)). When the timer latch function operates, the fault signal is output and stops the gate driver output. Selecting standby mode or changing to pulse-by-pulse mode the operation setting1 (OCPTIM) releases the latch.

Over Current Protection Circuit Operation Setteing2

| OCP1 | OCP0 | Timer Latch Detection Time |
|---|---|---|
| 0 | 0 | Oscillation Period × 1024 |
| 0 | 1 | Oscillation Period × 1024 × 2 |
| 1 | 0 | Oscillation Period × 1024 × 4 |
| 1 | 1 | Oscillation Period × 1024 × 8 |

It can be adjusted the Over Current Detection Current by changing the Current Limiting Detection Voltage.

Over Current Protection Circuit Operation Setteing3

| OCP | Current Limit Detection Voltage |
|---|---|
| 0 | 0.35V typ. (Current Limit Detection Voltage 1 $V_{DCS1}$) |
| 1 | 0.25V typ. (Current Limit Detection Voltage 2 $V_{DCS2}$) |

Current Feedback Rate Switching

Regarding the boost DC/DC converter that is PWM type with current mode, it might occur subharmonics with DUTY cycle over 50 percent from the characteristic. To prevent the subharmonics, in the NJW4605 has the slope compensation circuit. The current that flows in the inductor of the boost circuit is converted the voltage by the external current detection resistance of the CS pin. And the voltage gives feedback to the internal logic from the CS pin. The lamp signal generated with the built-in oscillation circuit and the feedback signal are summed with the slope compensation circuit. The summed signal is used to control the DC/DC converter. The feedback value can be selected from the below table by the instruction.

| SLOPE | Current Feedback Rate (typ.) |
|---|---|
| 0 | 1 |
| 1 | 1.48 |

9.6 Gradual Dimming Setting

It can set the dimming automatically.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 04h | PRTY | | | COEF1 | COEF0 | FRM2 | FRM1 | FRM0 |

The Gradual Dimming is a function that changes it while interpolating the middle data to the PWM data newly set from the PWM data that has already been set. It complements the pulse-dimming signal with maximum 1024 steps.

It can be set the reference frame number and the calculation table by the instruction. The gradual dimming function calculates the difference value between the present value and the setting value of the pulse dimming data. And, the calculation of plus (add) or minus (subtract) 1 is repeated until the present value reaches the setting value. The 1 step holding time is changed by present value, the reference frame number and the calculation table.

Reference Frame Number

| FRM2 | FRM1 | FRM0 | Reference Frame Number (FRM) |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

Calculation Table

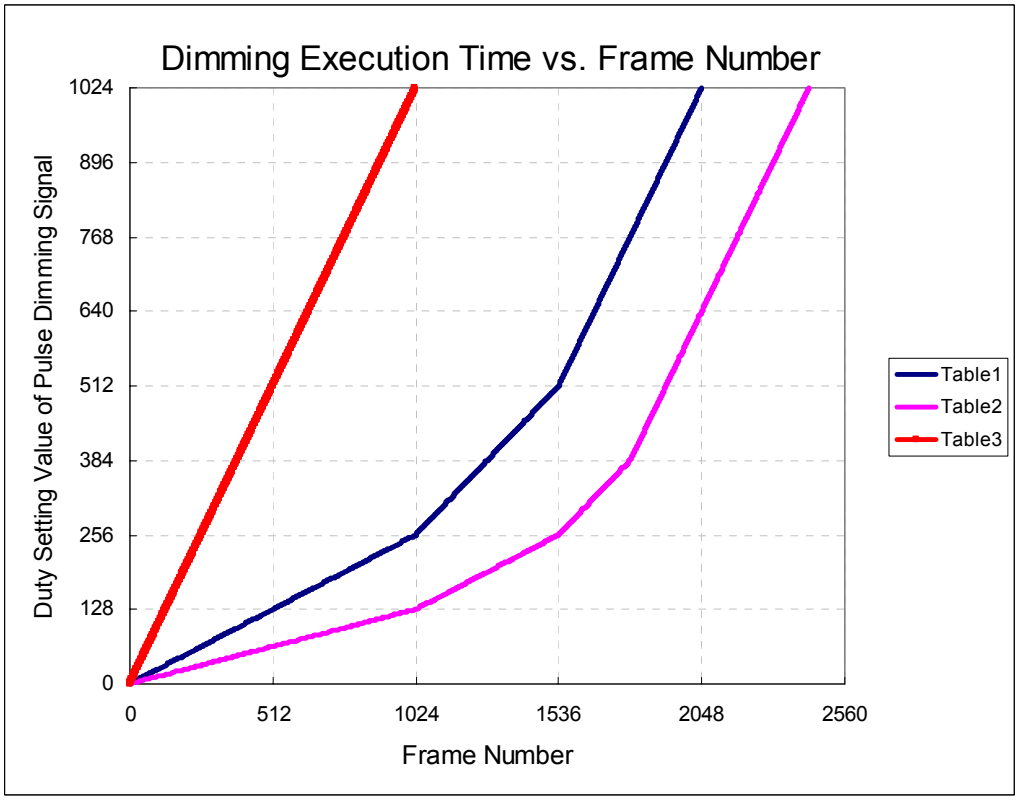
The Calculation Table is as the following.

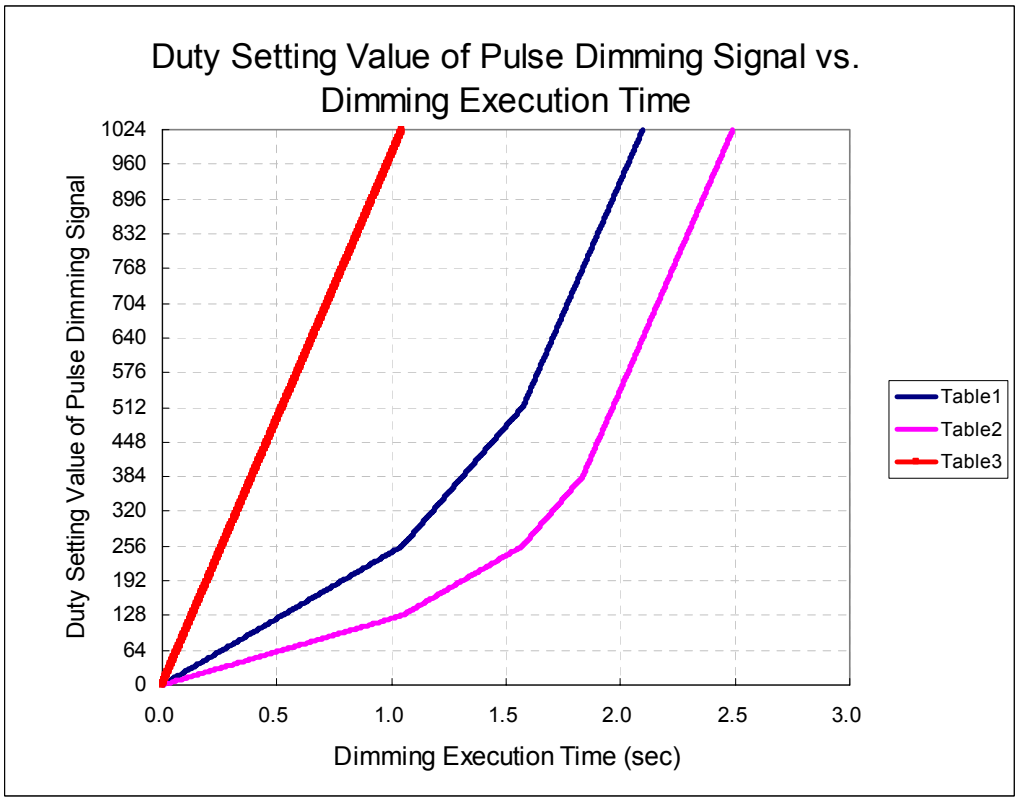
| COEF1 | COEF0 | CALCULATION TABLE |
|---|---|---|
| 0 | 0 | TABLE 1 |
| 0 | 1 | TABLE 2 |
| 1 | - | TABLE 3 (Linear Interpolation) |

The 1 step holding time and the selectable table are as follows. The 1 step holding time is changed by high-order 3 bit of the present value in table 1 and table 2. Moreover, the combination changes by selected table.

| PWM Data Present Value | | Frame Number per 1 Step | | |
|---|---|---|---|---|
| High-order 3 Bit | RANGE | TABLE 1 | TABLE 2 | TABLE 3 |
| 000 | 0 to 127 | FRM×4 | FRM×8 | FRM×1 |
| 001 | 128 to 255 | FRM×4 | FRM×4 | FRM×1 |
| 010 | 256 to 383 | FRM×2 | FRM×2 | FRM×1 |
| 011 | 384 to 511 | FRM×2 | FRM×1 | FRM×1 |
| 100 | 512 to 639 | FRM×1 | FRM×1 | FRM×1 |
| 101 | 640 to 767 | FRM×1 | FRM×1 | FRM×1 |
| 110 | 768 to 895 | FRM×1 | FRM×1 | FRM×1 |
| 111 | 896 to 1024 | FRM×1 | FRM×1 | FRM×1 |

Example of FD=1, FRM=1, $f_{OSC}$ =1MHz


Dimming Execution Time vs. Frame Number
Duty Setting Value of Pulse Dimming Signal
1024
896
768
640
512
384
256
128
0
0
512
1024
1536
2048
2560
Frame Number
Table1
Table2
Table3


Duty Setting Value of Pulse Dimming Signal vs.
Dimming Execution Time
Duty Setting Value of Pulse Dimming Signal
1024
960
896
832
768
704
640
576
512
448
384
320
256
192
128
64
0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Dimming Execution Time (sec)
Table1
Table2
Table3

9.7 Pulse Dimming Data Setting

It can set the pulse dimming data that is output to LED pin. The numbers of data steps are 1025 steps from 0 to 1024.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 05h | PRTY | PWM10 | PWM9 | PWM8 | PWM7 | PWM6 | PWM5 | PWM4 |
| 06h | PRTY | | | | PWM3 | PWM2 | PWM1 | PWM0 |

The below table shows the pulse dimming signal DUTY that corresponds with pulse dimming data.

| PWM10 | PWM9 | PWM8 | PWM7 | PWM6 | PWM5 | PWM4 | PWM3 | PWM2 | PWM1 | PWM0 | PWM DUTY |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1024 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/1024 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2/1024 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3/1024 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4/1024 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5/1024 |

⋮

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 10201024 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1021/1024 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1022/1024 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1023/1024 |
| 1 | * | * | * | * | * | * | * | * | * | * | 1024/1024 |

9.8 Gradual Dimming Start

It can be set Start/Stop of the gradual dimming function and the pulse dimming signal outputs by gradual dimming start instruction.

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 07h | PRTY | | | | | | SKIP | START |

9.8.1 Start/Stop of Gradual Dimming

START: Gradual Dimming Function Start/Stop

The gradual dimming function starts by setting of START=1 that synchronizes to frame signal. It operates that the pulse dimming data reaches up to setting value. This function operates that the pulse dimming data until the setting value. It becomes BUSY status under operation and is not able to access except address 07h. And it does not send ACK back during BUSY status. It can forced-stop by setting of START=0.

The I2C slave address and register address writing are always acceptable unaffectedly of BUSY status.

9.8.2 Skip of Gradual Dimming

SKIP: Gradual Dimming Function Skip

0: The Gradual Dimming Function is not skipped.

1: The Gradual Dimming Function is not skipped. And it outputs the Pulse Dimming Signal without Gradual Dimming Setting.

9.9 Fault/BUSY Read

| ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 00h | 0 | 0 | 0 | BUSY | OCP | TSD | ISET | OVP |
| 01h | 0 | 0 | SHORT3 | OPEN3 | SHORT2 | OPEN2 | SHORT1 | OPEN1 |
| 03h | Error Flag Clear | | | | | | | |

OVP: Over Voltage Protection Circuit
ISET: ISET Pin Short Protection Circuit (AGND)
TSD: Thermal Shutdown Circuit
OCP: Over Current Protection Circuit
BUSY: BUSY State
OPEN1 to 3: LED Open Protection Circuit
SHORT1 to 3: LED Short Protection Circuit ($V_{LED\_SHORT}$>)

The internal register clears by reading 03h (except BUSY). However when an error cause is not removed, the register is re-set.

You should read out the internal register according to the following procedure.
1. It should be sent an address that wants to be read out following the start condition and slave address (62h Write).
2. Whenever a device receives 8-bit data correctly, it sends the ACK.
3. If the start conditions and the slave address are transmitted, after that the device will transmit 8-bit data to the master. The first data is invalid. The data of 2nd byte becomes into data of the address specified first. Each time to send an ACK from the master side, the device address counter is incremented, take the following data, and becomes the waiting for sending.
4. After receiving the last data, without sending the ACK, the master should send a stop condition.
5. It should be referred to data input timing in regard to read out timing.

At the time of the power supply turns-on an error flag that wrong might be latched. (FLT status is normal operation output) Therefore, after the power supply turns-on to the first read-out of the fault status from serial interface, you should clear an error flag by carrying out 03-h read-out first. And, you should use the data from on second or subsequently.

9.10 Data Input Timing

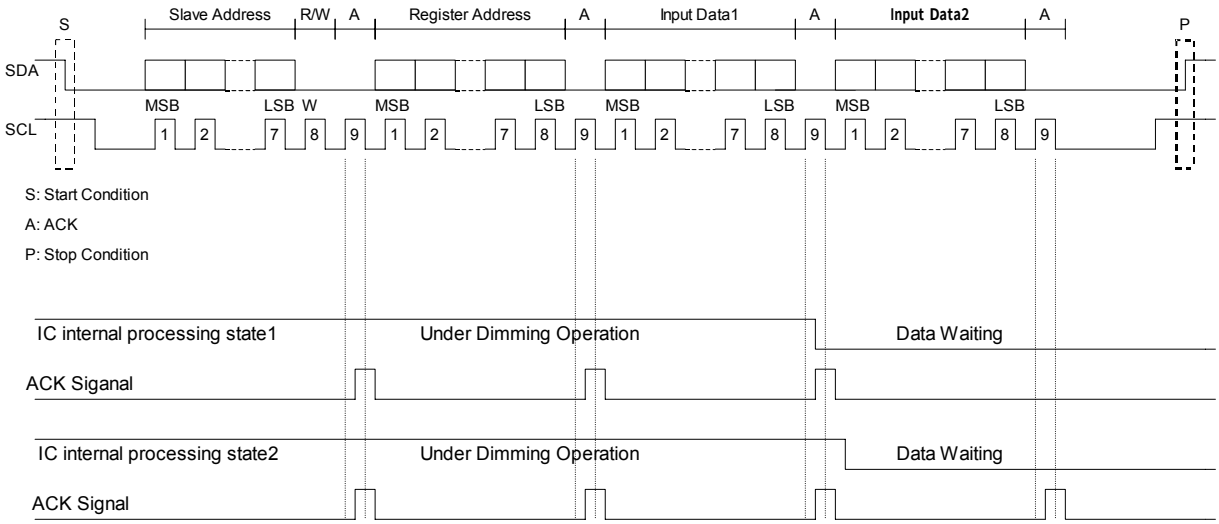
The Data Format is as the following.

In addition to the slave address, there is a register address and it is used to identify each instruction.

The SDA data is retrieved at timing of the SCL rise up.

It is possible to write in an instruction continuously by auto-increment function, until I2C stop conditions are satisfied.

9.10.1 Write Mode




① Start Condition

When the SCL pin is High level, a data reading starts with entering a falling edge to the SDA pin.

② Slave Address

You should enter a slave address and a Write condition to data of 1st byte. The slave address is (0110_0010). If the slave address was match, ACK is output at 9th bit. Do not correspond with General call address.

③ Register Address

You should enter a register address to data of 2nd byte. When the slave address is match even if the register address does not match, ACK is output at 9th bit.

④ Data

You should enter a data from 3rd byte.

Only when the internal process does not complete by gradual dimming, the ACK does not output (IC internal process status 2) against the input data. If the ACK does not output, you should re-enter a data from start condition. Regarding gradual dimming operating time, refer to 9.6 Gradual Dimming Setting.

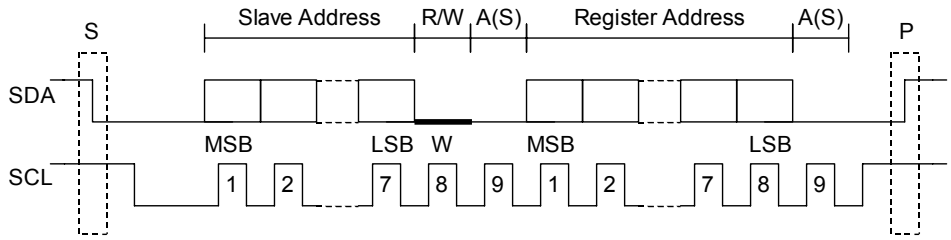
⑤ Stop Condition

When the SCL pin is high level, a data sending stops with entering a rising edge to the SDA pin.

⑥ Re-start Condition

After start condition setting when the SCL pin is high level, a data sending re-starts with entering a falling edge to the SDA pin.

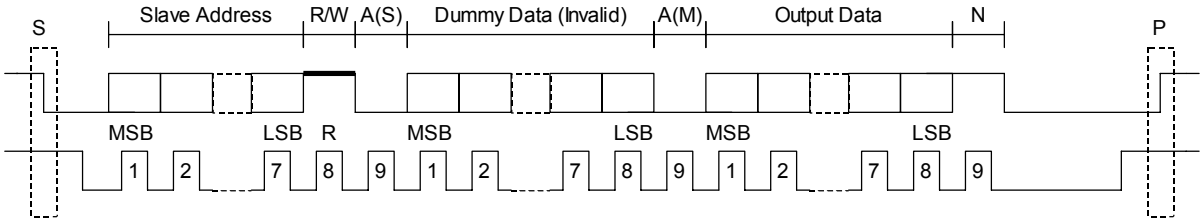
9.10.2 Read Mode




S: Start Condition
A(S): Slave Device ACK
A(M): Master Device ACK
N: NACK
P: Stop Condition

① Read Address Set

You should set the Read address like same procedure of the Write mode, Start condition, Slave address, Register address and Stop condition (arbitrarily).




② Start Condition

When the SCL pin is High level, a data reading starts with entering a falling edge to the SDA pin.

③ Slave Address

You should enter a slave address and a Read condition to data of 1st byte. The slave address is (0110_0011). If the slave address was match, ACK is output at 9th bit. Do not correspond with General call address.

④ Dummy Data

You should send the ACK from master device with read 1byte data. At this time, this data becomes invalid data. The internal register value is retrieved into a shift register by ACK.

⑤ Output Data

When the output data reads continuously, you should send the ACK from master device. The increment of the register address is carried out and data is retrieved into a shift register. The register for error flag clears when the register address becomes (0000_0011). However when an error cause is not removed, the register is re-set.

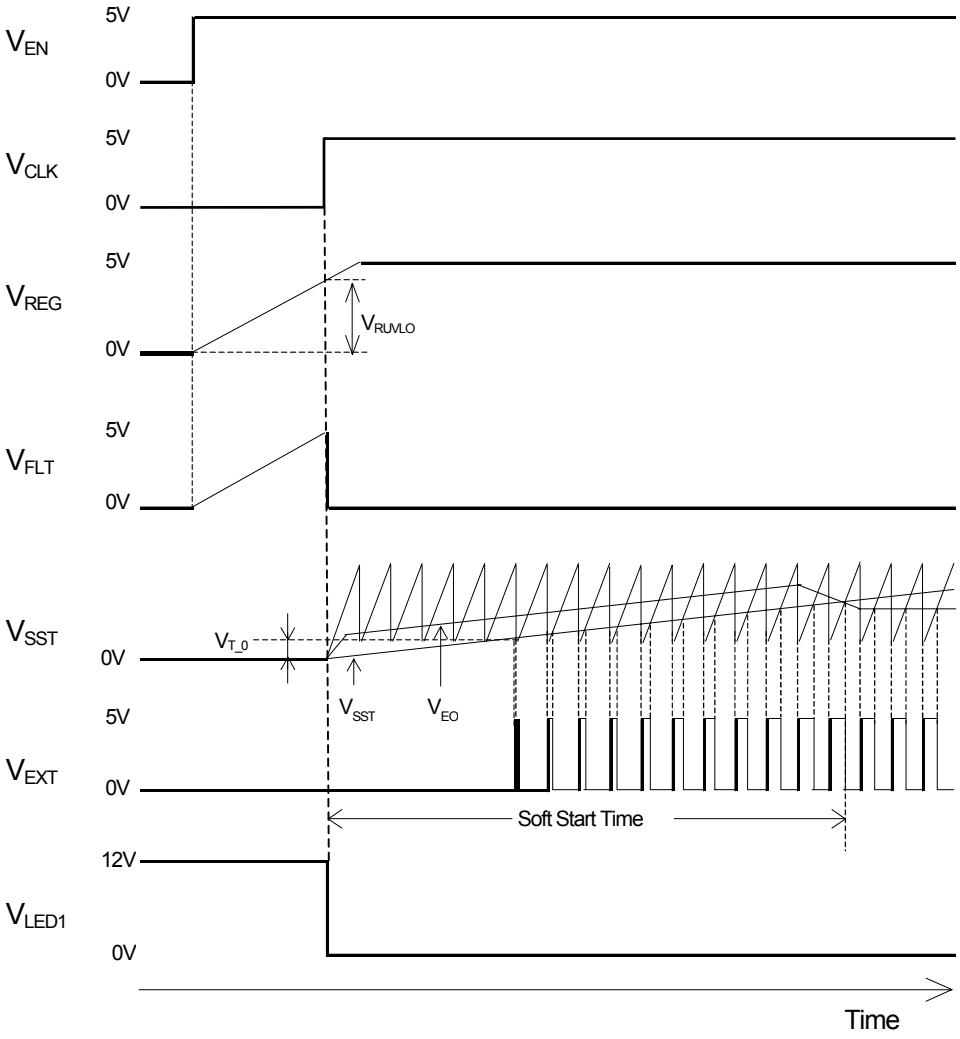
⑥ Stop Condition

When you enter a stop condition, should open a bus line without ACK sending after previous reading data. After that, the SCL pin becomes high level and a data sending is terminated by entering rise edge into SDA

■ Operation Example of Each Pin

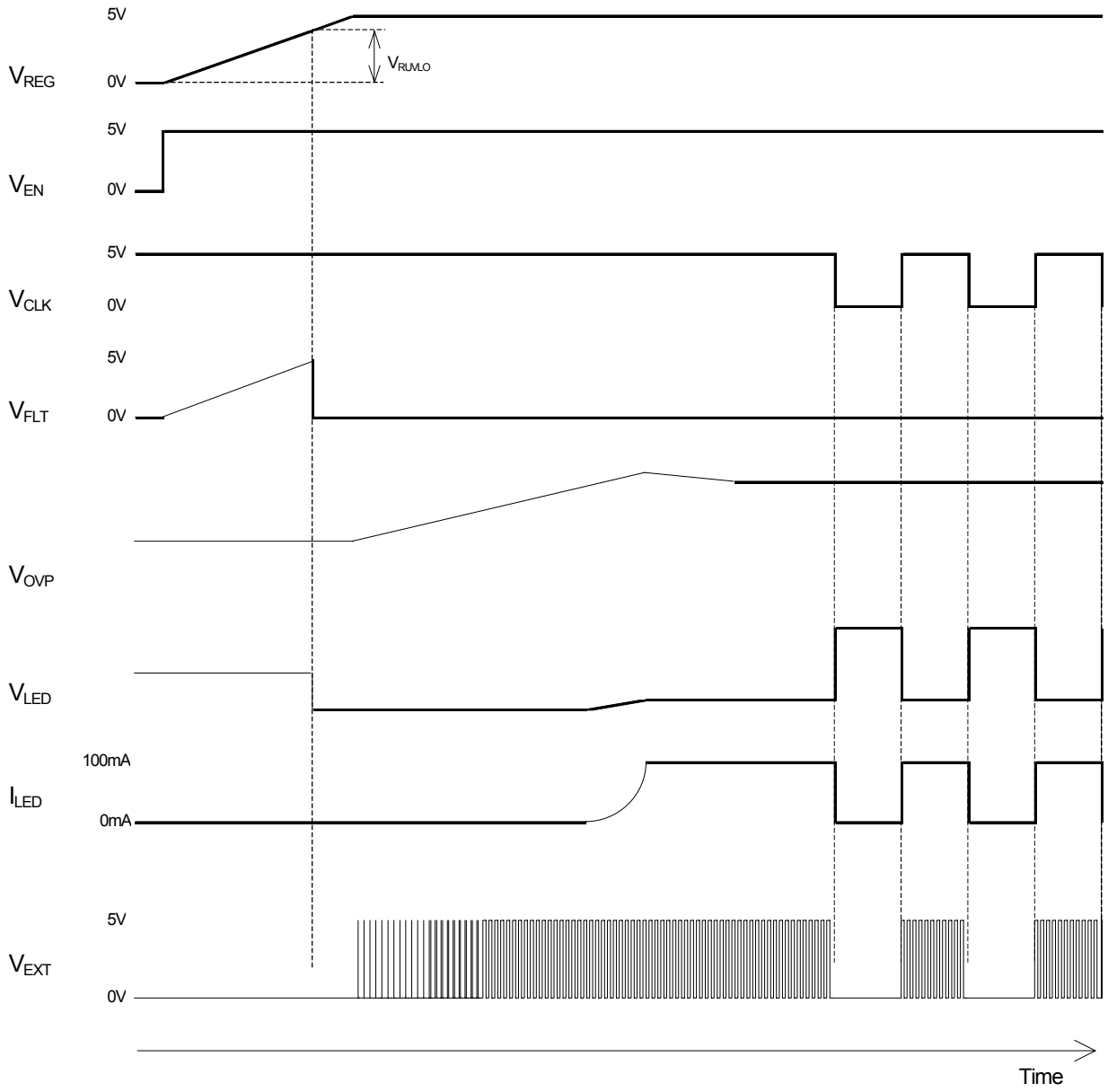
Each Pin Voltage at Start-up

$V^+$=12V, $C_{REG}$=1μF, $R_{FLT}$=47kΩ, $R_{ISET}$=10kΩ, (At Inputting External Pulse Dimming Signal)



Each Pin Voltage of PWM Dimming

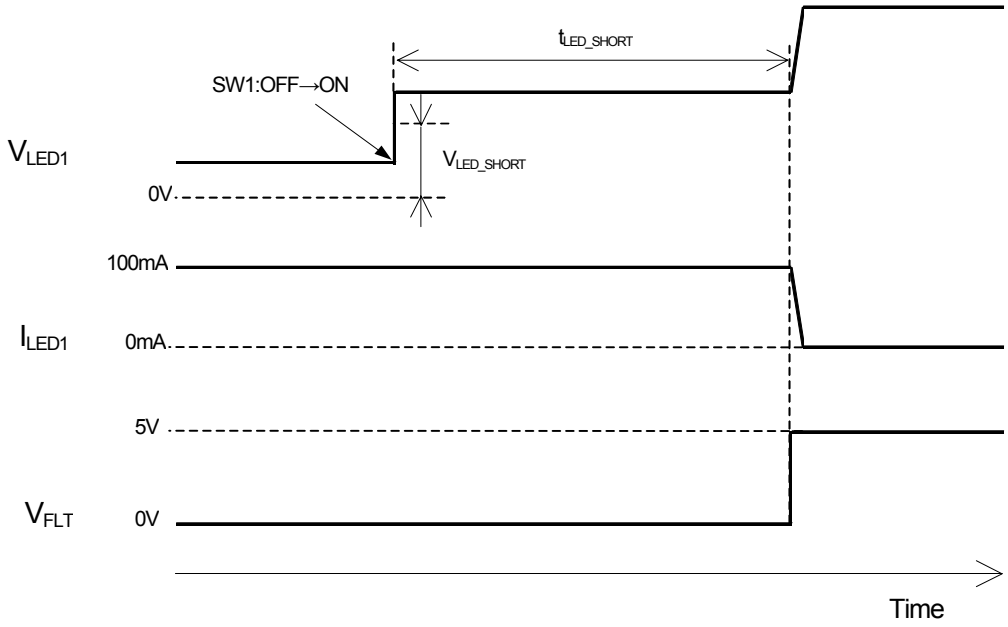
$V^+$=12V, $C_{REG}$=1μF, $R_{FLT}$=47kΩ, $R_{ISET}$=10kΩ, (At Inputting External Pulse Dimming Signal)

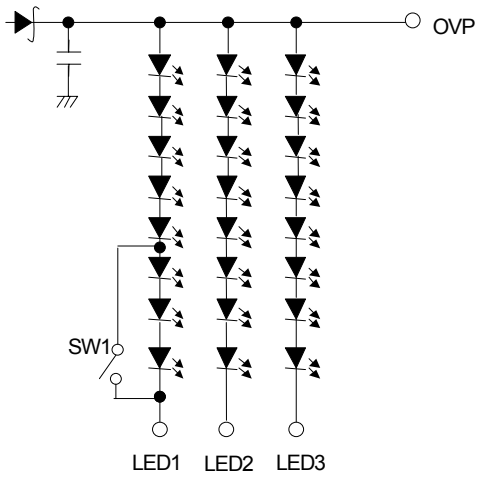


Operation Example at Short protection Circuit Operating

$V^+$=12V, $C_{REG}$=1μF, $R_{FLT}$=47kΩ, $R_{ISET}$=10kΩ, (at Inputting External Pulse Dimming Signal)

Shorten a LED(s) connected to LED1 like measurement circuit




MEASUREMENT CIRCUIT

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