

## 1-channel High Side Switch

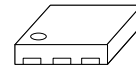
### ■ GENERAL DESCRIPTION

The NJW4832 is the single high-side switch that can supply 0.2A. The active clamp circuit, overcurrent and thermal shutdown are built-in to Pch MOS FET.

A logic signal (3V/5V) can be input directly. Especially, the NJW4832 is suitable for various Sensors output block as PNP type. The FLT logic has two versions: Active-high (A-ver) and Active-low (B-ver).

Also, The NJW4832 is a complementary product to the NJW4822.

### ■ PACKAGE OUTLINE

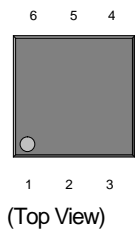


NJW4832KH1

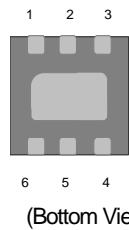
### ■ FEATURES

- Drain-Source Voltage                    45V
- Output Current                            0.2A
- Corresponding with Logic Voltage Operation: 3V/5V
- Low On-Resistance                      0.75Ω (typ.)
- Low Consumption Current              110μA (typ.)
- Active Clamp Circuit
- Over Current Protection (Self recovery type current limiting function)
- Thermal Shutdown
- Package Outline                            DFN6-H1 (ESON6-H1)

### ■ PIN CONFIGURATION

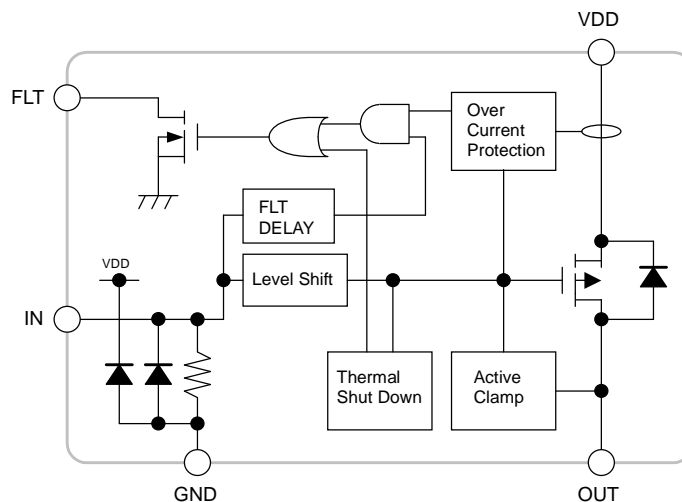


1. VDD
2. NC
3. OUT
4. IN
5. GND
6. FLT



Exposed PAD on backside connect to GND.

### ■ BLOCK DIAGRAM



# NJW4832

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	REMARK
Drain-Source Voltage	$V_{DS}$	45	V	VDD-OUT Pin
Supply Voltage	$V_{DD}$	45	V	VDD-GND Pin
Input Pin Voltage	$V_{IN}$	-0.3 to +6	V	IN-GND Pin
FLT Pin Voltage	$V_{FLT}$	-0.3 to +6	V	FLT-GND Pin
Power Dissipation	$P_D$	445 (*1) 1135 (*2)	mW	-
Active Clamp Tolerance (Single Pulse)	$E_{AS}$	100	mJ	-
Active Clamp Current	$I_{AP}$	0.2	A	-
Junction Temperature	$T_j$	-40 to +150	°C	-
Operating Temperature	$T_{opr}$	-40 to +125	°C	-
Storage Temperature	$T_{stg}$	-50 to +150	°C	-

(\*1): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(\*2): Mounted on glass epoxy board (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)  
(4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

## ■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Drain-Source Voltage	$V_{DS}$	0	-	40	V	VDD-OUT Pin
Supply Voltage	$V_{DD}$	4.6	-	40	V	VDD-GND Pin
Output Current	$I_O$	0	-	0.2	A	VDD-OUT Pin
Input Pin Voltage	$V_{IN}$	0	-	5.5	V	IN-GND Pin
FLT Pin Voltage	$V_{FLT}$	0	-	5.5	V	FLT-GND Pin

## ■ PRODUCT VERSION

PRODUCT NAME	FLT LOGIC
NJW4832KH1-A	Active High
NJW4832KH1-B	Active Low

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V_{DS}=13V$ ,  $T_a=25^{\circ}C$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain-Source Clamp Voltage	$V_{DSS\_CL}$	$V_{IN}=0V$ , $I_O=1mA$ , $V_{DD}=40V$	$V_{DD}-45$	–	–	V
High Level Input Voltage	$V_{IH}$	$I_O=10mA$	2.64	–	–	V
Low Level Input Voltage	$V_{IL}$	$I_O=100\mu A$	–	–	0.9	V
Protection Circuit Function Input Voltage Range	$V_{IN\_opr}$		2.64	–	5.5	V
OUT Pin Leak Current at OFF State	$I_{OLEAKOUT}$	$V_{IN}=0V$ , $V_{DD}=40V$	–	–	1	$\mu A$
Quiscent Current 1	$I_{DD1}$	$V_{IN}=0V$ , $V_{DD}=40V$	–	–	1	$\mu A$
Quiscent Current 2	$I_{DD2}$	$V_{IN}=5V$	–	110	150	$\mu A$
Input Current	$I_{IN}$	$V_{IN}=5V$	–	150	190	$\mu A$
On-State Resistance	$R_{DS\_ON}$	$V_{IN}=5V$ , $I_O=0.2A$	–	0.75	1.2	$\Omega$
Over Current Protection	$I_{LIMIT}$	$V_{IN}=5V$ , $V_{DS}=5V$	0.2	0.4	0.8	A
Turn-on Time	$t_{ON}$	$V_{IN}=0$ to $5V$ , $I_O=0.2A$	–	10	–	$\mu s$
Turn-off Time	$t_{OFF}$	$V_{IN}=5$ to $0V$ , $I_O=0.2A$	–	10	–	$\mu s$
OUT–VDD Voltage Difference	$V_{PDOV}$	$V_{IN}=0V$ , $I_{ORH}=0.2A$	–	0.85	1.2	V
FLT Pin Low Level Output Voltage	$V_{VFLT}$	$I_{FLT}=500\mu A$	–	0.25	0.5	V
FLT Pin Leak Current at OFF State	$I_{OLEAKFLT}$	$V_{FLT}=5.5V$	–	–	1	$\mu A$
FLT Delay Time	$t_{DFLT}$	$V_{IN}=0$ to $5V$	–	5	–	ms

# NJW4832

## ■ TRUTH TABLE

[A-version: Active-high]

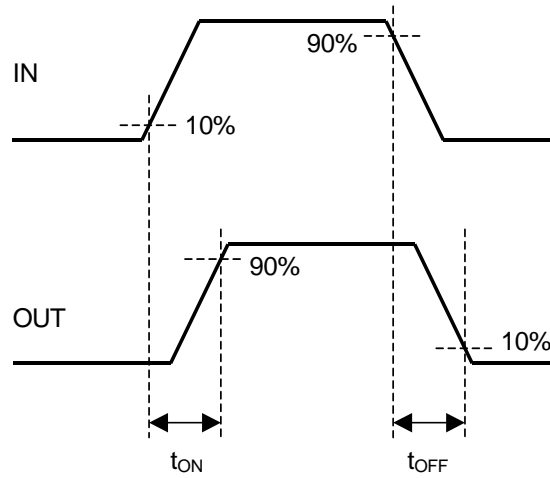
Input Signal	Operating Condition	FLT Pin	Output Status
L	Normal	H	OFF
H		L	ON
L	Over Current $I_{LIMIT}$	H	OFF
H		H	$I_{LIMIT}$
L	$T_j > 150^\circ\text{C}$	H	OFF
H		H	OFF

[B-version: Active-low]

Input Signal	Operating Condition	FLT Pin	Output Status
L	Normal	H	OFF
H		H	ON
L	Over Current $I_{LIMIT}$	H	OFF
H		L	$I_{LIMIT}$
L	$T_j > 150^\circ\text{C}$	H	OFF
H		L	OFF

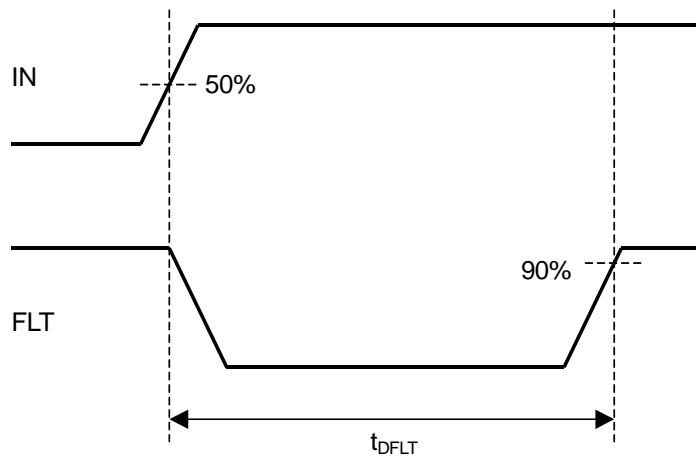
## ■ TIMING CHART

ON, OFF Switching Time ( $V_{IN}=0$  to 5V,  $V_{DD}=13V$ ,  $I_O=0.2A$ )

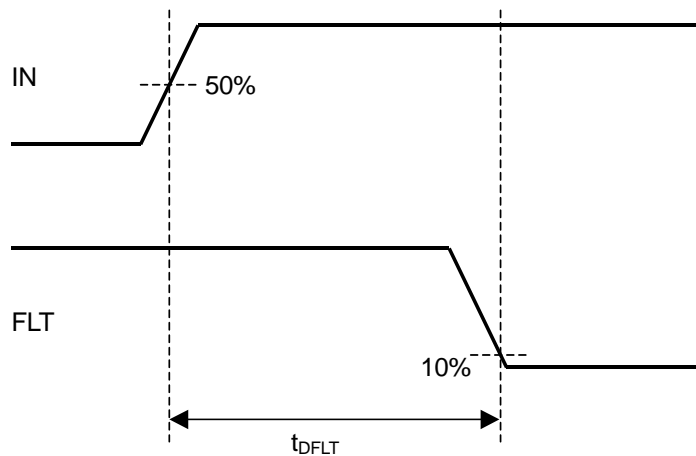


FLT Delay Time ( $V_{IN}=0$  to 5V,  $V_{DD}=V_{DS}=13V$ , FLT=Pull-up, OUT-GND shorting)

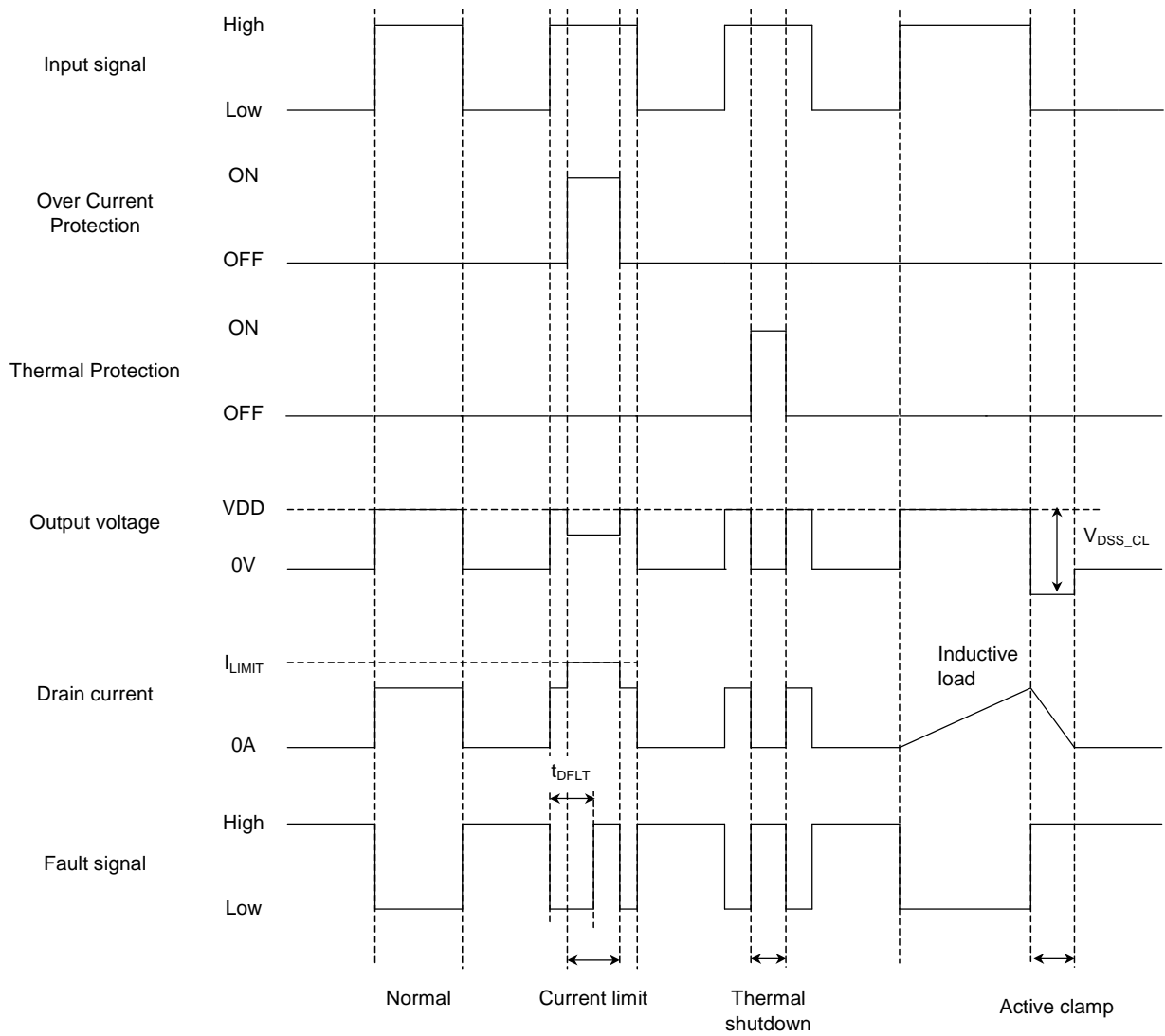
[A-version: Active-high]



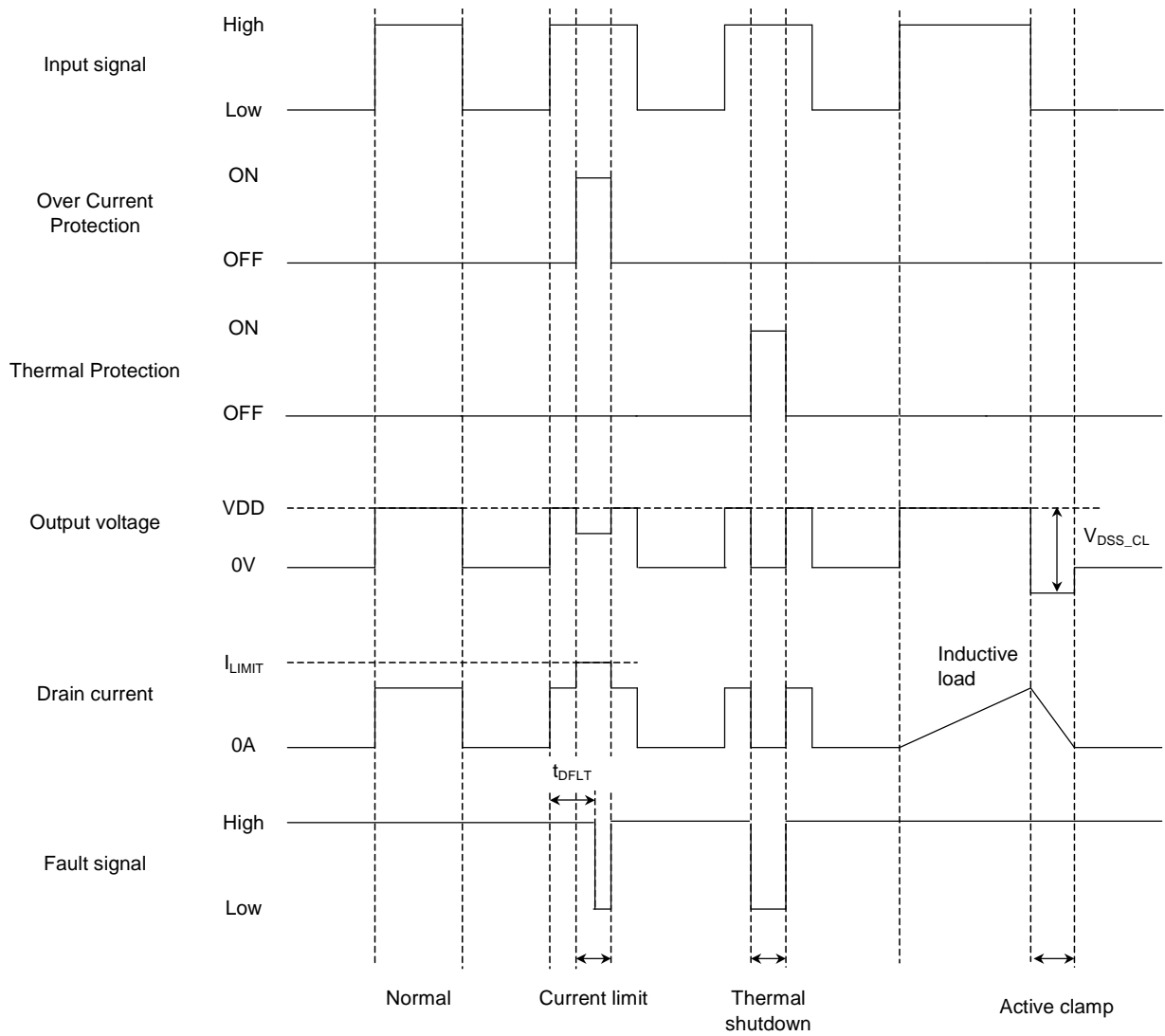
[B-version: Active-low]



[A-version: Active-high]

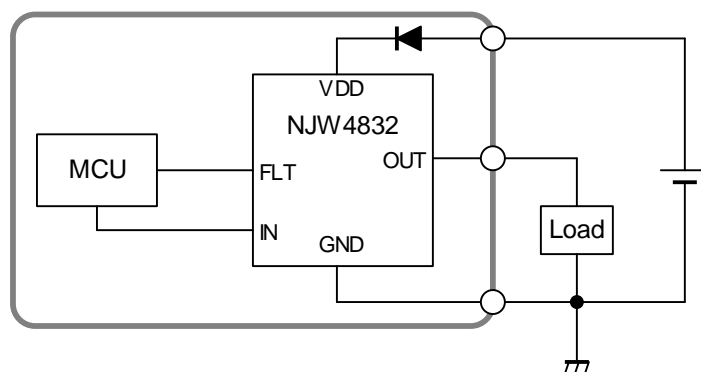


[B-version: Active-low]



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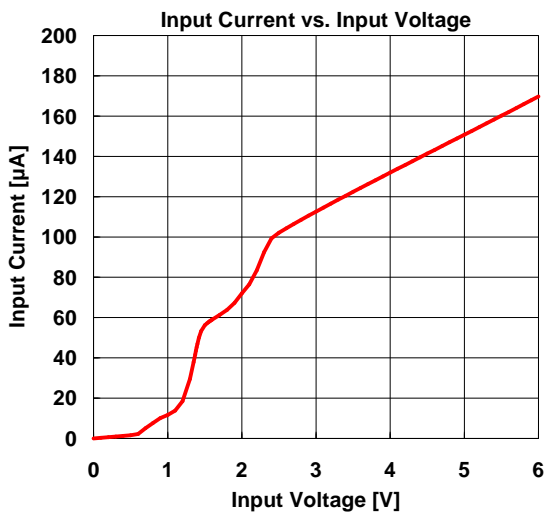
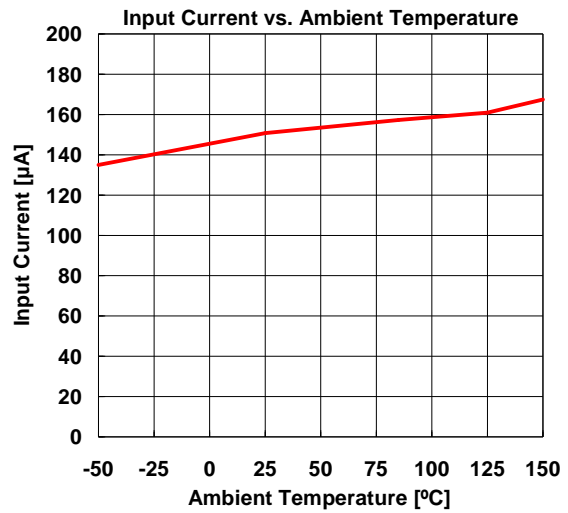
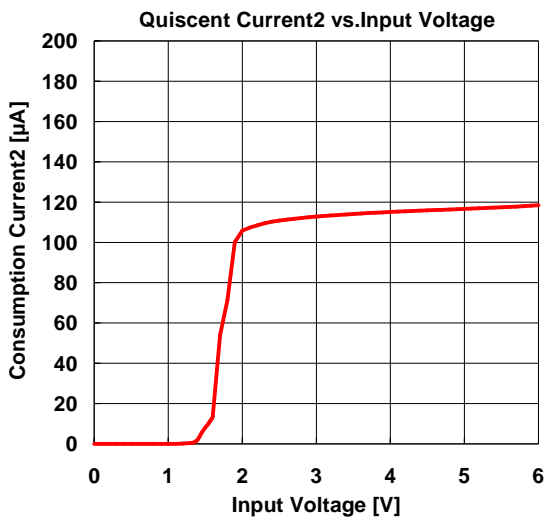
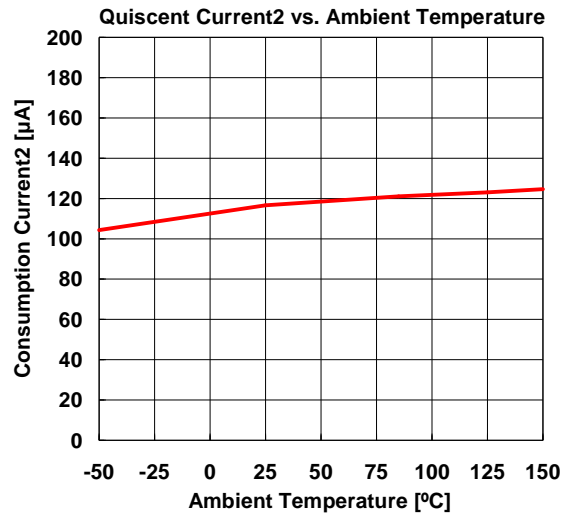
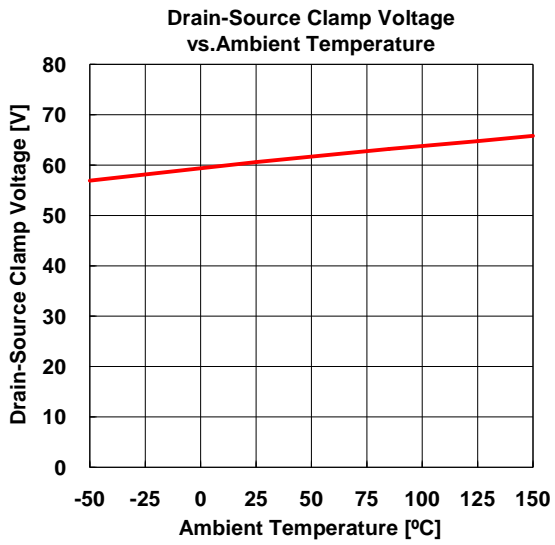
## ■ TYPICAL APPLICATION



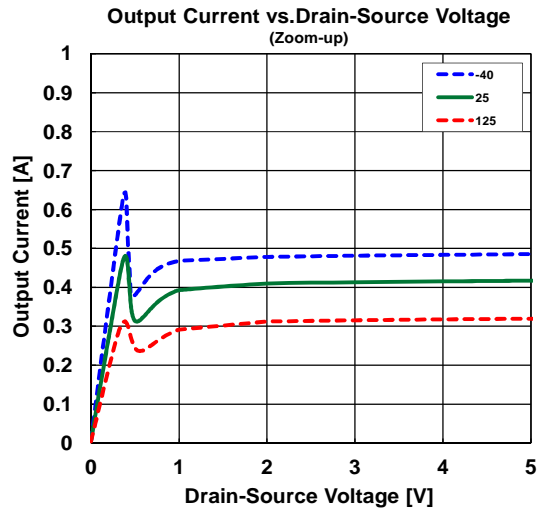
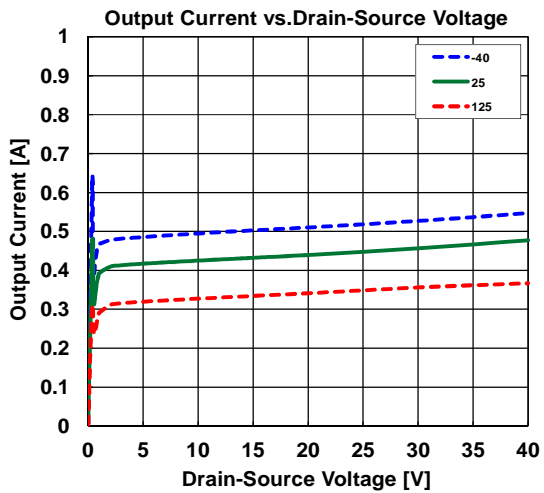
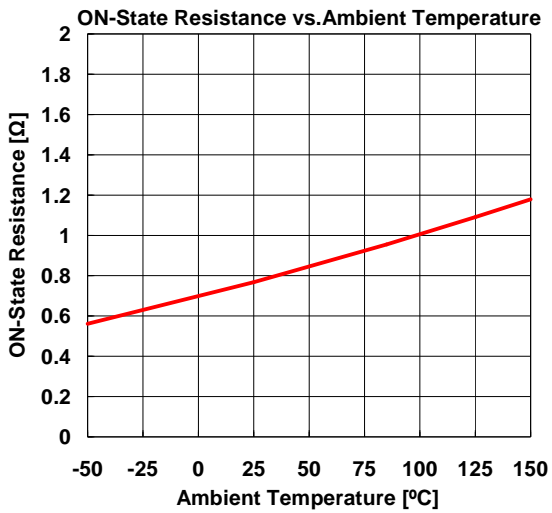
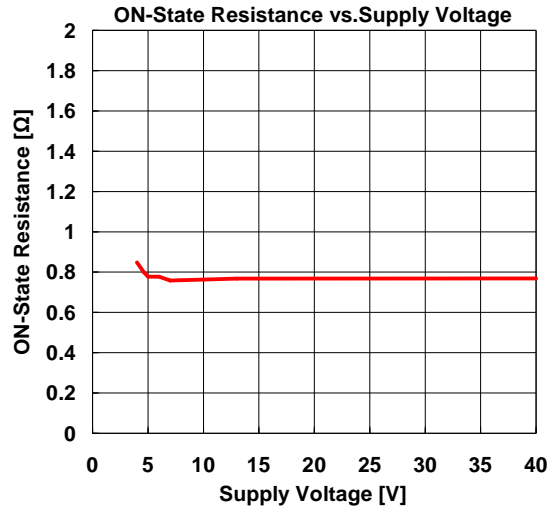
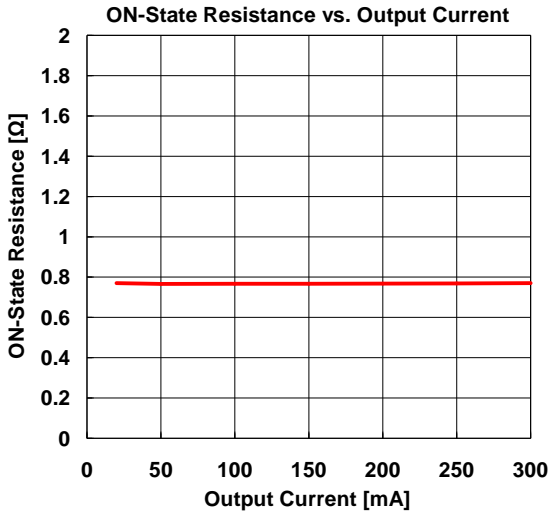
You should insert a pull-up resistor when you connect the FLT pin with other power supplies etc.



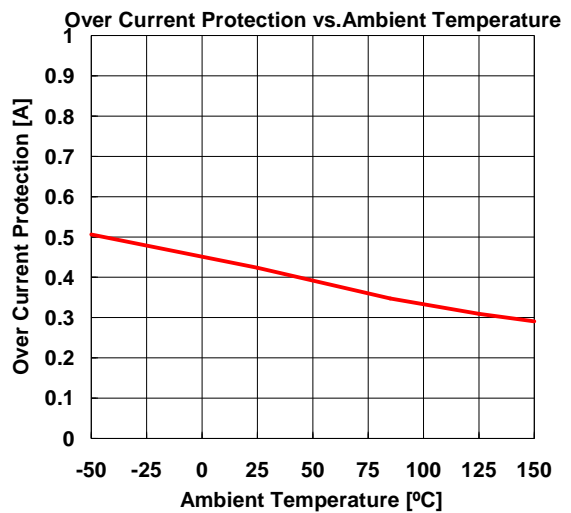
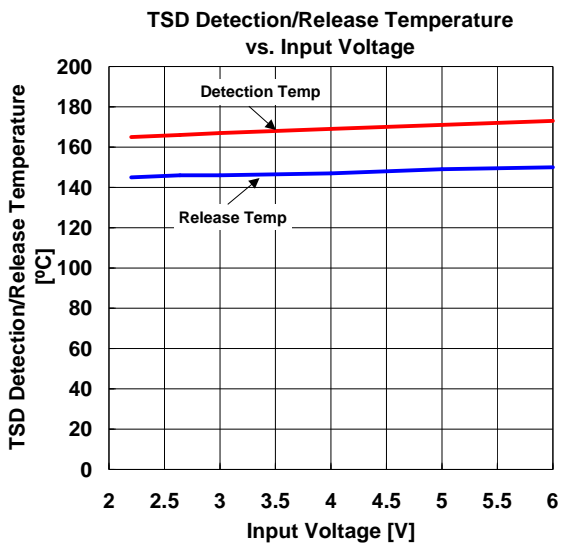
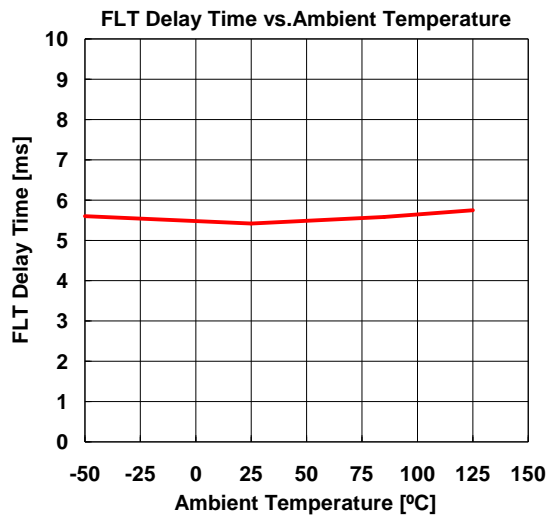
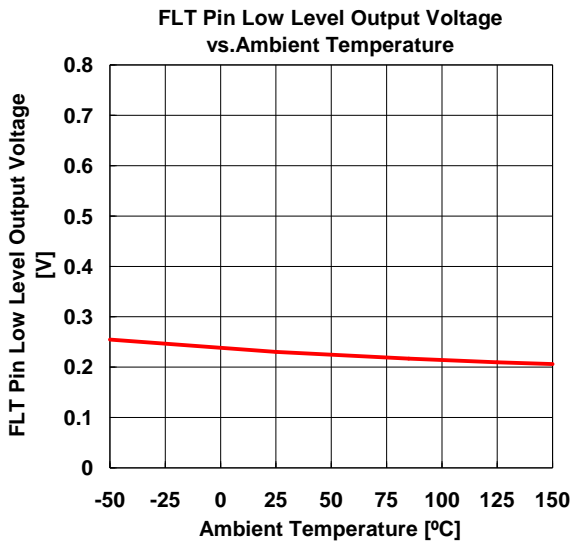
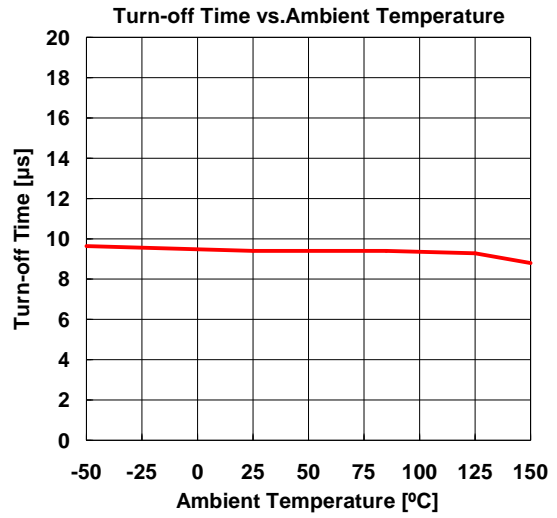
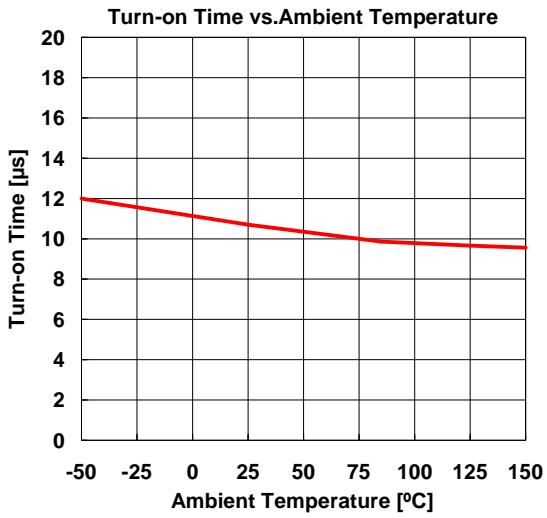
## ■ CHARACTERISTICS



## CHARACTERISTICS



## CHARACTERISTICS



### ■ Regarding Active Clamp Capacity of High/Low side Switch Products

- What is “Active Clamp Capacity”.

The IC might suffer to damage by the inductive kickback at the transient time of ON state to OFF state, when an inductive load such as a solenoid or motor is used for the load of the high-side/low-side switch.

The protection circuit for the inductive kickback is the active clamp circuit. The energy that can be tolerated by the active clamp circuit is called "Active Clamp Capacity ( $E_{AS}$ )".

When using an inductive load to the high-side/low-side switch, you should design so that the  $E_{SW}$  does not exceed the active clamp capability.

- IC operation without an external protection parts (Fig 1)

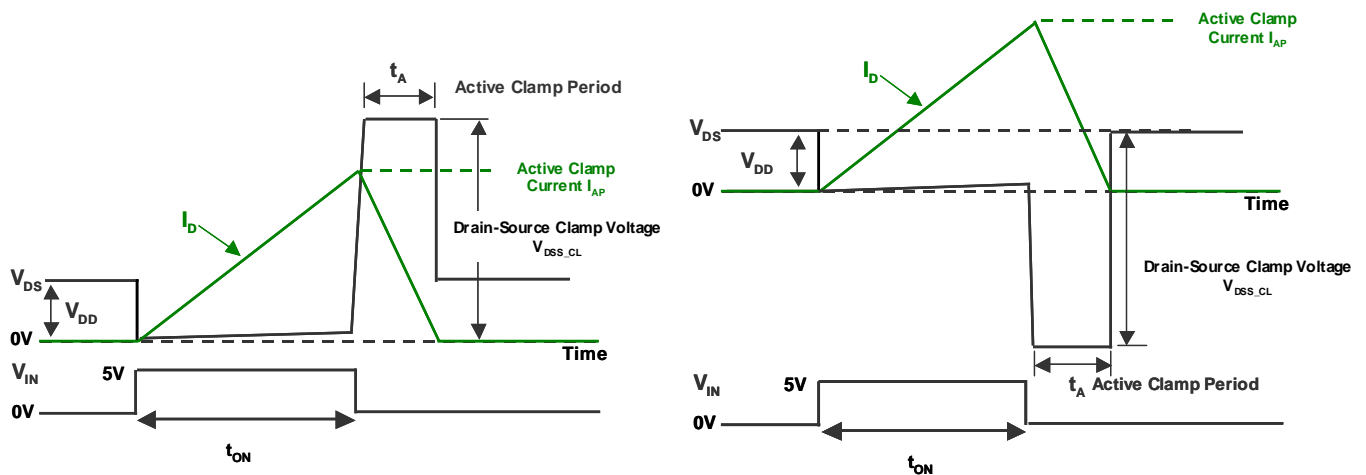


Fig1. Active Clamp Waveform (Left: Low-side Switch / Light High-side Switch)

At when the  $V_{IN}$  turns off, the drain-source voltage ( $V_{DS}$ ) increases rapidly by the behavior of the inductive load that is keeping current flowing. However, it will be clamped at  $V_{DSS\_CL}$  by the active clamp circuit. At the same time, the drain current is flowed by adjusting the gate voltage of the output transistor, and the energy is dissipated at the output transistor. The energy:  $E_{SW}$  is shown by the following formula.

$$E_{SW} = \int_0^{t_A} V_{DS}(t) \cdot I_D(t) dt = \frac{1}{2} L I_{AP}^2 \cdot \frac{V_{DSS\_CL}}{V_{DSS\_CL} - V_{DD}}$$

The  $E_{SW}$  is consumed inside IC as heat energy. However, the thermal shutdown does not work when the  $V_{IN}$  is 0V. Therefore in worst case the IC might break down. When using the active clamp, you should design  $E_{SW}$  does not exceed the  $E_{AS}$ .

- Application Hint

The simplest protection example is to add an external flywheel diode at the load to protect IC from an inductive kickback. (Fig.2)

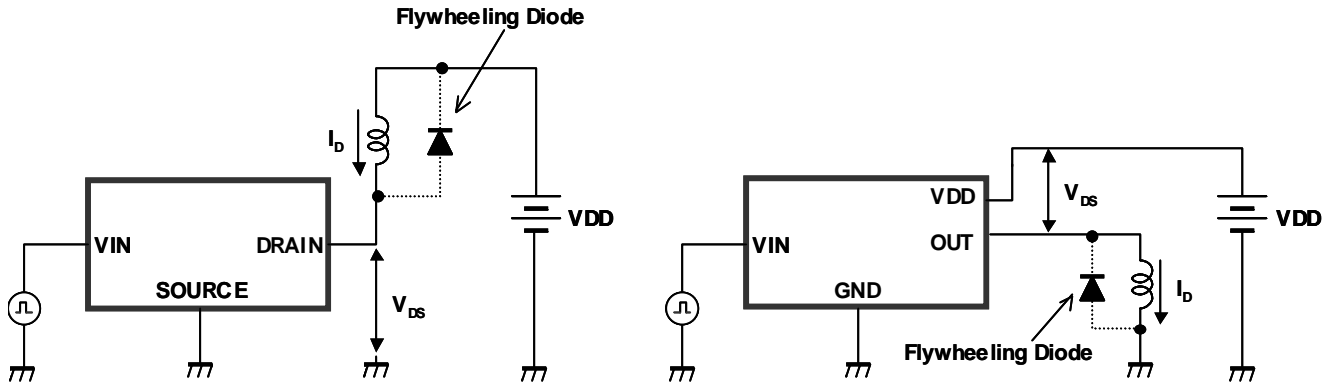


Fig 2. Application Circuit of Inductance Load Driving (Left: Low-side Switch / Light High-side Switch)

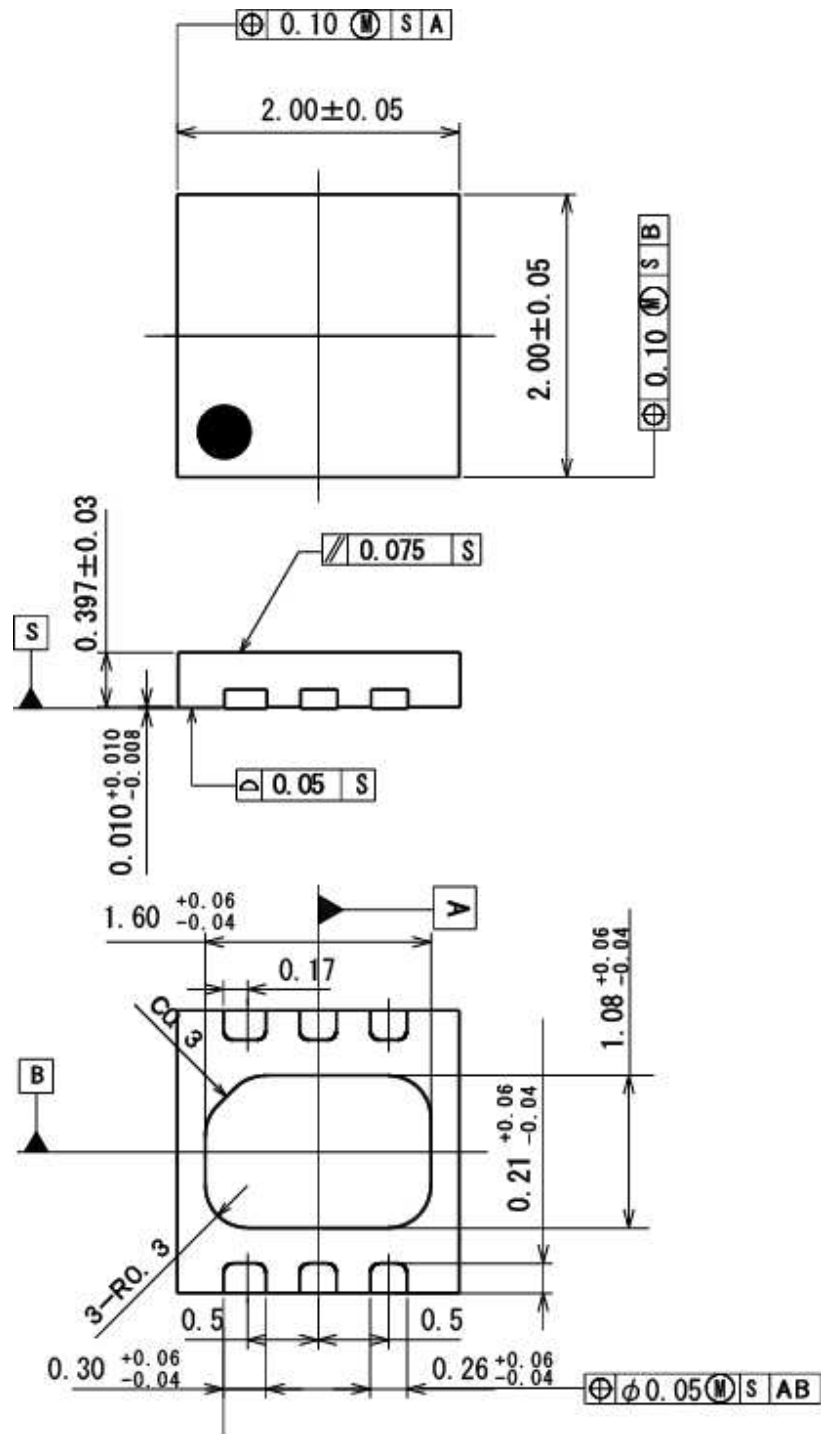
**[CAUTION]**

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# NJW4832

■ PACKAGE OUT LINE

■ DFN6-H1 (ESON6-H1)



GD-N00602A-0  
UNIT: mm