High Speed Switching Gate Driver

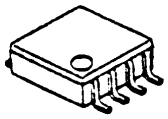
■ GENERAL DESCRIPTION

The NJW4840 is a High Speed Switching Gate Driver that is applicable 4A peak current.

The NJW4840 features are Withstand voltage of 24V, Operating voltage range: 8V to 20V and Fast switching time (27.5ns typical at 4700pF load).

The NJW4840 is suitable for PDP Sustain Pulse Drive, DC / AC Motor Drive, Switching Power Supply, and DC / DC Converter Applications.

■ PACKAGE OUTLINE

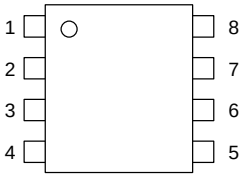


NJW4840R
(MSOP8 (VSP8))

■ FEATURES

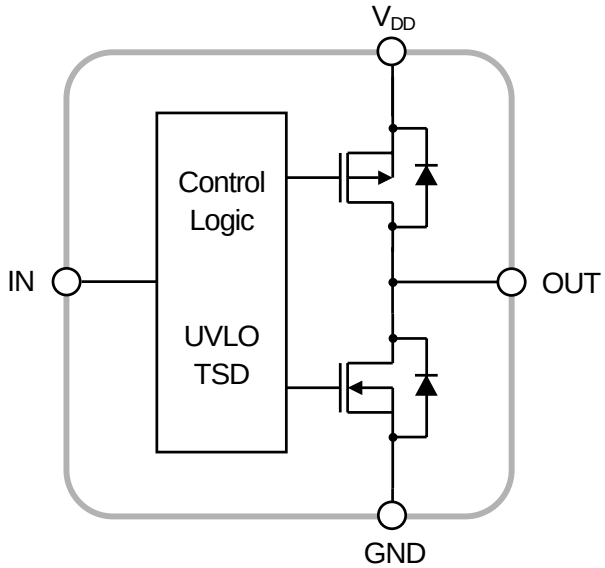
- Output Peak Current: ±4A (peak)
- Operating Voltage Range: 8V to 20V
- High Speed Switching: 27.5nsec(typ.)@CL=4,700pF
- Built-in Thermal Shut Down
- Under Voltage Lockout
- Short Circuit Protection (power / ground fault)
- Package: MSOP8 (VSP8)
  * MEET JEDEC MO-187-DA

■ PIN CONNECTION



1. GND
2. GND
3. GND
4. IN
5. GND
6. GND
7. OUT
8. V_{DD}

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYNBOL	RATINGS	UNIT	REMARK
Supply Voltage	V_{DD}	+24	V	V_{DD}-GND Pin
Input Voltage	V_{IN}	–0.3 to +6	V	V_{IN}-GND Pin
Input Voltage (Pulse)	$V_{IN\text{-}pulse}$	–0.3 to +7		
Power Dissipation	P_D	720 (*1) 1,100 (*2)	mW	–
Junction Temperature	T_j	–40 to +150	°C	–
Operating Temperature	T_{opr}	–40 to +105	°C	–
Storage Temperature	T_{stg}	–50 to +150	°C	–

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),
internal Cu area: 74.2×74.2mm

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Operating Voltage	Vopr	8.0	–	20	V	V_{DD}-GND Pin
Input Voltage	V_{IN}	0	–	5.5	V	V_{IN}-GND Pin

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{DS}=16V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
Quiescent Current	I_{Q1}	V_{IN}=5V	–	0.93	1.6	mA
	I_{Q2}	V_{IN}=0V	–	0.7	1.4	mA
Output Block						
Output Peak Current	I_{PK1}	PW≤400us, V_{OUT}=0V	–	4	–	A
	I_{PK2}	PW≤400us, V_{OUT}=16V	–	4	–	A
Output ON Resistance (High-Side / Low-Side)	R_{DSH}	$I_{O\text{-}SOURCE}$=100mA	–	0.8	1.5	Ω
	R_{DSL}	$I_{O\text{-}SINK}$=100mA	–	0.8	1.5	Ω
Pull Down Resistance	R_{PD}		60	100	140	kΩ
Input Circuit Block						
IN Pin High Resistance	V_{IHIN}		3.0	–	5.5	V
IN Pin Low Resistance	V_{ILIN}		0	–	1.5	V
IN Pin Sink Current	I_{IIN}	V_{IN}=5.5V	–	–	1	μA
IN Pin Hysteresis Voltage	ΔV_{in}	$V_{IHIN} - V_{ILIN}$	–	0.3	–	V
UVLO Block						
UVLO Release Voltage	V_{UVLO2}		6.3	7	7.7	V
UVLO Operating Voltage	V_{UVLO1}		6	6.7	7.4	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	$V_{UVLO2} - V_{UVLO1}$	–	0.3	–	V

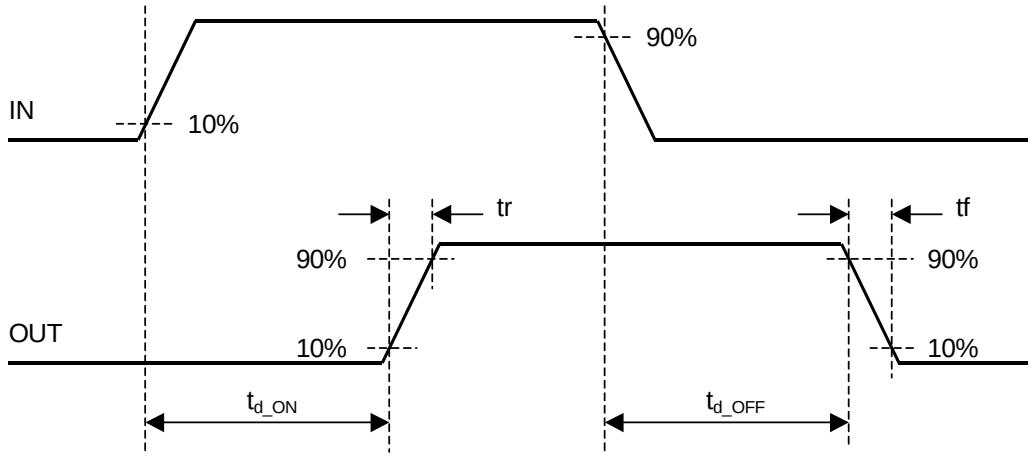
■ Output Rise / Fall Characteristics

(V^+=16V, Ta=25°C, Design Value*)

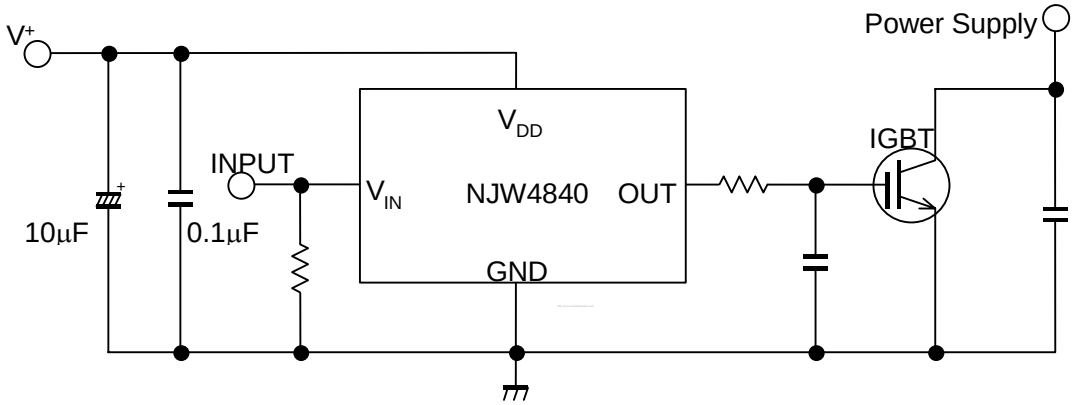
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	Tr	C_L=4700pF, V_{IN}=0 to 5V	15.0	27.5	40.0	ns
Output Fall Time	Tf	C_L=4700pF, V_{IN}=5 to 0V	15.0	27.5	40.0	ns
Rise Delay Time	t_{d_ON}	C_L=4700pF, V_{IN}=0 to 5V	17.5	30.0	42.5	ns
Fall Delay Time	t_{d_OFF}	C_L=4700pF, V_{IN}=5 to 0V	25.0	37.5	50.0	ns

* It is design guaranteed, not tested.

■ Timing Chart



■ TYPICAL APPLICATION



■ APPLICATION TIPS

In the application that does a high-speed switching of NJW4840, because the current flow corresponds to the input frequency, the substrate (PCB) layout becomes an important.

NJW4840 is driving the High-side/Low-side SW gate with high speed to reduce switching losses. The transient voltage is generated by parasitic inductance and a high-speed current change of high side and low side SW.

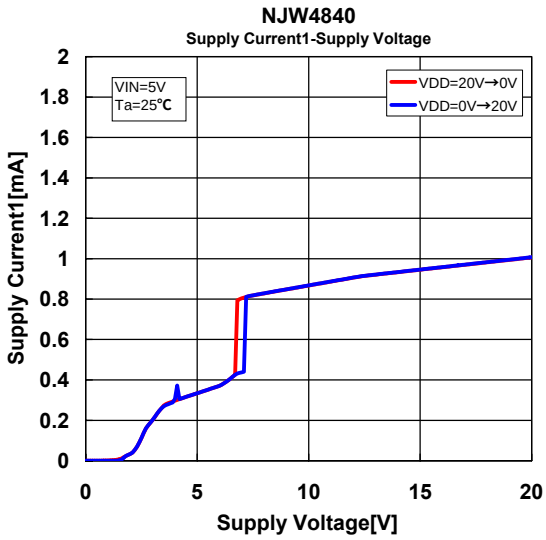
You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible.

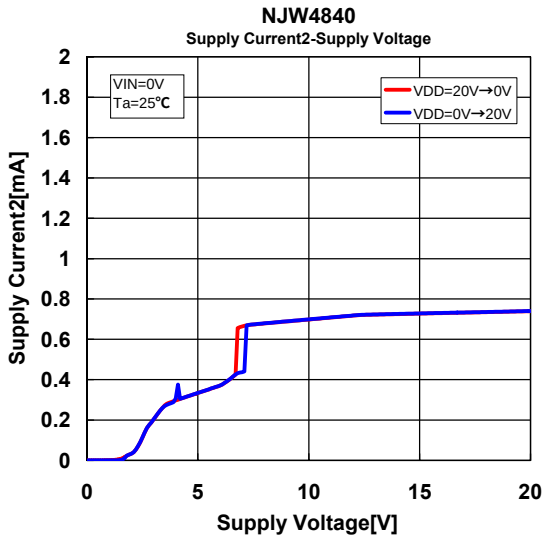
You should insert a bypass capacitor between the V_{DD} pin and the GND pin to prevent malfunction by generating over voltage and/or exceed maximum input voltage rating. The recommended bypass capacitor is low ESR and high frequency characteristic (NJRC recommends 0.1μF or more).

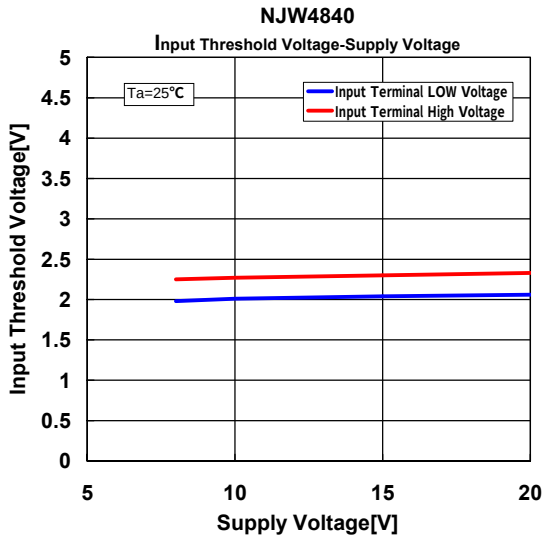
An aluminum electrolysis capacitor is recommended for smoothing condenser. (NJRC recommends 10μF or more). However, you should use large capacitor by sufficient evaluation (assessment) due to load condition and/or application use environment. (There is a possibility that the supply voltage rises by inductive kickback when the supply current of the inductive load is large.)

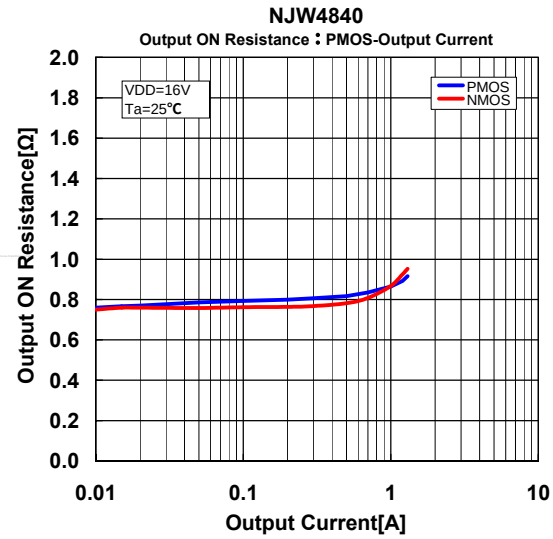
The bypass capacitors should be connected as much as possible near the VDD pin.

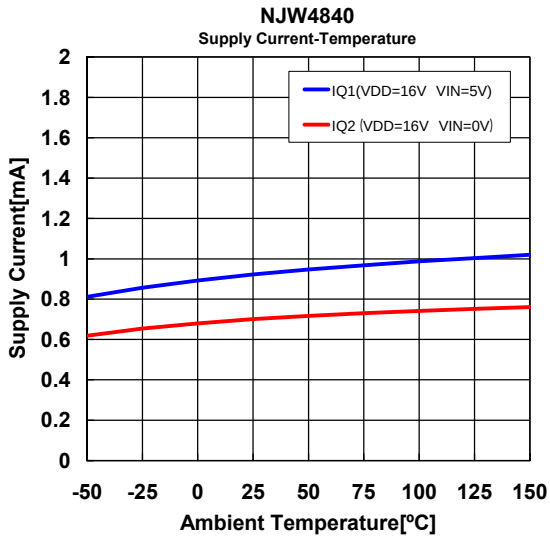
■ CHARACTERISTICS

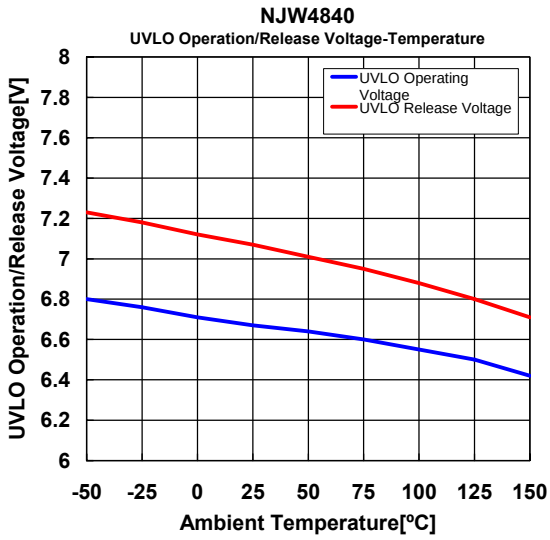












■ CHARACTERISTICS