

## 1-channel Switching Gate Driver

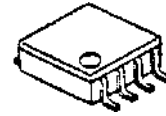
### ■ GENERAL DESCRIPTION

The NJW4841 is a High Speed Switching Gate Driver that is applicable 2A peak current.

The NJW4841 features are Withstand voltage of 40V, recommended operating voltage range: 4V to 20V and Fast switching time

The NJW4841 is suitable for DC / AC Motor Drive, Switching Power Supply and DC / DC Converter Applications.

### ■ PACKAGE OUTLINE



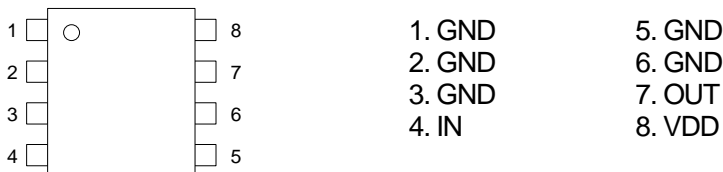
NJW4841R  
(MSOP8 (VSP8))\*

### ■ FEATURES

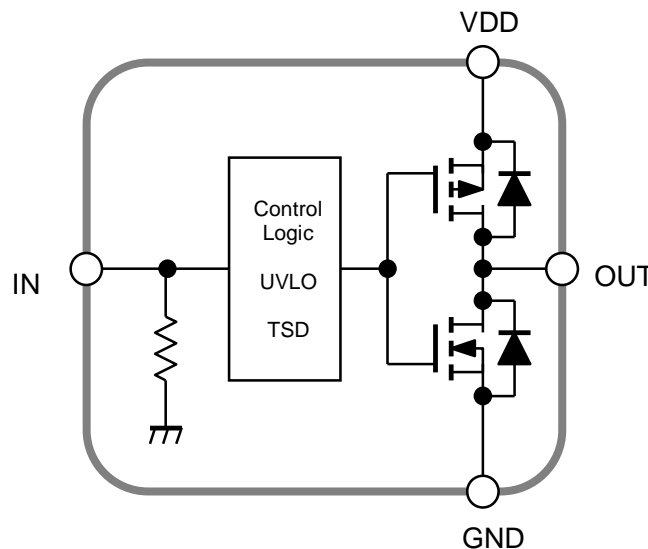
- Output Peak Current:  $\pm 2A$  (peak)
- Operating Voltage Range: 4V to 20V
- High Speed Switching:  $t_r/t_f=25ns/20ns$ (typ.) at  $C_L=2200pF$
- Corresponding with Logic Voltage Operation: 3V/5V
- Built-in Thermal Shut Down
- Under Voltage Lockout
- Package: MSOP8 (VSP8)\*

MSOP8 (VSP8)\*  
\* MEET JEDEC MO-187-DA

### ■ PIN CONFIGURATION



### ■ BLOCK DIAGRAM



# NJW4841-T1

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	REMARK
Supply Voltage	V <sub>DD</sub>	+40	V	VDD-GND Pin
Input Voltage	V <sub>IN</sub>	-0.3 to +6	V	IN-GND Pin
Power Dissipation	P <sub>D</sub>	720 (*1) 1100 (*2)	mW	-
Junction Temperature	T <sub>j</sub>	-40 to +150	°C	-
Operating Temperature	T <sub>opr</sub>	-40 to +125	°C	-
Storage Temperature	T <sub>stg</sub>	-50 to +150	°C	-

(\*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 2Layers)

(\*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm: based on EIA/JDEC standard, 4Layers),

internal Cu area: 74.2×74.2mm

## ■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Operating Voltage	V <sub>DD</sub>	4.0	-	20	V	VDD-GND Pin
Input Voltage	V <sub>IN</sub>	0	-	5.5	V	IN-GND Pin

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V_{DD}=16V$ ,  $T_a=25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
Quiescent Current	$I_{Q1}$	$V_{IN}=5V$	–	1.5	2.5	mA
		$V_{IN}=5V, T_a=-40$ to $+125^\circ C$	–	–	2.5	
	$I_{Q2}$	$V_{IN}=0V$	–	1.3	2.3	mA
		$V_{IN}=0V, T_a=-40$ to $+125^\circ C$	–	–	2.3	

### Output Block

Output Peak Current	$I_{PK1}$	Pulse Width $\leq 10\mu s, V_{OUT}=0V$	–	2	–	A
	$I_{PK2}$	Pulse Width $\leq 10\mu s, V_{OUT}=16V$	–	2	–	A
Output ON Resistance (High-Side / Low-Side)	$R_{DSH}$	$I_{O-SOURCE}=100mA$	–	2.1	3.9	$\Omega$
	$R_{DSL}$	$I_{O-SINK}=100mA$	–	1.5	2.8	$\Omega$
Output Pull Down Resistance	$R_{OUTPD}$		60	100	140	k $\Omega$
		$T_a=-40$ to $+125^\circ C$	40	–	160	

### Input Circuit Block

IN Pin High Voltage	$V_{IHIN}$		2.0	–	5.5	V
		$T_a=-40$ to $+125^\circ C$	2.0	–	5.5	
IN Pin Low Voltage	$V_{ILIN}$		0	–	0.8	V
		$T_a=-40$ to $+125^\circ C$	0	–	0.8	
Input Pull Down Resistance	$R_{INPD}$		60	100	140	k $\Omega$
		$T_a=-40$ to $+125^\circ C$	40	–	160	

### UVLO Block

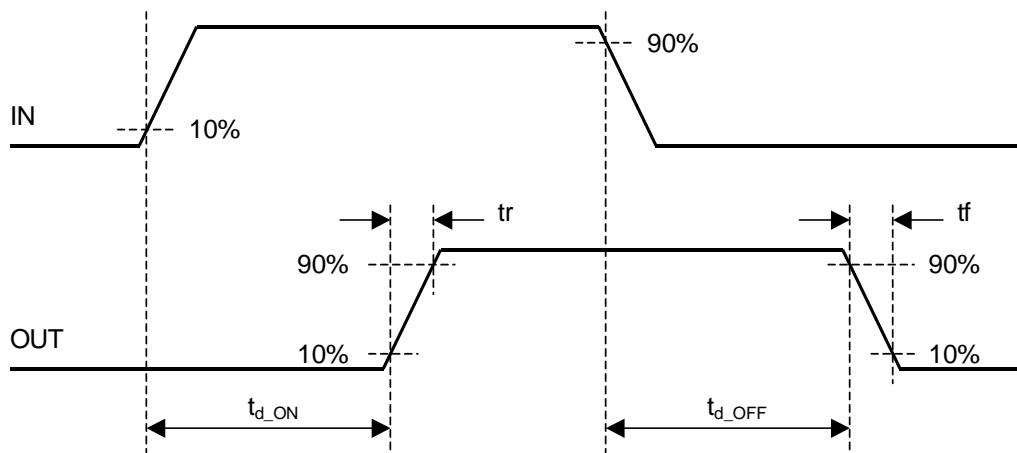
UVLO Release Voltage	$V_{UVLO2}$		2.8	3.3	3.8	V
		$T_a=-40$ to $+125^\circ C$	2.8	–	3.8	
UVLO Operating Voltage	$V_{UVLO1}$		2.5	3.0	3.5	V
		$T_a=-40$ to $+125^\circ C$	2.5	–	3.5	
UVLO Hysteresis Voltage	$V_{UVLO}$	$V_{UVLO2} - V_{UVLO1}$	–	0.3	–	V

### Output Rise/Fall characteristics

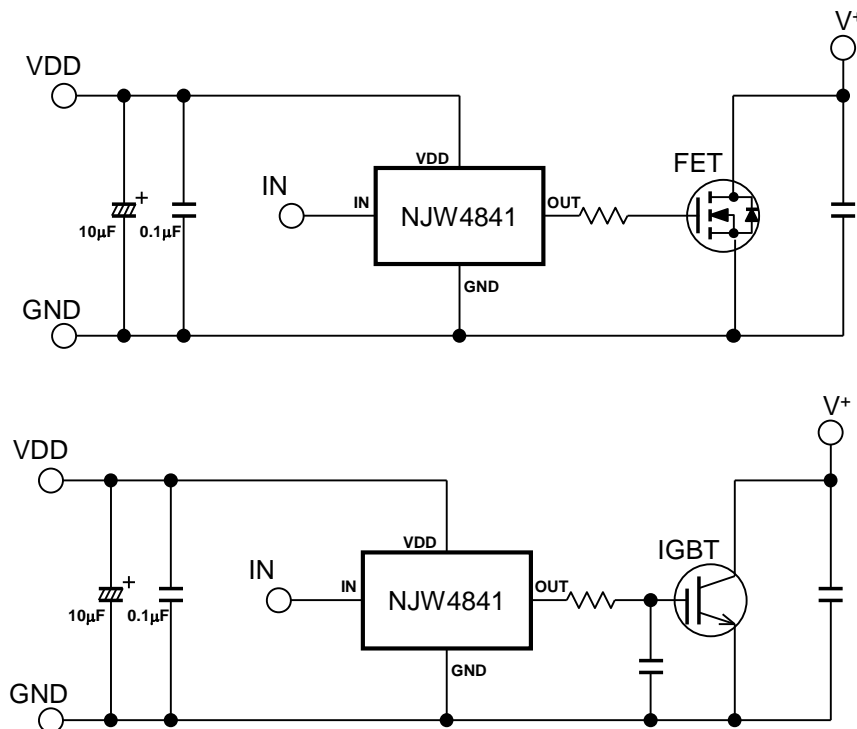
Output Rise Time	$t_r$	$C_L=2200pF, V_{IN}=0$ to $5V$	–	25	–	ns
Output Fall Time	$t_f$	$C_L=2200pF, V_{IN}=5$ to $0V$	–	20	–	ns
Rise Delay Time	$t_{d\_ON}$	$C_L=2200pF, V_{IN}=0$ to $5V$	–	40	–	ns
Fall Delay Time	$t_{d\_OFF}$	$C_L=2200pF, V_{IN}=5$ to $0V$	–	45	–	ns

# NJW4841-T1

## ■ TIMING CHART



## ■ TYPICAL APPLICATION



## ■ APPLICATION TIPS

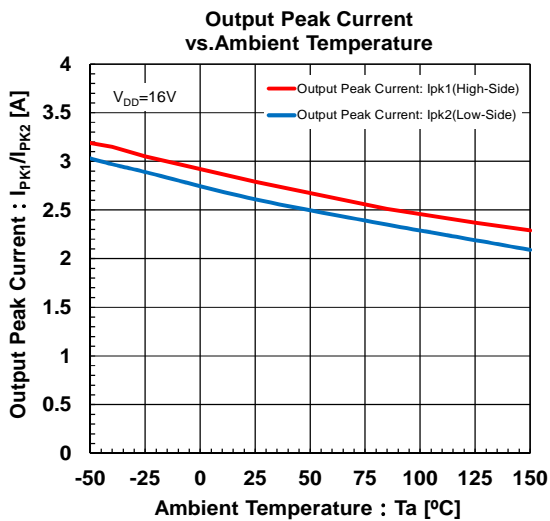
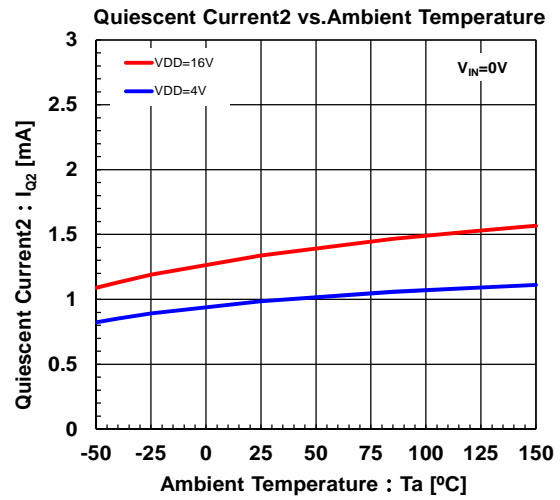
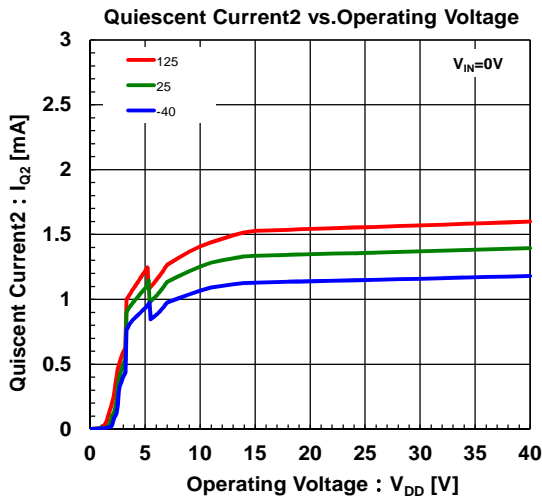
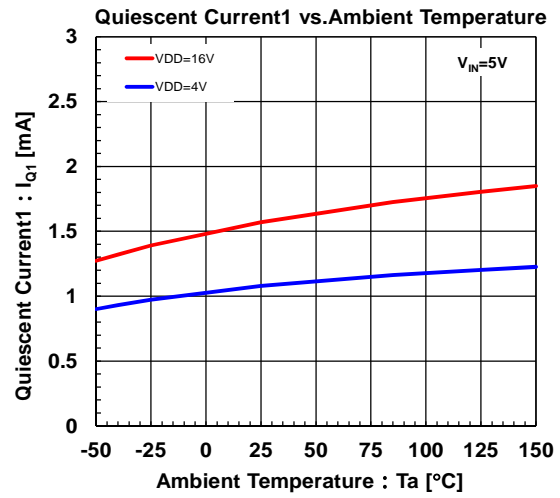
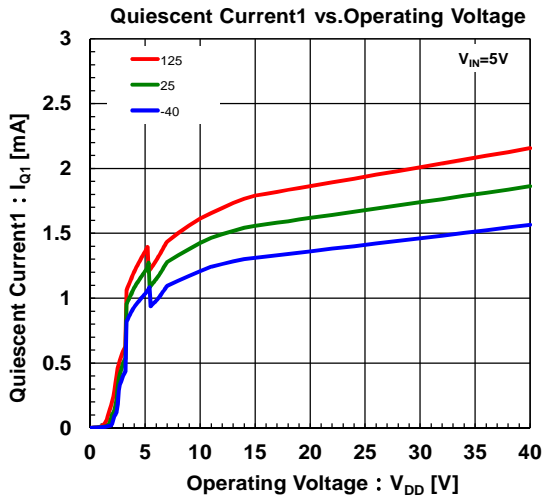
In the application that does a high-speed switching of NJW4841, because the current flow corresponds to the input frequency, the substrate (PCB) layout becomes an important.

NJW4841 is driving the High-side/Low-side SW gate with high speed to reduce switching losses. The transient voltage is generated by parasitic inductance and a high-speed current change of high side and low side SW.

You should attempt the transient voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible.

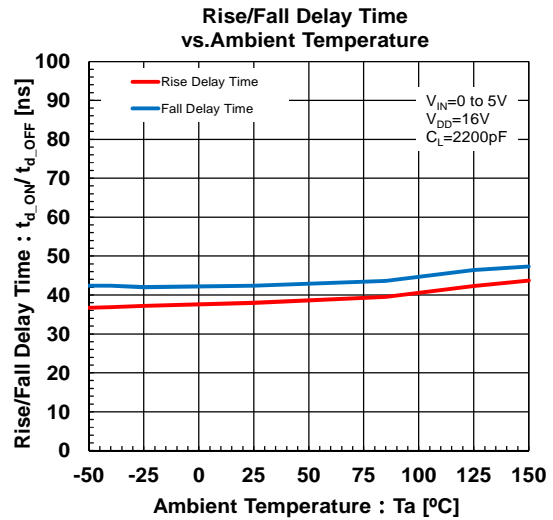
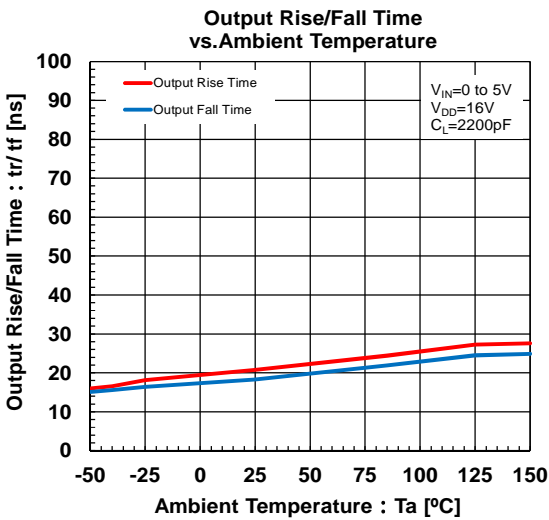
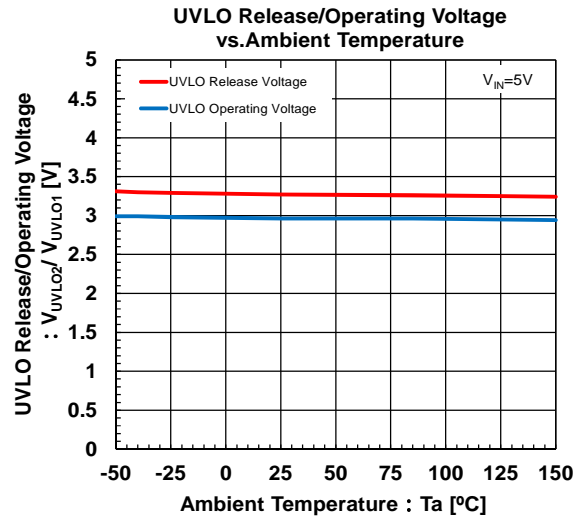
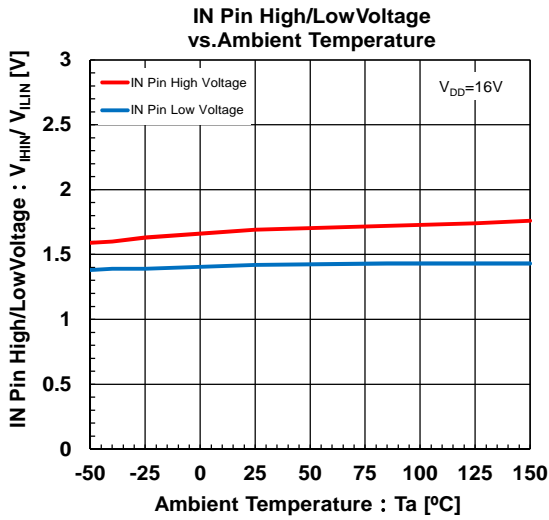
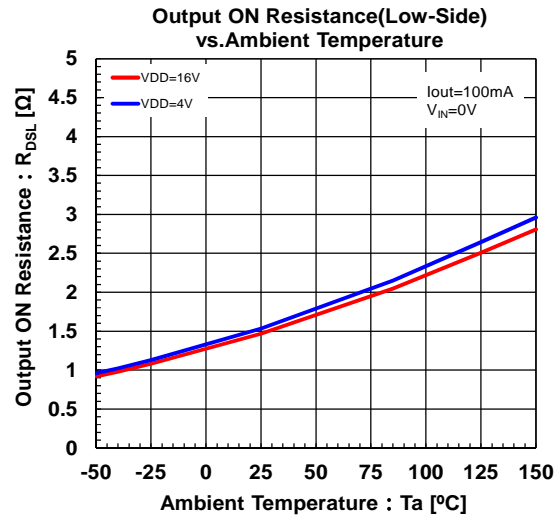
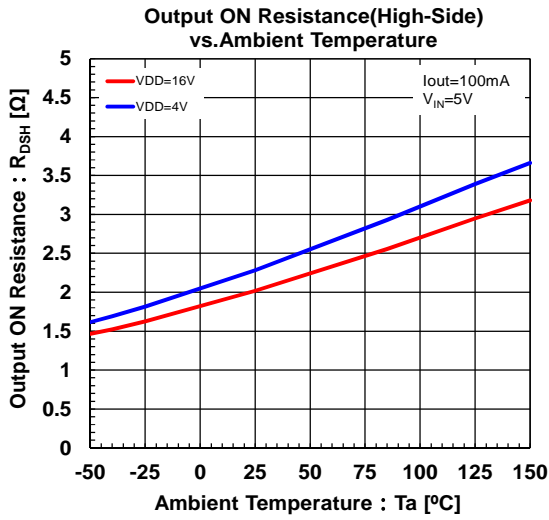
You should insert a bypass capacitor between the VDD pin and the GND pin to prevent malfunction by transient voltage and/or exceed maximum input voltage rating. The recommended bypass capacitor is low ESR and fine high frequency characteristic (NJRC recommends 0.1µF or more). An aluminum electrolytic capacitor is recommended for smoothing capacitor (NJRC recommends 10µF or more). However, you should use large capacitor by sufficient evaluation (assessment) due to load condition and/or application use environment. (There is a possibility that the supply voltage rises by inductive kickback when the supply current of the inductive load is large.) The bypass capacitors should be connected as near as possible to the VDD pin.

## CHARACTERISTICS



# NJW4841-T1

## CHARACTERISTICS



**[CAUTION]**

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