

# TFT COLOR LCD MODULE

Type: NL10276AC30-07 38cm (15 Type), XGA

# **SPECIFICATIONS**

(First Edition)

# **PRELIMINARY**

This document is preliminary. All information in this document is subject to change without prior notice.

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Application examples recommended by NEC Corporation.

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3/27

# **CONTENTS**

1.	DESCRIPTION	P.4
2.	FEATURES	P.4
3.	APPLICATIONS	P.4
4.	STRUCTURE AND FUNCTIONS	P.4
5.	OUTLINE OF CHARACTERISTICS (at room temperature)	P.5
6.	BLOCK DIAGRAM	P.6
7.	GENERAL SPECIFICATIONS	P.7
8.	ABSOLUTE MAXIMUM RATINGS	P.7
9.	ELECTRICAL CHARACTERISTICS	P.7
10.	SUPPLY VOLTAGE SEQUENCE	P.9
11.	INTERFACE PIN CONNECTIONS	P.11
12.	DISPLAY COLORS vs INPUT DATA SIGNALS	P.16
13.	INPUT SIGNAL TIMINGS	P.17
14.	OPTICAL CHARACTERISTICS	P.21
15.	RELIABIBILITY TEST	P.23
16.	ESTIMATED LIFE-TIME OF THE BARE LAMP	P.23
17.	GENERAL CAUTIONS	P.24
18.	OUTLINE DRAWINGS	P.26

#### 1. DESCRIPTION

NL10276AC30-07 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC30-07 has a built-in backlight with an inverter.

The 38cm(15 Type) diagonal display area contains  $1024 \times 768$  pixels and can display 16,777,216 colors simultaneously.

#### 2. FEATURES

- Parallel 8bit interface (2 port)
- Ultra-wide viewing angle (with lateral electric field)
- Fast response time
- · High luminance
- High contrast
- · Wide color gamut
- · Luminance control
- · Small foot print
- Incorporated direct type backlight
- Replaceable backlight unit and inverter

#### 3. APPLICATIONS

PC monitor, FA monitor

### 4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. And the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel. RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

# **5. OUTLINE OF CHARACTERISTICS** (at room temperature)

Display area  $304.128 \text{ (H)} \times 228.096 \text{ (V)mm}$ 

Drive system a-Si TFT active matrix

Display colors 16,777,216 colors

Number of pixels  $1024 \times 768$ 

Pixel arrangement RGB vertical stripe

Pixel pitch  $0.297 \text{ (H)} \times 0.297 \text{ (V)mm}$ 

Module size  $330.0 \text{ (H)} \times 255.4 \text{ (V)} \times 32.0 \text{ Max. (D)} \text{ mm}$ 

Weight 1200 g (Typ.)

Contrast ratio 300:1 (Typ.)

Viewing angle (more than the contrast ratio of 10:1)

Horizontal: 85 ° (Typ., left side, right side)
Vertical: 85 ° (Typ., left side, right side)

Designed viewing direction

Optimum grayscale ( =2.2): perpendicular

Polarizer Pencil-hardness 2 H (Min., at JIS K5400)

Color gamut 60 % (Typ., At center, To NTSC)

Response time Ton(10% 90%) + Toff(90% 10%) = 30 ms (Typ.)

Luminance TBD (design target: 400cd/m<sup>2</sup> Typ.)

Signal system Parallel 8bit interface (2port)

[RGB 8bit data, CLK, DE]

Supply voltage 5V (Logic, LCD driving), 12V (Backlight)

Backlight Direct light type: Eight cold cathode fluorescent lamps and an inverter

[Replaceable parts]
Backlight unit: TBD

· Inverter: TBD

Power consumption 24 W (Typ., Checker flag pattern, at 400 cd/m<sup>2</sup> Typ.)

# 7. GENERAL SPECIFICATIONS

Items	Specifications	Unit
Module size	$330.0 \pm 1.0 \text{ (H)} \times 255.4 \pm 1.0 \text{ (V)} \times 32.0 \text{ Max. (D)}$	mm
Display area	304.128 (H) × 228.096 (V)	mm
	[Diagonal display area: 38cm (Type 15.0)]	
Number of pixels	1024 (H) × 768 (V)	pixel
Dot pitch	0.099 (H) × 0.297 (V)	mm
Pixel pitch	0.297 (H) × 0.297 (V)	mm
Pixel arrangement	RGB (red, green, blue) vertical stripe	
Display colors	16,777,216 (6bit + FRC)	color
Weight	1200(Typ.), TBD(Max.)	g

#### 8. ABSOLUTE MAXIMUM RATINGS

o. ADSOLUTE MAXIMI		100		T	
Parameters	Symbols	Ratings	Unit	Remarks	
Supply voltage	VDD	-0.3 to +16	V	Ta = 25	
Supply voltage	VDDB	-0.3 to +16		1a – 23	
Logic input voltage (LCD)	Vin1	-0.3 to +4.0	V		
Logic input voltage (backlight-BRTP signal)	Vin2	-0.3 to TBD	V	Ta = 25	
Logic input voltage (backlight- BRTC, PWSEL signal)	Vin3	-0.3 to +5.5	V	VDDB=12V	
Logic input voltage (backlight- BRTL signal)	Vin4	-0.3 to TBD	V		
Storage temperature	Tst	-20 to +60		-	
On anoting town anotype	Top1	0 to +55		Module front surface Note1	
Operating temperature	Top2	TBD		Module rear surface Note2	
D 1 ( 1 11 (DII)		≤ 95		Ta≤ 40	
Relative humidity (RH)	Note3	≤ 85	%	40 <ta≤ 50<="" td=""></ta≤>	
	Notes	≤ 70		50 <ta≤ 55<="" td=""></ta≤>	
Absolute humidity	Note3	Absolute humidity shall not exceed Ta=55 , RH =70%.	g/m <sup>3</sup>	Ta > 55	
Operating altitude		TBD	m	$0 \leq Ta \leq 55$	
Storage altitude		TBD	m	-20 ≤ Ta ≤ 60	

Note1: Measure at the display area (including self heat) Note2: Measure at the rear shield (including self heat)

Note3: No condensation

# 9. ELECTRICAL CHARACTERISTICS

(1) Logic/ LCD driving

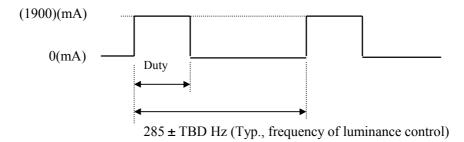
Ta = 25

Parameters	Symbols	Min.	Тур.	Max.	Unit	Remarks
Supply voltage	VDD	4.5	5.0	5.5	V	-
Ripple voltage	VRP	-	-	100	mV	for VDD
Logic input "L" voltage	VTL	0	-	0.8	V	
Logic input "H" voltage	VTH	2.0	-	3.6	V	-
Supply current	ICC	-	300 Note1	TBD Note2	mA	VCC=12.0V

Note1: Checker flag pattern (in EIAJ ED-2522) Note2: Theoretical maximum current pattern (2) Backlight Ta = 25

Parameters	Symbols	Min.	Тур.	Max.	Unit	Remarks	
Supply voltage	VDDB	11.4	12.0	12.6	V	Backlight power supply	
Logic input "L" current2	IiL2	TBD	-	-	V	C. DDTD	
Logic input "H" current2	IiH2	-	-	TBD	V	for BRTP	
Logic input "L" current3	IiL3	TBD	-	-	V	for DDTC DWCEI	
Logic input "H" current3	IiH3	-	-	TBD	V	for BRTC, PWSEL	
Logic input "L" current4	IiL4	TBD	-	-	V	for DDTI	
Logic input "H" current4	IiH4	-	-	TBD	V	for BRTL	
Supply current	IDDB	_	1900	TBD	mA	VDDB=12.0V	
Supply cultent	מעמו	-	1300	וממו	ША	(at Max. luminance)	

#### Inverter current wave



Maximum luminance control : 100% (Duty) Minimum luminance control : 20% (Duty)

Luminance control frequency : 285 ± TBD Hz (Typ.)

Please see 11.INTERFACE PIN CONNECTIONS (4) Luminance control.

### (3)Fuse

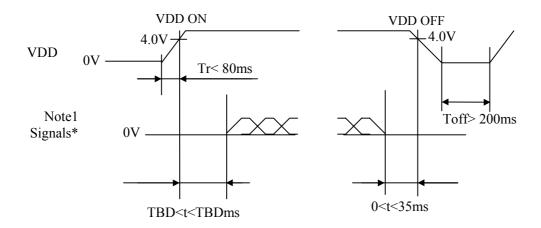
This LCD module uses fuses as follows.

Supply voltage	Part No.	Supplier	Ratings	Remarks
VCC	TBD	TBD	TBD	TBD
VDDB	TBD	TBD	TBD	TBD

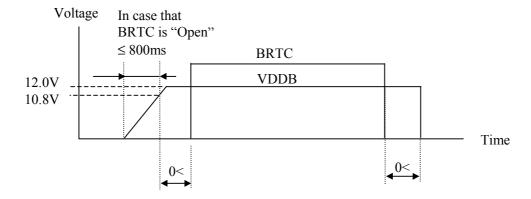
Remark: Before the power is designed, fuses should be considered. The power capacity should be used more than 2.0 times of fuses rating. When the power capacity is less than 2.0 times of fuses rating, the module must be evaluated enough from safety point of view.

#### 10. SUPPLY VOLTAGE SEQUENCE

(1) Supply voltage sequence and backlight control sequence



\* Signals: DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7



Note1: The values of signals are in terminal of resistor 100 ohm.

Remark1: Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

Remark2: When the power supply voltage (VDD) fluctuates less than 4V, the LCD module may not be worked by the protection circuit.

Remark3: Turn on the backlight should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

Remark4: 12V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turn off.

Remark5: The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms.

Remark6: Do not input "H" PWSEL, when VDDB is 0V or BRTC is "L".

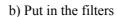
# (2)Ripple of supply voltage

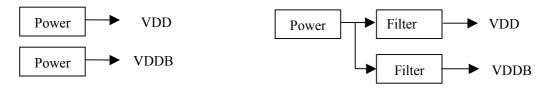
Supply voltage	VDD	VDDB
	(for logic and LCD driver: 5V)	(for backlight: 12V)
Acceptable range	≤ 100 m V p-p	≤ 200 m V p-p

Note1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

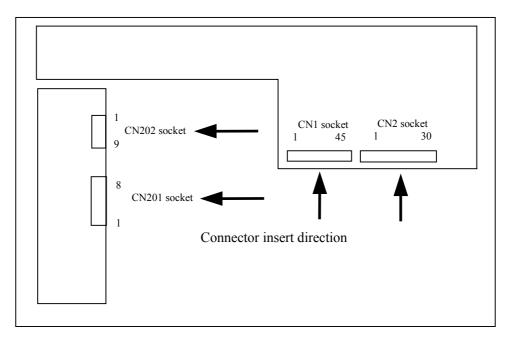
a) Separate the power supplies





# 11. INTERFACE PIN CONNECTIONS

(1) Interface connectors for signals and power



(2) Interface connector for signals and power CN1 socket: IL-FHR-F45S-HF(JAE)

Adaptable plug: TBD

Pin No.	Symbols	Signals type	Functions
1	GND	Ground	Connect to system ground.
2	CLK	Dot clock	Dot clock input
3	GND	Ground	Connect to system ground.
4	DE	Data enable	Data enable input
5	GND	Ground	Connect to system ground.
6	N.C.	Non-connection	Keep the terminal open
7	GND	Ground	Connect to system ground.
8	N.C.	Non-connection	Keep the terminal open
9	GND	Ground	Connect to system ground.
10	N.C.	Non-connection	Keep the terminal open
11	GND	Ground	Connect to system ground.
12	BA7		
13	BA6	Odd pixel data B	Odd pixel data B input
14	BA5	Odd pixei data B	BA7: Most significant bit
15	BA4		
16	GND	Ground	Connect to system ground.
17	BA3		
18	BA2	Odd missal data D	Odd pixel data B input
19	BA1	Odd pixel data B	BA0: Least significant bit
20	BA0		

# CN1 socket

Pin No.	Symbols	Signals type	Functions			
21	GND	Ground	Connect to system ground.			
22	GA7					
23	GA6	044	Odd pixel data G input			
24	GA5	Odd pixel data G	GA7: Most significant bit			
25	GA4					
26	GND	Ground	Connect to system ground.			
27	GA3					
28	GA2	Odd missal data C	Odd pixel data G input			
29	GA1	Odd pixel data G	GA0: Least significant bit			
30	GA0		-			
31	GND	Ground	Connect to system ground.			
32	RA7	Odd pixel data R				
33	RA6		Odd pixel data R input			
34	RA5		RA7: Most significant bit			
35	RA4					
36	GND	Ground	Connect to system ground.			
37	RA3					
38	RA2	Odd pixel data R	Odd pixel data R input			
39	RA1	Oud pixei data K	RA0: Least significant bit			
40	RA0					
41	VDD					
42	VDD	+5V Dower Supply	+5V±TBD%			
43	VDD	+5V Power Supply	T3 V <u>T</u> 1 DD 70			
44	VDD					
45	N.C.	Non-connection	Keep the terminal open			

CN1 socket: Figure from socket view

1 2 • • • • 44 45

CN2 socket: IL-FHR-F30S-HF(JAE)

Adaptable plug: TBD

Pin No.	Symbols	Signals type	Functions
1	GND	Ground	Connect to system ground.
2	BB7		
3	BB6	Even missel data D	Even pixel data B input
4	BB5	Even pixel data B	BB7: Most significant bit
5	BB4		
6	GND	Ground	Connect to system ground.
7	BB3	Even pixel data B	
8	BB2		Even pixel data B input
9	BB1		BB0: Least significant bit
10	BB0		
11	GND	Ground	Connect to system ground.
12	GB7		
13	GB6	Even pixel data G	Even pixel data G input
14	GB5		GB7: Most significant bit
15	GB4		

### CN2 socket

Pin No.	Symbols	Signals type	Functions				
16	GND	Ground	Connect to system ground.				
17	GB3						
18	GB2	Evan nival data C	Even pixel data G input				
19	GB1	Even pixel data G	GB0: Least significant bit				
20	GB0						
21	GND	Ground	Connect to system ground.				
22	RB7						
23	RB6	Evan nival data D	Even pixel data R input				
24	RB5	Even pixel data R	RB7: Most significant bit				
25	RB4						
26	GND	Ground	Connect to system ground.				
27	RB3						
28	RB2	Even pixel data R	Even pixel data R input				
29	RB1	Even pixei data K	RB0: Least significant bit				
30	RB0						

CN2 socket: Figure from socket view

1 2 · · · · 29 30

(3) Connector for backlight unit

CN201 socket: DF3-8P-2H (HIROSE ELECRIC Co., Ltd.)

Adaptable plug: TBD

Pin No.	Symbols	Functions
1	GNDB	Ground for backlight
2	GNDB	(Connect to system ground.)
3	GNDB	
4	GNDB	
5	VDDB	Power supply for backlight
6	VDDB	$(+12V \pm 5\%)$
7	VDDB	
8	VDDB	

CN201 socket: Figure from socket view

1 2 ..... 7 8

CN202 socket: IL-Z-9PL1-SMTY(JAE)

Adaptable plug: TBD

Pin No.	Symbols	Functions			
1	GNDB	Ground for backlight			
2	GNDB	(Connect to system ground.)			
3	N.C.	Keep the terminal open			
4	BRTC	Backlight ON/OFF control signal "H" or "Open" : Backlight ON "L" : Backlight OFF			
5	BRTH				
6	BRTL	Luminance control signal, Please see (4) Luminance control.			
7	BRTP	Lummance control.			
8	GNDB	Ground for backlight			
9	PWSEL	Select signal of PWM luminance control function Please see (4) Luminance control.			

CN202 socket: Figure from socket view

9 8 ..... 2 1

Remark1: Do not keep pins free (except N.C. Pin) to avoid noise issue.

Remark2: GND and GNDB should be connected to system ground in customer equipment.

#### (4) Luminance control

( ) = 0,11111111111111111111111111111111111	* * * * * * * * * * * * * * * * * * * *		
Form	PWM	Voltage	Variable resistor
How to adjust	PWSEL="L"	PWSEL="H" or "Ope	n" and BRTP="OPEN"
	See OUTSIDE	BRTH should be fixed to 0V to control	The variable resistor for luminance control
	CONTROL	luminance by voltage. The range of	should be 10 k $\Omega$ type, and zero point of the
	FOR	input voltage between BRTL and	resistor corresponds to the minimum of
	LUMINANCE	GNDB is as follows.	luminance.
		Maximum luminance: 1V(TBD%)	
		Minimum luminance: 0V(TBD%)	BRTH BRTL
			Maximum luminance: R=10 kΩ(TBD%)
			Minimum luminance : $R=0 \Omega(TBD\%)$
			Mating variable resistor: $10 \text{ k}\Omega$
			B curve, 1/10W
		1	

Remark: The display may be disturbed depend on input signal timing in this luminance control method. In this case, adopt outside control for luminance to avoid interference of the input signal timing and backlight driving timing.

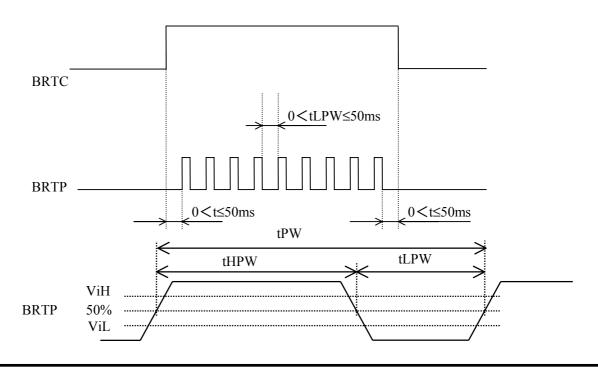
### [OUTSIDE CONTROL FOR LUMINANCE]

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.

Duty=100%: luminance is maximum.

Duty=20%: luminance is minimum.

BRTC must not fix on "L" in the condition of PWSEL= "L" and BRTC ="H" or "Open". Otherwise, the inverter stops. In this case, even if BRTP pulse is input again, the backlight will not turn on. Please input power supply to the inverter again.



DOD-M-0094

15/27

Parameters	Symbols	Min.	Тур.	Max.	Units	Remarks
Frequency	1/tPW	185	1	325	Hz	Note1
"L" period	tLPW	-	-	50	ms	Note2
Pulse-width	tHPW/tPW	20	1	100	%	Duty=100%: Luminance is maximum. Duty=20%: Luminance is minimum.
Luminance	Lu	-	30-100	-	%	-
Immust violate as	ViL	0	-	0.8	V	-
Input voltage	ViH	2.0	-	5.0	V	-

Note1: Regarding set up for frequency, refer to the below method.

Set up frequency = Vsync frequency  $\times$  (n+0.25) or (n+0.75)

Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

Note2: The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms.

16/27

# 12. DISPLAY COLORS vs INPUT DATA SIGNALS

			Data signal (0: Low level, 1: High level)																						
Display	colors	RA7	RA6	RA5	RA5 RA4 RA3 RA2 RA1 RA0   GA7 GA6 GA5 GA4 GA3 GA2 GA1 GA0   BA7 BA6 BA5 BA4 BA3 BA2 BA1 BA0				BA0																
		RB7	RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0			RB0	GB7 GB6 GB5 GB4 GB3 GB2 GB1 GB0				BB7 BB6 BB5 BB4 BB3 BB2 BB1 BB0														
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Basic	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
colors	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red						:								:								:			
grayscale														:											
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Green						:								:								:			
grayscale						:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Blue						:								:								:			
grayscale						:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

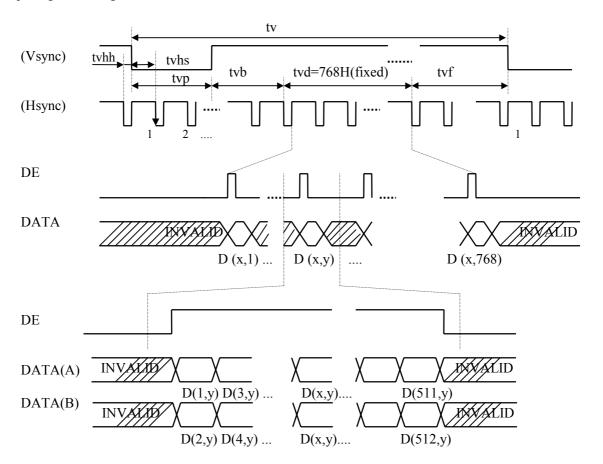
Note1: Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 16,777,216 (256 x 256 x 256) colors.

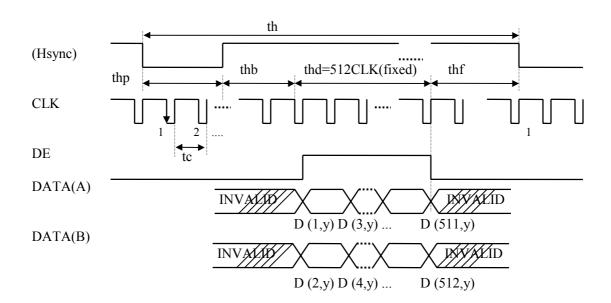
# 13. INPUT SIGNAL TIMINGS

(1) Input signal specifications for LCD controller (2 port input)

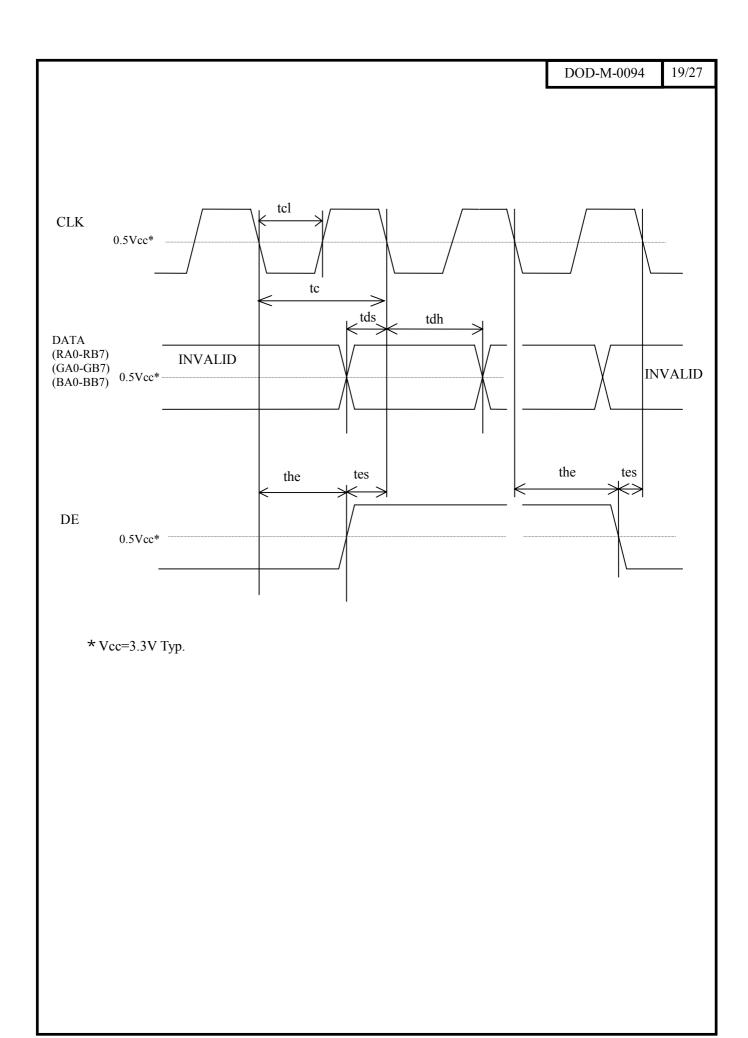
	Parameters		Symbols	Min.	Тур.	Max.	Units	Remarks
CLK		Vf=75Hz		TBD	39.375	TBD	MHz	
	Frequency	V1-7311Z	1/ tc	-	25.397	-	ns	_
	rrequency	Vf=60Hz	17 tc	TBD	32.500	TBD	MHz	_
	_	VI OOIIZ		-	30.769	-	ns	
	Duty	T	tcl / tc	0.4	0.5	0.6	-	-
Hsync	Period	Vf=75Hz	-th	(12.3) (550)	16.660 656	(1000)	μs CLK	Typ.=60.023kHz
	i criod	Vf=60Hz	ui	(12.3) (550)	20.677 672	- (1000)	μs CLK	Typ.=48.363kHz
	Display period	•	thd	-	512	-	CLK	-
	Event manels	Vf=75Hz	thf	-	8	-	CLV	
	Front-porch	Vf=60Hz	7411	-	12	-	CLK	-
	Pulse width	Vf=75Hz	thp *	-	48	-	CLK	
	Puise width	Vf=60Hz	uip ·	-	68	-	CLK	-
	Back-porch	Vf=75Hz	thb *	-	88	-	CLK	
	Баск-роген	Vf=60Hz	uib .	-	80	-	CLK	-
	* thp + thb			(38)	-	-	CLK	-
Vsync	David 4	Vf=75Hz	4	- (771)	13.328 800	TBD -	ms H	Typ=75.029Hz
	Period	Vf=60Hz	tv	- (771)	16.666 806	TBD -	ms H	Typ=60.0Hz
	Display period	II.	tvd	-	768	-	Н	-
	Front-porch	Vf=75Hz	tvf*	-	1	-	Н	
	Pront-porch	Vf=60Hz	tvi	-	3	-	11	-
	Pulse width		tvp *	-	3	-	Н	
	ruise width		tvp ·	-	6	-	11	-
	Back-porch		tvb *	-	28	-	Н	
	Back-porch		tvo ·	-	29	-	11	-
		* $tvp + tvb$	+tvf	(3)	-	-	Н	-
	Vsync-Hsync t	iming	tvhs	1	-	-	CLK	-
	Hsync-Vsync t	iming	tvhh	1	-	-	CLK	-
DATA (RA0-RB7)	DATA-CLK (S	let up)	tds	(2)	-	-	ns	-
(GA0-GB7) (BA0-BB7)	CLK-DATA (H	Iold)	tdh	(2)	-	-	ns	-
DE	DE-CLK timin	g	tes	(2)	-	-	ns	-
	CLK-DE timin	g	the	(2)	-	-	ns	-

# (2) Input signals timing chart for LCD





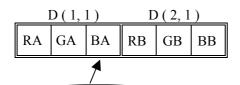
DATA(A): RA0-RA7, GA0-GA7, BA0-BA7 DATA(B): RB0-RB7, GB0-GB7, BB0-BB7



# (3) Display positions of input data

Odd Pixel: RA= R DATA
Odd Pixel: GA= G DATA
Odd Pixel: BA= B DATA

Even Pixel: RB=R DATA
Even Pixel: GB=G DATA
Even Pixel: BB=B DATA



	D(1,1)	D( 2,1 )	•••	D( 1024,1 )
	D(1,2)	D(2,2)	•••	D(1024,2)
	•	•	•	•
	•	•	•	•
	•	•	•	•
	•	•	•	•
•	D(1,768)	D(2,768)	•••	D(1024,768)

### 14. OPTICAL CHARACTERISTICS

(Ta= 25, VDD= 5V, VDDB=12V, Note1)

Parameters	Symbols	Conditions	Min.	Тур.	Max.	Units	Remarks
Contrast ratio	CR	Note 3	TBD	(300)	ı	1	Note2
Luminance	Lumax	Note 3	TBD	TBD (design target: 400cd/m² Typ.)	1	cd/m <sup>2</sup>	-
Luminance uniformity	-	Max. / Min.	-	(1.1)	1.3	-	Note3,6
	W	White $(x, y)$	-	(0.300, 0.315)	1	1	
Chromaticity	R	Red(x, y)	-	TBD	1	-	Nata?
Coordinates	G	Green (x, y)	-	TBD	. 1	-	Note3
	В	Blue (x, y)	-	TBD	-	-	

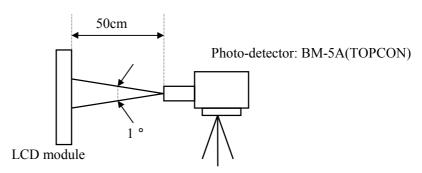
Reference data

(Ta= 25, VDD= 5V, VDDB=12V, Note1)

					( 1	$\mathfrak{a}$ 23, $\mathfrak{v}$ $\mathfrak{D}$ $\mathfrak{D}$	$\mathcal{I}$ , $\mathcal{I}$	DD 12 1	, 110101)	
Parar	neters	Symbols Conditions		ditions	Min.	Тур.	Max.	Units	Remarks	
Color gamu	ut	C	To N	NTSC	50	60	-	%	Note3	
Viewing	Homizontol	x+	CR>10,	v= ±0°	70	85	-	deg.		
Angle	Horizontal	Х-	CR>10,	y – ±0	70	85	-	deg.		
Range		y+	CD> 10	x = ±0 °	70	85	-	deg.		
(CR>10)	Vertical	y-	CR>10,	X - 10	70	85	-	deg.	Noted	
Viewing	II1	χ+	CD>5	0.9	-	85	-	deg.	Note4	
Angle	Horizontal	Х-	CR>5,	y= ±0 °	-	85	-	deg.		
Range		y+	CD>5	0.9	-	85	-	deg.		
(CR>5)	Vertical	y-	CR>5,	$x = \pm 0$ °	-	85	-	deg.		
Response ti	ime	Ton	White to black	90% 10%	-	TBD	TBD			
(Module fro	ont surface	Iodule front surface mperature = TBD)		Black to white	10% 90%	ı	TBD	TBD	ms	Note3,5
1	,	Ton(10%	90%) + Tof	f(90% 10%)	-	(30)	-			
Luminance range	control	-	Maximum luminannce:	100%	-	30-100	-	%	-	

Note1: Optical characteristics are measured after 20 minutes from the module works. Typical value is measured after luminance saturation. The luminance is measured in dark room.

Input signal timing: XGA-60Hz mode



Note2: The contrast ratio is calculated by using the following formula.

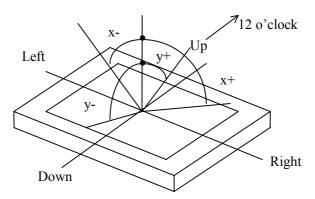
Contrast ratio (CR) = Luminance with all pixels in white

Luminance with all pixels in black

Note3: Viewing angle is  $x = \pm 0^{\circ}$ ,  $y = \pm 0^{\circ}$  and at center.

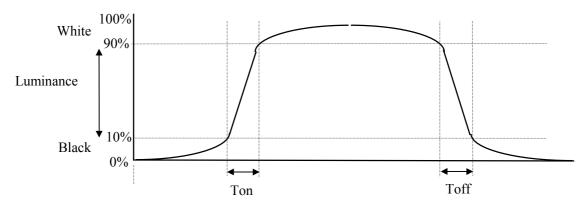
Note4: Definitions of viewing angle are as follows

# Perpendicular



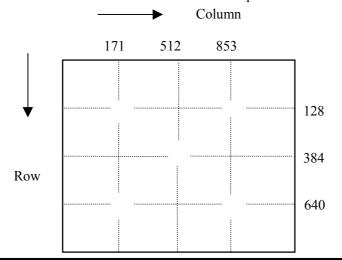
Note5: Definitions of response time are as follows.

Photo-detector output signal is measured when the luminance changes "white" to "black" or "black" to "white". Response time is the time between 10% and 90% of the photo-detector output amplitude.



Note6: Luminance uniformity is calculated by using the following formula.

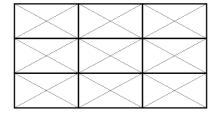
The luminance is measured at near the five points shown below.



#### 15. RELIABILITY TEST

Test items	Test conditions	Judgment			
High temperature/humidity	$60 \pm 2$ , RH= $60\%$	*1			
operation	240 hours, Display data is black.				
Heat cycle (operation)	0 ± 3 ··· 1 hour	*1			
	55 ± 3 · · · 1 hour				
	50 cycles , 4 hours/cycle				
	Display data is black.				
Thermal shock	-20 ± 3 ··· 30 minutes	*1			
(non-operation)	$60 \pm 3 \cdots 30$ minutes				
	100 cycles				
	Temperature transition time is within				
	5 minutes.				
Vibration (non-operation)	5-100Hz, 11.76m/s <sup>2</sup> , 1 minute/cycle,	*1, *2			
	X,Y,Z direction				
	50 times each direction				
Mechanical shock	294m/s <sup>2</sup> , 11ms	*1, *2			
(non-operation)	X,Y,Z direction				
	3 times each direction				
ESD (operation)	$150 pF, 150 , \pm 10 kV$	*1			
	9 places on a panel *3				
	10 times each place at one-second intervals				
Dust (operation)	15 kinds of dust (JIS-Z 8901)	*1			
	Hourly 15 seconds stir, 8 times repeat				

- \*1: Display function is checked by the same condition as LCD module out-going inspection.
- \*2: Physical damage
- \*3: Discharge points are shown in the figure.



# 16. ESTIMATED LIFE-TIME OF THE BARE LAMP

	Bare lamp							
Conditions	Luminance Maximum							
Conditions	Room temp. ( $25 \pm 2$ ), Continuous operation	Note3						
Estimated value	50,000h	Note 1,2						
(MTTF)								
Criteria	Half value luminance (compared with initial value.)							

Note1: The life-time is **estimated value** (reference).

Note2: **This estimated value is based on the test results with a bare lamp operation.** The MTTF for the module may be different from these values, because of the influence of ambient and clamshell conditions.

Note3: The life-time becomes short if the module is operated under the low and high temperature environment.

#### 17. GENERAL CAUTIONS

Because the following statements are very important, please be sure you understand their contents completely.



# **CAUTION**

This figure is a warning that you will get hurt and/or the module will be damaged if you make a mistake in operation.



This figure is a warning that you will get an electric shock if you make a mistake in operation.



This figure is a warning that you will get hurt if you make a mistake in operation.



#### CAUTIONS



Do not touch an inverter on which there is a caution label is stuck while the LCD module is in operation, because of dangerous high voltage.

#### (1) Caution when taking out the module

Pick up the pouch only, when removing the module from a carrier box.

#### (2) Cautions for handling the module

As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges. Peel protection sheet out from the LCD panel surface as slowly as possible.



As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

Do not pull the interface connectors in or out while the LCD module is operating.

Put the module display side down on a flat horizontal plane.

Handle connectors and cables with care.

When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

The torque for mounting screws should never exceed 0.39N·m.

Don't push or rub the surface of LCD module please.

If you do, the scratches or the marks like rubbing marks may be left on the surface of the module.

Do not give the stress too much on interface connectors. The module may become function deficiency by a contact defective and damages. Pay attention to handling at the time of matching connector connection and in the connection condition.

Do not put front side (display surface side ) of the module on a desk or a table for a long time, because the display may become un-uniformity.

## (3) Cautions regarding atmosphere

Dew-drop atmosphere must be avoided.

Do not store and/or operate the LCD module in a high-temperature and/or high-humidity atmosphere.

Storage in an anti-static pouch and under the room temperature atmosphere is recommended.

This module uses cold cathode fluorescent lamps. Therefore the lifetime of lamps is shortened if the module is operated under the low temperature environment.

Do not operate the LCD module in high magnetic field.

### (4) Cautions about the module characteristics

Do not apply any fixed pattern data for a long time to the LCD module. It may cause image sticking. Use screen savers if the display pattern is fixed.

This module has the lends sheet which may cause the variation of the color hue in the different viewing angles. The ununiformity may appear on the screen under the high temperature operation.

The light vertical stripe may be observed depending on the display pattern. This is not defects or malfunctions.

The noise from the inverter circuit may observed in the luminance control mode. This is not defects or malfunctions.

#### (5) Other cautions

Do not disassemble and/or reassemble the LCD module.

Do not readjust variable resistors nor switches in the module.

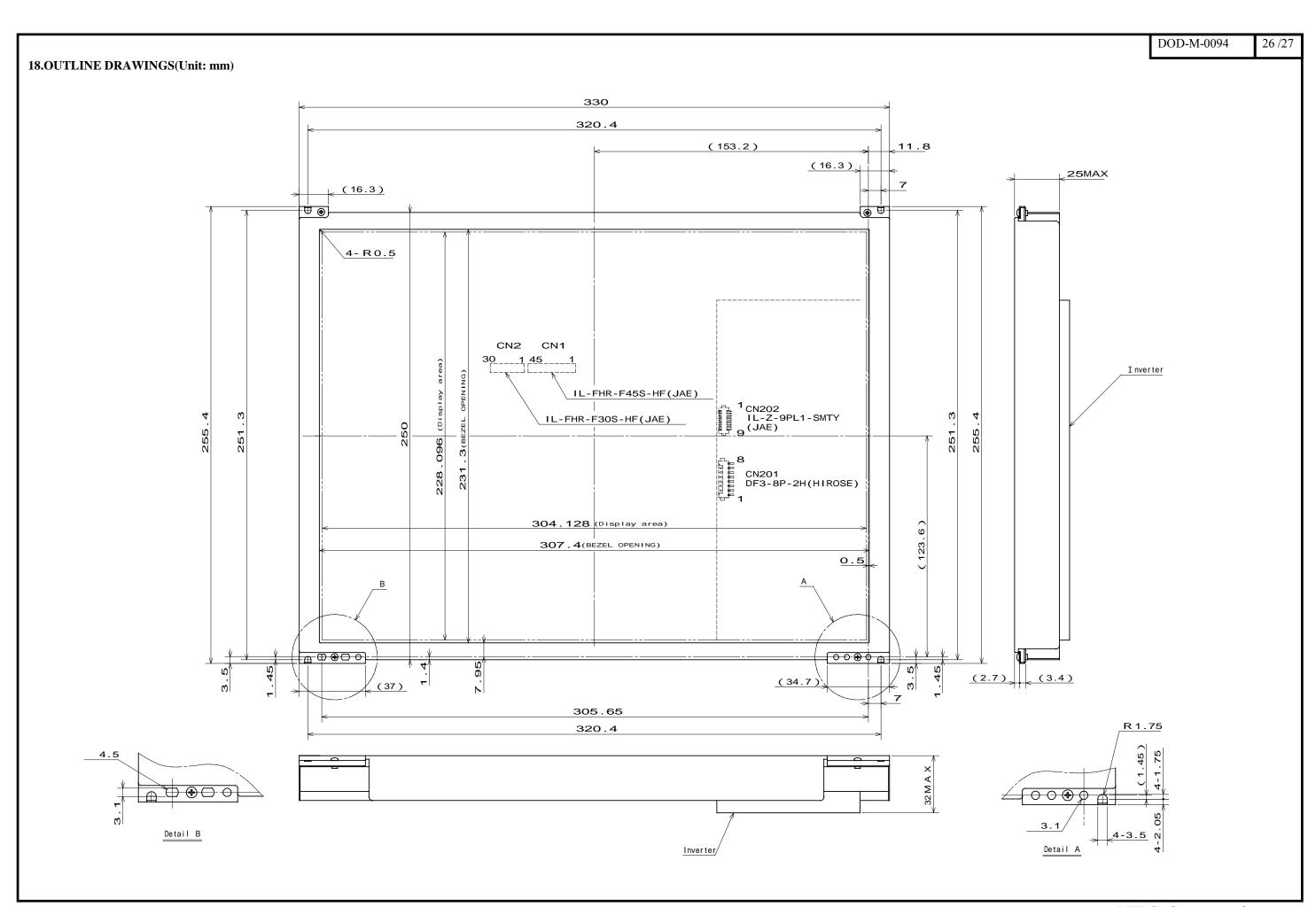
When returning the module for repair, etc., please pack the module properly to avoid any damages. NEC recommends using original shipping packages.

The liquid crystal display has the following specific characteristics. These are not defects or malfunctions.

The optical characteristics of this module may be affected by the ambient temperature.

This module has cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will be changed by the progress in time.

Uneven brightness and/or small spots may be observed depending on different display patterns.



Revision History				DO	DOD-M-0094	
Rev.	prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	Jan. 25, 2001	DOD-M-0094(abstract)	allinto	-	R. Kawashina	-