NEC

TFT COLOR LCD MODULE

Type: NL128102AC28-07
46cm (18.1 Type), SXGA
LVDS interface (2 port)

SPECIFICATIONS

(Second Edition)

PRELIMINARY

This document is preliminary. All information in this document is subject to change without prior notice.

NEC Corporation NEC Electron Devices Display Device Operations Unit Color LCD Division Application Engineering Department		
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Prepared		Nov. 8, 2000

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CONTENTS

1. DESCRIPTION

The NL128102AC28-07 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL128102AC28-07 has a built-in backlight with an inverter.
The 46 cm (18.1 Type) diagonal display area contains 1280×1024 pixels and can display 16,194,277 colors simultaneously.

2. FEATURES

- LVDS interface (adapted THC63LVDF84A ×2,THine Electronics, Inc. as a receiver)
- Fast response time
- Ultra-wide viewing angle (with lateral electric field)
- Narrow frame structure
- Light weight
- Thin thickness
- High luminance
- Wide color gamut
- Low reflection
- Incorporated direct type backlight
- Replaceable backlight unit and inverter

3. APPLICATIONS

- Desk top PCs, Engineering work stations
- Display terminals for control systems
- Monitors

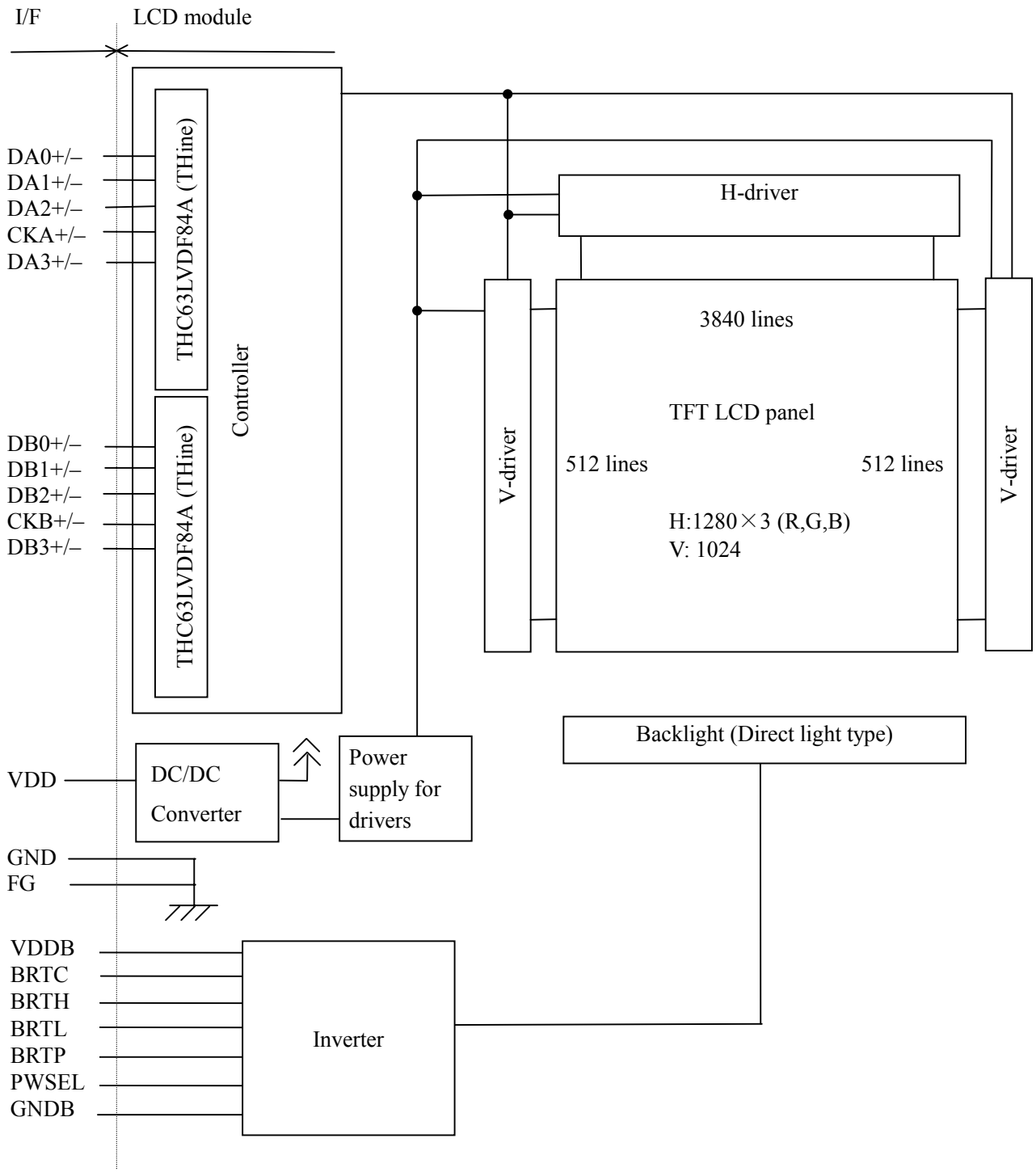
4. STRUCTURE AND FUNCTION

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure. After the driver LSIs are connected to the panel, the backlight assembly is attached to the back side of the panel.
RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active-matrix addressing by the onboard signal processor and sent to the driver LSIs, which in turn addresses the individual TFT cells.
Acting as an Electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	359.04 (H) × 287.232 (V) mm
Drive system	a-Si TFT active matrix
Display colors	16,777,216 colors
Number of pixels	1280 (H) × 1024 (V)
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.2805 (H) × 0.2805 (V) mm
Module size	389.0 (Typ., H) × 317.2 (Typ., V) × 30.3 (Typ., D) mm
Weight	2000 g (Typ.)
Contrast ratio	350:1 (Typ.)
Viewing angle (more than the contrast ratio of 10:1)	・ Horizontal: 85 ° (Typ., left side, right side) ・ Vertical: 85 ° (Typ., up side, down side)
Designed viewing direction	・ Optimum gray-scale (γ =2.2): Perpendicular
Polarizer pencil-hardness	2 H (Min., at JIS K5400)
Color gamut	60 % (Typ., at center, To NTSC)
Response time	Ton + Toff = 40 ms (Typ.)
Luminance	200 cd/m^2 (Typ.)
Signal system	LVDS interface (Receiver: THC63LVDF84A×2, THine Electronics, Inc.) RGB 8-bit signals, Synchronous signals (Hsync, Vsync), Data enable signal (DE) and Dot clock (CLK) encoded with THC63LVDF83A are preferable.
Supply voltage	12 V (Logic, LCD driving)
Backlight	Direct light type: Twelve cold cathode fluorescent lamps and an inverter [Replaceable parts] · Backlight unit: T.B.D. · Inverter: T.B.D.
Power consumption	39 W (Typ.)

6. BLOCK DIAGRAM



Note1: GND (signal ground), FG (frame ground) and GNDB(backlight ground) should be connected to system ground in customer equipment.

7. GENERAL SPECIFICATIONS

Items	Specifications	Units
Module size	389.0 ±1.0 (H) × 317.2 ±1.0 (V) × 30.3 (Typ., D)	mm
Display area	359.04 (H) × 287.232 (V) [Diagonal display area: 46cm (Type 18.1)]	mm
Number of pixels	1280 (H) × 1024 (V)	pixel
Dot pitch	0.0935 (H) × 0.2805 (V)	mm
Pixel pitch	0.2805 (H) × 0.2805 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	16,777,216	color
Weight	2000 (Typ.), 2100 (Max.)	g

8. ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Units	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta = 25℃
	VDDB	-0.3 to +14		
Logic input voltage (LCD)	Vi	-0.3 to +3.6	V	Ta = 25℃ VDD= 12V
Logic input voltage (BRTC)	ViBL1	-0.3 to +5.5		Ta = 25℃ VDDB= 12V
Logic input voltage (BRTL)	Vin4	-0.3 to +1.5		
Storage temperature	Tst	-20 to +60	℃	-
Operating temperature	Top1	0 to +55		Module front surface Note 1
	Top2	T.B.D.		Module rear surface Note 2
Relative humidity (RH) Note 3		≤ 95	%	Ta≤ 40℃
		≤ 85		40℃<Ta≤ 50℃
		≤ 70		50℃<Ta≤ 55℃
Absolute humidity Note 3		Absolute humidity shall not exceed Ta= 55℃, RH = 70% .	g/m^3	Ta>55℃
Operating altitude		T.B.D.	m	0℃≤ Ta ≤ 55℃
Storage altitude		T.B.D.	m	-20℃≤ Ta ≤ 60℃

Note1: Measure at the display area (including self heat)
Note2: Measure at the rear shield (including self heat)
Note3: No condensation

9. ELECTRICAL CHARACTERISTICS

(1) Logic/ LCD driving (Ta = 25℃)

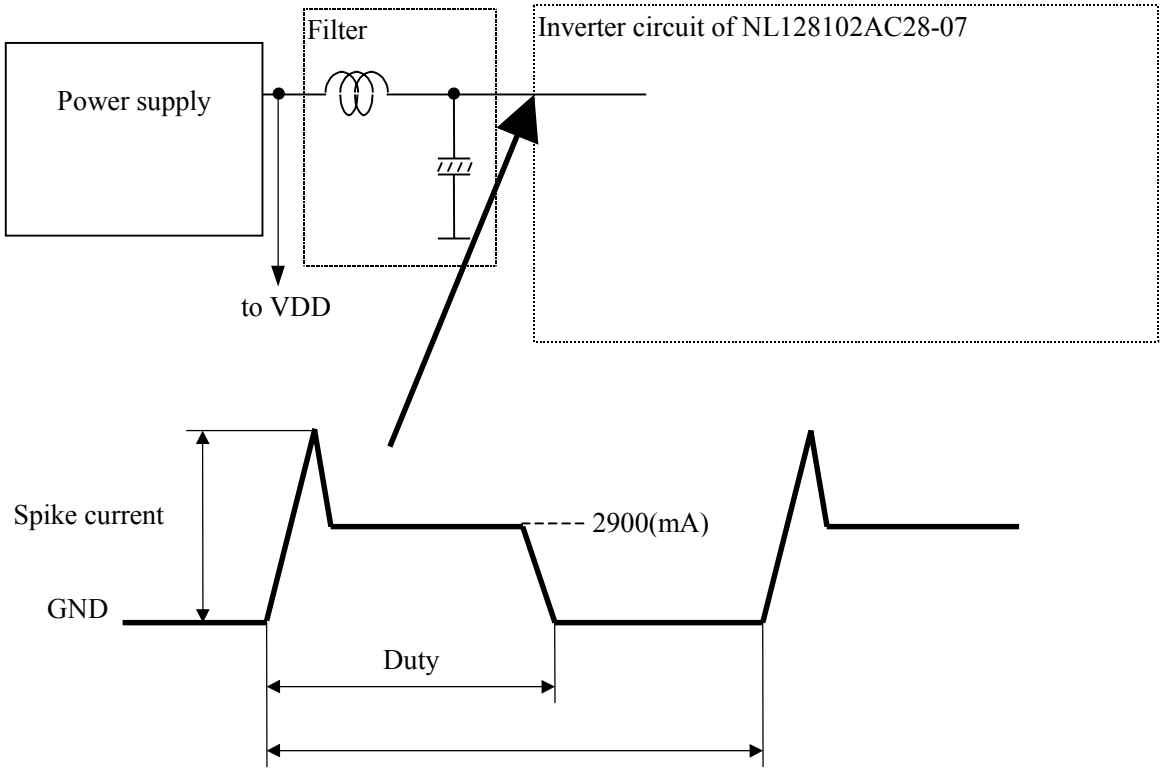
Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Supply voltage	VCC	10.8	12.0	13.2	V	—
Ripple voltage	VRP	-	-	+100	mV	for VCC
Differential input (H) Threshold voltage	VTH	-	-	+100	mV	VCM=1.2V Note 1
Differential input (L) Threshold voltage	VTL	-100	-	-	mV	
Differential Input voltage	VI	0	-	2.4	V	—
Terminating resistor	RT	-	100	-	Ω	—
Supply current	ICC	-	300 Note 2	700 Note 3	mA	VCC= 12.0V

Note1: Common mode voltage in LVDS transmitter
Note2: Checker flag pattern (in EIAJ ED-2522)
Note3: Theoretical maximum current pattern

(2) Backlight

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Supply voltage	VDDB	10.8	12.0	13.2	V	backlight power supply
Logic input "L" current	IiL1	-1580	-	-	µA	for BRTP
Logic input "H" current	IiH1	-	-	3500	µA	
Logic input "L" current	IiL2	-810	-	-	µA	for BRTC, PWSEL
Logic input "H" current	IiH2	-	-	440	µA	
Supply current	IDDB	-	2900	3500	mA	VDDB=12.0V (at Max. luminance)

(3) Inverter current wave



237 to 273, 255Hz (typ., frequency of luminance control)

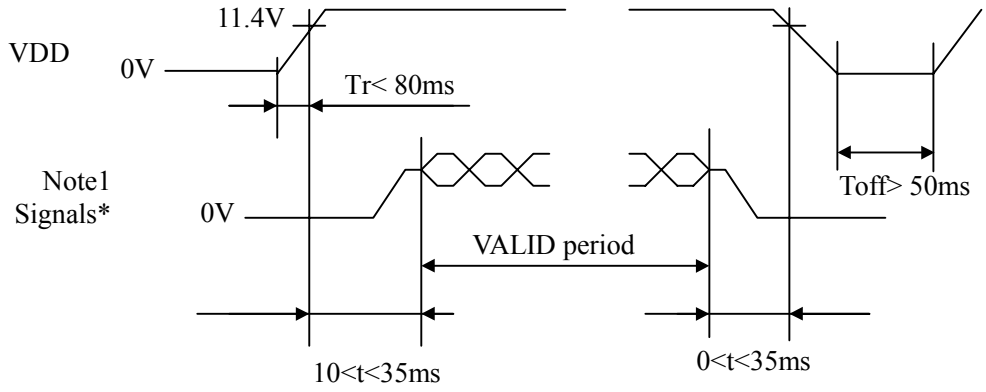
Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 237 to 273Hz, 276Hz (Typ.)

Note1: The power supply lines (VDDB and GNDB) have large ripple voltage while dimming. There is the possibility that the ripple voltage produce an acoustic noise and signal wave noise in a system circuit (e.g. audio circuit).
If the noise occurred in a system circuit, add aluminum electrolytic capacitor (5000 to 6000 μF) between the power source lines (VDDB and GNDB), and the aluminum electrolytic capacitor will be able to reduce the noise.

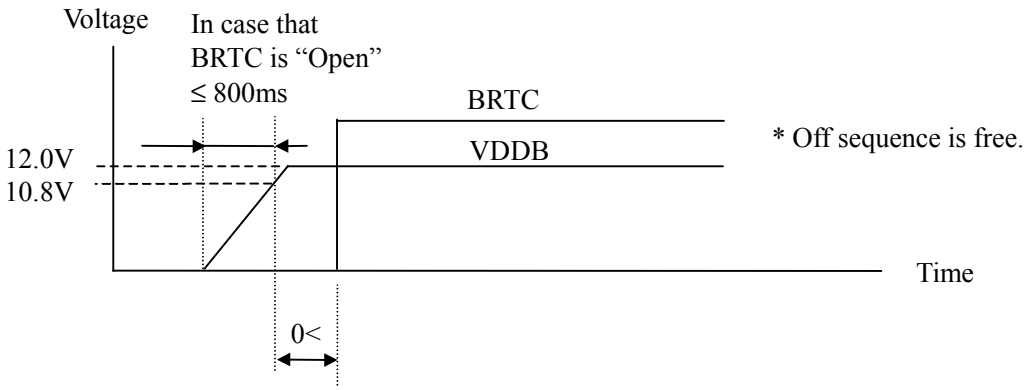
Note2: Please refer to 11.INTERFACE PIN FUNCTIONS Note2 "Luminance control by voltage and a variable resister."

10. SUPPLY VOLTAGE SEQUENCE

(1) Supply voltage sequence and backlight control sequence



* Signals: Hsync, Vsync, DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7



Note1: The values of signals are in terminal of resistor 100 Ω.

Remark1: Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.

Remark2: When the power supply voltage fluctuates between 10.8V to less than 11.4V, the LCD module may not be worked by the protection circuit.

Remark3: Turn on the backlight should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals.

Remark4: 12V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turn off.

Remark5: The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms.

Remark6: Do not input "H" ACA and PWSEL, when VDD is 0V or BRTC is "L".

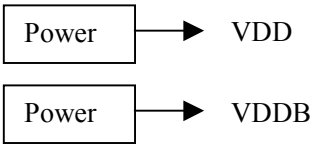
(2)Ripple of supply voltage

Supply voltage	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable range	≤ 100 m V p-p	≤ 200 m V p-p

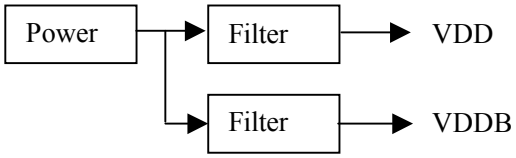
Note1: The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supplies



b) Put in the filters



(3)This LCD module uses fuses as follows.

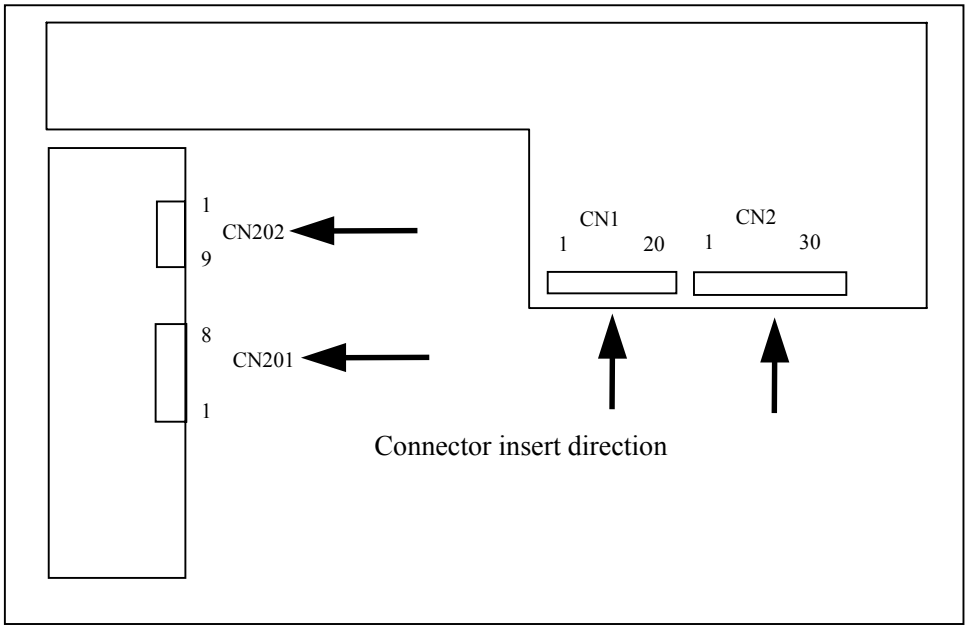
Fuse

	Type name	Producer	Ratings
VDD	CCP2E40	KOA	1.6A
VDDB	T.B.D.	T.B.D.	T.B.D.

Remark1: Before the power is designed, fuses should be considered. The power capacity should be used more than 2.0 times of fuses rating. When the power capacity is less than 2.0 times of fuses rating, the module must be evaluated enough from safety point of view.

11. INTERFACE PIN CONNECTIONS

(1) Interface connectors for signals and power



CN1 socket: 53780-2010
Adaptable plug: 51146-2000
Supplier: Molex Incorporated.

Pin No.	Symbols	Signals type	Functions
1	N.C.	Non-connection	Keep the terminal open
2	N.C.		
3	GND	Ground	Connect to system ground Note 1
4			
5	DA0-	Odd pixel data 0	Odd pixel data input 0 (LVDS level) Note 2
6	DA0+		
7	GND	Ground	Connect to system ground Note 1
8	DA1-	Odd pixel data 1	Odd pixel data input 1 (LVDS level) Note 2
9	DA1+		
10	GND	Ground	Connect to system ground Note 1
11	DA2-	Odd pixel data 2	Odd pixel data input 2 (LVDS level) Note 2
12	DA2+		
13	GND	Ground	Connect to system ground Note 1
14	CKA-	Odd pixel clock	Odd pixel clock input (LVDS level) Note 2
15	CKA+		
16	GND	Ground	Connect to system ground Note 1
17	DA3-	Odd pixel data 3	Odd pixel data input 3 (LVDS level) Note 2
18	DA3+		
19	GND	Ground	Connect to system ground Note 1
20	N.C.	Non-connection	Keep the terminal open

Note1: Do not keep pins free (except 1, 2 and 20 pin) to avoid noise issue.
Note2: Use 100Ω twist pair wires for the cable.

Figure from socket view

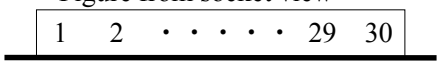
1	2	・・・・・	19	20

CN2 socket: 53780-3010
Adaptable plug: 51146-3000
Supplier: Molex Incorporated.

Pin No.	Symbols	Signals type	Functions	
1	N.C.	Non-connection	Keep the terminal open.	
2	N.C.			
3	GND	Ground	Connect to system ground.	Note 1
4	GND			
5	DB0-	Even pixel data 0	Even pixel data input 0 (LVDS level)	Note 2
6	DB0+			
7	GND	Ground	Connect to system ground.	Note 1
8	DB1-	Even pixel data 1	Even pixel data input 1 (LVDS level)	Note 2
9	DB1+			
10	GND	Ground	Connect to system ground.	Note 1
11	DB2-	Even pixel data 2	Even pixel data input 2 (LVDS level)	Note 2
12	DB2+			
13	GND	Ground	Connect to system ground.	Note 1
14	CKB-	Even pixel clock	Even pixel clock input (LVDS level)	Note 2
15	CKB+			
16	GND	Ground	Connect to system ground.	Note 1
17	DB3-	Even pixel data 3	Even pixel data input 3 (LVDS level)	Note 2
18	DB3+			
19	GND	Ground	Connect to system ground.	Note 1
20	Reserved	Reserved	Keep the terminal open.	
21	Reserved			
22	Reserved			
23	Reserved			
24	GND	Ground	Connect to system ground	Note 1
25	GND			
26	GND			
27	N.C.	Non-connection	Keep the terminal open.	
28	VDD	+12V Power Supply	12V±5%	
29	VDD			
30	VDD			

Note1: Do not keep pins free (except 1, 2, 20, 21, 22, 23 and 27 pin) to avoid noise issue.
Note2: Use 100Ω twist pair wires for the cable.

Figure from socket view



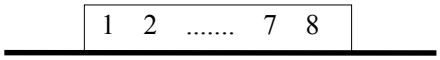
(2) Connector for backlight unit

CN201 socket: DF3-8P-2H
Adaptable plug: DF3-8S-2C
Supplier: HIROSE ELECTRIC Co,. Ltd.

Pin No.	Symbols	Signals type	Functions
1	GNDB	Ground for backlight	Note 1
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	12V power supply	+12V±10%
6	VDDB		
7	VDDB		
8	VDDB		

Note1: GNDB should be connected to system ground in customer equipment.
Remark1: Do not keep pins free to avoid noise issue.

Figure from socket view

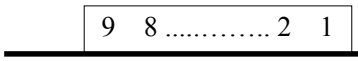


CN202 socket: IL-Z-9PL1-SMTY
Adaptable plug: IL-Z-9S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

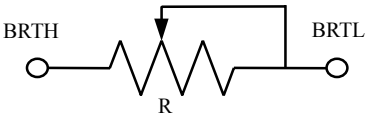
Pin No.	Symbols	Signals type	Functions
1	GNDB	Ground for backlight	Note 1
2	N.C.	Non-connection	Keep the terminal open
3	N.C.		
4	BRTC	Backlight ON/OFF control signal	"H" or "Open" : Backlight on "L" : Backlight off
5	BRTH	Luminance control signal	-
6	BRTL	Luminance control signal	
7	BRTP	Luminance control signal	-
8	GNDB	Ground for backlight	Note 1
9	PWSEL	Luminance control select signal	-

Note1: GNDB should be connected to system ground in customer equipment.
Remark1: Do not keep pins free (except 2 and 3) to avoid noise issue.

Figure from socket view

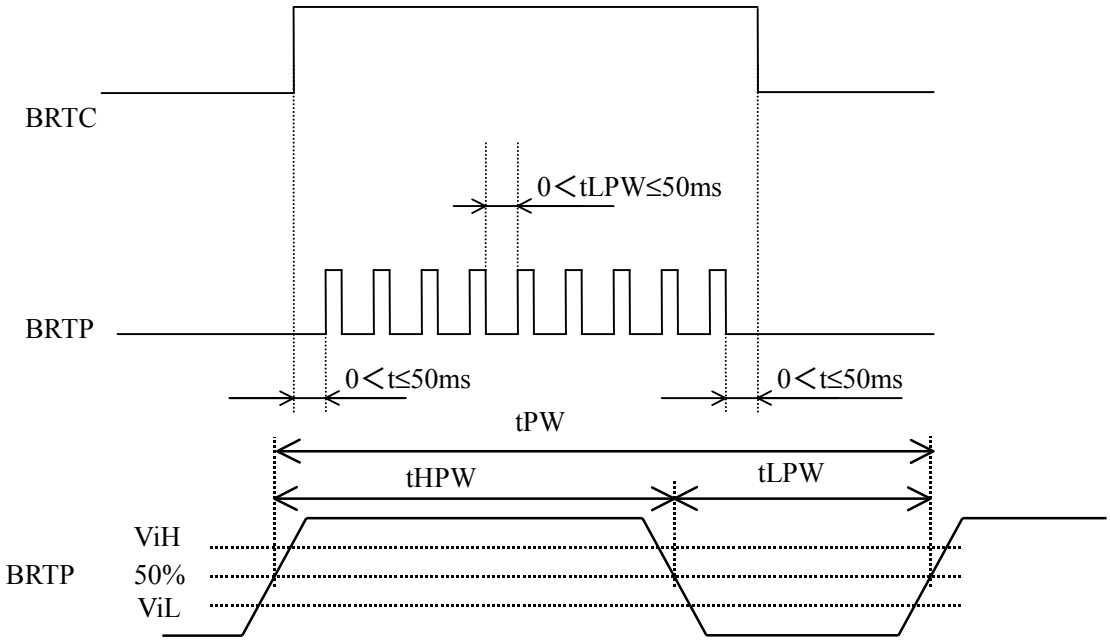


Note2: Luminance control

Form	PWM	Voltage	Variable resistor
How to adjust	PWSEL="L"	PWSEL="H" or "Open" and BRTP="OPEN"	
	See **OUTSIDE CONTROL FOR LUMINANCE**	BRTH should be fixed to 0V to control luminance by voltage. The range of input voltage between BRTL and GNDB is as follows. Maximum luminance: 1V(T.B.D.) Minimum luminance: 0V(T.B.D.)	The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Maximum luminance: R=10 kΩ Minimum luminance : R= 0 Ω(T.B.D.) Mating variable resistor: 10 kΩ(T.B.D.) B curve, 1/10W

[OUTSIDE CONTROL FOR LUMINANCE]

Outside control is valid, when PWSEL="L" and input signal for BRTP. Luminance can be controlled by the duty value of input signal for BRTP.
Duty=100%: luminance is maximum.
Duty=20%: luminance is minimum.



Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Frequency	1/tPW	185	—	325	Hz	Note1
"L" period	tLPW	—	—	50	ms	Note2
Pulse-width	tHPW/tPW	20	—	100	%	Duty=100%: luminance is maximum. (T.B.D.) Duty=20%: luminance is minimum. (T.B.D.)
Input voltage	ViL	0	—	0.8	V	—
	ViH	2.0	—	5.25	V	—

Note1: Regarding set up for frequency, refer to the below method.

Set up frequency = Vsync frequency × (n+0.25) or (n+0.75)

Adopt the frequency evaluating the display quality, because the display will be disturbed depend on frequency.

Note2: The backlight is turned off with safety circuit, when "L" period of BRTP signal is input more than 50 ms.

12. METHOD OF CONNECTION FOR THC63LVDM83A

System side ◄——► LCD module side

			TRANSMITTER				I/F CN			RECIEVER				INPUT to LCD
			pin	THC63LVDF83A		pin	pin	CN1		pin	THC63LVDF84A	pin		
Odd pixel data and control signal	RA2	→	51	TA0			1	N.C.			RA0	27	→	RA2
	RA3	→	52	TA1			2	N.C.			RA1	29	→	RA3
	RA4	→	54	TA2			3	GND			RA2	30	→	RA4
	RA5	→	55	TA3			4	GND			RA3	32	→	RA5
	RA6	→	56	TA4	TA-	48	5	DA0-	→	9	RA-	33	→	RA6
	RA7	→	3	TA5	TA+	47	6	DA0+	→	10	RA+	35	→	RA7
	GA2	→	4	TA6			7	GND			RA6	37	→	GA2
	GA3	→	6	TB0	TB-	46	8	DA1-	→	11	RB-	38	→	GA3
	GA4	→	7	TB1	TB+	45	9	DA1+	→	12	RB+	39	→	GA4
	GA5	→	11	TB2			10	GND			RB2	43	→	GA5
	GA6	→	12	TB3	TC-	42	11	DA2-	→	15	RC-	45	→	GA6
	GA7	→	14	TB4	TC+	41	12	DA2+	→	16	RC+	46	→	GA7
	BA2	→	15	TB5			13	GND			RB5	47	→	BA2
	BA3	→	19	TB6	TCLK-	40	14	CKA-	→	17	RCLK-	51	→	BA3
	BA4	→	20	TC0	TCLK+	39	15	CKA+	→	18	RCLK+	53	→	BA4
	BA5	→	22	TC1			16	GND			RB6	54	→	BA5
	BA6	→	23	TC2	TD-	38	17	DA3-	→	19	RD-	55	→	BA6
	BA7	→	24	TC3	TD+	37	18	DA3+	→	20	RD+	1	→	BA7
	Hsync	→	27	TC4			19	GND			RC4	3	→	Hsync
	Vsync	→	28	TC5			20	N.C.			RC5	5	→	Vsync
	DE	→	30	TC6							RC6	6	→	DE
	RA0	→	50	TD0							RD0	7	→	RA0
	RA1	→	2	TD1							RD1	34	→	RA1
	GA0	→	8	TD2							RD2	41	→	GA0
	GA1	→	10	TD3							RD3	42	→	GA1
	BA0	→	16	TD4							RD4	49	→	BA0
	BA1	→	18	TD5							RD5	50	→	BA1
Note1	RSVD	→	25	TD6							RD6	2	→	RSVD
	CLK	→	31	CLKIN			pin	CN2			CLKOUT	26	→	CLKA
Even pixel data	RB2	→	51	TA0			1	N.C.			RA0	27	→	RB2
	RB3	→	52	TA1			2	N.C.			RA1	29	→	RB3
	RB4	→	54	TA2			3	GND			RA2	30	→	RB4
	RB5	→	55	TA3			4	GND			RA3	32	→	RB5
	RB6	→	56	TA4	TA-	48	5	DB0-	→	9	RA-	33	→	RB6
	RB7	→	3	TA5	TA+	47	6	DB0+	→	10	RA+	35	→	RB7
	GB2	→	4	TA6			7	GND			RA6	37	→	GB2
	GB3	→	6	TB0	TB-	46	8	DB1-	→	11	RB-	38	→	GB3
	GB4	→	7	TB1	TB+	45	9	DB1+	→	12	RB+	39	→	GB4
	GB5	→	11	TB2			10	GND			RB2	43	→	GB5
	GB6	→	12	TB3	TC-	42	11	DB2-	→	15	RC-	45	→	GB6
	GB7	→	14	TB4	TC+	41	12	DB2+	→	16	RC+	46	→	GB7
	BB2	→	15	TB5			13	GND			RB5	47	→	BB2
	BB3	→	19	TB6	TCLK-	40	14	CKB-	→	17	RCLK-	51	→	BB3
	BB4	→	20	TC0	TCLK+	39	15	CKB+	→	18	RCLK+	53	→	BB4
	BB5	→	22	TC1			16	GND			RB6	54	→	BB5
	BB6	→	23	TC2	TD-	38	17	DB3-	→	19	RD-	55	→	BB6
	BB7	→	24	TC3	TD+	37	18	DB3+	→	20	RD+	1	→	BB7
	RSVD	→	27	TC4			19	GND			RC4	3	→	RSVD
Note1	RSVD	→	28	TC5			20	Reserved			RC5	5	→	RSVD
	RSVD	→	30	TC6			21	Reserved			RC6	6	→	RSVD
	RB0	→	50	TD0			22	Reserved			RD0	7	→	RB0
	RB1	→	2	TD1			23	Reserved			RD1	34	→	RB1
	GB0	→	8	TD2			24	GND			RD2	41	→	GB0
	GB1	→	10	TD3			25	GND			RD3	42	→	GB1
	BB0	→	16	TD4			26	GND			RD4	49	→	BB0
	BB1	→	18	TD5			27	N.C.			RD5	50	→	BB1
Note1	RSVD	→	25	TD6			28	VDD:12V			RD6	2	→	RSVD
	CLK	→	31	CLKIN			29	VDD:12V			CLKOUT	26	→	CLKB
							30	VDD:12V						

Use 100Ω twist pair wires for the Cable.

Note1: RSVD must connect to system GND.

13. DISPLAY COLORS vs. INPUT DATA SIGNALS

Display colors		Data signal (0: Low level, 1: High level)																									
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note1: Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 16,777,216 (256×256×256) colors.

14. INPUT SIGNAL TIMINGS

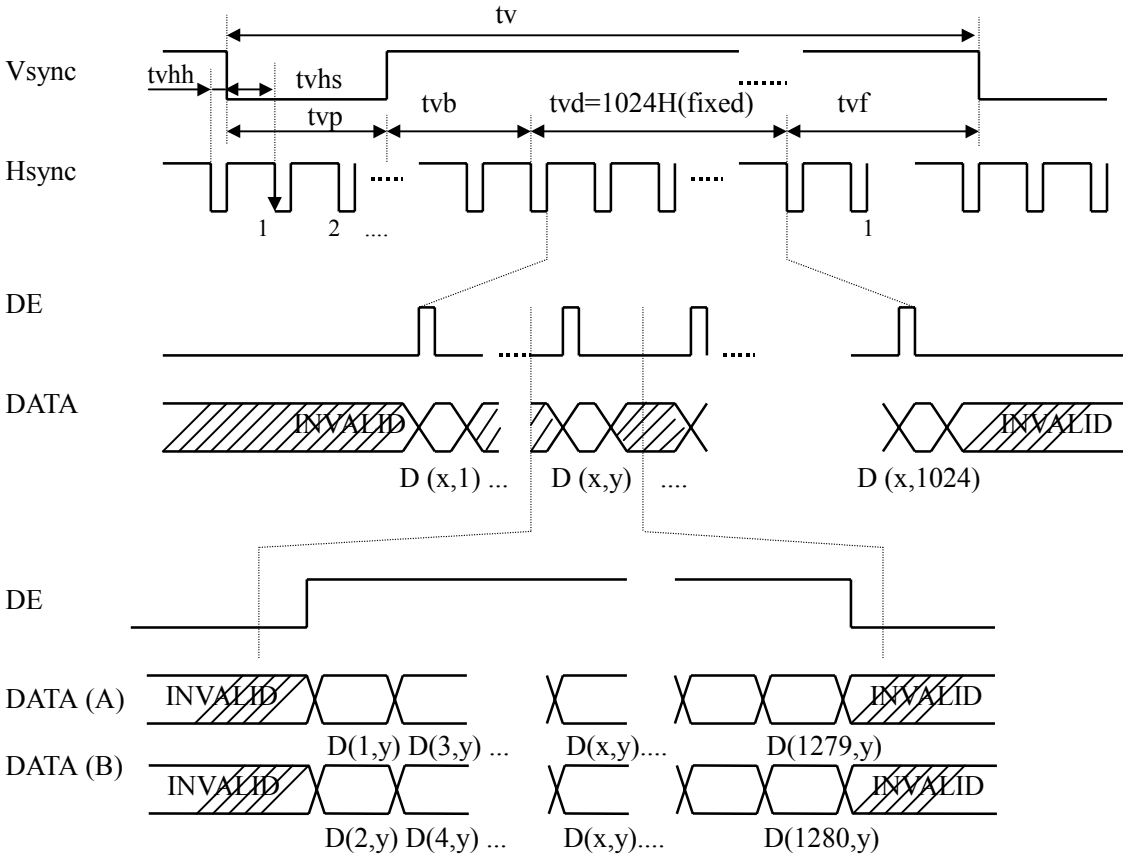
(1) Input signal specifications for LCD controller

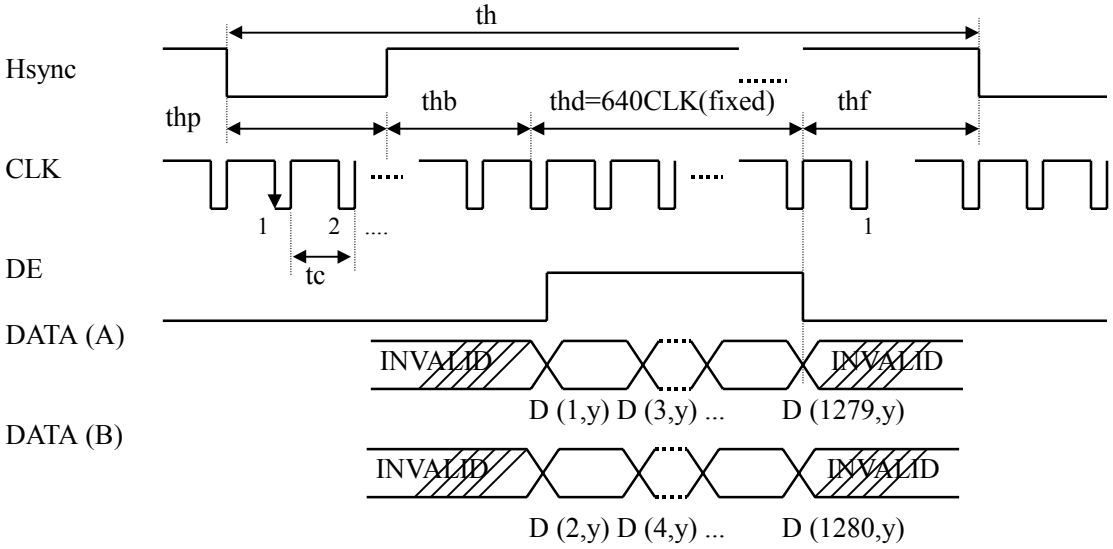
	Parameters		Symbols	Min.	Typ.	Max.	Units	Remarks
CLK	Frequency	Vf=60Hz	1/ tc	51.5 —	54.0 18.52	56.5 —	MHz ns	—
	Duty		tc / tcl	Note 1			—	—
	Rise, fall		tcrf				ns	—
Hsync	Period	Vf=60Hz	th	12.3 750	15.630 844	— —	μs CLK	Typ=64.0kHz Note 2
	Display period		thd	—	640	—	CLK	—
	Front-porch		thf	—	—	—	CLK	—
	Pulse width	Vf=60Hz	thp *	—	56	—	CLK	—
	Back-porch		thb *	—	124	—	CLK	—
	* thp + thb			110	—	—	CLK	—
Vsync	Period	Vf=60Hz	tv	— 1028	16.661 1066	17.47 —	ms H	Typ=60.0Hz
	Display period		tvd	—	1024	—	H	—
	Front-porch		tvf *	—	1	—	H	—
	Pulse width		tvp *	—	3	—	H	—
	Back-porch		tvb *	—	38	—	H	—
	* tvf + tvp +tvb			4	—	—	H	—
	Vsync-Hsync timing		tvhs	1	—	—	CLK	for Hsync
	Hsync-Vsync timing		tvhh	1	—	—	CLK	for Hsync
DATA	DATA-CLK (Set up)		ts	Note 1			ns	—
	CLK-DATA (Hold)		th				ns	—
	Rise, fall		trf				ns	—

Note1: These values are in the timing regulation of THC63LVDF83A (THine).
The product equivalent to THC63LVDF83A (THine) is recommended to the input of LVDS transmitter.

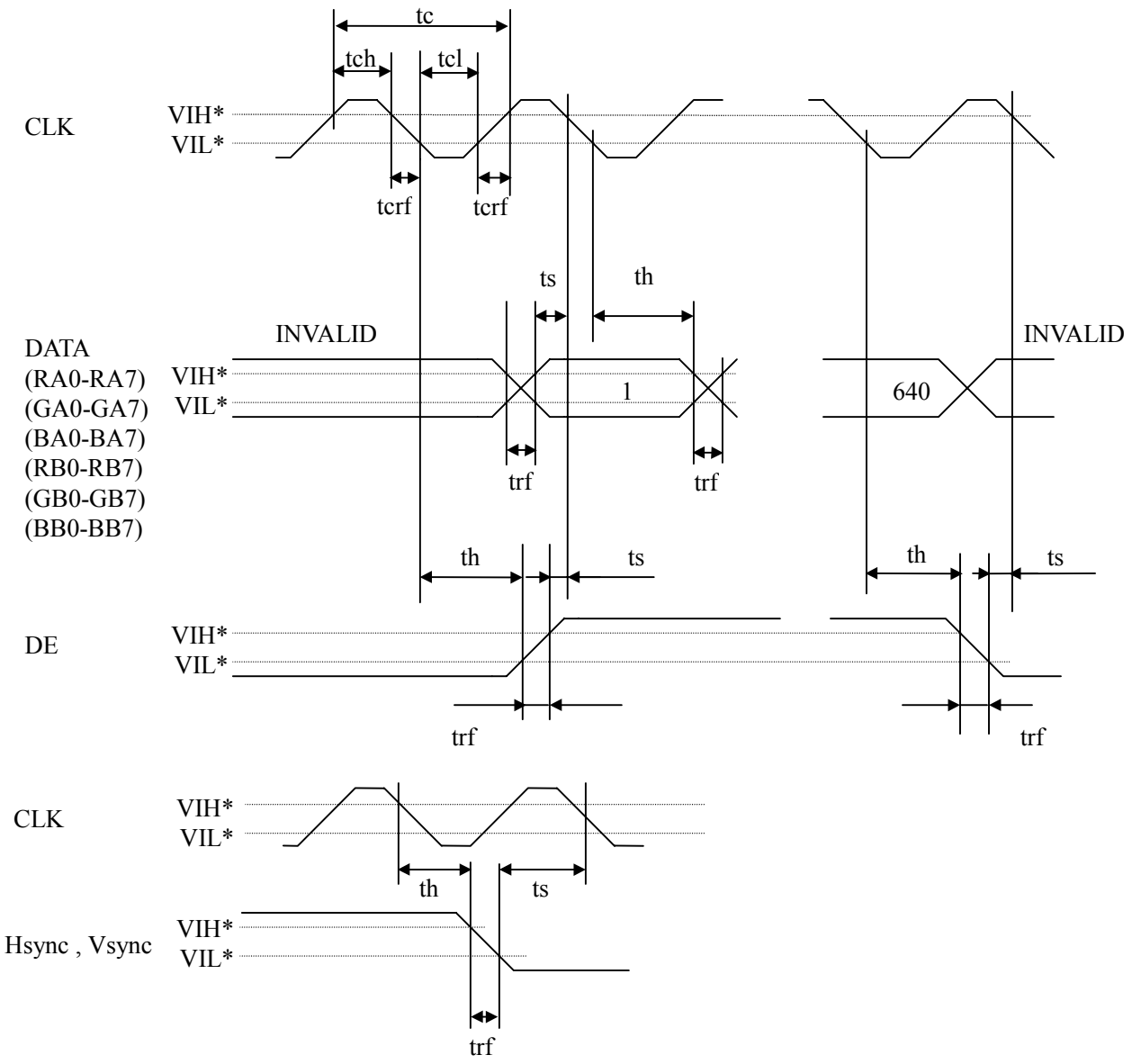
Note2: Minimum value of "th" must be satisfied with both time and CLK number.

(2) Input signals timing chart for LCD





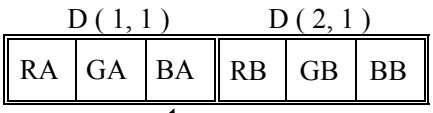
Note1: DATA (A): RA0-RA7, GA0-GA7, BA0-BA7
DATA (B): RB0-RBA7, GB0-GB7, BB0-BB7



* VIH, VIL: Refer to LVDS transmitter specifications.

(3) Display positions of input data

Odd Pixel: RA= R DATA Even Pixel : RB=R DATA
Odd Pixel: GA= G DATA Even Pixel : GB=G DATA
Odd Pixel: BA= B DATA Even Pixel : BB=B DATA



D(1, 1)	D(2,1)	•••	D(1280,1)
D(1,2)	D(2, 2)	•••	D(1280,2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,1024)	D(2,1024)	•••	D(1280,1024)

15. OPTICAL CHARACTERISTICS

(Ta= 25 ℃, VDD= 12V, VDDB=12V, Note1)

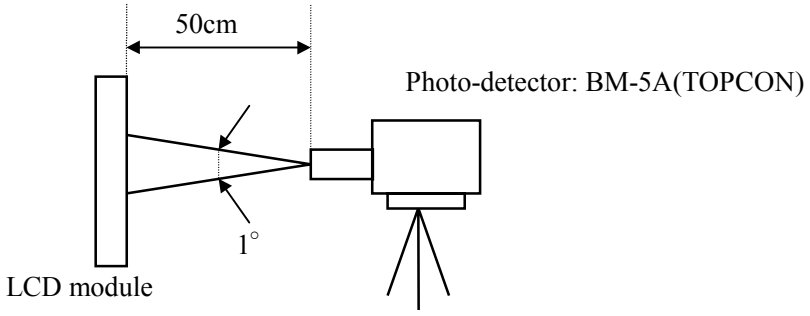
Parameters	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks
Contrast ratio	CR	Note 3	200	350	-	-	Note 2
Luminance	Lumax	Note 3	150	200	-	cd/m^2	-
Luminance uniformity	-	Max. / Min., Note 3	-	1.1	1.3	-	Note 6

Reference data

(Ta= 25 ℃, VDD= 12V, VDDB=12V, Note1)

Parameters		Symbols	Conditions		Min.	Typ.	Max.	Units	Remarks
Contrast ratio		CR	Best contrast angle θ x= ±0°, θ y= -10°		-	300	-	-	Note 2
Color gamut		C	To NTSC		50	60	-	%	Note 3
Chromaticity Coordinates		W	White (x, y)		-	T.B.D.	-	-	-
		R	Red (x, y)		-	T.B.D.	-	-	
		G	Green (x, y)		-	T.B.D.	-	-	
		B	Blue (x, y)		-	T.B.D.	-	-	
Viewing Angle Range (CR>10)	Horizontal	θ x+	CR>10, θ y = ±0°		70	85	-	deg.	Note 4
		θ x-			70	85	-	deg.	
	Vertical	θ y+	CR>10, θ x = ±0°		70	85	-	deg.	
		θ y-			70	85	-	deg.	
Viewing Angle Range (CR>5)	Horizontal	θ x+	CR>5, θ y = ±0°		-	85	-	deg.	
		θ x-			-	85	-	deg.	
	Vertical	θ y+	CR>5, θ x = ±0°		-	85	-	deg.	
		θ y-			-	85	-	deg.	
Response time (Module front surface temperature=T.B.D.)		Ton	White to black	100%→10%	-	T.B.D.	T.B.D.	ms	Note 5
				90%→10%	-	T.B.D.	-		
		Toff	Black to white	0%→90%	-	T.B.D.	T.B.D.		
				10%→90%	-	T.B.D.	-		
		Ton + Toff			-	40	-		
Luminannce control range		-	Maximum luminannce:100%		-	T.B.D.	-	-	%

Note1: Optical characteristics are measured after 20 minutes from the module works, with all pixels in " white ".Typical value is measured after luminance saturation. The luminance is measured in dark room.

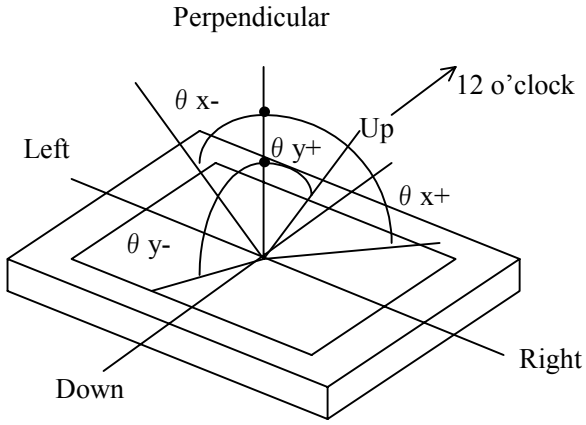


Note2: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

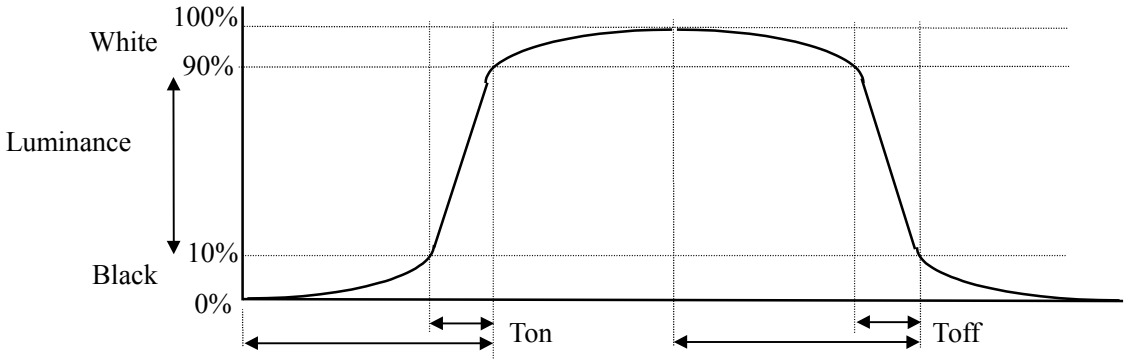
Note3: Viewing angle is θ x = ±0°, θ y = ±0° and at center.

Note4: Definitions of viewing angle are as follows



Note5: Definitions of response time is as follows.

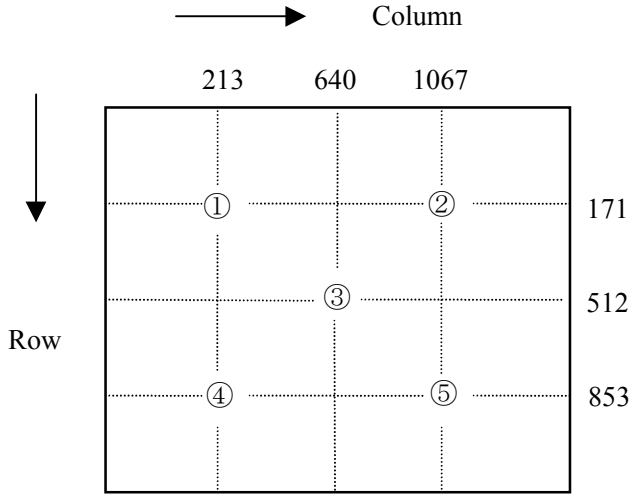
Photo-detector output signal is measured when the luminance changes "white" to "black" or "black" to "white".



Note6: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

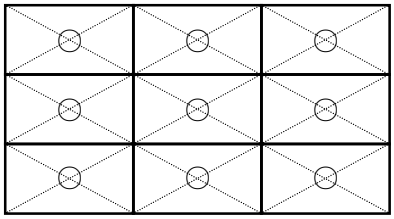
The luminance is measured at near the five points shown below.



16. RELIABILITY TEST

Test items		Test conditions	Judgment
High temperature / humidity operation		60±2℃, RH= 60% 240 hours, Display data is black.	Note 1
Heat cycle (operation)		① 0℃±3℃・・・1 hour 55℃±3℃・・・1 hour ② 50 cycles , 4 hours / cycle ③ Display data is black.	Note 1
Thermal shock (non-operation)		① -20℃±3℃・・・30 minutes 60℃±3℃・・・30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	Note 1
Vibration (non-operation)		① 5-100Hz, 11.76m/s^2 1 minute / cycle, X,Y,Z direction ② 10 times each direction	Note 1 Note 2
Mechanical shock (non-operation)		① 294 m/s^2 , 11ms X,Y,Z direction ② 3 times each direction	Note 1 Note 2
ESD (operation)		150pF, 150Ω, ±10kV 9 places on a panel Note 3 10 times each place at one-second intervals	Note 1
Dust (operation)		15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	Note 1
Reduced pressure	operation	T.B.D. kPa 0℃±T.B.D.・・・24 hours 55℃±T.B.D.・・・24 hours	Note 1
	non-operation	T.B.D. kPa -20℃±T.B.D.・・・24 hours -60℃±T.B.D.・・・24 hours	

Note1: Display function is checked by the same condition as LCD module out-going inspection.
Note2: Physical damage
Note3: Discharge points are shown as follows.



17. ESTIMATED LIFE-TIME OF THE BARE LAMP

Note 1,3

	Bare lamp
Conditions	Luminance Maximum Room temp.（25±2℃）, Continuous operation
Expected value (MTTF)	50,000h (IL=6.0mArms) Note 2
Criteria	Half value luminance (compared with initial value.)

Note1: The life-time is estimated value (reference only).
Note2: This estimated value is based on the test results with a bare lamp operation.
The MTTF for the module may be different from these values, because of the influence of ambient and clamshell conditions.
Note3: The life-time becomes short if the module is operated under the low/high temp. environment.

18. GENERAL CAUTIONS

Because the following statements are very important, please be sure you understand their contents completely.

⚠ **CAUTION**	This figure is a warning that you will get hurt and/or the module will be damaged if you make a mistake in operation.

	This figure is a warning that you will get an electric shock if you make a mistake in operation.
	This figure is a warning that you will get hurt if you make a mistake in operation.

⚠ CAUTIONS

Do not touch an inverter on which there is a caution label is stuck while the LCD module is in operation, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick up the pouch only, when removing the module from a carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges. Peel protection sheet out from the LCD panel surface as slowly as possible.

②  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one or more of these signals is lost, the LCD panel would be damaged.

⑧ The torque for mounting screws should never exceed 0.45 N·m.

⑨ Don't push or rub the surface of LCD module please.
If you do, the scratches or the marks like rubbing marks may be left on the surface of the module.

⑩ Do not give the stress too much on interface connectors. The module may become function deficiency by a contact defective and damages. Pay attention to handling at the time of matching connector connection and in the connection condition.

⑪ Do not put front side (display surface side) of the module on a desk or a table for a long time, because the display may become un-uniformity.

(3) Cautions regarding atmosphere

① Dew-drop atmosphere must be avoided.

② Do not store and/or operate the LCD module in a high-temperature and/or high-humidity atmosphere. Storage in an anti-static pouch and under the room temperature atmosphere is recommended.

③ This module uses cold cathode fluorescent lamps. Therefore the lifetime of lamps is shortened if the module is operated under the low temperature environment.

④ Do not operate the LCD module in high magnetic field.

(4) Cautions about the module characteristics

① Do not apply any fixed pattern data for a long time to the LCD module. It may cause image sticking. Use screen savers if the display pattern is fixed more than 30 minutes.

② This module has the lends sheet which may cause the variation of the color hue in the different viewing angles. The ununiformity may appear on the screen under the high temperature operation.

③ The light vertical stripe may be observed depending on the display pattern. This is not defects or malfunctions.

④ The noise from the inverter circuit may observed in the luminance control mode. This is not defects or malfunctions.

(5) Other cautions

① Do not disassemble and/or reassemble the LCD module.

② Do not readjust variable resistors nor switches in the module.

② When returning the module for repair, etc., please pack the module properly to avoid any damages. NEC recommends using original shipping packages.

③ In case that the scan converter is used to convert VGA signal to NTSC, it is recommended using the frame-memory type, not the line-memory.

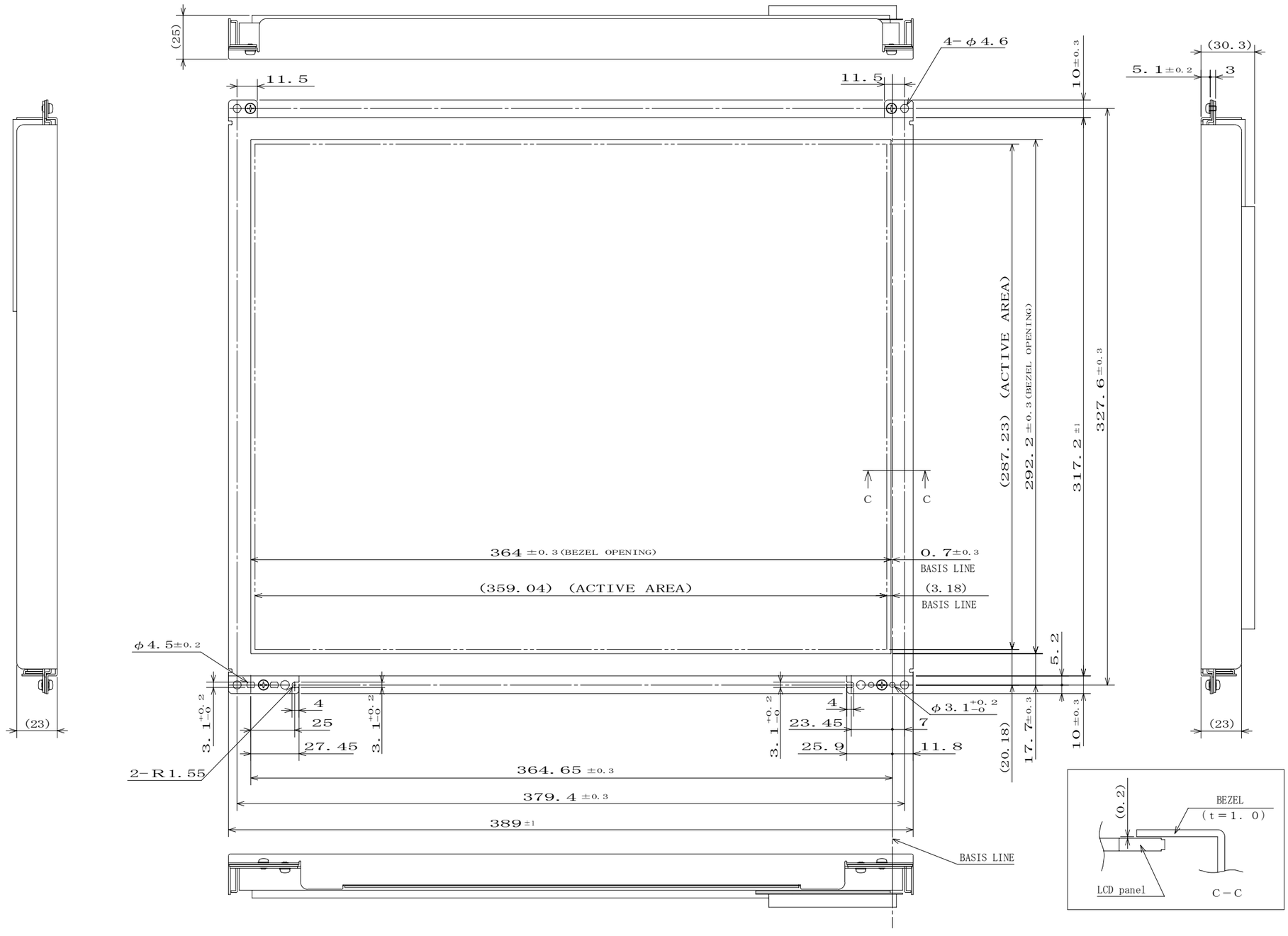
The liquid crystal display has the following specific characteristics. These are not defects or malfunctions.

The optical characteristics of this module may be affected by the ambient temperature.
This module has cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will be changed by the progress in time.

Uneven brightness and/or small spots may be observed depending on different display patterns.

19.OUTLINE DRAWINGS (Unit: mm)

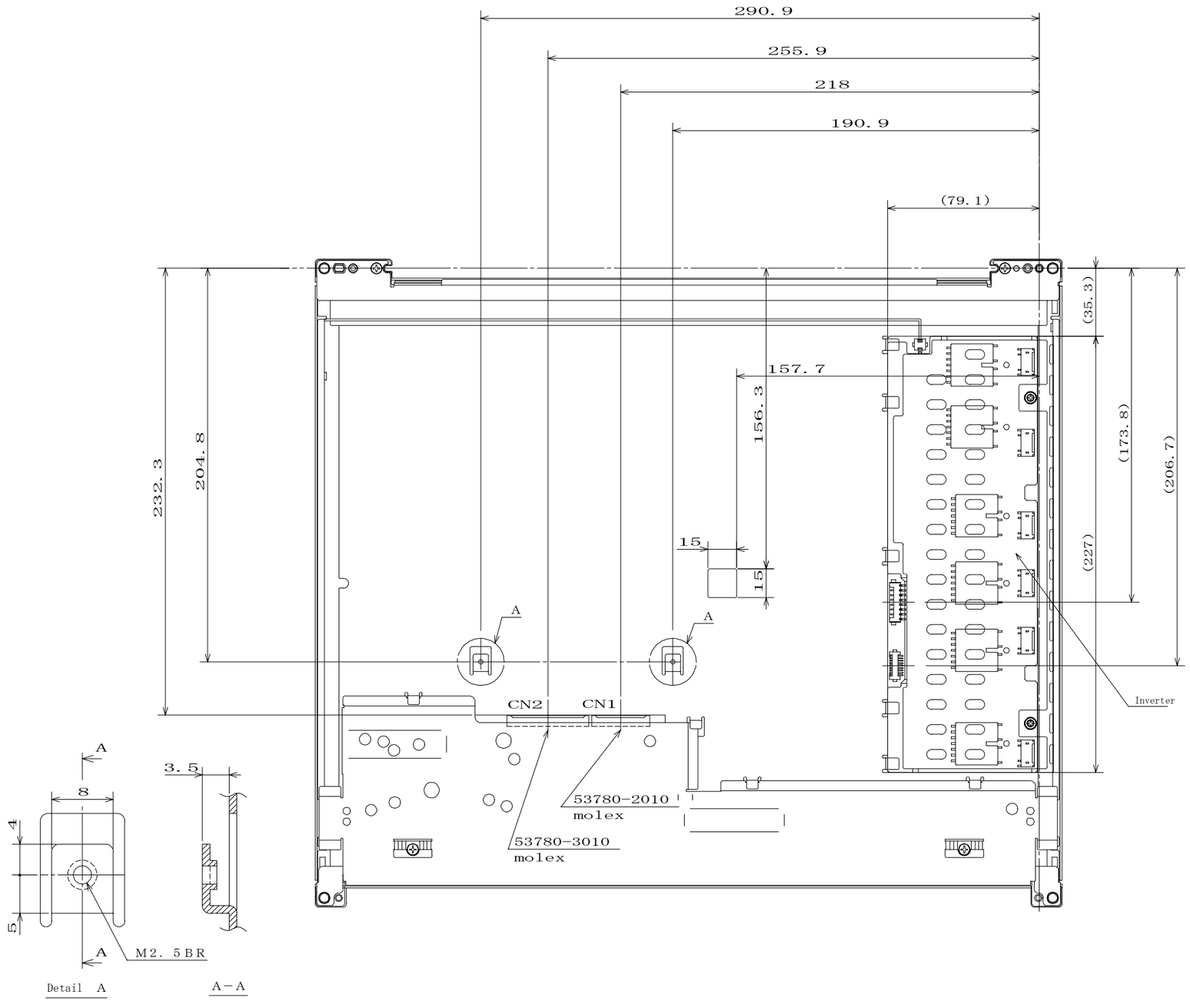
19.1.Front view



Note1: The torque for mounting screws should never exceed 0.45N·m.

Note2: Tolerances of dimensions not shown is ±0.5mm.

19.2.Rear view



Note1: The torque for mounting screws should never exceed 0.45N·m.

Note2: Tolerances of dimensions not shown is ±0.5mm.

Revision History

Rev.	Prepared Date	Revision contents	Approved	Checked	Prepared	Issued Date
1	Sep. 29, 2000	DOD-H-8109 (abstract)	A. Okamoto	T. Kusanagi	N. Kano	-
2	Nov. 8, 2000	DOD-H-8173	A. Okamoto	T. Kusanagi	N. Kano	-