NEC

TFT COLOR LCD MODULE

Type: NL128102AC31-01B
51cm (20.1 Type), SXGA

DATA SHEET

First edition

All information in this document are subject to change without prior notice.

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Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special : Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

CONTENTS

1. DESCRIPTION

NL128102AC31-01B is a TFT(thin film transistor) active matrix color liquid crystal display(LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit, a CRT interface board and a backlight. NL128102AC31-01B has a built-in backlight with an inverter.

The 51cm(20.1 Type) diagonal display area contains 1280 × 1024 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has wide viewing angle and multi-scan function. Therefore, this module calls Super Fine TFT.

NL128102AC31-01B is a model which mounted the CRT interface board on NL128102AC31-01.

2. FEATURES

- Ultra-wide viewing angle and low reflection
- CRT interface board
  - Auto recognition of input signal (Analog RGB signals, Composite synchronous signal and Sync. On Green signal)
  - Digital control: e.g., Brightness, Display position
  - Corresponding to DDC1 and DDC2B
  - Corresponding to VESA and DPMS
  - Free supply voltage sequence
- Multi-scan function: e.g., SXGA, XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated direct type backlight (Ten cold cathode fluorescent lamps, Inverter)
- Lamp unit replaceable (Unit No.: 201LHS01)

VESA:	Video Electronics Standards Association
DPMS:	Display Power Management Signaling
DDC1:	Display Data Channel 1
DDC2B:	Display Data Channel 2B

3. APPLICATIONS

- Desk-top PC, Engineering work station
- Display terminals for control system
- Monitors for process controller

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

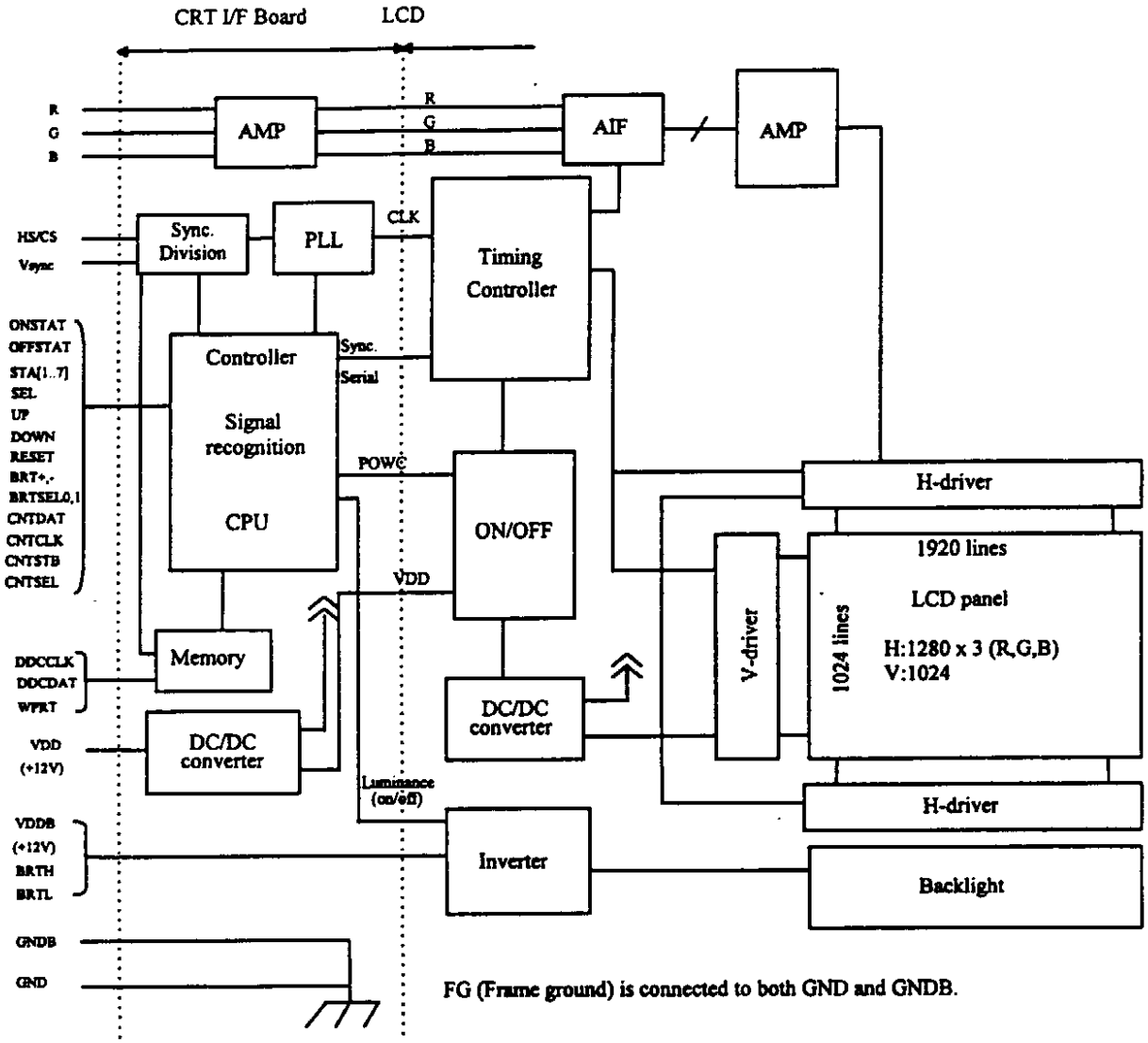
RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.36(H) x 19.488(V)mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1280 x 1024
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.312(H) x 0.312(V)mm
Module size	470.0(H) x 382.0(V) x 45.0 typ.(D)mm
Weight	3560g(typ.)
Contrast ratio	220:1(typ.)
Viewing angle (more than the contrast ratio of 10:1)	
· Horizontal:	80° (typ. , left side, right side)
· Vertical:	80° (typ. , up side., down side)
Color gamut	40%(min. At center, To NTSC)
Response time	58 ms(typ.), " black " to " white "
Luminance	150cd/m^2(typ.)
Signal system	Analog RGB signals, Synchronous signals(HS, VS, CS), Digital data
Supply voltage	12V, 12V (Logic/LCD driving, Backlight)
Backlight	Ten cold cathode fluorescent lamps with an inverter
Power consumption	55.8W(typ.)

6. BLOCK DIAGRAM



FG (Frame ground) is connected to both GND and GNDB.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Item	Contents	Unit
Module size	470.0±0.5 (H) x 382.0±0.5 (V) x 48.0 (max.)(D)	mm
Display area	399.36 (H) x 319.488 (V)	mm
Number of dots	1280 x 3 (H) x 1024 (V)	dots
Pixel pitch	0.312 (H) x 0.312 (V)	mm
Dot pitch	0.104 (H) x 0.312 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	full color	color
Weight	3600 (max.)	g

7.2 ABSOLUTE MAXMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VDD	-0.3 to +14	V	Ta=25℃
	VDDB	0 to +14	V	
Logic input voltage	Vin1	-0.3 to +5.5	V	Ta=25℃
R,G, B input voltage	Vin2	-4.0 to +4.0	V	VDD=12V
Storage temp.	Tst	-20 to +60	℃	–
Operating temp.	Top	0 to +50	℃	Module surface note 1
Humidity (no condensation)	≦95% relative humidity			Ta≦40 ℃
	≦85% relative humidity			40<Ta≦50 ℃
	Absolute humidity shall not exceed Ta=50℃, 85% relative humidity level.			Ta>50 ℃

note 1: Measured at the LCD panel

7.3 ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving, Backlight

(Ta=25℃)

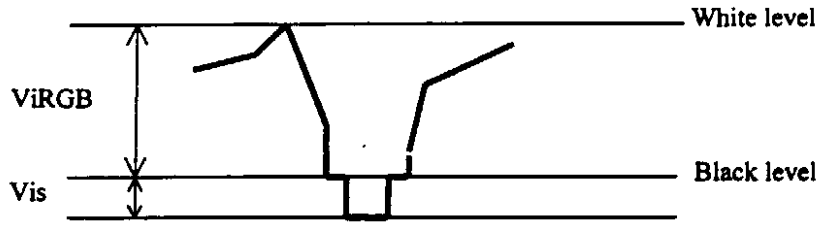
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	11.4	12.0	12.6	V	for Logic and LCD driving
	VDDB	11.4	12.0	12.6	V	for backlight
Logic input " L " voltage	ViL	0	–	0.8	V	for HS/CS, Vsync, UP, DOWN, SEL, RESET, BRTSEL0,1, BRT+, BRT-, DDCCLK,DDCDAT, WPRT
Logic input " H " voltage	ViH	2.2	–	5.25	V	
Logic output " L " voltage	VoL	–	–	0.4	V	CNTCLK, CNTDAT, CNTSTB, DDCDAT
Logic output " H " voltage	VoH	2.4	–	–	V	
Logic output " L " current 1	IoL1	-1	–	–	mA	CNTCLK, CNTDAT, CNTSTB
Logic output " H " current 1	IoH1	–	–	1	mA	
Logic output " H " current 2	IoH2	–	–	50	mA	STA1 to 8, ONSTAT, OFFSTAT(at VoH=4.45V)
Logic output " L " current 3	IoL3	–	–	3	mA	DDCDAT
Logic output " H " current 3	IoH3	-1	–	–	mA	
Supply current (Dot- checkered pattern)	IDD	–	1050	2400	mA	VDD=12.0V
		–	200	300	mA	Power save mode
	IDDB	–	3600	4900	mA	VDDB=12.0V (Max. luminance)
		–	1	10	mA	Power save mode

note 1:

(2) Video signal (R, G, B) input

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	ViRGB	0 (black)	0.7	0.8	Vp-p	–
DC input level (black)	VidcRGB	-0.5	–	+2.5	V	–
Sync. level	Vis	0.2	–	0.6	Vp-p	G terminal in Sync. On Green



7.4 POWER SUPPLY

(1) Power supply sequence

This module does not have the power supply sequence.

The supply voltage should not be applied while the control signals (SEL, UP ,DOWN, RESET, BRT+ and BRT−) are connected to GND. Otherwise, the module may cause malfunction.

(2) Ripple of supply voltage

	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable range	≦ 100 mVp-p	≦ 200 mVp-p

note 1: The acceptable range of ripple voltage includes spike noises.

7.5 INTERFACE PIN CONNECTIONS

(1) CN101

Part No. : MRF03-6R-SMT

Adaptable socket : MRF03-2 × 6P-1.27(For cable type) or MRF03-6PR-SMT(For board to board type)

Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Coaxial cable : UL20537PF75VLAS

Supplier : HITACHI CO., LTD.

note 1: A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	HS/CS
3	R	6▼	N.C.

Figure from socket view

(2) CN102

Part No. : IL-Z-15PL1-SMTY

Adaptable socket : IL-Z-15S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	SEL	9	GND
2	UP	10	BRT+
3	DOWN	11	BRT−
4	RESET	12	GND
5	GND	13	BRTSEL0
6	CNTCLK	14	BRTSEL1
7	CNTDAT	15▼	GND
8	CNTSTB		

Figure from socket view

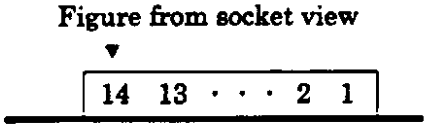
(3) CN103

Part No. : IL-Z-14PL1-SMTY
Adaptable socket : IL-Z-14S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GND	8	STA4
2	ONSTAT	9	GND
3	OFFSTAT	10	STA5
4	GND	11	STA6
5	STA1	12	STA7
6	STA2	13	N.C.
7	STA3	14 ▼	GND

note 1: N.C. (No connection) should be open.

Figure from socket view



(4) CN104

Part No. : IL-Z-8PL1-SMTY
Adaptable socket : IL-Z-8S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	5	GND
2	VDD	6	GND
3	VDD	7	GND
4	VDD	8▼	GND

note 1: N.C. (No connection) should be open.

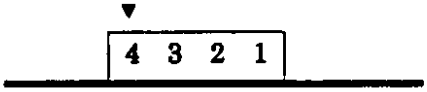
Figure from socket view

(5) CN105

Part No. : IL-Z-4PL-SMTY
Adaptable socket : IL-Z-4S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	DDCCLK	3	WPRT
2	DDCDAT	4▼	GND

Figure from socket view



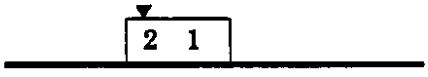
(6) CN107

Part No. : IL-Z-2PL-SMTY
Adaptable socket : IL-Z-2S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	BRTH	2▼	BRTL

note 1: When do not you use the pins, these should be open.

Figure from socket view



(7) CN201

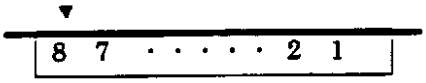
Part No. : DF3-8P-2H

Adaptable socket : DF3-8S-2C

Supplier : HIROSE ELECTRIC CO,. LTD.

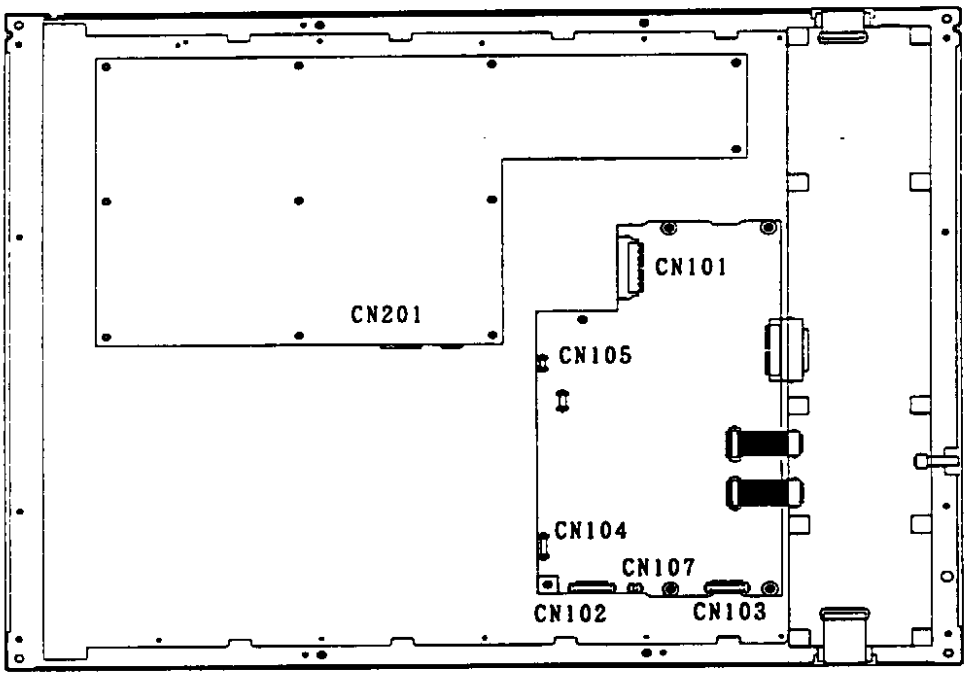
Pin No.	Symbol	Pin No.	Symbol
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8	VDDB

Figure from socket view



note 1: The cable connected the CN201 must have a capable of more than 2 A.

Rear view

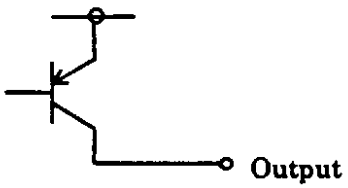
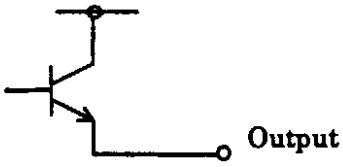


7.6 PIN FUNCTIONS

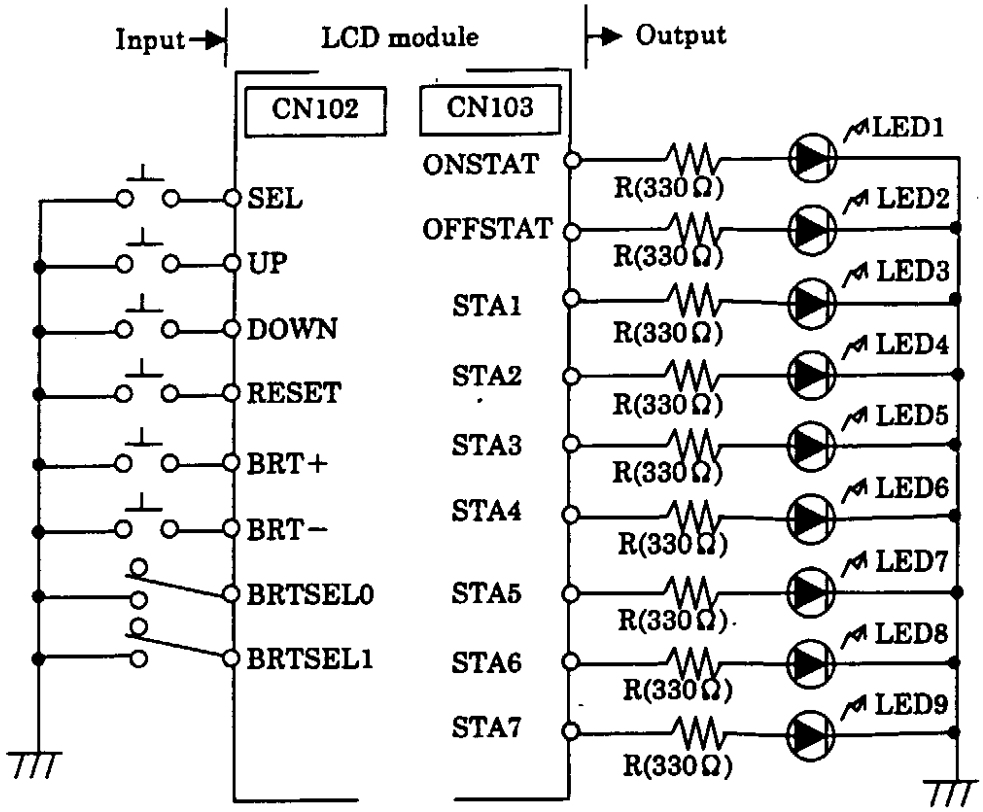
Symbol	I/O	Logic	Description
HS/CS	Input	Positive Negative	Horizontal synchronous signal input or composite synchronous signal input (TTL level), Positive/Negative auto recognition
Vsync	Input	Positive Negative	Vertical synohronous signal input (TTL level) Positive/Negative auto recognition
R	Input	–	Red video signal input (0.7Vp-p, 75Ω)
G	Input	–	Green video signal input (0.7Vp-p, 75Ω) Sync. On Green input (1.0Vp-p, 75Ω)
B	Input	–	Blue video signal input (0.7Vp-p, 75Ω)
SEL	Input	Negative	Control function select signal (TTL level) Function: Luminance, Horizontal synchronous total, CLK delay, Vertical position, Horizontal position, Reset SEL is pulled up into the module. "H" or "open": SEL off, "L": SEL on Detail of the functions are mentioned in **CONTROL FUNCTIONS.**
UP	Input	Negative	Control signal (TTL level) The signal increases the function value. UP is pulled up into the module. "H" or "open": UP off, "L": UP on
DOWN	Input	Negative	Control signal (TTL level) The signal decreases the function value. DOWN is pulled up into the module. "H" or "open": DOWN off, "L": DOWN on
RESET	Input	Negative	Control signal (TTL level) The signal initializes the selected function. RESET is pulled up into the module. "H" or "open": RESET off, "L": RESET on
BRT+	Input	Negative	Control signal (TTL level) The signal increases the luminance value. BRT+ is pulled up into the module. "H" or "open": BRT+ off, "L": BRT+ on
BRT–	Input	Negative	Control signal (TTL level) The signal decreases the luminance value. BRT– is pulled up into the module. "H" or "open": BRT- off, "L": BER- on
BRTSEL0 BRTSEL1	Input	Negative	Luminance control select signal (TTL level) The signals determines how to control the luminance. Detail of the functions are mentioned in **CONTROL FUNCTIONS.**
CNTCLK	Output	Positive	CLK for display control (TTL level) Detail of CNTCLK is mentioned in **STATUS READ FUNCTIONS.**
CNTDAT	Output	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **STATUS READ FUNCTIONS.**
CNTSTB	Output	Positive	Latch pulse for display control (TTL level) Detail of CNTSTB is mentioned in **STATUS READ FUNCTIONS.**
ONSTAT	Output	Positive	Power status signal "H": Normal operation, "L": Other status
OFFSTAT	Output	Positive	Power status signal "H": Power saving, "L": Other status
STA1	Output	Positive	Indicator for luminance control "H": Luminance select, "L": Other status
STA2	Output	Positive	Indicator for horizontal total count "H": Horizontal total count select, "L": Other status

Symbol	I/O	Logic	Description
STA3	Output	Positive	Indicator for CLK delay "H": CLK delay select, "L": Other status
STA4	Output	Positive	Indicator for vertical position "H": Vertical position select, "L": Other status
STA5	Output	Positive	Indicator for horizontal position "H": Horizontal position select, "L": Other status
STA6	Output	Positive	Indicator for initialization "H": Reset select, "L": Other status
STA7	Output	Positive	This pin should be opened.
DDCCLK	Input	Positive	CLK for DDC1 and DDC2B
DDCDAT	Input /output	Positive	Data for DDC1 and DDC2B Read/write
WPRT	Input	Positive	Select signal for DDC1 and DDC2B "H" or "Open": Reading mode, "L": Writing mode
BRTH BRTL	Input	–	Luminance control signal with variable resistor (TTL level) Detail of the control is mentioned in **CONTROL FUNCTIONS.**
VDD	–	–	Power supply for Logic and LCD driving +12V (±5%)
VDDB	–	–	Power supply for backlight. +12V (±5%)
GND	–	–	Signal ground for I/F board, Logic and LCD driving (Connect to a system ground). GND is connected to Flame(FG).
GNDB	–	–	Ground for backlight. GNDB is connected to Flame(FG).

[Equivalent circuit]

Symbol	I/O	Equivalent circuit
ONSTAT	Output	
OFFSTAT	Output	
STA1	Output	
STA2	Output	
STA3	Output	
STA4	Output	
STA5	Output	
STA6	Output	
STA7	Output	Product: Rohm DTC143ZUA or equivalent

Recommendation circuit diagram



7.7 INPUT SYNCHRONOUS SIGNAL

This module can recognize the synchronous signals automatically as follows.

Auto recognition mode	Synchronous signal			STAT signal	
	HS/CS	Vsync	Sync. On Green	ON-STAT	OFF-STAT
Separate synchronous signal mode (Hsync, Vsync)	Input	Input	Input or no input	H	L
Composite synchronous signal mode	Input	No input	Input or no input	H	L
Sync. On Green mode	No input	No input	Input	H	L
Power save mode	No input	No input	No input	L	H

note 1: Power save mode corresponds to VESA DPMA.

7.8 EXPANSION FUNCTION

7.8.1 EXPANSION MODE

Expansion mode is a function to expand screen. For example, SVGA signal has 800 × 600 pixels. But, if the display data can expanded to 1.6 times vertically and horizontally, SVGA screen image can be displayed fully on the screen of SXGA resolution.

This LCD module has this function mentioned in the followings.

Please adopt this mode after evaluating display quality, because the appearance in the expansion mode is happened to become bad in some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal note 1
SXGA	1280 x 1024	1	1
XGA	1024 x 768	1.25	1.25
SVGA	800 x 600	1.6	1.6
VGA	640 x 480	2.0	2.0
VGA text	720 x 400	2.5	1.7
PC9801	640 x 400	2.5	2.0
MAC	832 x 624	1.6	1.5

7.8.2 AUTO RECOGNITION DATA

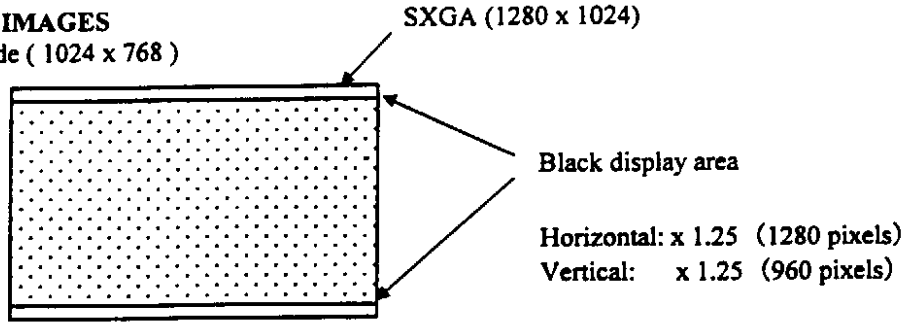
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Input signal: Horizontal: Front porch [CLK]	Pulse width [CLK]	Back porch [CLK]	Count num. [CLK]	P/N etc.	Vertical: Front porch [H]	Pulse width [H]	Back porch [H]	Count num. [H]	P/N etc.
SXGA(1280 x 1024)													
VESA	108.0	63.981	60.02	48	112	248	1688	P	1	3	38	1066	P
SUN	117.0	71.691	67.189	16	112	224	1632	*	2	8	33	1067	*
EWS4800	118.0	75.120	71.204	32	128	224	1664	*	3	3	25	1055	*
SGI	119.076	76.968	72.000	32	140	238	1690	*	3	3	39	1069	*
HP	135.0	78.125	73.005	64	192	192	1728	*	3	3	55	1085	*
VESA	135.0	79.976	75.025	16	144	248	1688	P	1	3	38	1066	P
XGA (1024 x 768)													
VESA	65	48.363	60.004	24	136	160	1344	N	3	6	29	806	N
VESA	75	56.476	70.069	24	136	144	1328	N	3	6	29	806	N
VESA	78.75	60.023	75.029	16	96	176	1312	N	1	3	28	800	N
MAC(832 × 624)													
MAC	57.283	49.725	74.5	32	64	224	1152	*	1	3	39	667	*
SVGA(800 x 600)													
VESA	36	35.156	56.25	24	72	128	1024	P	1	2	22	625	P
VESA	40	37.879	60.317	40	128	88	1056	P	1	4	23	628	P
VESA	50	48.077	72.188	56	120	44	1040	P	37	6	23	666	P
VESA	49.5	46.875	75.0	16	80	160	1056	P	1	3	21	625	P
VGA(640 x 480)													
IBM	25.175	31.469	59.94	16	96	48	800	N	10	2	33	525	N
VESA	31.5	37.861	72.809	24	40	128	832	N	9	3	28	520	N
VESA	31.5	37.5	75.0	16	64	120	840	N	1	3	16	500	N
MAC	30.24	35.0	66.667	64	64	96	864	*	3	3	39	525	*
VGA-text(720 x 400)													
IBM	28.322	31.469	70.087	27	108	45	900	N	12	2	35	449	P
PC9801(640 x 400)													
PC9801	21.053	24.827	56.424	64	96	48	848	N	7	8	25	440	N

*: Sync. On Green

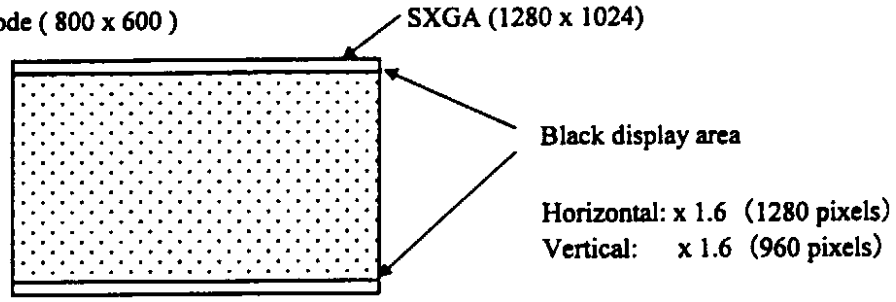
note 1: Horizontal and vertical display position should be adjusted properly.
note 2: Mistaken or other input timing cause malfunctions.
note 3: Any noises on RGB signals may cause the noise on the screen.
note 4: Even if the above timing are inputted the module correctly, any noises on Hsync and Vsync may cause un-uniformity display.
note 5: P/N is logic polarity of input synchronous signal.
"P": The logic is positive., "N": The logic is negative.

7.8.3 DISPLAY IMAGES

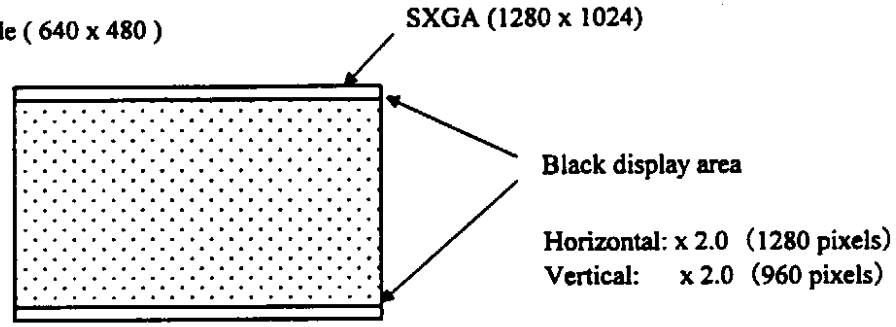
1) XGA mode (1024 x 768)



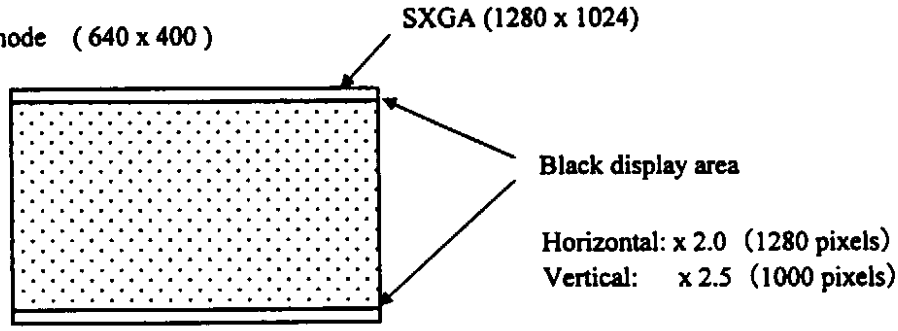
2) SVGA mode (800 x 600)



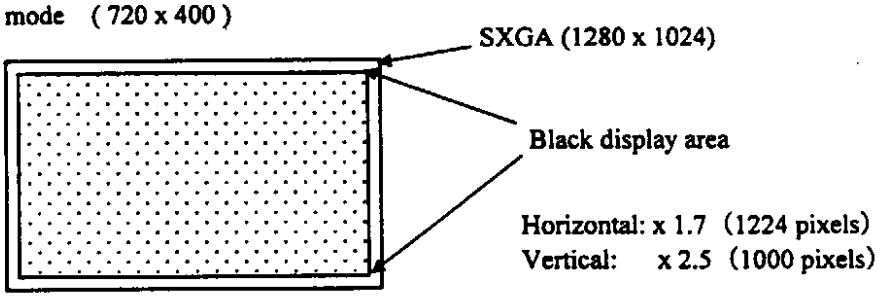
3) VGA mode (640 x 480)



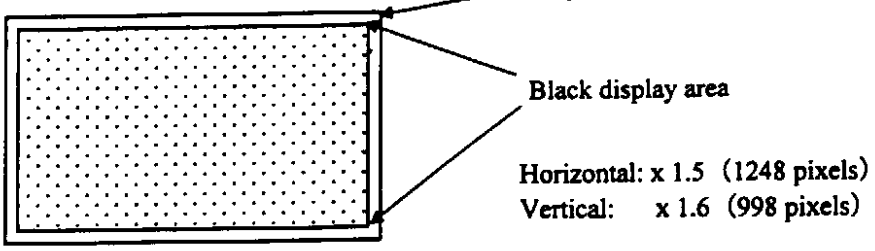
4) PC9801 mode (640 x 400)



5) VGA text mode (720 x 400)



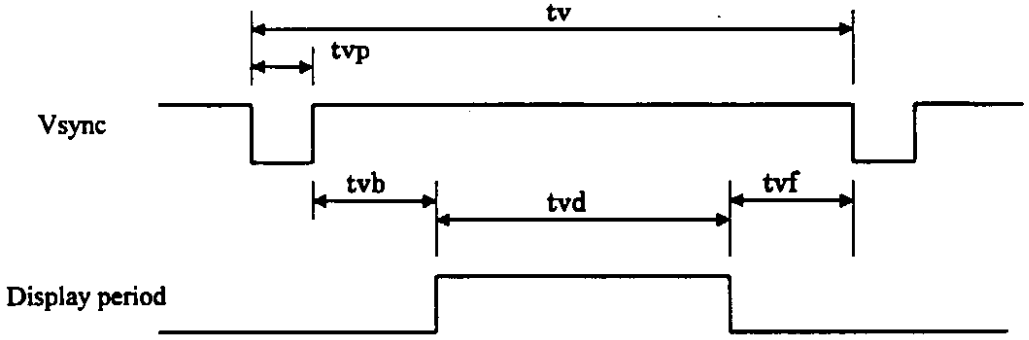
6) 832 x 624 MAC mode (832 x 624)

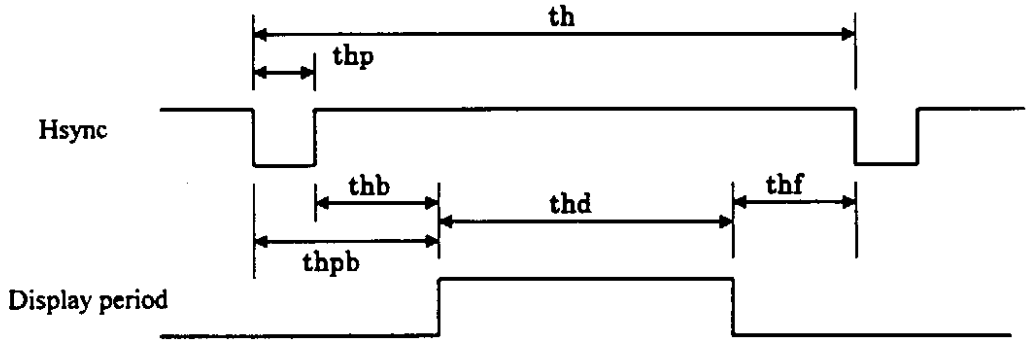


7.9 INPUT SIGNAL TIMINGS

7.9.1 SXGA MODE (STANDARD)

Name		Symbol	Min.	Typ.	Max.	Unit	Remark
Hsync	Period	th	12.3	15.630	17.0	µs	63.981kHz (typ.)
	Display	thd	–	11.852	–	µs	–
	Front-porch	thf	–	0.444	–	µs	–
	Pulse-width	thp	–	1.037	–	µs	–
	Back-porch	thb	1.0	2.296	–	µs	–
	Pulse-width +Back-porch	thpb	1.8	–	–	µs	–
	Rise / Fall	thrf	–	–	10	ns	–
Vsync	Period	tv	13.3 –	16.661 1066	18.5 –	ms H	60.020Hz (typ.)
	Display	tvd	– –	16.005 1024	– –	µs H	–
	Front-porch	tvf	– 1	0.016 1	– –	µs H	–
	Pulse-width	tvp	– 2	0.047 3	– –	µs H	–
	Back-porch	tvb	– 8	0.594 38	– –	µs H	–
	Rise / Fall	tvrf	–	–	10	ns	
Analog R,G,B		tda	5	–	–	ns	–



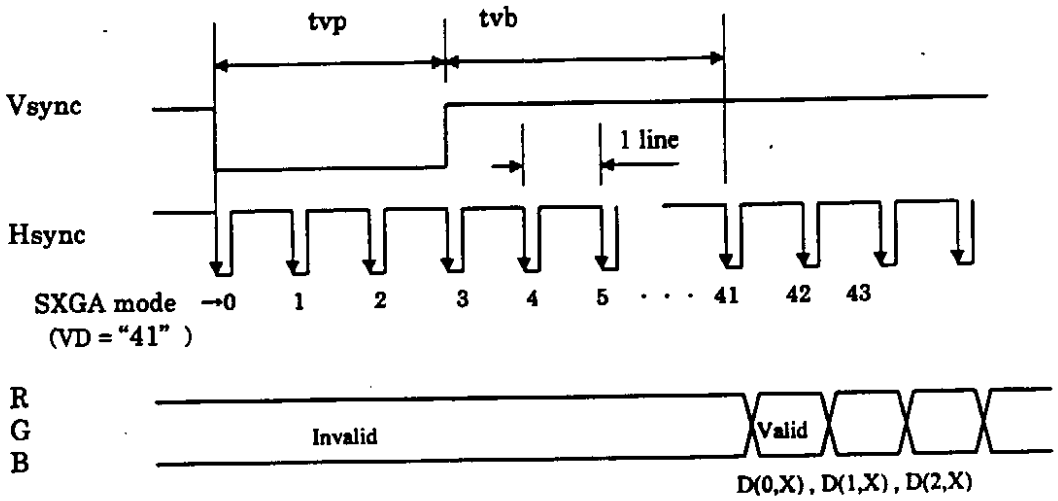


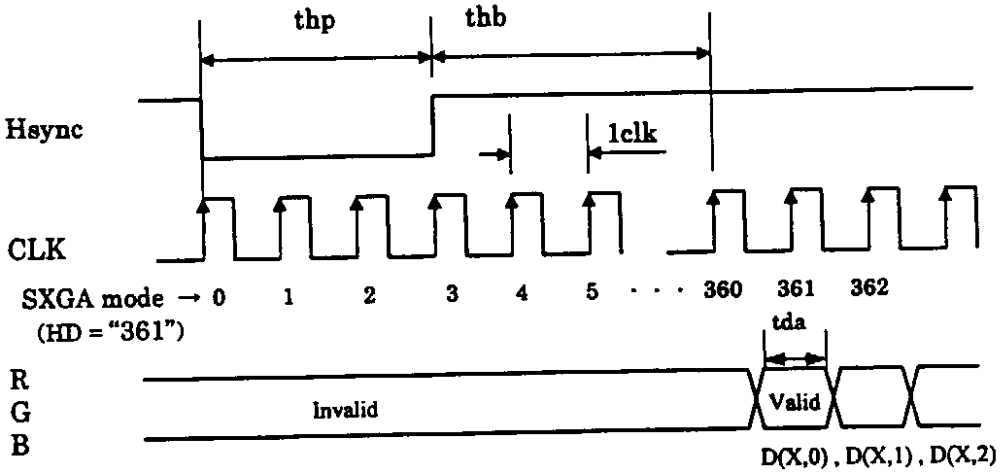
7.10 INPUT SIGNAL AND DISPLAY POSITION

7.10.1 SXGA standard timing

Pixels

D(0,0)	D(0,1)	D(0,2)	. . . . .	D(0.1279)
D(1,0)	D(1,1)	D(1,2)	. . . . .	D(1,1279)
D(2,0)	D(2,1)	D(2,2)	. . . . .	D(2,1279)
.	.	.		.
.	.	.		.
.	.	.		.
.	.	.		.
D(1023,0)	D(1023,1)	D(1023,2)	. . . . .	D(1023,1279)





note 1: The tda should be more than 4ns

7.11 CONTROL FUNCTIONS

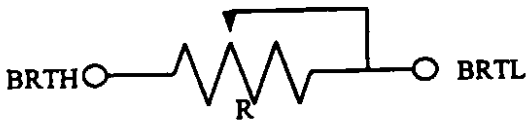
This module has the functions to adjust the following four items.

- Luminance: This function controls luminance.
- Horizontal total count:
  This function controls horizontal total count. If the display is un-uniformity, should adjust this function using the display with the vertical stripe pattern(white line and black line).
- CLK delay: CLK delay should be adjusted when the contour of character fails.
- Display position (Horizontal and vertical):
  This function controls horizontal and vertical display position. The display should be adjusted in the center of the screen.

(1) Luminance control selection

BRTSEL0	BRTSEL1	Function
L	L	Luminance can be controlled by BRT+ or BRT– signal.
L	H	Luminance(STA1) is selected by SEL signal. And luminance can be controlled by UP or DOWN signal.
H	L	Luminance can be controlled by UP or DOWN signal.
H	H	note 1

note 1: The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor correspond to the minimum of luminance.



Portion: CN107 connector
Maximum luminance (100%): R= 10 KΩ
Minimum luminance (50%): R= 0 Ω

Mating variable resistor: 10 KΩ ±5%, B curve

note 2: Luminance control selection has to be set up with power off. If the power supply is on, the display have un-uniformity.

note 3: Initial value of luminance is maximum except note 1 at the luminance control ways.

(2) Flow chart of control function

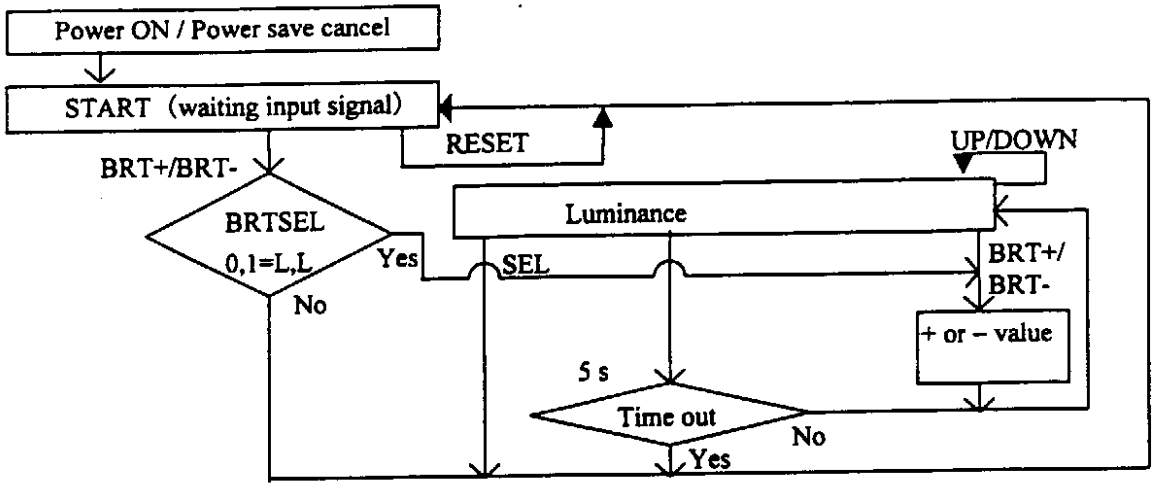
Each selected value is memorized into LCD memory after SEL signal input or time out. The memorized value are in LCD memory even if a selected mode is changed another one or power is turned off. But the selected value is not memorized if a selected mode is changed another one or power is turned off before time out (5 s).

These functions do not work in power save mode.

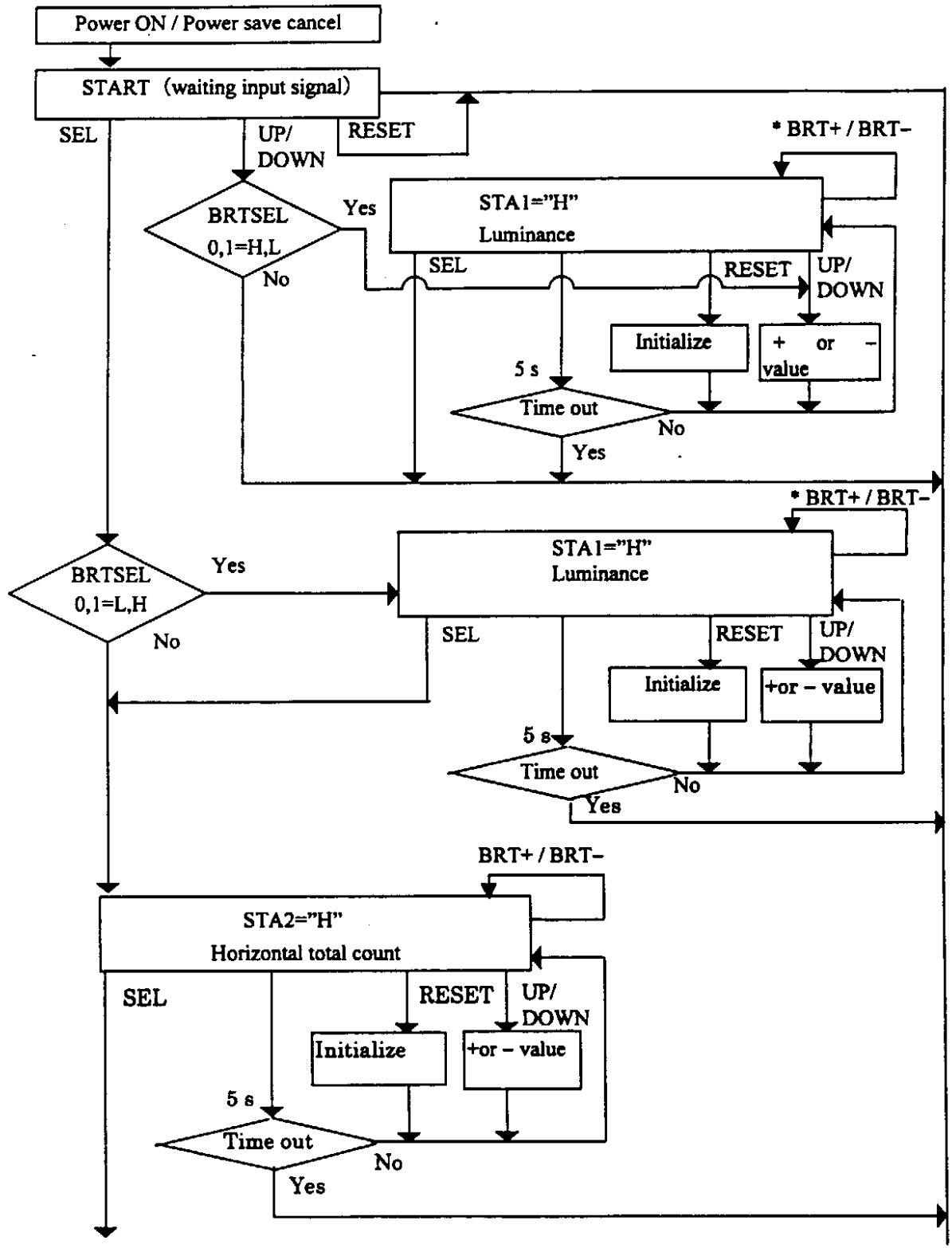
- If the input period of a signal is short, LCD memory may not accept the selected signal.
- The value of selected input signals(UP, DOWN, BRT+, BRT–) is continuously incremented if the input signal is held more than approx. one second.
- Each RESET signal initializes only the memorized input signal. RESET signal in All reset mode (STA6= "H") initializes all memorized input signal. RESET signal should be held more than approx. two seconds.
- No input signals more than five seconds shall be regarded "Time out ".
- STA signals which do not mention should set STA="L" up.

7.11.1 FLOW CHART OF CONTROL FUNCTIONS

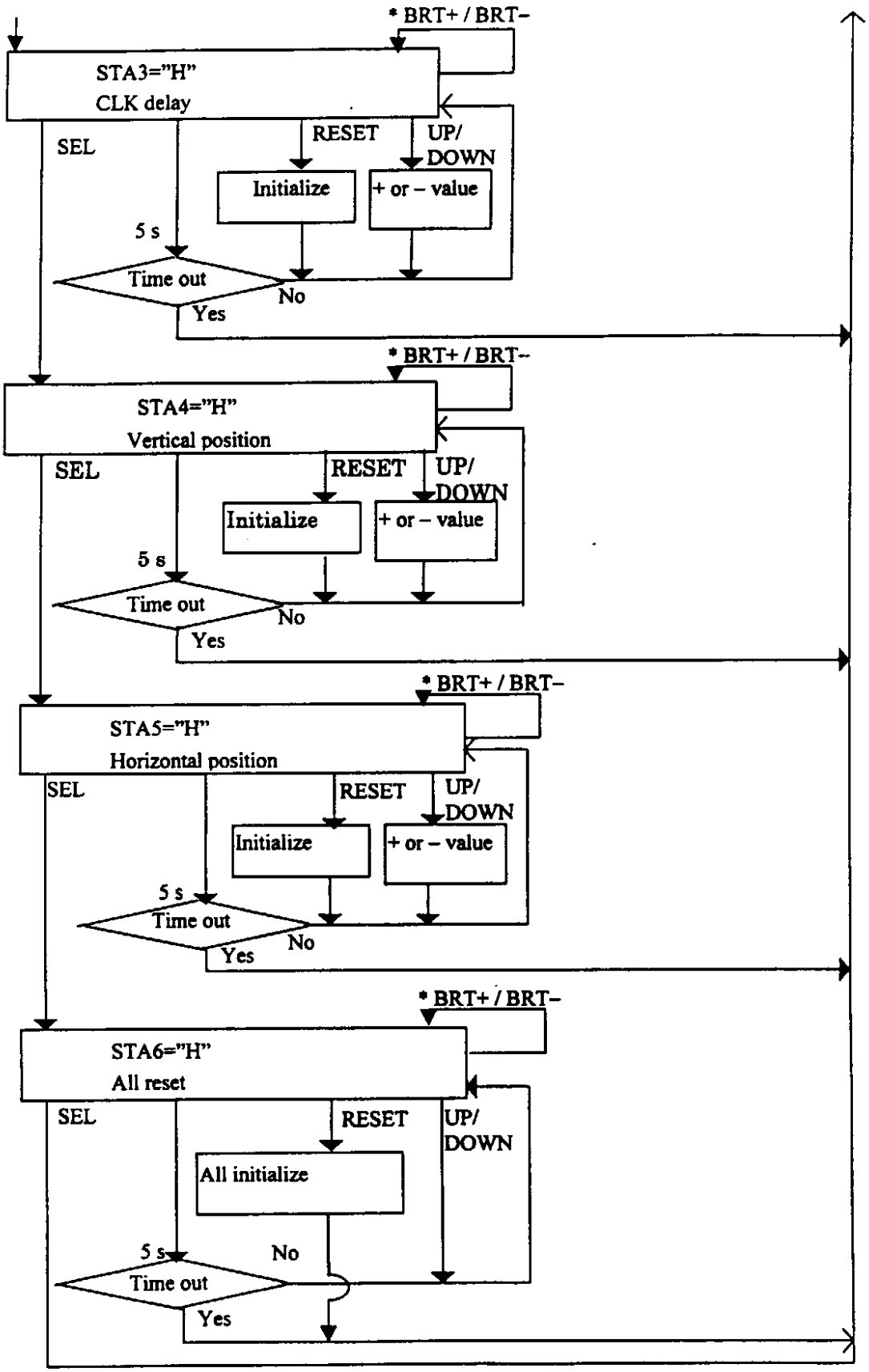
Flow chart of control way for BRT+ and BRT−



Flow chart of control way for SEL, UP, DOWN and RESET



* BRT+ / BRT-: Refer to Flow chart of control way for BRT+ and BRT-



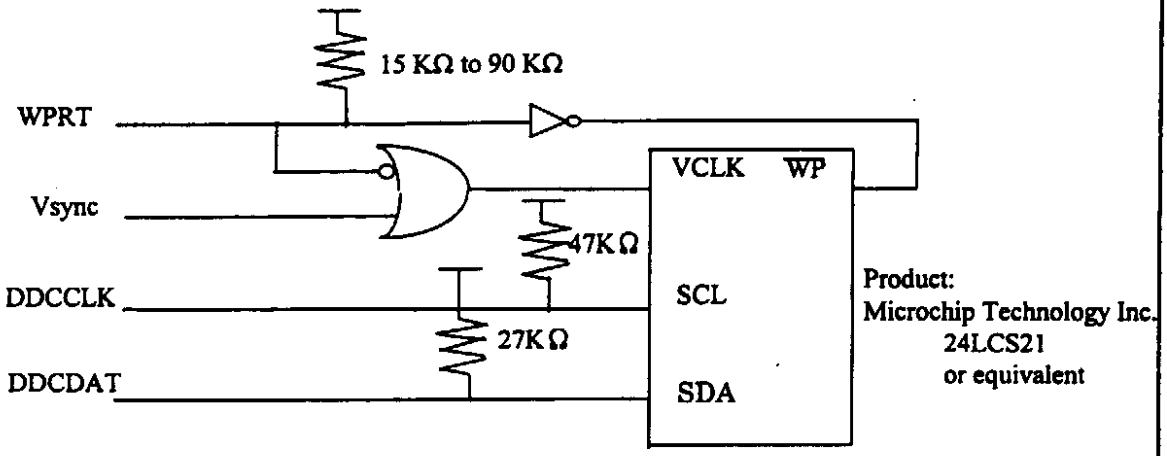
* BRT+ / BRT–: Refer to Flow chart of control way for BRT+ and BRT–

7.11.2 DDC FUNCTION

The usage of this function is based on VESADDC™ and EDID™.

- Writing mode: WPRT= "L"
- Reading mode: WPRT= "H" or Open

Please write data into necessary addresses in advance, when you use this function. Data "55H" is set in the address "00H" when the module is shipped. The input equivalent circuit diagram is as follow.

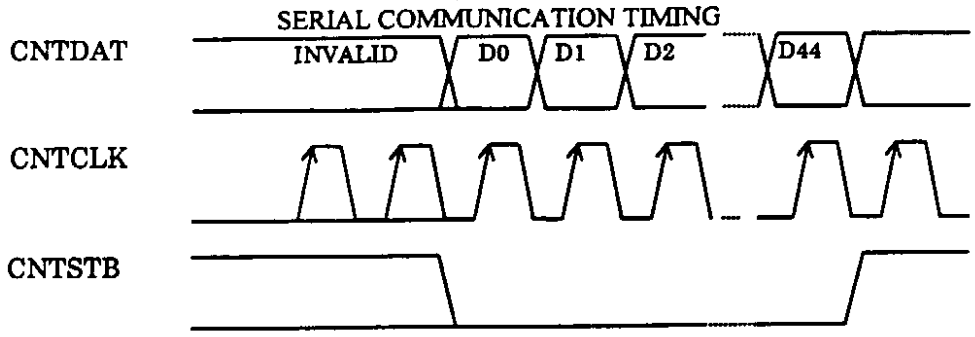


7.12 STATUS READ FUNCTIONS

This LCD module can be monitored serial data of following functions (Table 1.)

(1) Expansion mode:	See table 2 and **7.8 EXPANSION FUNCTION**
(2) Display position control (VERTICAL):	See table 3
(3) Display position control (HORIZONTAL):	See table 6
(4) CLK delay control:	See table 4
(5) CLK fall/rise synchronous change:	See table 5
(7) CLK counts of horizontal period:	See table 7
(8) CLK frequency range:	See table 8

7.12.1 SERIAL COMMUNICATION TIMING AND WAVEFORM



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	twck	350	–	ns	CNTCLK
CLK frequency	fclk	–	1.25	MHz	
DATA set-up-time	tdst	50	–	ns	CNTDAT
DATA hold-time	tdhl	350	–	ns	
Latch pulse-width	twlp	8	–	ns	CNTSTB
Latch set-up-time	tlst	1.2	–	ns	
Rise / fall time	tr , tf	–	50	ns	CNT xxx

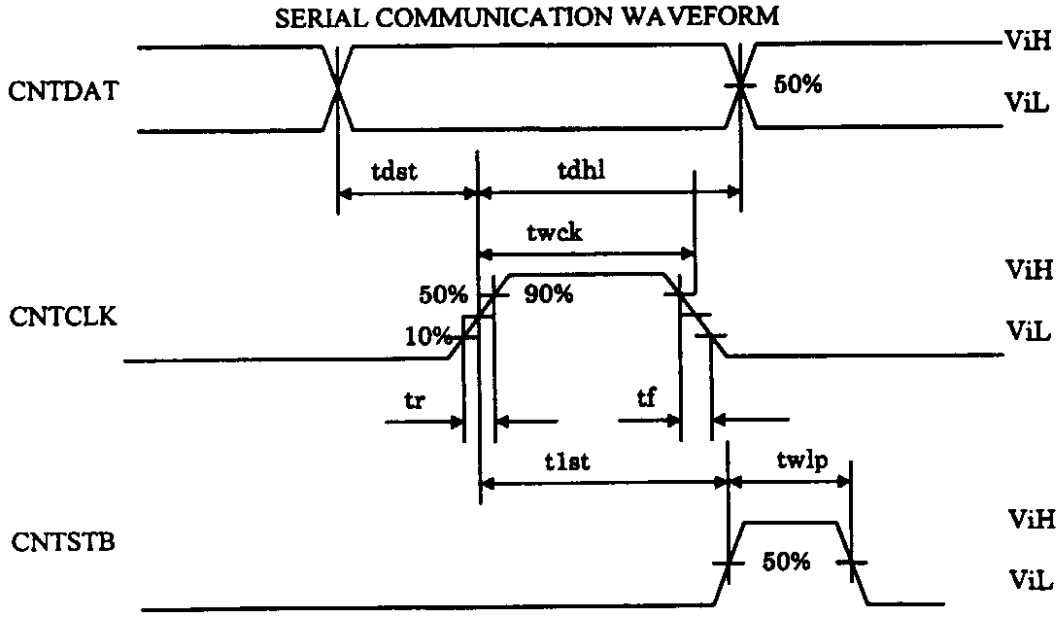


Table 1. CNTDAT Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19	DELAY2	CLK delay	
D20	DELAY1	CLK delay	
D21	DELAY0	CLK delay (LSB)	
D22	CKS	CLK signal	See table 5
D23	HD8	Horizontal display position (MSB)	See table 6
D24	HD7	Horizontal display position	
D25	HD6	Horizontal display position	
D26	HD5	Horizontal display position	
D27	HD4	Horizontal display position	
D28	HD3	Horizontal display position	
D29	HD2	Horizontal display position	
D30	HD1	Horizontal display position	
D31	HD0	Horizontal display position (LSB)	
D32	HSE10	CLK count of horizontal period (MSB)	See table 7
D33	HSE9	CLK count of horizontal period	
D34	HSE8	CLK count of horizontal period	
D35	HSE7	CLK count of horizontal period	
D36	HSE6	CLK count of horizontal period	
D37	HSE5	CLK count of horizontal period	
D38	HSE4	CLK count of horizontal period	
D39	HSE3	CLK count of horizontal period	
D40	HSE2	CLK count of horizontal period	
D41	HSE1	CLK count of horizontal period	
D42	HSE0	CLK count of horizontal period (LSB)	
D43	MOD1	CLK frequency select	See table 8
D44	MOD0	CLK frequency select	

Table 2. Display mode (VEX3 to VEX0 : 4bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	SXGA	Standard note 1
0	0	0	1	1.25	XGA	See 7.8.3 DISPLAY IMAGE
0	0	1	0	1.6	SVGA, MAC	
0	0	1	1	2.0	VGA	
0	1	0	0	2.5	PC98,VGA-TEXT	
0	1	0	1	—	Prohibit	
0	1	1	0	—	Prohibit	
0	1	1	1	—	Prohibit	
1	0	0	0	—	Prohibit	
1	0	0	1	—	Prohibit	
1	0	1	0	—	Prohibit	
1	0	1	1	—	Prohibit	
1	1	0	0	—	Prohibit	
1	1	0	1	—	Prohibit	
1	1	1	0	—	Prohibit	
1	1	1	1	—	Prohibit	

Table 3. Vertical position (VD10 to VD0 : 11bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] note 1
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 note 2

note 1: The number of horizontal line between Vsync-fall and RGB data valid.
note 2: The maximum number is based on horizontal line count of the display mode.

Table 4. CLK delay (DELAY6 to DELAY0 : 7bit)

DELAY[6..0]	Delay	Unit
00H	7.0	ns
01H	7.6	ns
02H	8.2	ns
03H	8.8	ns
04H	9.4	ns
05H	10.0	ns
06H	10.5	ns
07H	11.2	ns
08H	11.8	ns
09H	12.4	ns
0AH	13.0	ns
0BH	13.7	ns
0CH	14.2	ns
0DH	14.8	ns
0EH	15.3	ns
0FH	15.9	ns
10H	16.6	ns
11H	17.2	ns
12H	17.8	ns
13H	18.4	ns
14H	18.9	ns
15H	19.5	ns
16H	20.1	ns
17H	20.7	ns
18H	21.4	ns
19H	22.0	ns
1AH	22.6	ns
1BH	23.2	ns
1CH	23.8	ns
1DH	24.4	ns
1EH	24.9	ns
1FH	25.6	ns
20H	26.3	ns
21H	26.9	ns
22H	27.4	ns
23H	28.1	ns
24H	28.5	ns
25H	29.1	ns
26H	29.7	ns
27H	30.3	ns
28H	31.0	ns
29H	31.6	ns
2AH	32.2	ns
2BH	32.8	ns
2CH	33.3	ns
2DH	33.9	ns
2EH	33.4	ns
2FH	35.1	ns

DELAY[6..0]	Delay	Unit
30H	35.6	ns
31H	36.1	ns
32H	36.8	ns
33H	37.5	ns
34H	37.9	ns
35H	38.5	ns
36H	39.1	ns
37H	39.7	ns
38H	40.4	ns
39H	41.0	ns
3AH	41.5	ns
3BH	42.1	ns
3CH	42.6	ns
3DH	43.2	ns
3EH	43.8	ns
3FH	44.4	ns
40H	45.0	ns
41H	45.6	ns
42H	46.2	ns
43H	46.8	ns
44H	47.3	ns
45H	47.8	ns
46H	48.4	ns
47H	49.0	ns
48H	49.6	ns
49H	50.2	ns
4AH	50.8	ns
4BH	51.4	ns
4CH	51.9	ns
4DH	52.6	ns
4EH	53.1	ns
4FH	53.7	ns
50H	54.5	ns
51H	55.0	ns
52H	55.6	ns
53H	56.3	ns
54H	56.8	ns
55H	57.4	ns
56H	57.9	ns
57H	58.5	ns
58H	59.2	ns
59H	59.8	ns
5AH	60.4	ns
5BH	61.1	ns
5CH	61.6	ns
5DH	62.2	ns
5EH	62.7	ns
5FH	63.3	ns

DELAY[6..0]	Delay	Unit
60H	64.0	ns
61H	64.7	ns
62H	65.3	ns
63H	66.0	ns
64H	66.5	ns
65H	67.1	ns
66H	67.7	ns
67H	68.3	ns
68H	68.9	ns
69H	69.5	ns
6AH	70.1	ns
6BH	70.7	ns
6CH	71.2	ns
6DH	71.9	ns
6EH	72.4	ns
6FH	73.1	ns
70H	73.6	ns
71H	74.2	ns
72H	74.8	ns
73H	75.4	ns
74H	75.9	ns
75H	76.5	ns
76H	77.0	ns
77H	77.7	ns
78H	78.3	ns
79H	79.0	ns
7AH	79.6	ns
7BH	80.2	ns
7CH	80.8	ns
7DH	81.4	ns
7EH	81.9	ns
7FH	82.5	ns

note 2: This delay value is typical value at Ta=25℃. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

① Variation of CLK delay by temperature drift. (only reference) The temperature constant of CLK delay is 0.2%/℃.

Calculated example:

In case of delay time is 20ns at Ta=25℃;

(a) In case Ta rising to 50℃.

Increase of delay time → (50℃−25℃)×0.002×20ns=+1ns

So, the total delay time is 21 ns at Ta=50℃.

(b) In case Ta falling to 0℃.

Decrease of delay time → (0℃−25℃)×0.002×20ns=-1ns

So, the total delay time is 19 ns at Ta=0℃.

② Variation of CLK delay time against each LCD module. (only reference)

−10.5% to +14.4%

	MOD setting			
	0,0	0,1	1,0	1,1
The upper limit of CLK delay; DELAY[6..0]	49H	59H	6BH	7FH

Table 5. CLK signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK. 

Table 6. Display horizontal position (HD8 to HD0 : 9bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] note 1
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
0	0	1	1	0	1	1	0	1	Prohibit
0	0	1	1	0	1	1	1	0	110
0	0	1	1	0	1	1	1	1	111
·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

note 1: The number of CLK between Hsync-fall and RGB data valid.

Table 7. CLK count of horizontal period (HSE10 to HSE0 : 11bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count note 1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
·	·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

note 1: The number of CLK between Hsync signals.

Table 8. CLK frequency select (MOD1 to MOD0 : 2bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	90 to 135
0	1	65 to 90
1	0	50 to 65
1	1	20 to 50

7.13 OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	γ=2.2 viewing angle θR=0°, θL=0°, θD=0°, White／Black, at center	150	220	—	—	note 1
Luminance	Lvmax	White, at center	100	150	—	cd/m^2	note 2
Luminance uniformity	—	White	—	—	1.30	—	note 3
Color gamut	C	θR=0°, θL=0°,θU=0°, θD=0°, at center, to NTSC	40	—	—	%	—
Response time	tpd	Black to white	—	58	130	ms	note 4

Reference data

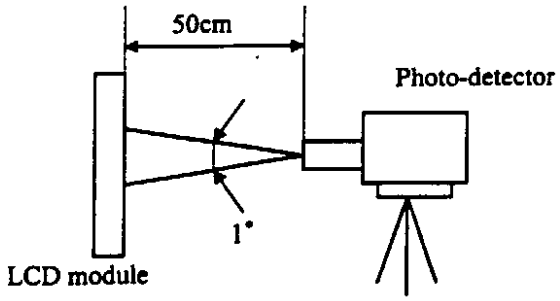
(Ta = 25℃, VDD = 12V, VDDB = 12V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle range	θR	CR > 10, θU=0°, θD=0°	70	80	—	deg.
	θL		70	80	—	deg.
	θU	CR > 10, θR=0°, θL=0°	70	80	—	deg.
	θD		60	80	—	deg.
Luminance control range	—	Maximum luminance: 100%	—	30 - 100	—	%

note 1: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

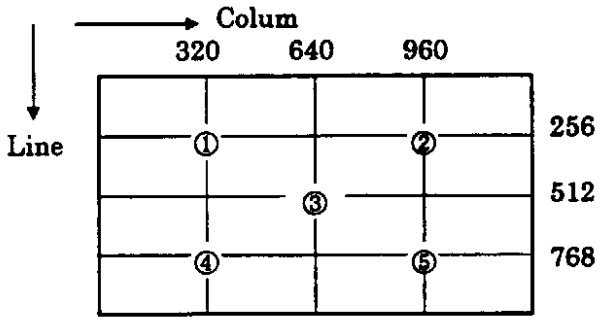
note 2: The luminance is measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.



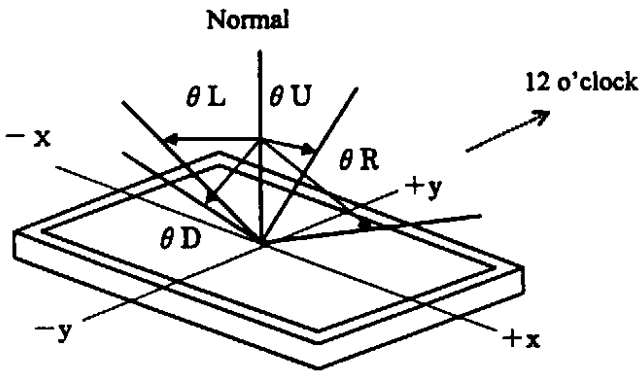
note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

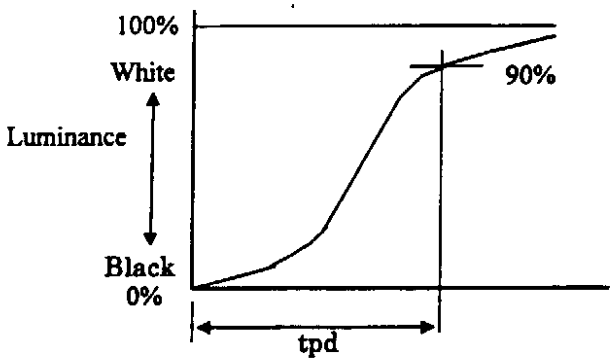
The luminance is measured at near the five points shown below.



note 4: Definitions of viewing angle are as follows.



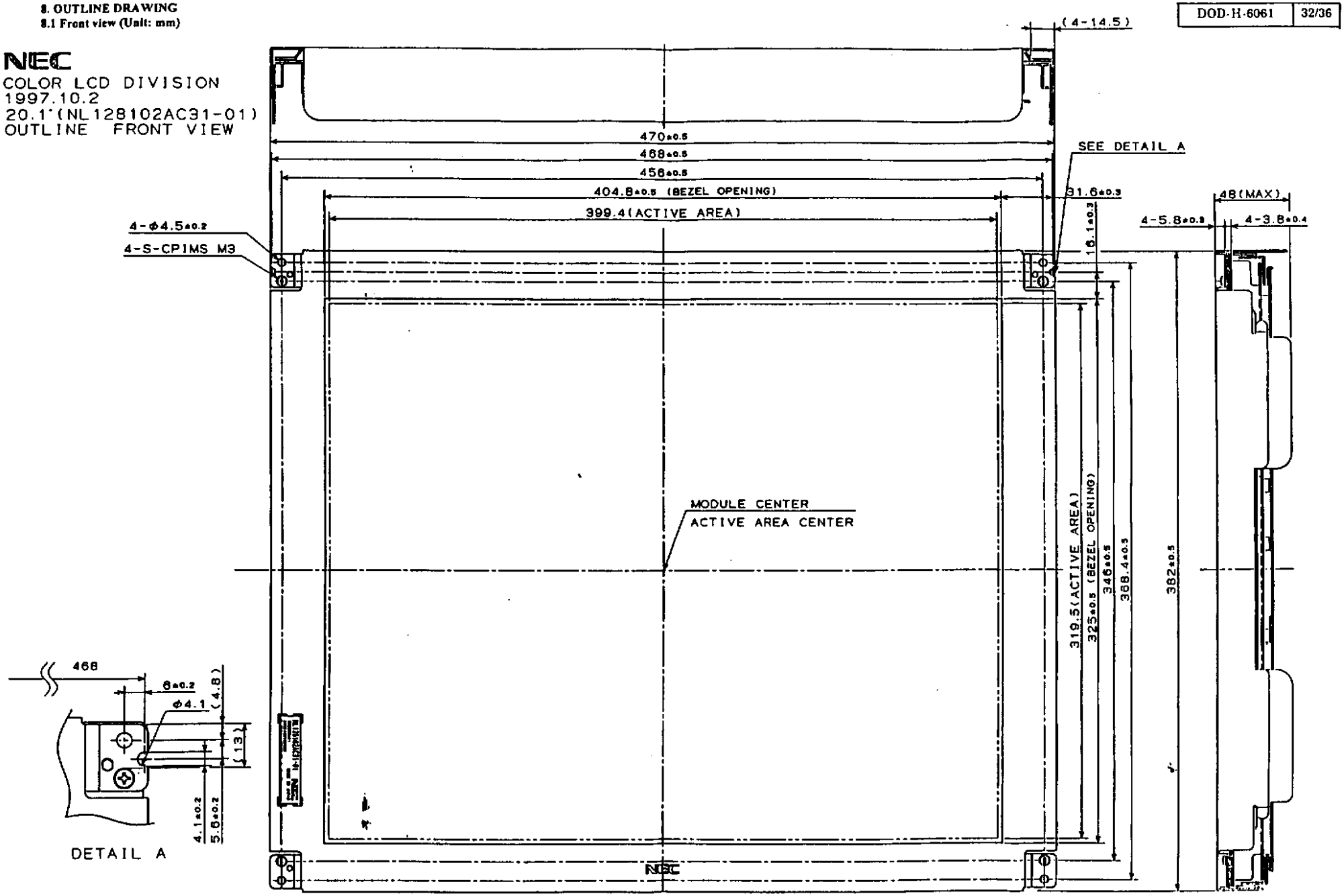
note 5: Definitions of response time is as follows.
Photo-detector out put signal is measured when the luminance changes "black" to "white". Response time is the time between 0% and 90% of the photo-detector output amplitude.



8. OUTLINE DRAWING

8.1 Front view (Unit: mm)

NEC
COLOR LCD DIVISION
1997.10.2
20.1"(NL128102AC31-01)
OUTLINE FRONT VIEW

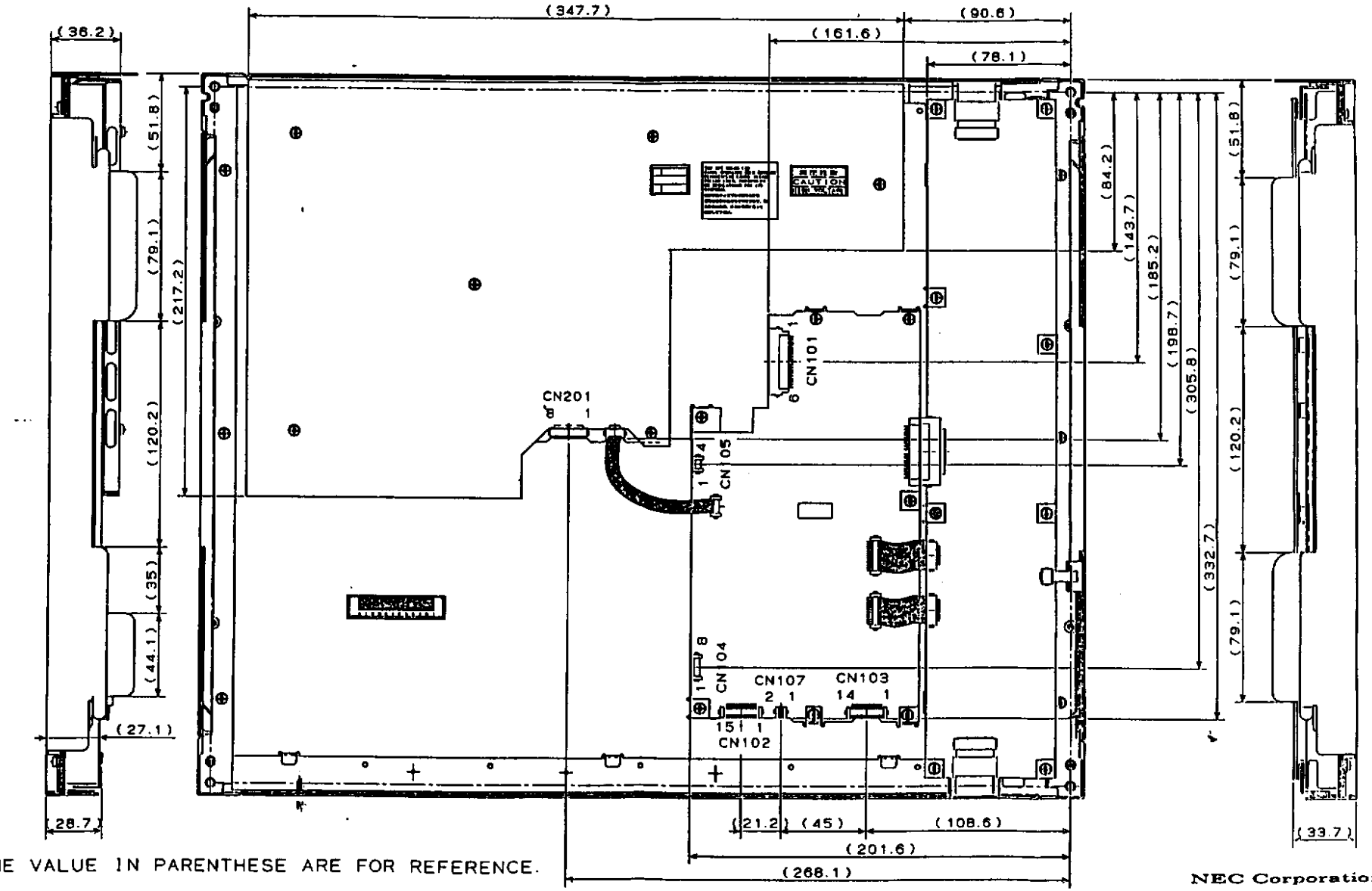


· THE VALUE IN PARENTHESE ARE FOR REFERENCE.

8.2 Rear view

NEC

COLOR LCD DIVISION
1997.10.2
20.1"(NL128102AC31-01B)
OUTLINE REAR VIEW



· THE VALUE IN PARENTHESE ARE FOR REFERENCE.

9. GENERAL CAUTIONS

Because next figures and sentences are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTION**

Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

① Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

②

 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

⑧ Do not pull the front side (display surface side)of the module on a desk or a table for a long time, because the display may become un-uniformity.

(3) Cautions for the atmosphere

①Dew drop atmosphere should be avoided.

②Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

③This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

④Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

① Do not apply fixed pattern data signal for a long time to the LCD module. It may cause image sticking. Please use screen savers if the display pattern is fixed more than 30 minutes.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistor or switch etc.

③ When returning the module for repair or etc., please pack the module not to be broken. We recommend to the original shipping packages.

Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

Revision History

Rev.	Prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	Feb 16, 1998	No. DOD-H-6061			M Yoshida / T. Kuwanagi	