

PRELIMINARY

**NEC** NEC LCD Technologies, Ltd.

# TFT COLOR LCD MODULE


**NL128102BC29-10**

**48.0cm (19.0 Type)**

**SXGA**

**LVDS Interface (2 ports)**

## PRELIMINARY DATA SHEET

DOD-PP-0492 (2nd edition) 

**This PRELIMINARY DATA SHEET is updated document from DOD-PP-0486(1)**

**All information is subject to change without notice. Please confirm the sales representative before starting to design your system.**

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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## 1. OUTLINE

### 1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL128102BC29-10 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

### 1.2 APPLICATION

- Monitor for PC

### 1.3 FEATURES

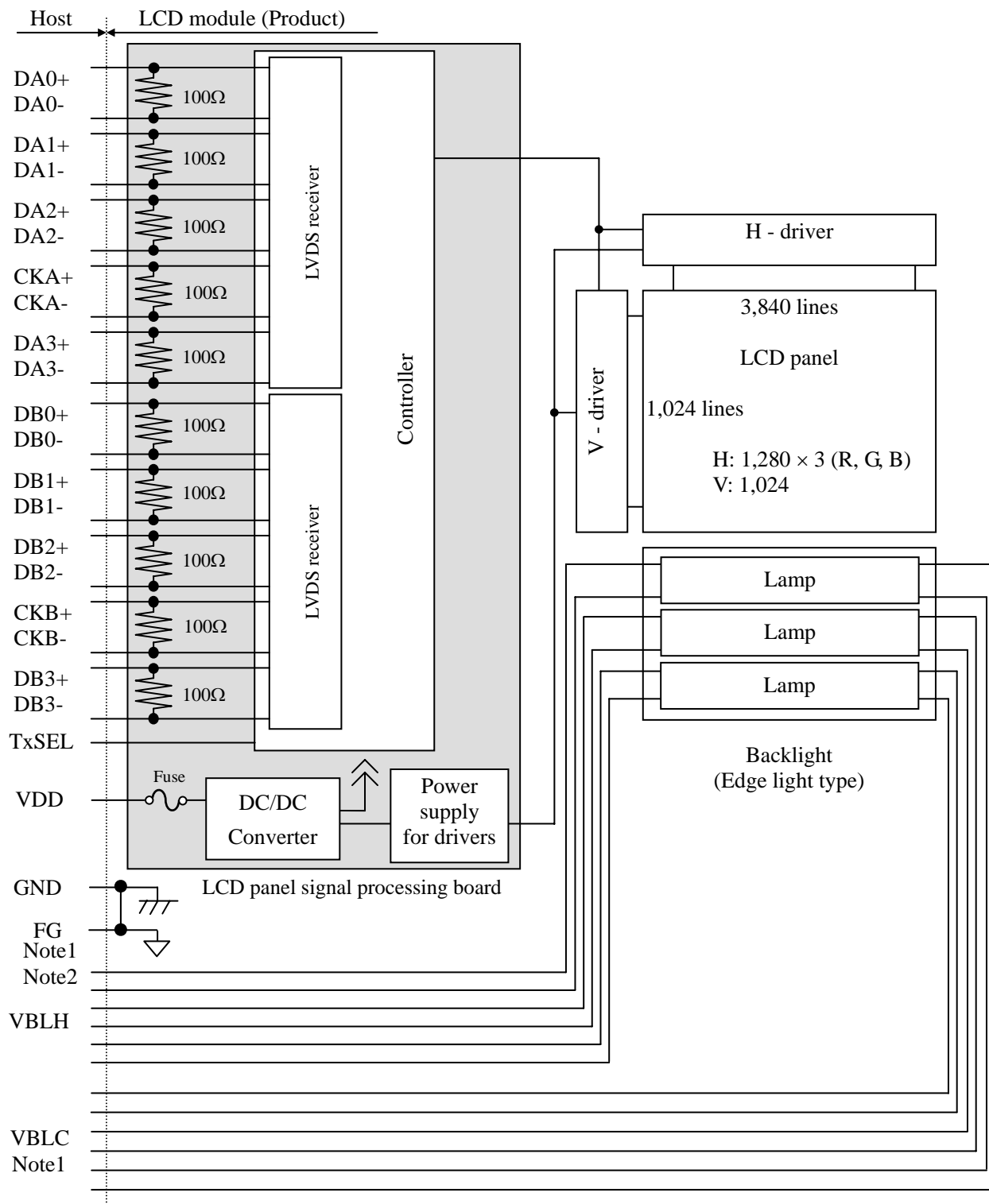
- Ultra-wide viewing angle (Adoption of Ultra-Advanced Super Fine TFT (UA-SFT))
- Wide color gamut
- High contrast
- LVDS interface
- Selectable LVDS data input map
- Edge light type (without inverter)

## 2. GENERAL SPECIFICATIONS

<b>Display area</b>	376.32 (H) × 301.056 (V) mm
<b>Diagonal size of display</b>	48cm (19.0 inches)
<b>Drive system</b>	a-Si TFT active matrix
<b>Display color</b>	16,777,216 colors
<b>Pixel</b>	1,280 (H) × 1,024 (V) pixels
<b>Pixel arrangement</b>	RGB (Red dot, Green dot, Blue dot) vertical stripe
<b>Dot pitch</b>	0.098 (H) × 0.294 (V) mm
<b>Pixel pitch</b>	0.294 (H) × 0.294 (V) mm
<b>Module size</b>	404.2 (W) × 330.0 (H) × 22.0 (D) mm (typ.)
<b>Weight</b>	(2,700) g (typ.)
<b>Contrast ratio</b>	(800:1) (typ.)
<b>Viewing angle</b>	At the contrast ratio $\geq 10:1$ <ul style="list-style-type: none"> <li>• Horizontal: Right side 88° (typ.), Left side 88° (typ.)</li> <li>• Vertical: Up side 88° (typ.), Down side 88° (typ.)</li> </ul>
<b>Designed viewing direction</b>	Viewing angle with optimum grayscale ( $\gamma=2.2$ ): normal axis (Perpendicular)
<b>Polarizer surface</b>	Antiglare
<b>Polarizer pencil-hardness</b>	3H (min.) [by JIS K5400]
<b>Color gamut</b>	At LCD panel center 72 % (typ.) [against NTSC color space]
<b>Response time</b>	$T_{on} + T_{off}$ (10% ← → 90%) (20) ms (typ.)
<b>Luminance</b>	At $IBL=6.0mArms / lamp$ (300) $cd/m^2$ (typ.)
<b>Signal system</b>	LVDS 2 port (Receiver: THC63LVDF84B, THine Electronics Inc. or equivalent) [8bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]
<b>Power supply voltage</b>	LCD panel signal processing board: 5.0V
<b>Backlight</b>	Edge light type: 6 cold cathode fluorescent lamps (without inverter)
<b>Power consumption</b>	At $IBL= 6.0mArms/lamp$ , Checkered flag pattern TBD W (typ., Power dissipation of the inverter is not included.)

2

### 3. BLOCK DIAGRAM



2

Note1: Relations between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the LCD module are as follows.

GND - FG	Connected
GND - VBLC	Not connected
FG - VBLC	Not connected

2

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

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## 4. DETAILED SPECIFICATIONS

### 4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	404.2 ± 0.5 (W) × 330.0 ± 0.5 (H) × 22.0 ± 0.3 (D) Note1	Note2 mm
Display area	376.32 (H) × 301.056 (V)	Note2 mm
Weight	(2,700) (typ.), (2,850) (max.)	g

Note1: Excluding lamp cable, cable clamp and projections.

Note2: See "7. OUTLINE DRAWINGS".

### 4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +6.0	V	Ta = 25°C
	Lamp voltage	VBLH	2,000	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to +2.8	V	Ta = 25°C VDD= 5.0V
	Function signal Note2	VF		V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note3
	Rear surface	TopR	0 to +60	°C	Note4
Relative humidity Note5		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	40 < Ta ≤ 50°C
			≤ 70	%	50 < Ta ≤ 55°C
Absolute humidity Note5		AH	≤ 73 Note6	g/m <sup>3</sup>	Ta > 55°C
Operating altitude		-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude		-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note2: Function signal is TxSEL.

Note3: Measured at center of LCD panel surface (including self-heat)

Note4: Measured at center of LCD module's rear shield surface (including self-heat)

Note5: No condensation

Note6: Water amount at Ta = 55°C and RH = 70%

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## 4.3 ELECTRICAL CHARACTERISTICS

### 4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage	VDD	4.5	5.0	5.5	V	-	
Power supply current	IDD	-	TBD Note1	TBD Note2	mA	at VDD = 5.0V	
Permissible ripple voltage	VRP	-	-	100	mVp-p	for VDD	
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM = 1.2V Note3
	Low	VTL	-100	-	-	mV	
Terminating resistance	RT	-	100	-	Ω	-	
Input voltage for TxSEL signal	High	VFH	Keep this pin open.			-	TxSEL Note4
	Low	VFL	-	-	0.5	V	
Input current for TxSEL signal	IFL	-80	-	-35	μA		

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS receiver

Note4: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)



### 4.3.2 Backlight lamp

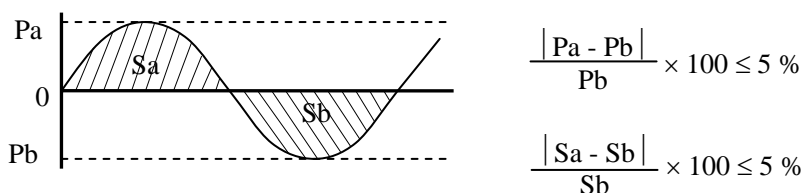
(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.5	6.0	7.0	mArms	at IBL=6.0mArms: (300) cd/m <sup>2</sup> Note3
Lamp voltage	VBLH	-	650	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,350	-	-	Vrms	Ta = 25°C Note2, Note3, Note6
		1,550	-	-	Vrms	Ta = 0°C Note2, Note3, Note6
Lamp oscillation frequency	FO	40	48	55	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative  
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "4.9.1 Timing characteristics".)

n: Natural number (1, 2, 3 .....)

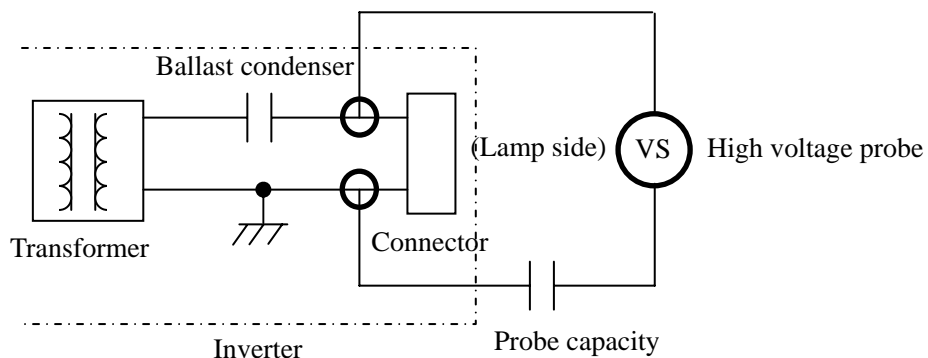
Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

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Note6: In case of Inverter with Ballast condenser, "VS" is the voltage level between Ballast condenser and Connector (Refer to the below "Example of measurement"). "VS" should be designed to be more than minimum "VS". Otherwise the lamp may not be turned on because the lamp starting voltage is less than minimum "VS".

Example of measurement

Probe capacity: 3pF (Tektronix, inc.: P6015A)



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### 4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	5.0V	≤ 100		mVp-p

Note1: The permissible ripple voltage includes spike noise.

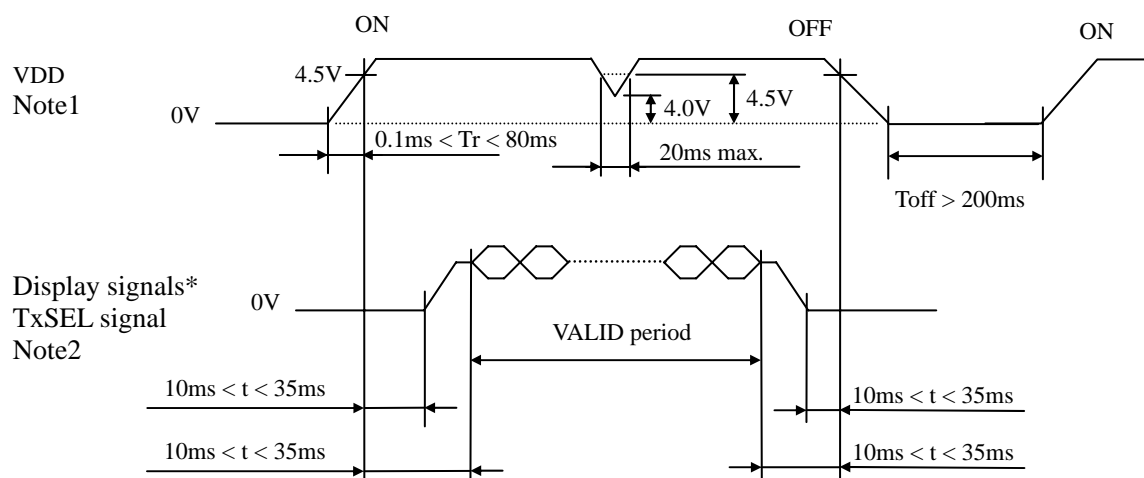
### 4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	TBD	TBD	(2.5 A)	(6.25 A) 5min. max.	Note1
			(32 V)		

2

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

## 4.4 POWER SUPPLY VOLTAGE SEQUENCE



\* These signals should be measured at the terminal of 100  $\Omega$  resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 4.5V, a protection circuit may work, and then this product may not work.

Note2: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-) and TxSEL signal must be "0" voltage, exclude the VALID period (See above sequence diagram). If these signals are higher than 0.3V, the internal circuit is damaged. If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

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## 4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

### 4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-X30SSL-HF (Japan Aviation Electronics Industry Limited (JAE))  
 Adaptable plug: FI-X30C series/ FI-X30H series/ FI-X30M series  
 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	Note2
8	CKA-	Odd pixel clock	Note1
9	CKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	Note2
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	Note2
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CKB-	Even pixel clock	Note1
21	CKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	Note2
25	TxSEL	Selection of LVDS data input map	Open: Mode A Low: Mode B Note3, Note4
26	RSVD	-	Keep this pin Open.
27	N.C.	-	Keep this pin Open.
28	VDD	Power supply	Note2
29			
30			

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "4.6 SELECTION OF LVDS DATA INPUT MAP".

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## 4.5.2 Backlight lamp

**Attention: VBLH and VBLC must be connected correctly. Wrong connections will cause electric shock and also break down of the product.**

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (Pink)
2	VBLC	Low voltage (Cold)	Cable color: (Gray)

2

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (White)
2	VBLC	Low voltage (Cold)	Cable color: (Gray)

2

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (Red)
2	VBLC	Low voltage (Cold)	Cable color: (Gray)

2

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (Pink)
2	VBLC	Low voltage (Cold)	Cable color: )Gray)

2

CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (White)
2	VBLC	Low voltage (Cold)	Cable color: (Gray)

2

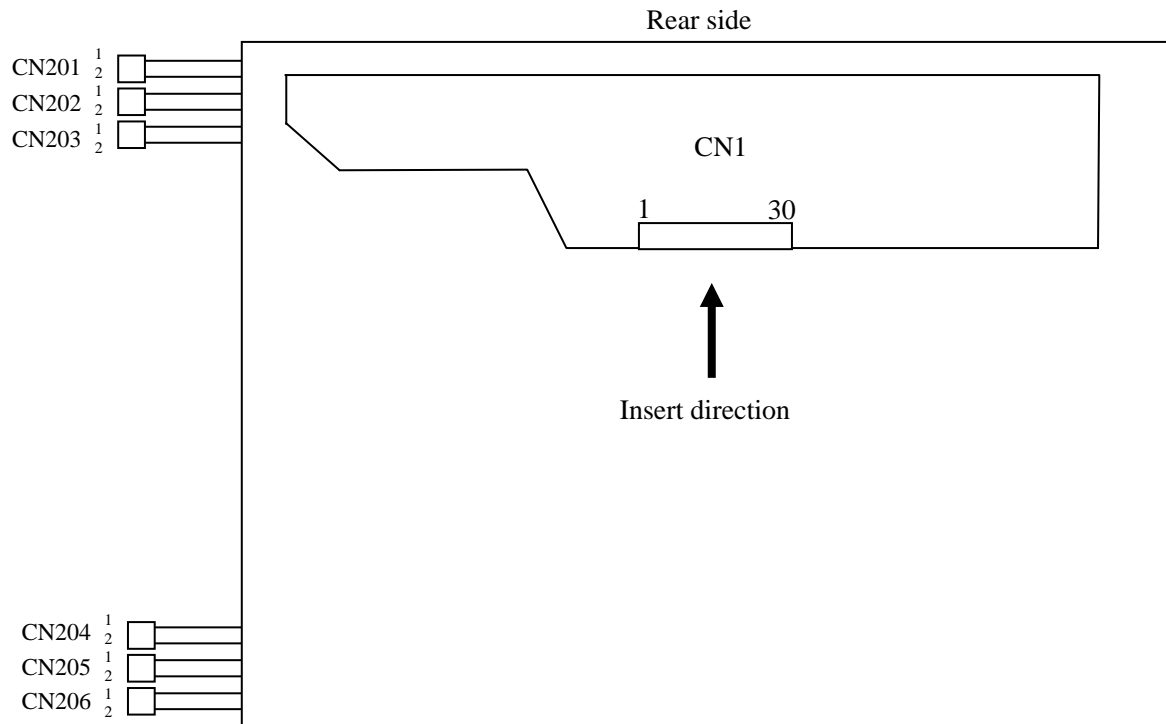
CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)  
Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)  
SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: (Red)
2	VBLC	Low voltage (Cold)	Cable color: (Gray)

2

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## 4.5.3 Positions of plug and socket



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## 4.6 SELECTION OF LVDS DATA INPUT MAP

### 4.6.1 Mode A

Input data		Note1		Transmitter				Note2		CN1	
				Pin	DS90CF383, C385 or equivalent					Pin	Symbol
Odd pixel data and control signal	RA0	→	51	TXIN0					1	DA0-	
	RA1	→	52	TXIN1	TA1-	→		2	DA0+		
	RA2	→	54	TXIN2	TA1+	→					
	RA3	→	55	TXIN3							
	RA4	→	56	TXIN4	TB1-	→		3	DA1-		
	RA5	→	3	TXIN6	TB1+	→		4	DA1+		
	GA0	→	4	TXIN7							
	GA1	→	6	TXIN8	TC1-	→		5	DA2-		
	GA2	→	7	TXIN9	TC1+	→		6	DA2+		
	GA3	→	11	TXIN12					7	GND	
	GA4	→	12	TXIN13	TCLK1-	→		8	CKA-		
	GA5	→	14	TXIN14	TCLK1+	→		9	CKA+		
	BA0	→	15	TXIN15							
	BA1	→	19	TXIN18	TD1-	→		10	DA3-		
	BA2	→	20	TXIN19	TD1+	→		11	DA3+		
	BA3	→	22	TXIN20							
	BA4	→	23	TXIN21							
	BA5	→	24	TXIN22							
	Note3	RSVD	→	27	TXIN24						
	Note3	RSVD	→	28	TXIN25						
		DE	→	30	TXIN26						
		RA6	→	50	TXIN27						
		RA7	→	2	TXIN5						
		GA6	→	8	TXIN10						
		GA7	→	10	TXIN11						
		BA6	→	16	TXIN16						
	Note3	BA7	→	18	TXIN17						
	Note3	RSVD	→	25	TXIN23						
		CLK	→	31	CLKIN						
	Even pixel data	RB0	→	51	TXIN0						
		RB1	→	52	TXIN1	TA2-	→		12	DB0-	
RB2		→	54	TXIN2	TA2+	→		13	DB0+		
RB3		→	55	TXIN3				14	GND		
RB4		→	56	TXIN4	TB2-	→		15	DB1-		
RB5		→	3	TXIN6	TB2+	→		16	DB1+		
GB0		→	4	TXIN7				17	GND		
GB1		→	6	TXIN8	TC2-	→		18	DB2-		
GB2		→	7	TXIN9	TC2+	→		19	DB2+		
GB3		→	11	TXIN12							
GB4		→	12	TXIN13	TCLK2-	→		20	CKB-		
GB5		→	14	TXIN14	TCLK2+	→		21	CKB+		
BB0		→	15	TXIN15							
BB1		→	19	TXIN18	TD2-	→		22	DB3-		
BB2		→	20	TXIN19	TD2+	→		23	DB3+		
BB3		→	22	TXIN20				24	GND		
BB4		→	23	TXIN21				25	TxSEL		
BB5		→	24	TXIN22				26	RSVD		
Note3		RSVD	→	27	TXIN24			27	N.C.		
Note3		RSVD	→	28	TXIN25			28	VDD		
Note3		RSVD	→	30	TXIN26			29	VDD		
		RB6	→	50	TXIN27			30	VDD		
		RB7	→	2	TXIN5						
		GB6	→	8	TXIN10						
		GB7	→	10	TXIN11						
		BB6	→	16	TXIN16						
		BB7	→	18	TXIN17						
Note3		RSVD	→	25	TXIN23						
		CLK	→	31	CLKIN						



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4.6.2 Mode B

Input data		Note1		Transmitter				Note2		CN1	
				Pin	THC63LVDF83A/R or equivalent	Pin	THC63LVD823 or equivalent			Pin	Symbol
Odd pixel data and control signal	RA2	→	51	TA0		53	R12				
	RA3	→	52	TA1		54	R13	TA1-	→	1	DA0-
	RA4	→	54	TA2		57	R14	TA1+	→	2	DA0+
	RA5	→	55	TA3		58	R15				
	RA6	→	56	TA4		59	R16	TB1-	→	3	DA1-
	RA7	→	3	TA5		60	R17	TB1+	→	4	DA1+
	GA2	→	4	TA6		63	G12				
	GA3	→	6	TB0		64	G13	TC1-	→	5	DA2-
	GA4	→	7	TB1		65	G14	TC1+	→	6	DA2+
	GA5	→	11	TB2		66	G15				
	GA6	→	12	TB3		67	G16	TCLK1-	→	8	GND
	GA7	→	14	TB4		68	G17	TCLK1+	→	9	CKA-
	BA2	→	15	TB5		73	B12				
	BA3	→	19	TB6		74	B13	TD1-	→	10	CKA+
	BA4	→	20	TC0	1st	75	B14	TD1+	→	11	DA3-
	BA5	→	22	TC1		76	B15				
	BA6	→	23	TC2		77	B16				
	BA7	→	24	TC3		78	B17				
	Note3	RSVD	→	27	TC4		7	RSVD			
	Note3	RSVD	→	28	TC5		8	RSVD			
		DE	→	30	TC6		9	DE			
		RA0	→	50	TD0		51	R10			
		RA1	→	2	TD1		52	R11			
		GA0	→	8	TD2		61	G10			
		GA1	→	10	TD3		62	G11			
		BA0	→	16	TD4		69	B10			
		BA1	→	18	TD5		70	B11			
	Note3	RSVD	→	25	TD6		-				
		CLK	→	31	CLKIN		10	CLK			
	Even pixel data	RB2	→	51	TA0		81	R22			
		RB3	→	52	TA1		82	R23	TA2-	→	12
RB4		→	54	TA2		83	R24	TA2+	→	13	DB0+
RB5		→	55	TA3		84	R25			14	GND
RB6		→	56	TA4		85	R26	TB2-	→	15	DB1-
RB7		→	3	TA5		86	R27	TB2+	→	16	DB1+
GB2		→	4	TA6		91	G22			17	GND
GB3		→	6	TB0		92	G23	TC2-	→	18	DB2-
GB4		→	7	TB1		93	G24	TC2+	→	19	DB2+
GB5		→	11	TB2		94	G25				
GB6		→	12	TB3		95	G26	TCLK2-	→	20	CKB-
GB7		→	14	TB4		96	G27	TCLK2+	→	21	CKB+
BB2		→	15	TB5		99	B22				
BB3		→	19	TB6		100	B23	TD2-	→	22	DB3-
BB4		→	20	TC0	2nd	1	B24	TD2+	→	23	DB3+
BB5		→	22	TC1		2	B25			24	GND
BB6		→	23	TC2		5	B26			25	TxSEL
BB7		→	24	TC3		6	B27			26	RSVD
Note3		RSVD	→	27	TC4		-			27	N.C.
Note3		RSVD	→	28	TC5		-			28	VDD
Note3		RSVD	→	30	TC6		-			29	VDD
		RB0	→	50	TD0		79	R20		30	VDD
		RB1	→	2	TD1		80	R21			
		GB0	→	8	TD2		89	G20			
		GB1	→	10	TD3		90	G21			
		BB0	→	16	TD4		97	B20			
		BB1	→	18	TD5		98	B21			
Note3		RSVD	→	25	TD6		-				
		CLK	→	31	CLKIN		-				

# PRELIMINARY

Note1: LSB (Least Significant Bit) – RA0, GA0, BA0, RB0, GB0, BB0

MSB (Most Significant Bit) – RA7, GA7, BA7, RB7, GB7, BB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

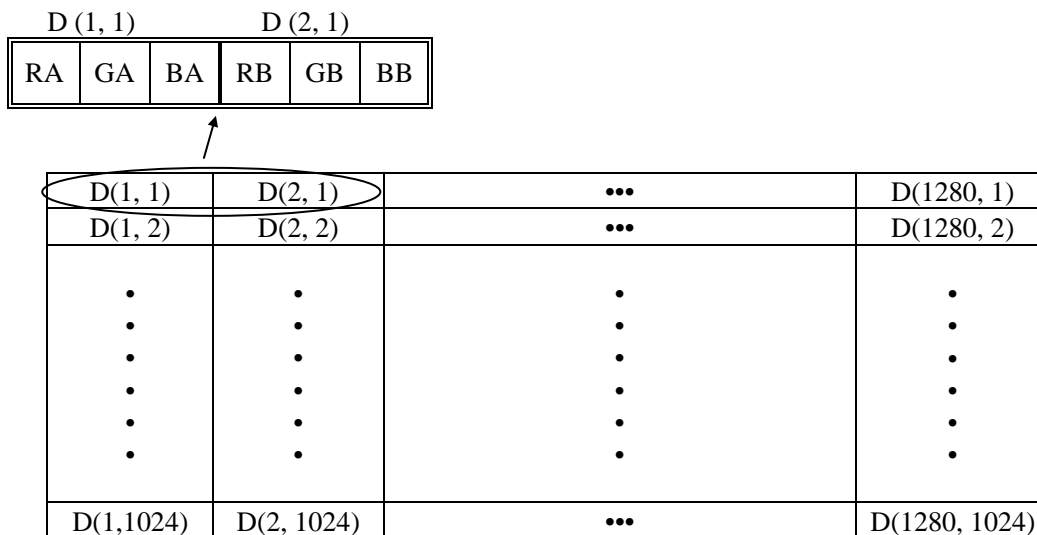
Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

## 4.7 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑																								
	↓																								
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑																								
	↓																								
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑																								
	↓																								
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

## 4.8 DISPLAY POSITION



## 4.9 INPUT SIGNAL TIMINGS

### 4.9.1 Timing characteristics

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency	1/tc	49	54	59	MHz	18.52 ns (typ.)	
	Duty	-	-			-	Note2	
	Rise time, Fall time	-				ns		
DATA	CLK-DATA	Setup time	-			ns	Note2	
		Hold time				ns		
	Rise time, Fall time	-	ns					
DE	Horizontal	Cycl	th	12.3	15.63	20.59	μs	64.0 kHz (typ.) Note1, Note2
		Display period	thd	660	844	1,024	CLK	
	Vertical (One frame)	Cycle	tv	13.1	16.6	17.5	ms	60.0 Hz (typ.) Note1
			Display period	tvd	1,030	1,066	1,422	
	CLK-DE	Setup time	-	-			ns	Note2
		Hold time	-				ns	
Rise time, Fall time		-	ns					

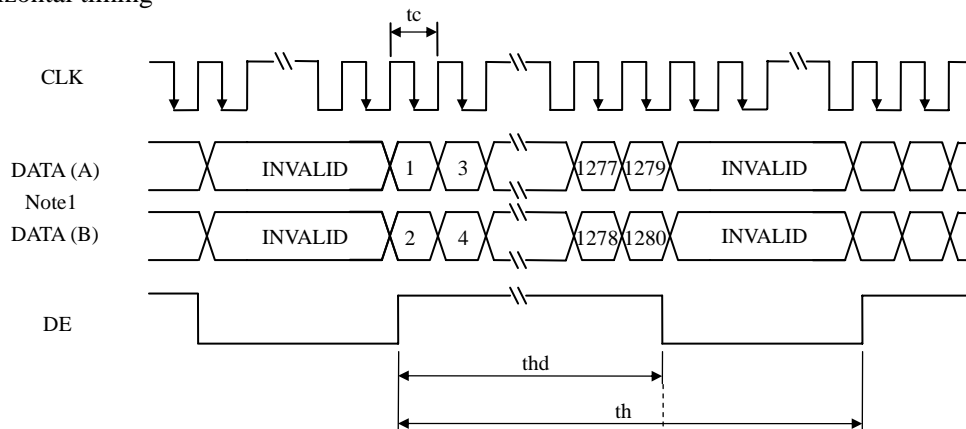
Note1: Definition of parameters is as follows.

tc = 1CLK, th = 1H

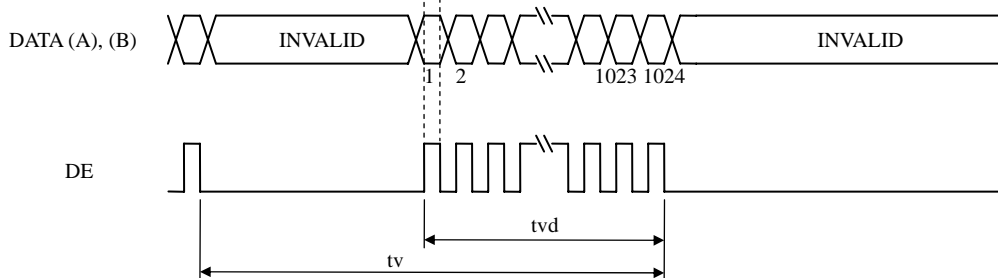
Note2: See the data sheet of LVDS transmitter.

### 4.9.2 Input signal timing chart

#### Horizontal timing



#### Vertical timing



Note1: DATA (A) = RA0-RA7, GA0-GA7, BA0-BA7  
 DATA (B) = RB0-RB7, GB0-GB7, BB0-BB7

## 4.10 OPTICS

### 4.10.1 Optical characteristics

(Note1, Note2)

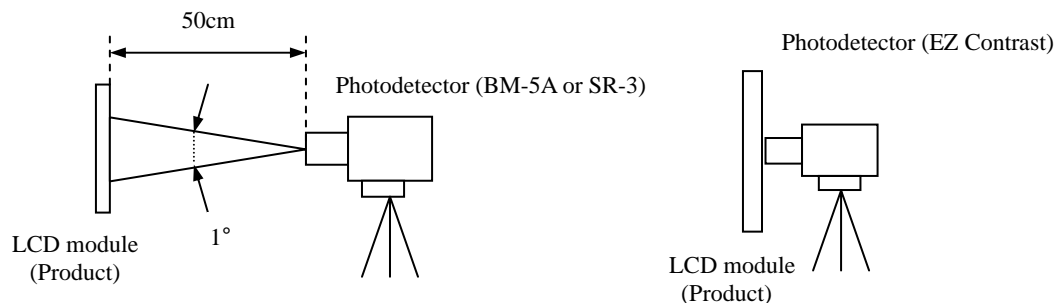
Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	(240)	(300)	-	cd/m <sup>2</sup>	BM5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	TBD	(800)	-	-	BM5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.1	1.25	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	-	0.313	-	-	SR-3	Note5
		y coordinate	Wy	-	0.329	-	-		
	Red	x coordinate	Rx	-	0.65	-	-		
		y coordinate	Ry	-	0.33	-	-		
	Green	x coordinate	Gx	-	0.29	-	-		
		y coordinate	Gy	-	0.62	-	-		
	Blue	x coordinate	Bx	-	0.14	-	-		
		y coordinate	By	-	0.08	-	-		
Color gamut	$\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$ at center, against NTSC color space	C	65	72	-	%			
Response time	Black to white	Ton	-	(10)	(20)	ms	BM-5A	Note6	
	White to black	Toff	-	(10)	(20)	ms		Note7	
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta R$	70	88	-	BM-5A, EZ Contrast	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	$\theta L$	70	88	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta U$	70	88	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	$\theta D$	70	88	-			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 5.0V, IBL = 6.0mArms/lamp, Display mode: SXGA,  
Horizontal cycle = 1/64.0kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "4.10.2 Definition of contrast ratio".

Note4: See "4.10.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = (35)°C

Note7: See "4.10.4 Definition of response times".

Note8: See "4.10.5 Definition of viewing angles".

### 4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

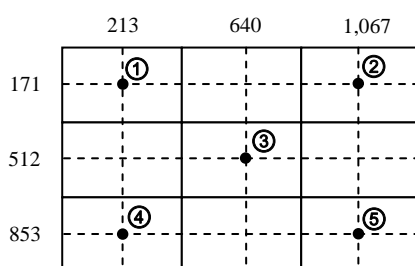
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

### 4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

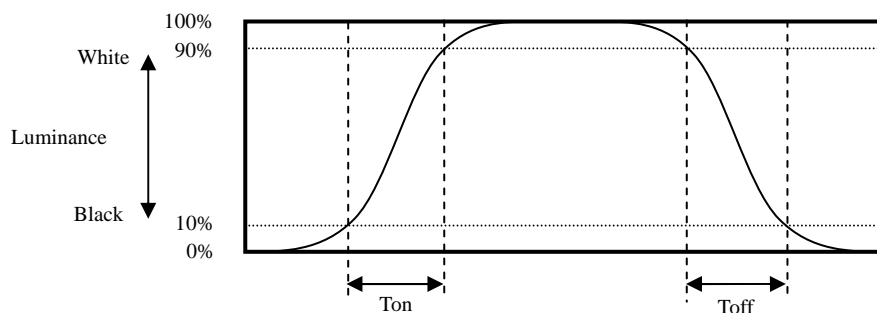
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

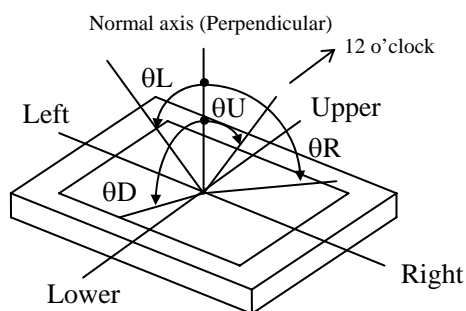


### 4.10.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



### 4.10.5 Definition of viewing angles

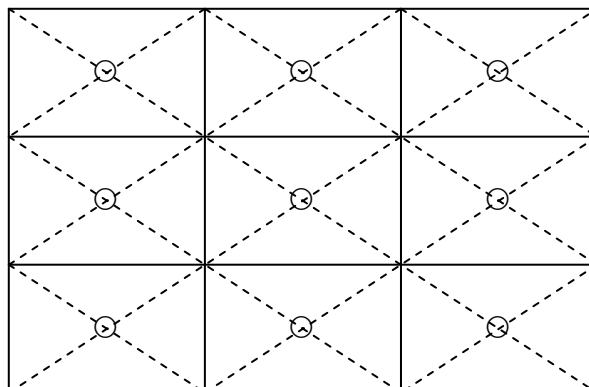


## 5. RELIABILITY TESTS

Test item		Condition	Judgment	Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions	
Heat cycle (Operation)		① 0 ± 3°C...1hour 55 ± 3°C...1hour ② 50cycles, 4hours/cycle ③ Display data is white.		
Thermal shock (Non operation)		① -20 ± 3°C...30minutes 60 ± 3°C...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.		
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s <sup>2</sup> ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages	
Mechanical shock (Non operation)		① 294m/s <sup>2</sup> , 11ms ② X, Y, Z directions ③ 3 times each directions		
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions	
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval		
Low pressure	Operation	① 53.3 kPa ② 0°C±3°C...24 hours ③ 55°C±3°C...24 hours		
	Non-operation	① 15 kPa ② -20°C±3°C...24 hours ③ 60°C±3°C...24 hours		

Note1: Display functions are checked under the same conditions as product inspection.

Note2: See the following figure for discharge points



## 6. PRECAUTIONS

## 6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**



This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.



This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.



This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

## 6.2 CAUTIONS



**\* Do not touch the working backlight. There is a danger of an electric shock.**



**\* Do not touch the working backlight. There is a danger of burn injury.**  
**\* Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s<sup>2</sup> and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

## 6.3 ATTENTIONS

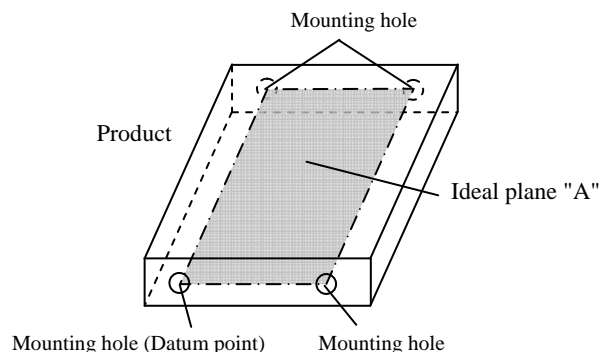


## 6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.67N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws from surface of plate(product side) must be 4.0mm to 7.0mm.



- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.  
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within  $\pm$ TBD mm.



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ Do not locate the lamp cable on the signal processing board. A noise may occur on the display image.
- ⑩ Properly connect the plug (backlight side) to adaptable socket (inverter side) without incomplete connection. After connecting, be careful not to hook the lamp cables because incomplete connection may occur by hooking the lamp cables. This incomplete connection may cause abnormal operation of high voltage circuit.
- ⑪ If the lamp cable is attached on the metal part of the product directly, high frequency leak current to the metal part may occur, then the brightness may decrease or the lamp may not be turned on.
- ⑫ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
- ⑬ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal for the worst, please wash it out with soap.

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### 6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

### 6.3.3 Characteristics

**The following items are neither defects nor failures.**

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.
- ⑧ After the product is stored under condition of low temperature or dark place for a long time, the cold cathode fluorescent lamp may not be turned on under the same condition because of the general characteristic of cold cathode fluorescent lamp. In addition, when Luminance control ratio is low in pulse width modulation method inverter, the lamp may not be turned on. In this case, power should be supplied again.

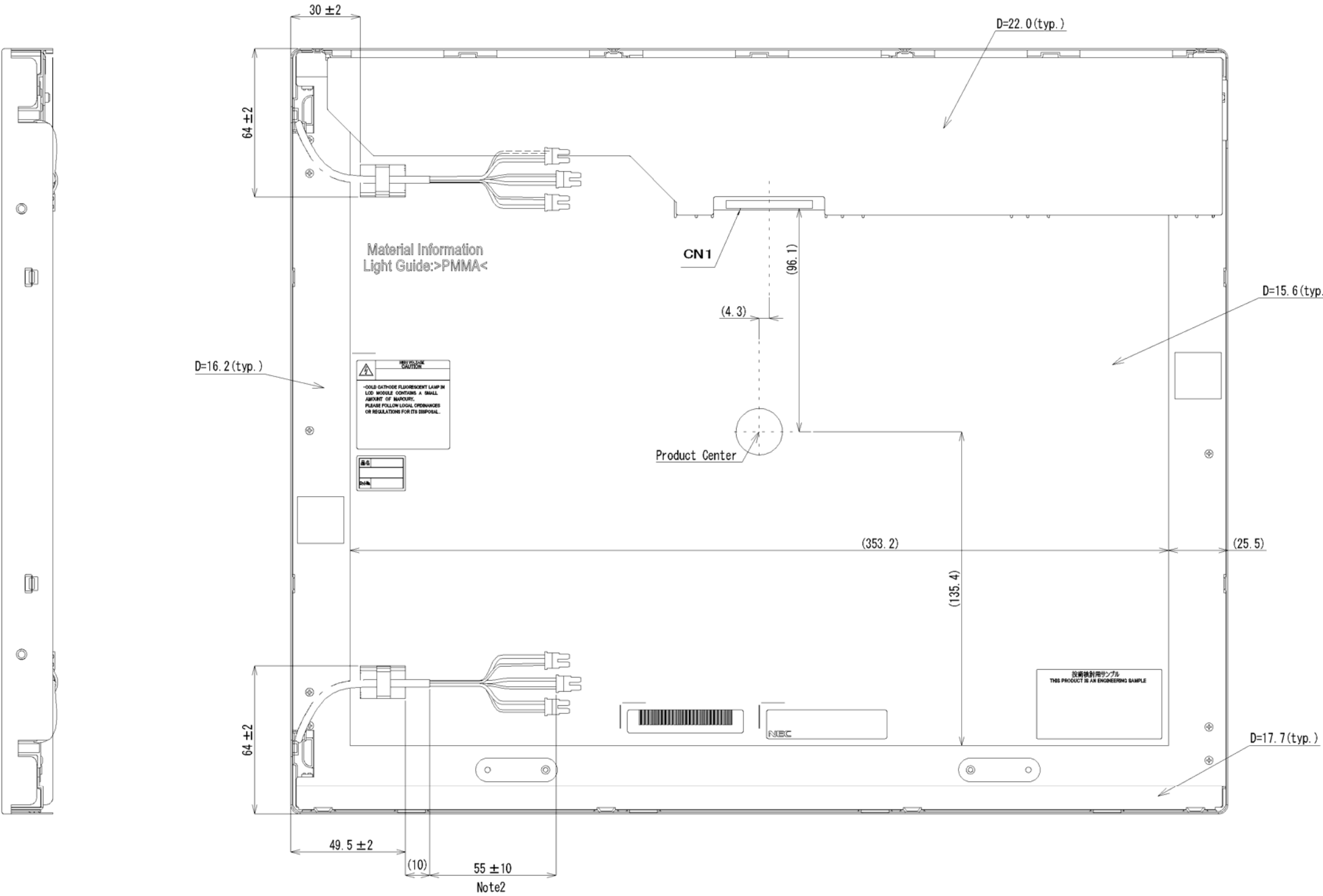
### 6.3.4 Other

- ① All GND and VDD terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.



# PRELIMINARY

7.2 REAR VIEW





Note1: The values in parentheses are for reference.  
Note2: The cable of up side and down side is the same length.

Unit: mm

# PRELIMINARY

## REVISION HISTORY

*The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.*

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-0486	Feb. 29, 2008	<p><b>Revision contents</b></p> <p>New issue</p> <p><b>Writer</b></p> <p>Approved by _____ Checked by _____ Prepared by _____</p> <p style="text-align: center;">T. OGAWA _____ E. KATAYAMA _____</p>
2nd edition	DOD-PP-0492	Mar. 10, 2008	<p><b>Revision contents</b></p> <p>P5 General specifications</p> <ul style="list-style-type: none"> <li>• Restonse time: (16) ms(typ.) → (20) ms(typ.)</li> </ul> <p>P6 Block diagram</p> <ul style="list-style-type: none"> <li>• GND-FG: Not connected → Connected</li> </ul> <p>P9 Electrical characteristics - Backlight lamp</p> <ul style="list-style-type: none"> <li>• Lamp current: 300cd/m<sup>2</sup> → (300)cd/m<sup>2</sup> (correction)</li> </ul> <p>P11 Fuse</p> <ul style="list-style-type: none"> <li>• Rating: (4.0A), (25V) → (2.5A), (32V)</li> <li>• Fusing current: (8.0A), 1min. max. → (6.25A), 5min. max.</li> </ul> <p>P14 Backlight lamp - CN201, CN202, CN203, CN204, CN205, CN206</p> <ul style="list-style-type: none"> <li>• Low voltage: Cable color: (White) → Cable color: (Gray)</li> </ul> <p>P21 Optical characteristics - Response time</p> <ul style="list-style-type: none"> <li>• Black to white, White to black: (8) ms(typ.), (16) ms(max.) → (10) ms(typ.), (20) ms(max.)</li> </ul> <p>P24-25 Attentions - Handling the product</p> <ul style="list-style-type: none"> <li>• ⑤ (change of expression)</li> <li>• ⑫ (elmination)</li> </ul> <p>P27 Outline drawings</p> <ul style="list-style-type: none"> <li>• Depth: 4.0 to 7.0 → Note1 (change)</li> </ul> <p><b>Signature of writer</b></p> <p>Approved by _____ Checked by _____ Prepared by _____</p> <p style="text-align: center;">             _____            T. OGAWA _____                       _____            E. KATAYAMA _____         </p>