

NEC NEC LCD Technologies, Ltd.

TFT MONOCHROME LCD MODULE

NL128102BM29-05A

48cm (19.0 Type)

SXGA

LVDS interface (2port)

DATA SHEET 

DOD-PD-1193 (1st edition)

**This DATA SHEET is updated document from
PRELIMINARY DATA SHEET DOD-PD-1064(5).**

**All information is subject to change without notice.
Please confirm the sales representative before
starting to design your system.**

INTRODUCTION

The Copyright to this document belongs to NEC LCD Technologies, Ltd. (hereinafter called "NEC"). No part of this document will be used, reproduced or copied without prior written consent of NEC.

NEC does and will not assume any liability for infringement of patents, copyrights or other intellectual property rights of any third party arising out of or in connection with application of the products described herein except for that directly attributable to mechanisms and workmanship thereof. No license, express or implied, is granted under any patent, copyright or other intellectual property right of NEC.

Some electronic parts/components would fail or malfunction at a certain rate. In spite of every effort to enhance reliability of products by NEC, the possibility of failures and malfunction might not be avoided entirely. To prevent the risks of damage to death, human bodily injury or other property arising out thereof or in connection therewith, each customer is required to take sufficient measures in its safety designs and plans including, but not limited to, redundant system, fire-containment and anti-failure.

The products are classified into three quality grades: "**Standard**", "**Special**", and "**Specific**" of the highest grade of a quality assurance program at the choice of a customer. Each quality grade is designed for applications described below. Any customer who intends to use a product for application other than that of Standard quality grade is required to contact an NEC sales representative in advance.

The **Standard** quality grade applies to the products developed, designed and manufactured in accordance with the NEC standard quality assurance program, which are designed for such application as any failure or malfunction of the products (sets) or parts/components incorporated therein a customer uses are, directly or indirectly, free of any damage to death, human bodily injury or other property, like general electronic devices.

Examples: Computers, office automation equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

The **Special** quality grade applies to the products developed, designed and manufactured in accordance with an NEC quality assurance program stricter than the standard one, which are designed for such application as any failure or malfunction of the products (sets) or parts/components incorporated therein a customer uses might directly cause any damage to death, human bodily injury or other property, or such application under more severe condition than that defined in the Standard quality grade without such direct damage.

Examples: Control systems for transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, medical equipment not specifically designed for life support, safety equipment, etc.

The **Specific** quality grade applies to the products developed, designed and manufactured in accordance with the standards or quality assurance program designated by a customer who requires an extremely higher level of reliability and quality for such products.

Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

CONTENTS

INTRODUCTION2

1. OUTLINE.....4

 1.1 STRUCTURE AND PRINCIPLE.....4

 1.2 APPLICATION.....4

 1.3 FEATURES.....4

2. GENERAL SPECIFICATIONS5

3. BLOCK DIAGRAM.....6

4. DETAILED SPECIFICATIONS7

 4.1 MECHANICAL SPECIFICATIONS.....7

 4.2 ABSOLUTE MAXIMUM RATINGS7

 4.3 ELECTRICAL CHARACTERISTICS.....8

 4.3.1 LCD panel signal processing board8

 4.3.2 Backlight lamp.....9

 4.3.3 Power supply voltage ripple.....10

 4.3.4 Fuse.....10

 4.4 POWER SUPPLY VOLTAGE SEQUENCE11

 4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS.....12

 4.5.1 LCD panel signal processing board12

 4.5.2 Backlight lamp.....13

 4.5.3 Positions of plugs and socket.....14

 4.6 SELECTION OF LVDS DATA INPUT MAP15

 4.6.1 Mode A15

 4.6.2 Mode B16

 4.7 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS.....17

 4.8 DISPLAY POSITION.....18

 4.9 INPUT SIGNAL TIMINGS.....18

 4.9.1 Timing characteristics.....18

 4.9.2 Input signal timing chart.....19

 4.10 OPTICS.....20

 4.10.1 Optical characteristics.....20

 4.10.2 Definition of contrast ratio.....21

 4.10.3 Definition of luminance uniformity21

 4.10.4 Definition of response times21

 4.10.5 Definition of viewing angles.....21

5. RELIABILITY TESTS.....22

6. PRECAUTIONS23

 6.1 MEANING OF CAUTION SIGNS23

 6.2 CAUTIONS23

 6.3 ATTENTIONS23

 6.3.1 Handling of the product23

 6.3.2 Environment.....24

 6.3.3 Characteristics.....25

 6.3.4 Other25

7. OUTLINE DRAWINGS26

 7.1 FRONT VIEW26

 7.2 REAR VIEW27

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL128102BM29-05A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

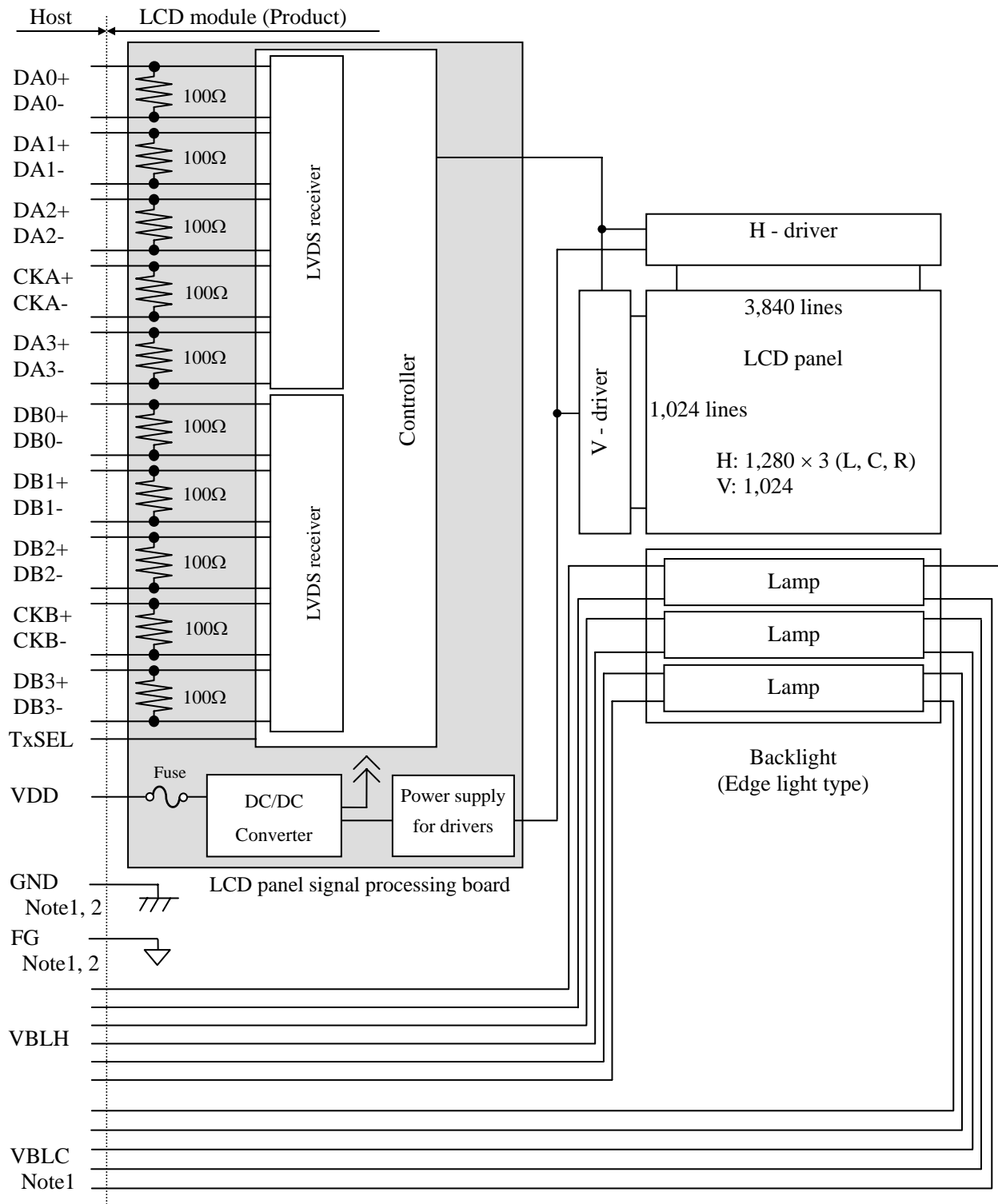
- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- 256 gray scales per 1 sub-pixel (8-bit)
- LVDS interface
- Selectable LVDS data input map
- Edge light type (without inverter)

2. GENERAL SPECIFICATIONS

Display area	376.32 (H) × 301.056 (V) mm
Diagonal size of display	48cm (19.0 inches)
Drive system	a-Si TFT active matrix
Display grayscale	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)
Pixel	1,280 (H) × 1,024 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
Pixel arrangement	LCR vertical stripe
Dot pitch	0.098 (H) × 0.294 (V) mm
Pixel pitch	0.294 (H) × 0.294 (V) mm
Module size	404.2 (W) × 330.0 (H) × 22.0 (D) mm (typ.)
Weight	2,900g (typ.)
Contrast ratio	900:1 (typ.)
Viewing angle	At the contrast ratio ≥10:1 <ul style="list-style-type: none"> • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ= DICOM): normal axis (perpendicular) <div style="text-align: right;">Note1</div>
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5400]
Response time	$T_{on} + T_{off}$ (10% ← → 90%) 35ms (typ.)
Luminance	At $IBL=6.0mA_{rms}$ / lamp 1,000cd/m ² (typ.)
Signal system	LVDS 2 port [LCR 8-bit data signals, Dot clock (CLK), Data enable (DE)]
Power supply voltage	LCD panel signal processing board: 5.0V
Backlight	Edge light type: 6 cold cathode fluorescent lamps (without inverter)
Power consumption	At $IBL=6.0mA_{rms}$ / lamp, Checkered flag pattern 26.8W (typ., Power dissipation of the inverter is not included.)

Note1: When the product luminance is 500cd/m², the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the product

GND - FG	Not connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	404.2 ± 0.5 (W) × 330.0 ± 0.5 (H) × 22.0 ± 0.3 (D) Note1	Note2 mm
Display area	376.32 (H) × 301.056 (V)	Note2 mm
Weight	2,900 (typ.), 3,100 (max.)	g

Note1: Excluding lamp cable, cable clamp and projections.

Note2: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +6.0	V	-
	Lamp voltage	VBLH	2,000	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to +2.8	V	VDD= 5.0V
	Function signal Note2	VF		V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note3
	Rear surface	TopR	0 to +60	°C	Note4
Relative humidity Note5		RH	≤ 70	%	Ta ≤ 55°C
Absolute humidity Note5		AH	≤ 73 Note6	g/m ³	Ta > 55°C
Operating altitude		-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude		-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note2: TxSEL

Note3: Measured at center of LCD panel surface (including self-heat)

Note4: Measured at center of LCD module's rear shield surface (including self-heat)

Note5: No condensation

Note6: Water amount at Ta= 55°C and RH= 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage	VDD	4.5	5.0	5.5	V	-	
Power supply current	IDD	-	680 Note1	1,400 Note2	mA	at VDD= 5.0V	
Permissible ripple voltage	VRP	-	-	100	mVp-p	for VDD	
Differential input threshold voltage for LVDS receiver	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3
	Low	VTL	-100	-	-	mV	
Terminating resistance	RT	-	100	-	Ω	-	
Input voltage for TxSEL signal	High	VFH	Keep this pin Open.			-	TxSEL Note4
	Low	VFL	-	-	0.5	V	
Input current for TxSEL signal	IFL	-80	-	-35	μA		

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS receiver

Note4: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)

4.3.2 Backlight lamp

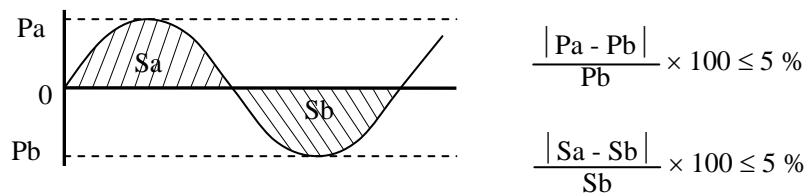
(Ta= 25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.5	6.0	7.0	mArms	at IBL= 6.0mArms: L= 1,000cd/m ² Note3
Lamp voltage	VBLH	-	650	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,350	-	-	Vrms	Ta= 25°C Note2, Note3
		1,550	-	-	Vrms	Ta= 0°C Note2, Note3
Lamp oscillation frequency	FO	40	48	55	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently. When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "4.9.1 Timing characteristics".)

n: Natural number (1, 2, 3)

Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	5.0V	≤ 100		mVp-p

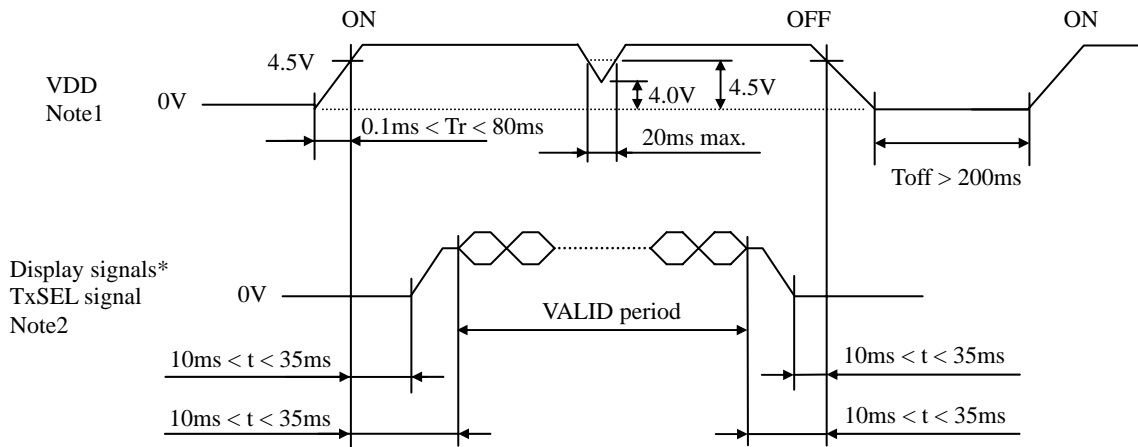
Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	KAB2402 402	Matsuo Electric Co., Ltd.	4.0A	8A, 1 minute maximum	Note1
			24V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE



* These signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 4.5V, a protection circuit may work, and then this product may not work.

Note2: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-) and TxSEL signal must be "0" voltage, exclude the VALID period (See above sequence diagram). If these signals are higher than 0.3V, the internal circuit is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VCC should be cut when the display and function signals are stopped.

Note3: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

☆

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-X30SSL-HF (Japan Aviation Electronics Industry Limited (JAE))
 Adaptable plug: FI-X30C series/ FI-X30H series/ FI-X30M series
 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	Note2
8	CKA-	Odd pixel clock	Note1
9	CKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	Note2
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	Note2
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CKB-	Even pixel clock	Note1
21	CKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	Note2
25	TxSEL	Selection of LVDS data input map	Open: Mode A Low: Mode B Note3, Note4
26	RSVD1	-	Keep this pin Open.
27	N.C.	-	Keep this pin Open.
28	VDD	Power supply	Note2
29			
30			

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: TxSEL is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "4.6 SELECTION OF LVDS DATA INPUT MAP".

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. Wrong connections will cause electric shock and also break down of the product.

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	VBLC	Low voltage (Cold)	Cable color: White

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: White
2	VBLC	Low voltage (Cold)	Cable color: White

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Sky blue
2	VBLC	Low voltage (Cold)	Cable color: White

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Pink
2	VBLC	Low voltage (Cold)	Cable color: White

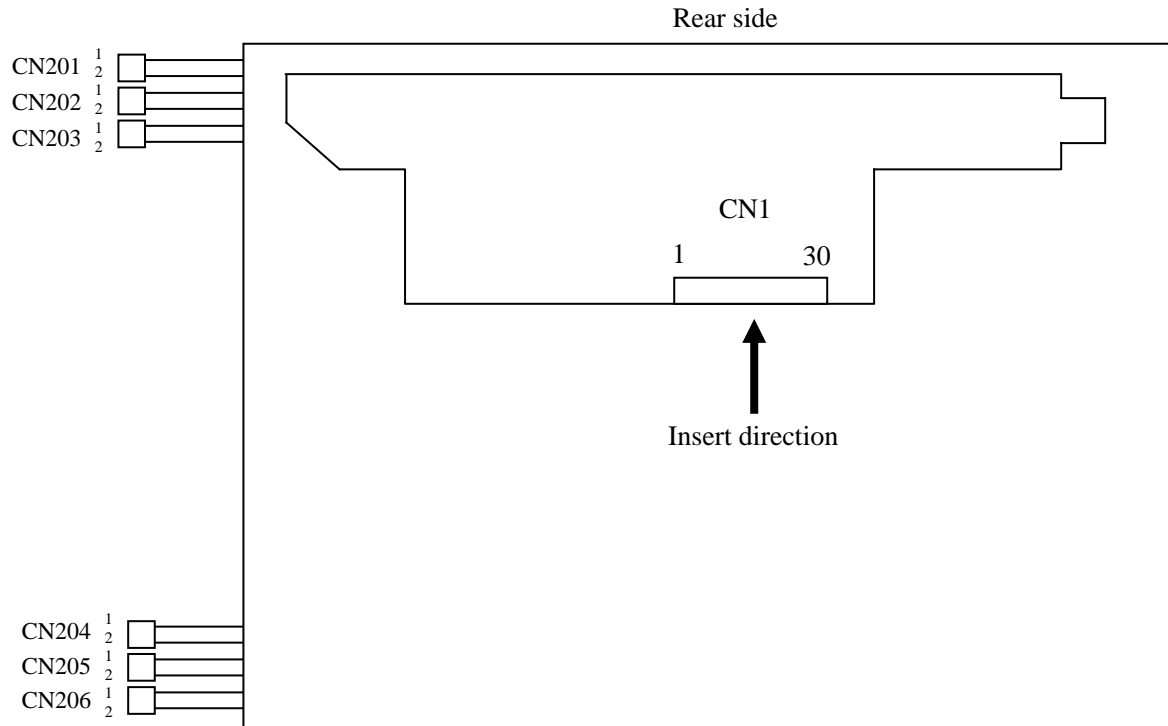
CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: White
2	VBLC	Low voltage (Cold)	Cable color: White

CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T Mfg. Co., Ltd.)
 Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) (J.S.T Mfg. Co., Ltd.)
 SM02B-BHSS-1-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Cable color: Sky blue
2	VBLC	Low voltage (Cold)	Cable color: White

4.5.3 Positions of plugs and socket



4.6 SELECTION OF LVDS DATA INPUT MAP

4.6.1 Mode A

Input data		Note1	Transmitter		CNI		
			Pin	DS90CF383, C385 or equivalent		Pin Symbol	
Odd pixel data and control signal	LA0	→	51	TXIN0			
	LA1	→	52	TXIN1	TA1-	→ 1 DA0-	
	LA2	→	54	TXIN2	TA1+	→ 2 DA0+	
	LA3	→	55	TXIN3			
	LA4	→	56	TXIN4	TB1-	→ 3 DA1-	
	LA5	→	3	TXIN6	TB1+	→ 4 DA1+	
	CA0	→	4	TXIN7			
	CA1	→	6	TXIN8	TC1-	→ 5 DA2-	
	CA2	→	7	TXIN9	TC1+	→ 6 DA2+	
	CA3	→	11	TXIN12			
	CA4	→	12	TXIN13	TCLK1-	→ 7 GND	
	CA5	→	14	TXIN14	TCLK1+	→ 8 CKA-	
	RA0	→	15	TXIN15			
	RA1	→	19	TXIN18	TD1-	→ 9 CKA+	
	RA2	→	20	TXIN19	TD1+	→ 10 DA3-	
	RA3	→	22	TXIN20			
	RA4	→	23	TXIN21			
	RA5	→	24	TXIN22			
	Note3	RSVD	→	27	TXIN24		
	Note3	RSVD	→	28	TXIN25		
		DE	→	30	TXIN26		
		LA6	→	50	TXIN27		
		LA7	→	2	TXIN5		
		CA6	→	8	TXIN10		
		CA7	→	10	TXIN11		
		RA6	→	16	TXIN16		
		RA7	→	18	TXIN17		
	Note3	RSVD	→	25	TXIN23		
		CLK	→	31	CLKIN		
	Even pixel data	LB0	→	51	TXIN0		
		LB1	→	52	TXIN1	TA2-	→ 12 DB0-
LB2		→	54	TXIN2	TA2+	→ 13 DB0+	
LB3		→	55	TXIN3		→ 14 GND	
LB4		→	56	TXIN4	TB2-	→ 15 DB1-	
LB5		→	3	TXIN6	TB2+	→ 16 DB1+	
CB0		→	4	TXIN7		→ 17 GND	
CB1		→	6	TXIN8	TC2-	→ 18 DB2-	
CB2		→	7	TXIN9	TC2+	→ 19 DB2+	
CB3		→	11	TXIN12			
CB4		→	12	TXIN13	TCLK2-	→ 20 CKB-	
CB5		→	14	TXIN14	TCLK2+	→ 21 CKB+	
RB0		→	15	TXIN15			
RB1		→	19	TXIN18	TD2-	→ 22 DB3-	
RB2		→	20	TXIN19	TD2+	→ 23 DB3+	
RB3		→	22	TXIN20		→ 24 GND	
RB4		→	23	TXIN21		→ 25 TxSEL	
RB5		→	24	TXIN22		→ 26 RSVD1	
Note3		RSVD	→	27	TXIN24		→ 27 N.C.
Note3		RSVD	→	28	TXIN25		→ 28 VDD
Note3		RSVD	→	30	TXIN26		→ 29 VDD
		LB6	→	50	TXIN27		→ 30 VDD
		LB7	→	2	TXIN5		
		CB6	→	8	TXIN10		
		CB7	→	10	TXIN11		
		RB6	→	16	TXIN16		
		RB7	→	18	TXIN17		
Note3		RSVD	→	25	TXIN23		
		CLK	→	31	CLKIN		

4.6.2 Mode B

Input data		Transmitter		CN1						
		Pin	THC63LVDF83A/R or equivalent			Pin	THC63LVD823 or equivalent			
Odd pixel data and control signal	Note1 LA2 →	51	TA0	53	R12	Note2	Pin	Symbol		
	LA3 →	52	TA1	54	R13		TA1-	1	DA0-	
	LA4 →	54	TA2	57	R14		TA1+	2	DA0+	
	LA5 →	55	TA3	58	R15					
	LA6 →	56	TA4	59	R16		TB1-	3	DA1-	
	LA7 →	3	TA5	60	R17		TB1+	4	DA1+	
	CA2 →	4	TA6	63	G12					
	CA3 →	6	TB0	64	G13		TC1-	5	DA2-	
	CA4 →	7	TB1	65	G14		TC1+	6	DA2+	
	CA5 →	11	TB2	66	G15			7	GND	
	CA6 →	12	TB3	67	G16		TCLK1-	8	CKA-	
	CA7 →	14	TB4	68	G17		TCLK1+	9	CKA+	
	RA2 →	15	TB5	73	B12					
	RA3 →	19	TB6	74	B13		TD1-	10	DA3-	
	RA4 →	20	TC0	75	B14		TD1+	11	DA3+	
	RA5 →	22	TC1	76	B15					
	RA6 →	23	TC2	77	B16					
	RA7 →	24	TC3	78	B17					
	Note3 RSVD →	27	TC4	7	RSVD					
	Note3 RSVD →	28	TC5	8	RSVD					
	DE →	30	TC6	9	DE					
	LA0 →	50	TD0	51	R10					
	LA1 →	2	TD1	52	R11					
	CA0 →	8	TD2	61	G10					
	CA1 →	10	TD3	62	G11					
	RA0 →	16	TD4	69	B10					
	RA1 →	18	TD5	70	B11					
	Note3 RSVD →	25	TD6	-	-					
	CLK →	31	CLKIN	10	CLK					
	Even pixel data	LB2 →	51	TA0	81		R22	TA2-	12	DB0-
		LB3 →	52	TA1	82		R23	TA2+	13	DB0+
LB4 →		54	TA2	83	R24		14	GND		
LB5 →		55	TA3	84	R25					
LB6 →		56	TA4	85	R26	TB2-	15	DB1-		
LB7 →		3	TA5	86	R27	TB2+	16	DB1+		
CB2 →		4	TA6	91	G22		17	GND		
CB3 →		6	TB0	92	G23	TC2-	18	DB2-		
CB4 →		7	TB1	93	G24	TC2+	19	DB2+		
CB5 →		11	TB2	94	G25					
CB6 →		12	TB3	95	G26	TCLK2-	20	CKB-		
CB7 →		14	TB4	96	G27	TCLK2+	21	CKB+		
RB2 →		15	TB5	99	B22					
RB3 →		19	TB6	100	B23	TD2-	22	DB3-		
RB4 →		20	TC0	1	B24	TD2+	23	DB3+		
RB5 →		22	TC1	2	B25		24	GND		
RB6 →		23	TC2	5	B26		25	TxSEL		
RB7 →		24	TC3	6	B27		26	RSVD1		
Note3 RSVD →		27	TC4	-	-		27	N.C.		
Note3 RSVD →		28	TC5	-	-		28	VDD		
Note3 RSVD →		30	TC6	-	-		29	VDD		
LB0 →		50	TD0	79	R20		30	VDD		
LB1 →		2	TD1	80	R21					
CB0 →		8	TD2	89	G20					
CB1 →		10	TD3	90	G21					
RB0 →		16	TD4	97	B20					
RB1 →		18	TD5	98	B21					
Note3 RSVD →		25	TD6	-	-					
CLK →		31	CLKIN	-	-					

Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0
 MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

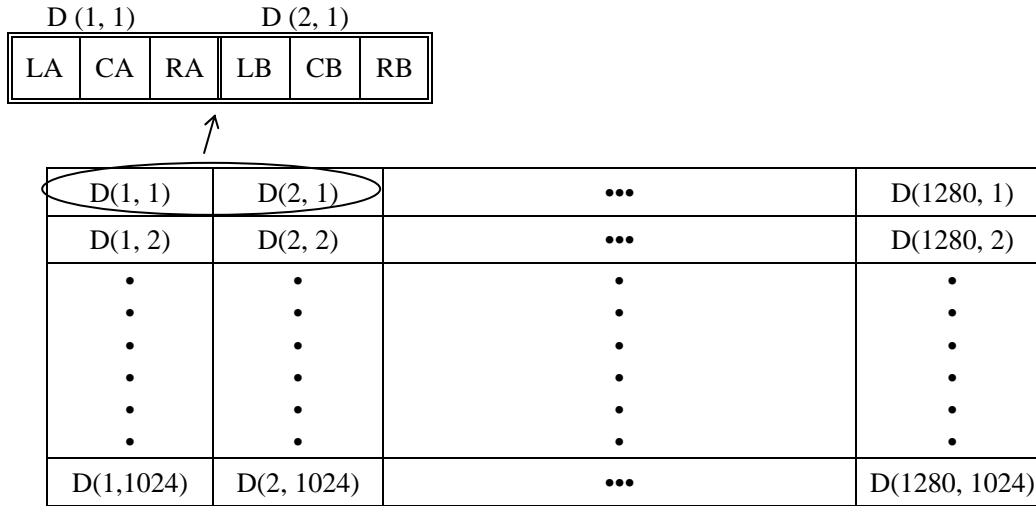
Note3: Input signal RSVD is not used inside the product, but do not keep this pin open to avoid noise problem.

4.7 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																							
		LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
Left dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Right dot gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
White		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.8 DISPLAY POSITION



4.9 INPUT SIGNAL TIMINGS

4.9.1 Timing characteristics

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency	1/tc	49	54	59	MHz	18.52ns (typ.)	
	Duty	-	-			-	Note2	
	Rise time, Fall time	-				ns		
DATA	CLK-DATA	Setup time	-			ns	Note2	
		Hold time				ns		
	Rise time, Fall time	-				ns		
DE	Horizontal	Cycle	th	12.3	15.63	20.59	μs	64.0kHz (typ.) Note1, Note2
		Display period	thd	640			CLK	
	Vertical (One frame)	Cycle	tv	13.1	16.6	17.5	ms	60.0Hz (typ.) Note1
		Display period	tvd	1,024			H	
	CLK-DE	Setup time	-	-			ns	Note2
		Hold time	-				ns	
Rise time, Fall time		-	ns					

Note1: Definition of parameters is as follows.

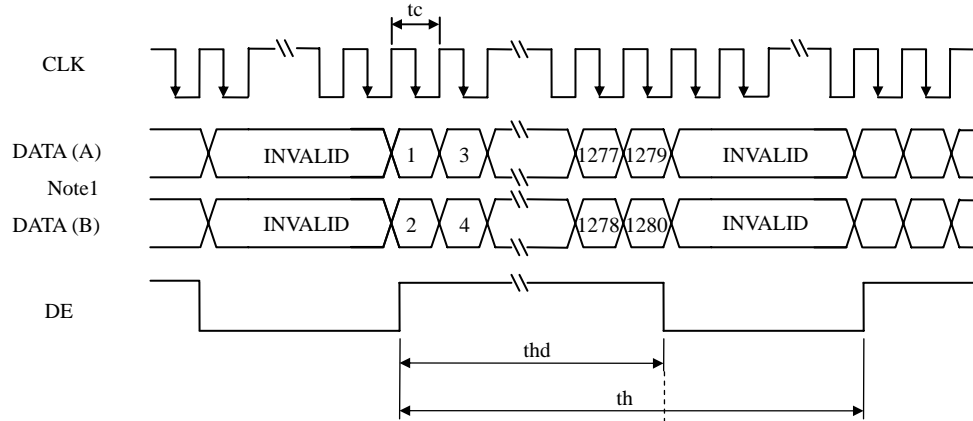
tc= 1CLK, th= 1H

Note2: See the data sheet of LVDS transmitter.

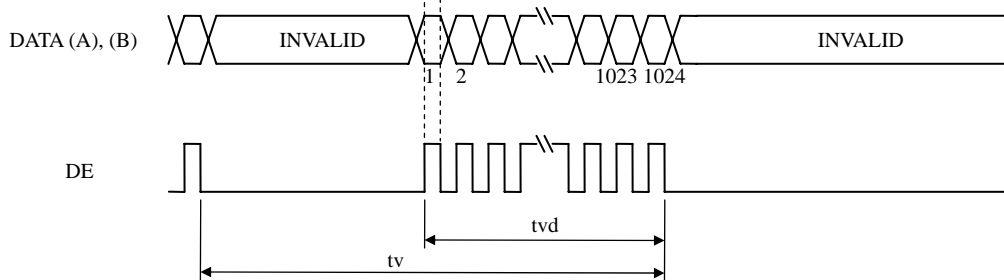
☆

4.9.2 Input signal timing chart

Horizontal timing



Vertical timing



Note1: DATA (A)= LA0-LA7, CA0-CA7, RA0-RA7
 DATA (B)= LB0-LB7, CB0-CB7, RB0-RB7

4.10 OPTICS

4.10.1 Optical characteristics

(Note1, Note2)

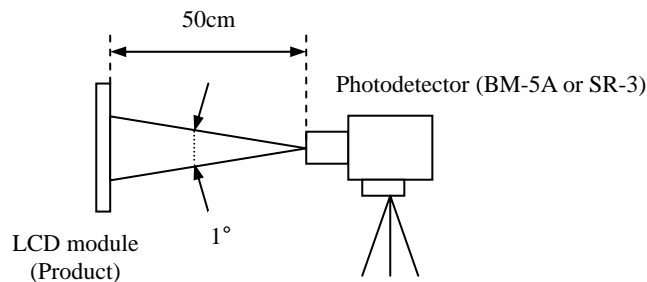
Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R=0^\circ, \theta L=0^\circ, \theta U=0^\circ, \theta D=0^\circ$	L	800	1,000	-	cd/m ²	BM-5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R=0^\circ, \theta L=0^\circ, \theta U=0^\circ, \theta D=0^\circ$	CR	600	900	-	-	BM-5A or SR-3	Note3	
Luminance uniformity	White $\theta R=0^\circ, \theta L=0^\circ, \theta U=0^\circ, \theta D=0^\circ$	LU	-	1.15	1.25	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	0.250	0.280	0.310	-	SR-3	Note5
		y coordinate	Wy	0.274	0.304	0.334	-		
Response time	Black to White	Ton	-	18	28	ms	BM-5A	Note6	
	White to Black	Toff	-	17	27	ms		Note7	
Viewing angle	Right	$\theta U=0^\circ, \theta D=0^\circ, CR \geq 10$	θR	70	85	-	BM-5A	Note8	
	Left	$\theta U=0^\circ, \theta D=0^\circ, CR \geq 10$	θL	70	85	-			
	Up	$\theta R=0^\circ, \theta L=0^\circ, CR \geq 10$	θU	70	85	-			
	Down	$\theta R=0^\circ, \theta L=0^\circ, CR \geq 10$	θD	70	85	-			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta= 25°C, VDD= 5.0V, IBL= 6.0mA/lamp, Display mode: SXGA,
Horizontal cycle= 1/64.0kHz, Vertical cycle= 1/60.0Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room.
Also measurement method for luminance is as follows.



Note3: See "4.10.2 Definition of contrast ratio".

Note4: See "4.10.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF= 35°C

Note7: See "4.10.4 Definition of response times".

Note8: See "4.10.5 Definition of viewing angles".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

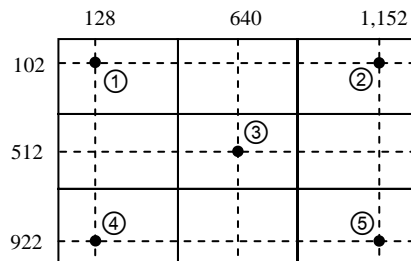
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

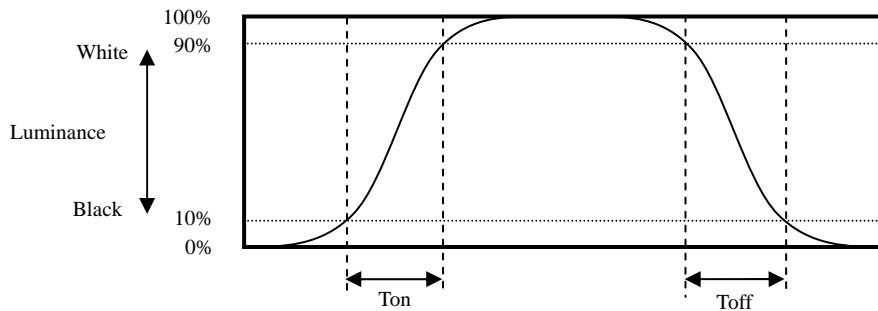
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

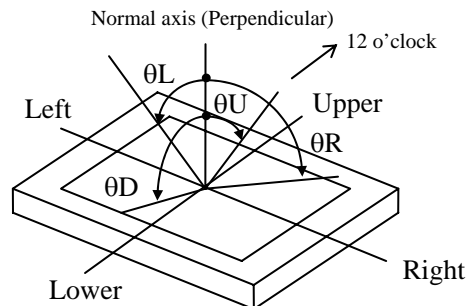


4.10.4 Definition of response times

Response time is measured, the luminance changes from " black " to " white ", or " white " to " black " on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.10.5 Definition of viewing angles

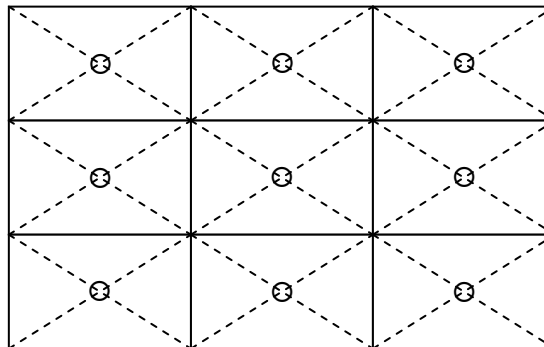


5. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C...1hour 55 ± 3°C...1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -20 ± 3°C...30minutes 60 ± 3°C...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s ² ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s ² , 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)		① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Operation	① 53.3kPa (Equivalent to altitude 4,850m) ② 0°C±3°C...24 hours ③ 55°C±3°C...24 hours	
	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② -20°C±3°C...24 hours ③ 60°C±3°C...24 hours	

Note1: Display functions are checked under the same conditions as product inspection.




Note2: See the following figure for discharge points




6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS


The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



*** Do not touch the working backlight. There is a danger of an electric shock.**



*** Do not touch the working backlight. There is a danger of burn injury.**
*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s² and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

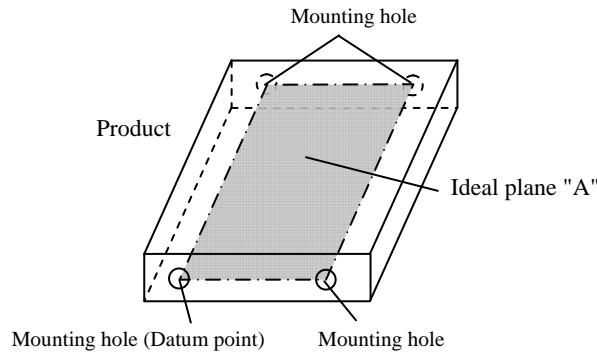
6.3 ATTENTIONS 

6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.67N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be 4.0mm to 7.0mm.

- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion except mounting hole portion may cause display mura.
 Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within $\pm 0.2\text{mm}$.

☆



- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.
- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ If the lamp cable is attached on the metal part of the product directly, high frequency leak current to the metal part may occur, then the brightness may decrease or the lamp may not be turned on.
- ⑩ When installing the lamp cable, do not locate the lamp cable on the signal processing board. A noise may occur on the display image.
- ⑪ When not connecting FG of the LCD module to the customer's equipment ground, inverter noise may create video noise on the LCD screen.
- ⑫ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

☆

6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

6.3.3 Characteristics

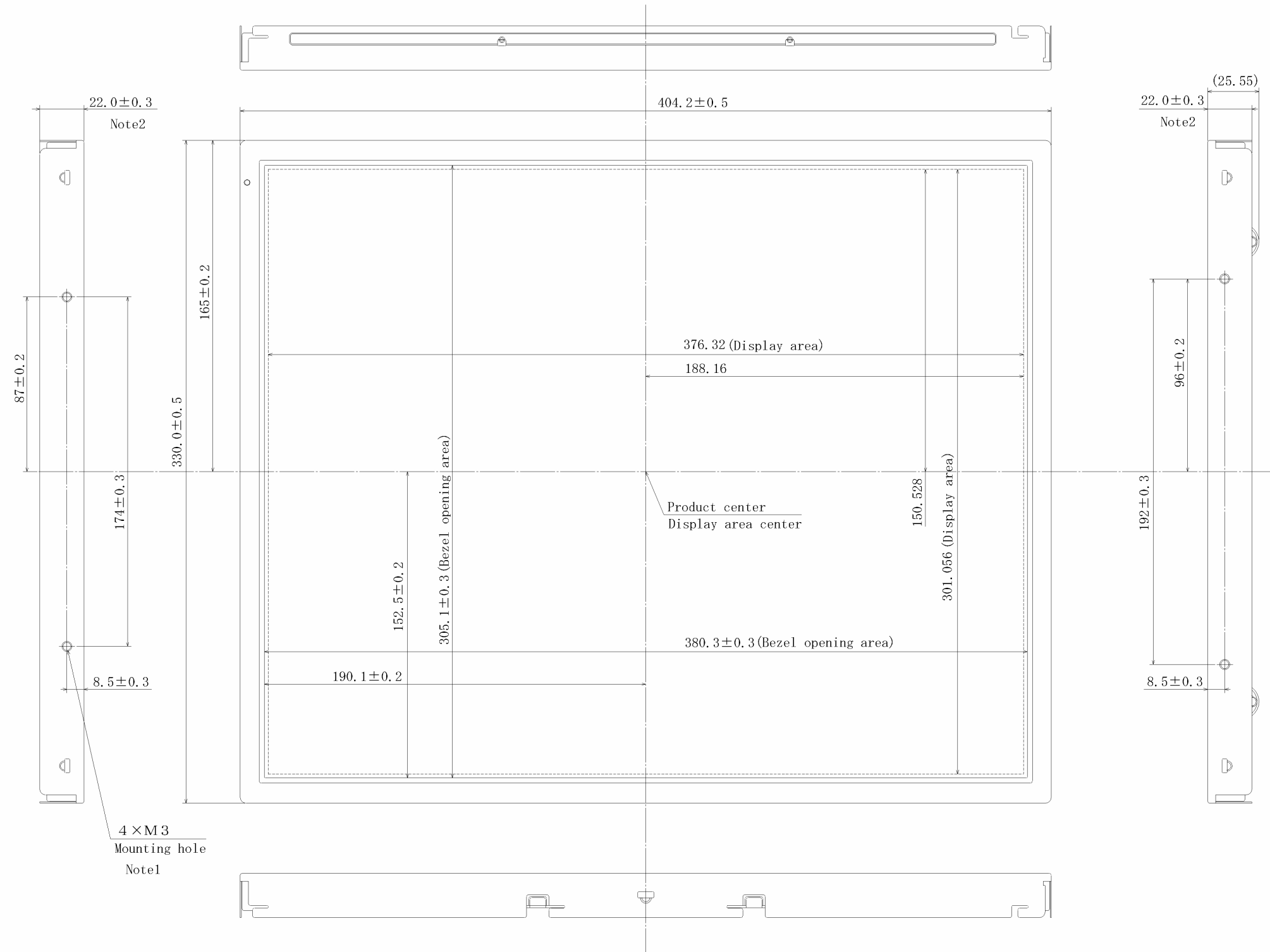
The following items are neither defects nor failures.

- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

6.3.4 Other

- ① All GND and VDD terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

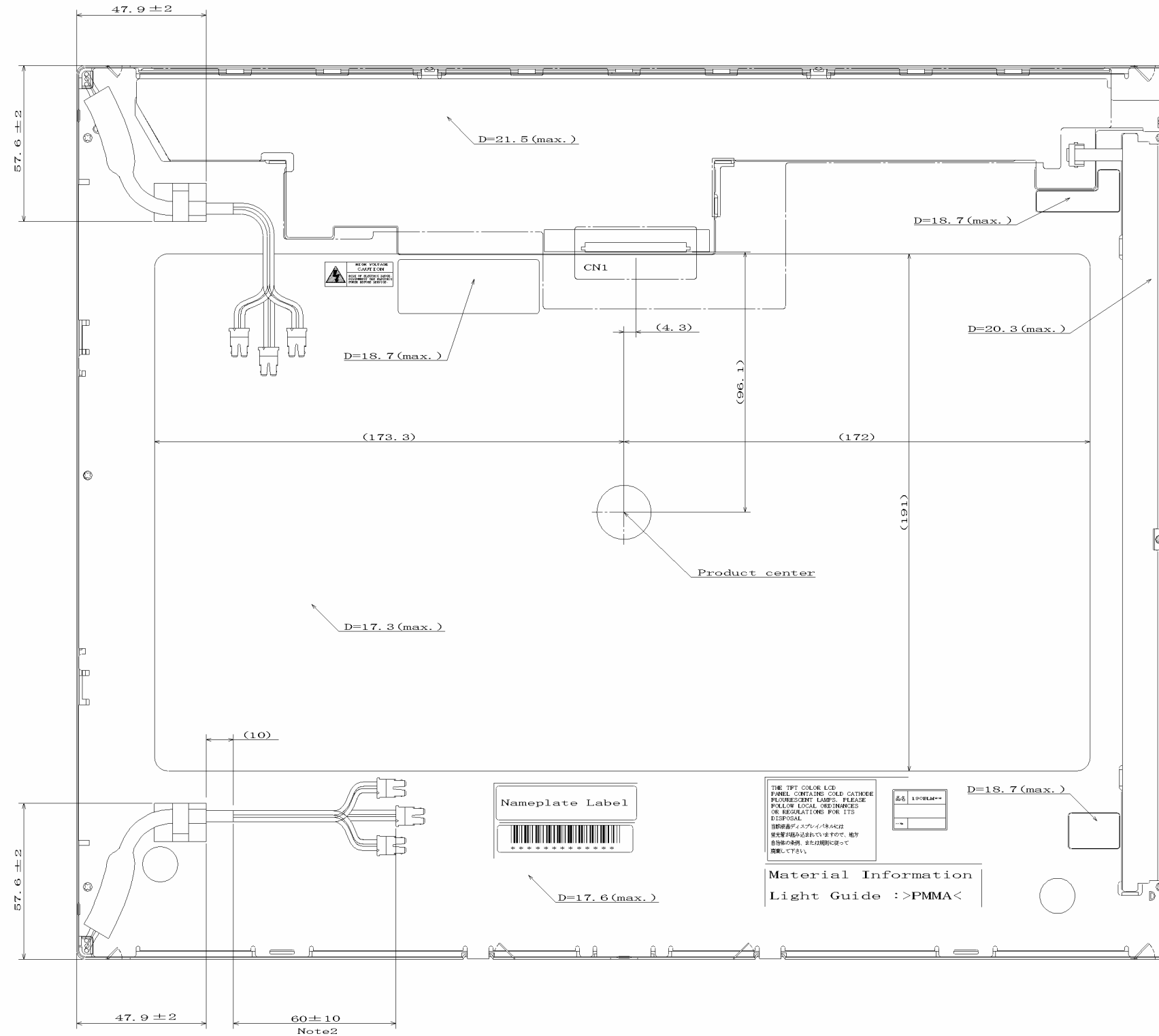
7. OUTLINE DRAWINGS
7.1 FRONT VIEW



Note1: The torque for product mounting screws must never exceed 0.67N·m. And the length of product mounting screws must be 4.0mm to 7.0mm.
Note2: Excluding lamp cable, cable clamp and projections.

Unit: mm

7.2 REAR VIEW



Note1: The values in parentheses are for reference.
 Note2: The cable of up side and down side is the same length.

Unit: mm